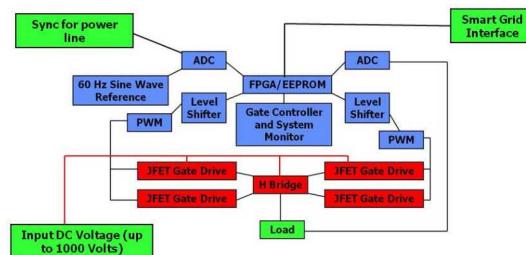
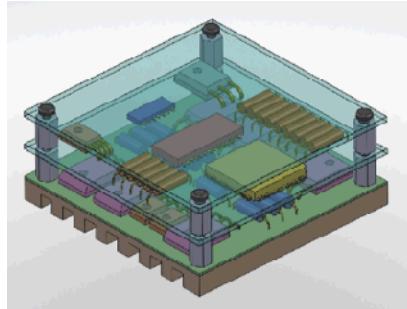
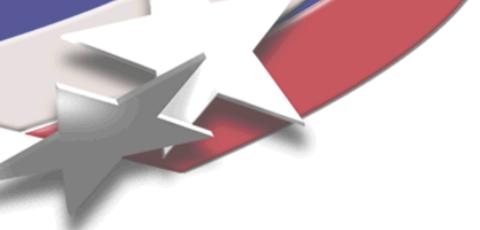


Development of an Integrated Power Controller Based on HT SOI and SiC

Joseph A. Henfling, Stan Atcity, Frank Maldonado, Sandia National Laboratories



Sandia National Laboratories is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin company, for the United State Department of Energy under contract DE-AC04-94AL85000.



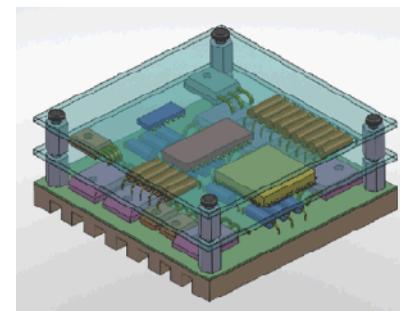
Overview

- **Program Goals for HT Power Controller**
 - Size reduction of power controllers
 - Ultimately a single module solution
- **Power Controller Design Details**
 - Two options investigated
 - APEI's HT SOI MOSFET power module
 - Sandia's JFET power module
- **Test Results**
- **Conclusions**
- **Future work**



Project Goals

- Design HT power controller that can be integrated into a single module
 - Benefits include:
 - Size reduction of power controllers
 - Integration of the SOI based controller with (near) SiC power devices
 - Ease thermal management requirements
 - Increase reliability
 - Designed using HT components and elimination of board-level interconnects
 - Increase efficiency
 - Optimized to fully exploit the benefits of using SiC technology in power controllers
 - Higher breakdown voltage coupled with a lower “ON” resistance can reduce energy losses by 3-4%
 - High voltage capable designs (SiC JFET’s rated at 1200 Volts)
- Establish commercialization path to quicken the adaptation of energy-saving SiC technology





Why a Single Module Solution?



+/-150MVAR STATCOM
Northeast Utilities' Glenbrook
Substation in Stamford, CT

Cooling
Pipes



Cooling System:
Pump, Pipes

GTOs &
Controls

7" x 12.5"

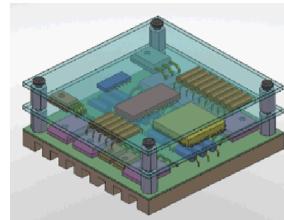


2.5" x 8.75" x 3.5"



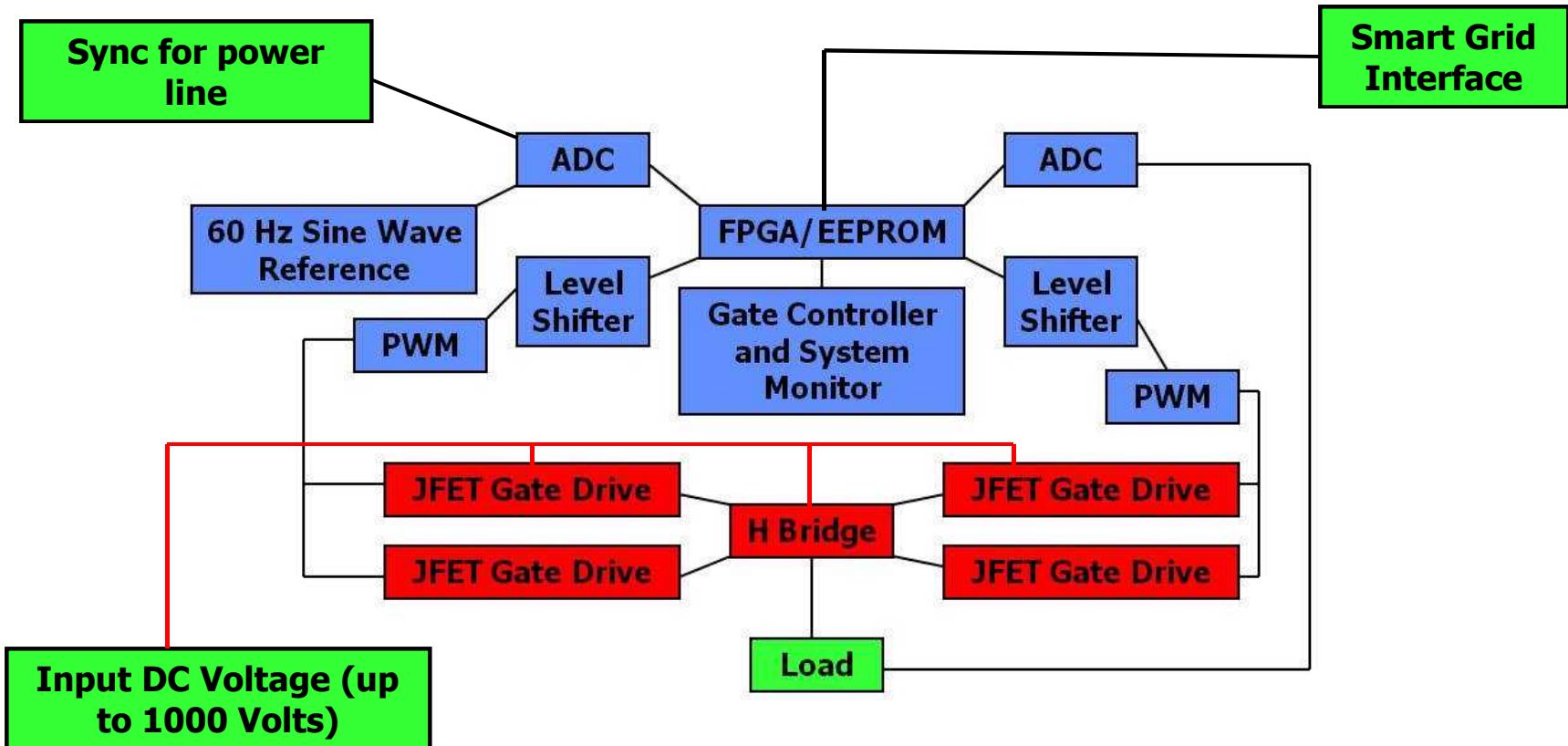
Phase 2

4" x 4" x 2"



Phase 3

Block Diagram of the Power Controller



$V_{out} = V_{in} (1 - \text{Duty Cycle})$

Blue – MCM 1
Red – MCM 2
Green – Outside Components



Phase I Accomplishments

Program Start Date FY09

- Successfully demonstrated a prototype microcontroller-based HT power controller at 240C
 - Basic control capabilities including monitoring the JFET (Junction Field Effect Transistor) case temperature
 - Safely shutting the system down if a programmed temperature was exceeded
- Demonstrated high side / low side SOI (Silicon-on-Insulator) gate drive for the JFET power devices
- Successfully tested SOI MESFET (MEtal-Semiconductor-Field-Effect-Transistor) gate drive



By combining SOI control and drive circuits with SiC, an intelligent system capable of operation up to 240°C (JFET junction temperature approaching 300°C) was successfully demonstrated

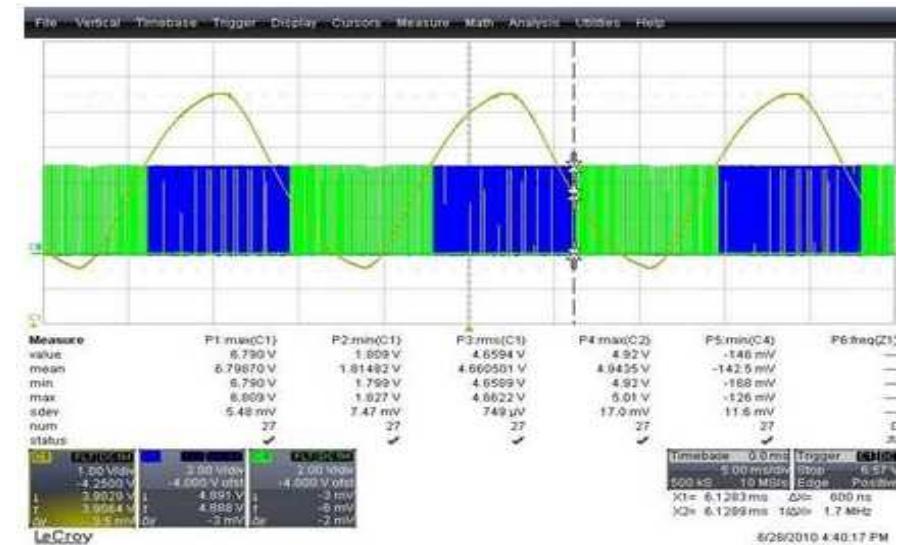
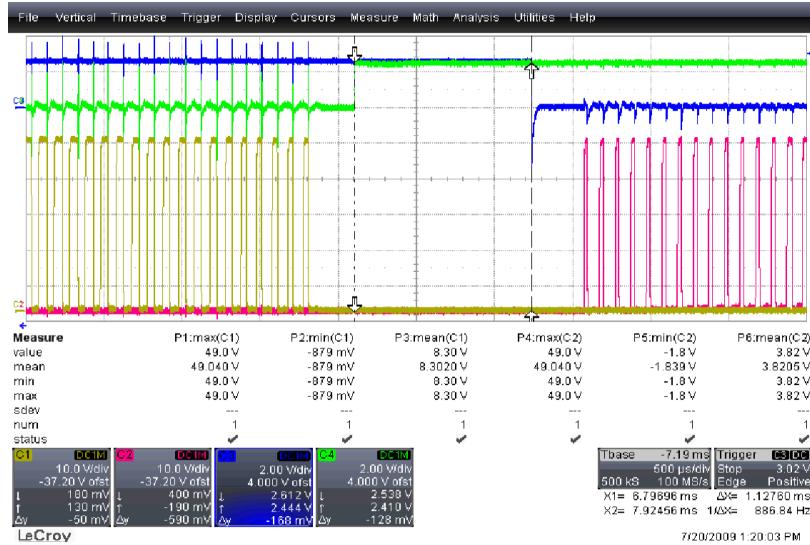


Phase II and III Accomplishments

- **“Fine-Tune” prototype design**
 - Designed, fabricated and tested a version 2 board with optimized system efficiency
 - Enhanced high side gate drive of the H bridge
 - Mitigated the current spikes
 - Minimized the switching “dead time”
 - Optimized the output filter
 - Improved microcontroller design
 - Better control of the power devices
 - Active feedback investigated; refinement required
- **Started evaluation of APEI’s power module**
 - Verified compatibility with Sandia’s controller
 - Performed 5 kW tests at APEI (room temperature)
 - Initiated oven tests with modules
- **Contracted with Honeywell to program HT FPGA with Sandia developed code – in progress**
- **Contracted with Life Bioscience to fabricate HT circuit board – in progress**



Enhanced Performance – Reduced Dead Band



Present design has a 600ns dead band

Prototype design exaggerated the dead band between cycles to ensure the JFETs were not damaged due to timing issues. This substantially reduced the overall efficiency.

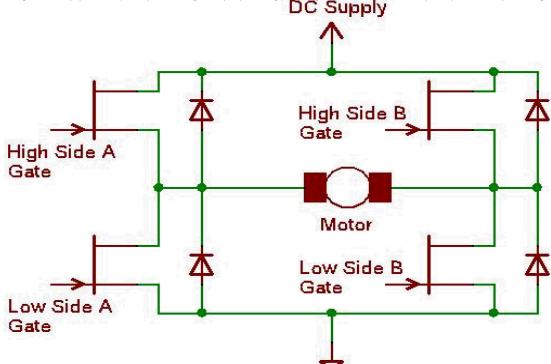
Enhanced Performance - Improved Gate Drive

- Enhanced switching methodology

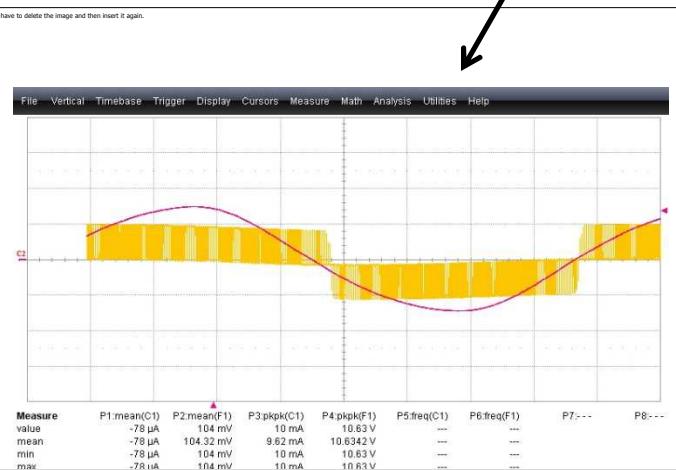
- Three-level continuous PWM

- Voltage harmonics are both decreased in amplitude and increased in frequency
 - Reduced output filter size requirements (to achieve a given current THD)
 - Increased efficiency

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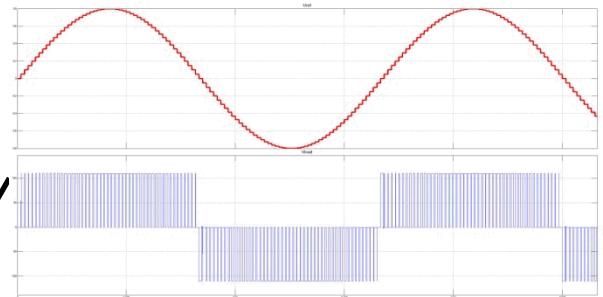


Prototype had PWM Gate Drive at Q1 and Q3; 60Hz at Q2 and Q4;
Discontinuous PWM



Gold – Reference signal,
Red – current waveform,
Yellow – resulting voltage waveform

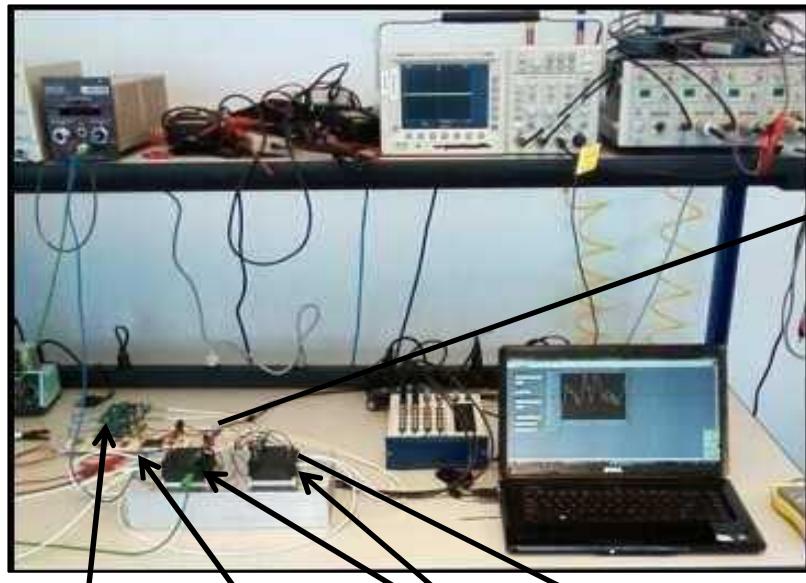
Simulink Simulation



Enhanced circuit has PWM Gate Drive at Q1, Q2, Q3 and Q4;
Three-level continuous PWM



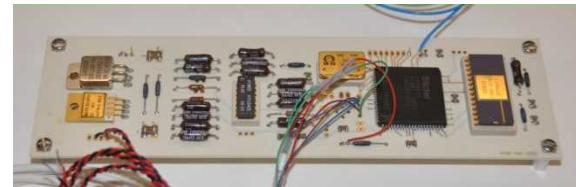
Test Results – Initial Testing at APEI



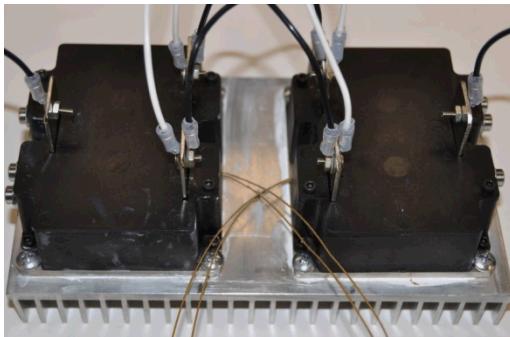
APEI Power Supplies

Sandia Controller

APEI Modules



Sandia Controller

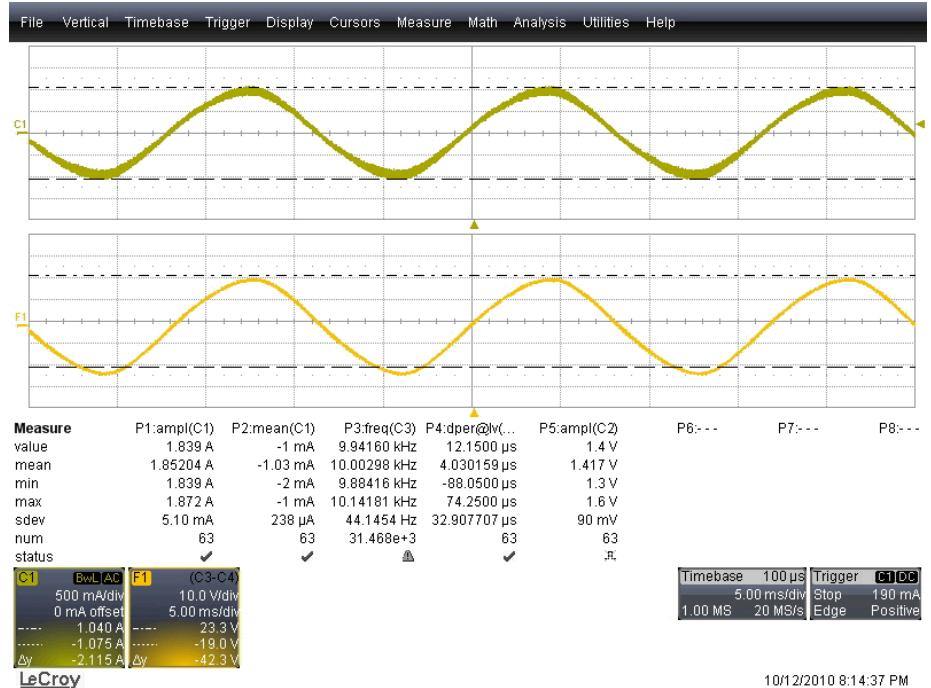


APEI Power module with integrated gate drive

APEI Test Results



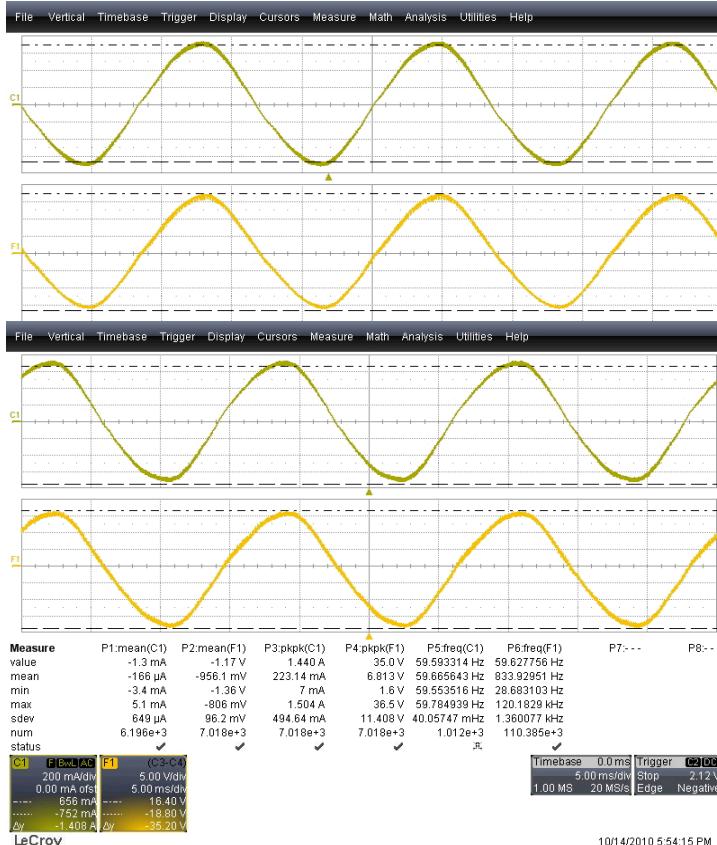
Test Results at 150 C



Testing APEI modules with Sandia's controller
at elevated temperatures

Testing Sandia's Controller with JFET Power Devices

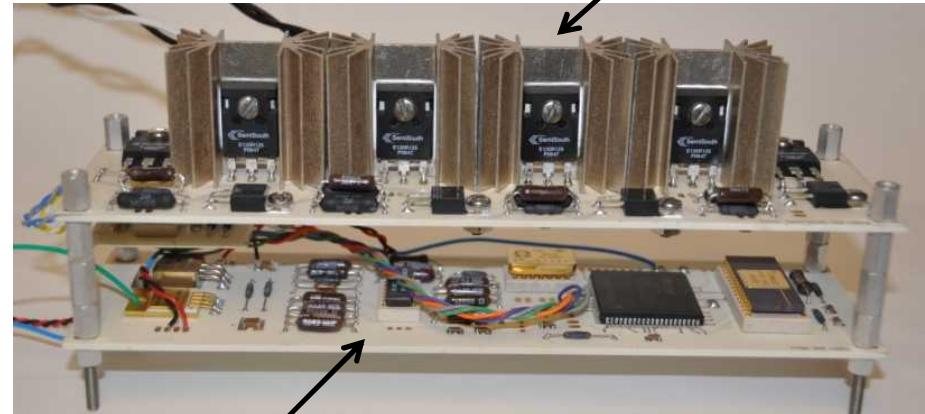
Resulting waveform at room temperature



Resulting waveform at 200°C



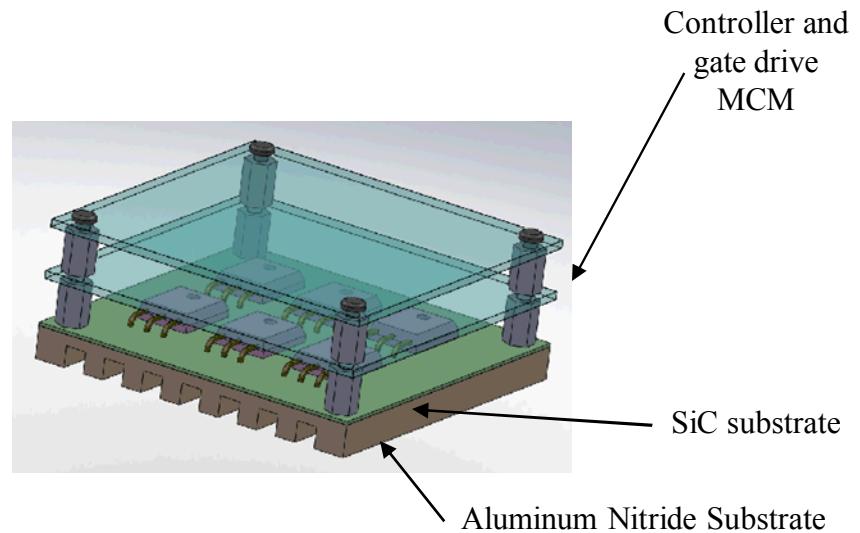
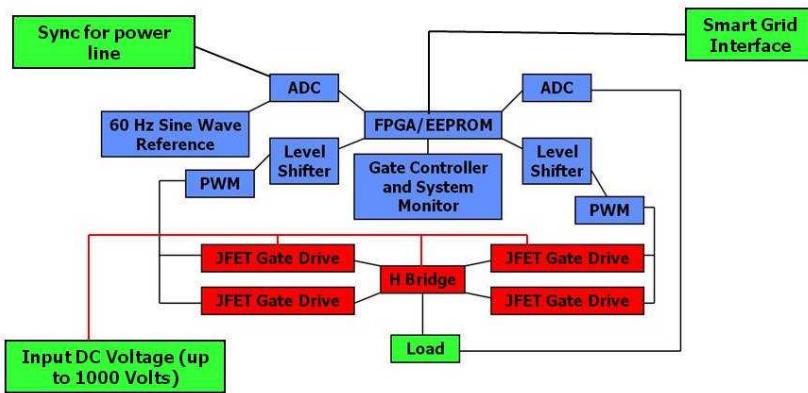
JFET Power
Devices and
Gate Drive



Controller



Updated Concept of the Power Controller Module



Investigating potentially utilizing same substrate for power devices and MultiChip Modules (MCM)



Future Plans

- Evaluate APEI's HT gate drive power supplies
- Investigate utilizing APEI's JFET power module with HT gate drive power supply and steps required to integrate into single module
- Refine feedback control
- Complete MCM design of controller
- Evaluate Honeywell HT SOI FPGA
- Evaluate HT circuit board
- Demonstrate “next step” in single module solution (Sandia or APEI power boards)



Conclusion

- Lab tested an enhanced controller board and a power board consisting of JFET power devices with gate drive
- Completed initial testing at APEI using APEI's power modules, LT gate drive power supply and Sandia's controller; 5kW tests
- Completed initial testing at Sandia at elevated temperatures
- In progress: conversion of Sandia code into a HT FPGA (Honeywell)
- In progress: fabrication of HT circuit board



Collaborative Effort with Academia and Industry

- DOE Funded

- Participants include:

- Sandia (Lead)
 - ASU (Circuit simulation, fabrication of test circuits using HT MESFET – JFET gate drive) - Phase I
 - PermaWorks (Inverter design simulation and fabrication of HV supply) – Phase I
 - APEI (Power modules, HT power supplies, thermal analysis) – Phase II, III
 - Life BioScience (HT circuit boards) – Phase II, III

- COTS suppliers

- Honeywell SSEC
 - Cissoid
 - SemiSouth

The authors would like to thank DOE Energy Program and Imre Gyuk for financial support of this research.