SAND2011-1083C

A New Wafer-Level Packaging Technology for MEMS with Hermetic Micro-Environment

By

Rajen Chanchani, Christopher D. Nordquist, Roy H. Olsson III, Tracy Peterson, Randy Shul, Catalina Ahlers, Thomas A. Plut, and Gary A. Patrizi

Sandia National Labs*

P.O. Box 5800, Albuquerque, NM 87185

Tel. (505) 844-3483, email: chanchr@sandia.gov

Abstract

We report a new wafer-level packaging technology for miniature MEMS in a hermetic micro-environment. The unique and new feature of this technology is that it only uses low cost wafer-level processes such as eutectic bonding, Bosch etching and mechanical lapping and thinning steps as compared to more expensive process steps that will be required in other alternative wafer-level technologies involving thru-silicon vias or membrane lids. We have demonstrated this technology by packaging silicon- based AlN microsensors in packages of size 1.3 x 1.3 mm^2 and 200 micrometer thick. Our initial cost analysis has shown that when mass produced with high yields, this device will cost $0.10 to $0.90.

The technology involves first preparing the lid and MEMS wafers separately with the sealring metal stack of Ti/Pt/Au on the MEMS wafers and Ti/Pt/Au/Ge/Au on the lid wafers. On the MEMS wafers, the Signal/Power/Ground interconnections to the wire-bond pads are isolated from the sealring metallization by an insulating AlN layer. Prior to bonding, the lid wafers were Bosch-etched in the wirebond pad area by 120 μm and in the center hermetic device cavity area by 20 μm. The MEMS and the lid wafers were then aligned and bonded in vacuum or in a nitrogen environment at or above the Au-Ge Eutectic temperature, 363^oC. The bonded wafers were then thinned and polished first on the MEMS side and then on the lid side. The MEMS side was thinned to 100 microns with a nearly scratch-free and crack-free surface. The lid side was similarly thinned to 100 microns exposing the wire-bond pads. After thinning, a 100 μm thick lid remained over the MEMS features providing a 20 μm high hermetic micro-environment. Thinned MEMS/Lid wafer-level assemblies were then sawed into individual devices. These devices can be integrated into the next-level assembly either by wire-bonding or by surface mounting.

The wafer-level packaging approach developed in this project demonstrated RF Feedthroughs with <0.3 dB insertion loss and adequate RF performance through 2 GHz. Pressure monitoring Pirani structures built inside the hermetic lids have demonstrated the ability to detect leaks in the package. In our preliminary development experiments, we have demonstrated >50% hermetic yields.

***Sandia is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company for the United States Department of Energy under contract DE-AC04-94AL85000.**

I. Introduction

RF MEMS resonators and switches allow miniaturization of RF systems by offering unique and compelling performance improvements in miniature volumes. The high-Q and miniature size of RF MEMS resonators provides the opportunity for substantial miniaturization of RF filters and frequency references. The low loss and low capacitance of RF MEMS switches offer improved adaptability and switching functions. However, to take advantage of these technologies over incumbent components, the technology's performance benefits must be maintained in a miniature volume. How these components are packaged and integrated play a crucial role on their applications in future radar, communications, and sensing systems.

Packaging of RF MEMS components presents a unique challenge because these devices require an empty volume to function, and the cleanliness and environmental integrity of that volume impacts the device performance and reliability. Thus, the empty volume around MEMS must be a hermetic microenvironment. For their widespread use, the packaging of MEMS devices must also be both cost-effective and high-yield for volume production. Additionally, the signal traces providing access from inside the volume to the outside of the package must have low resistance and capacitance to maintain the device performance and impedance matching. These packaging requirements eliminate discrete individual packaging approaches such as injection molding and assembly of individual MEMS die into lidded ceramic or plastic packages.

Wafer-level packaging offers the advantage of making miniaturized, lower cost and higher yielding packages. The wafer-level packaging concept to make chip-scale packages was first introduced in 1994 by investigators from Sandia National Labs [1, 2]. In the early part of this decade, several groups around the globe have investigated wafer-level processes for providing hermetic protection of MEMS [3-10]. These investigators have developed (i) wafer-level processes for silicon or glass lids to MEMS or (ii) wafer-processing to get local micro-encapsulation. These proposed packaging schemes are shown in Figure 1. As shown in Figures 1a and 1b, the lid wafers (silicon or glass) are bonded to MEMS (silicon) wafer and the I/O interconnects are routed out using either thru-substrate-vias (Figure 1a) or thru-lid-vias (Figure 1b). In the third technology (Figure 1c), wafers are processed to form hermetic membranes over MEMS using a sacrificial layer. These reported technologies require additional costlier and lower yielding semiconductor fabrication process steps involving thru-silicon vias or membrane lids.

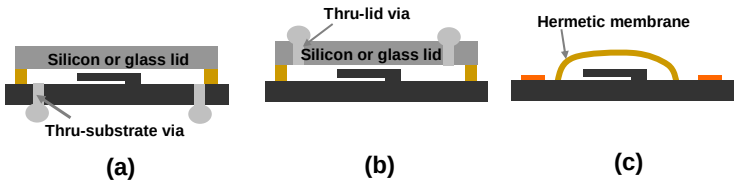


Figure 1: (a) Hermetic lid over MEMS with I/Os routed out in the substrate using thru-silicon vias.[9] (b) Hermetic lid over MEMS with I/Os routed out in the lid (silicon or glass) using thru-lid vias[6-8]. (c) Hermetic membrane [10].

In this study, we have developed a unique, but relatively simple wafer-level technology to provide hermetic environment over MEMS. The novelty and uniqueness of our technology is that it uses low cost wafer-level process steps. As illustrated in Figure 2, the technique involves bonding MEMS wafer to lid wafer and then exposing the I/O pads on the edge of the die by Bosch etching and mechanical thinning of the lid wafer. One of the key aspects of the technology, as illustrated in the figure, was to have two cavity depths in the lid. The shallow cavity (20 μm deep) is in the center providing an empty cavity over MEMS features. The deeper cavity (120 μm) is on the MEMS edge over the wire-bond pads and the remaining silicon in this area was removed by mechanical thinning exposing the wire-bond pads. The processed wafer and its magnified view, and the singulated MEMS device (<200 micron-thick) with hermetic micro-environment are shown in Figure 3. The exposed I/O pads on the edge of the MEMS hermetic device can be interconnected into next-level assembly by either wire-bonding or by attaching solder balls to these pads for surface mounting.

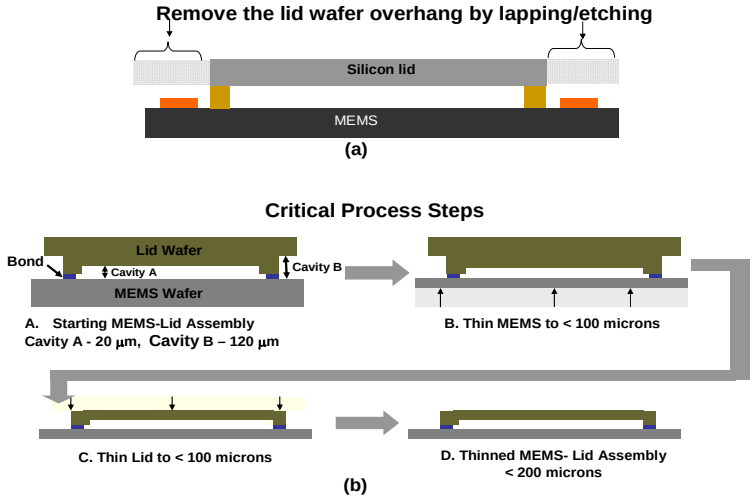


Figure 2: (a) The new low cost approach taken in this technology. (b) The critical process steps.

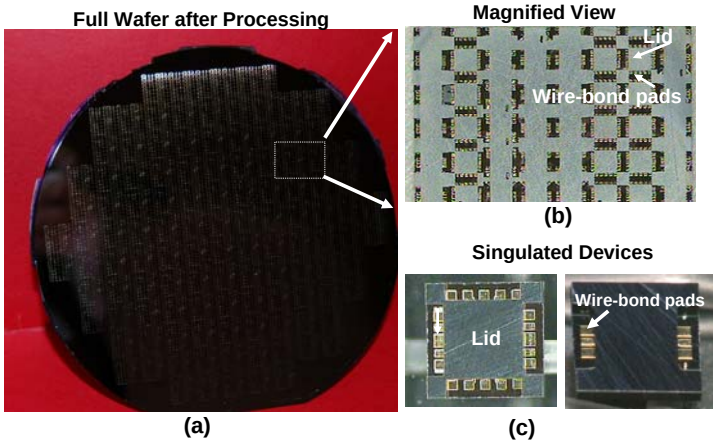


Figure 3: (a) The processed MEMS/lid assembled wafers. (b) Magnified view of the assembled wafers. (c) Singulated device showing exposed I/O pads.

II. Wafer-Level processes

The main steps involved in wafer-level experiments are shown in Figure 4.

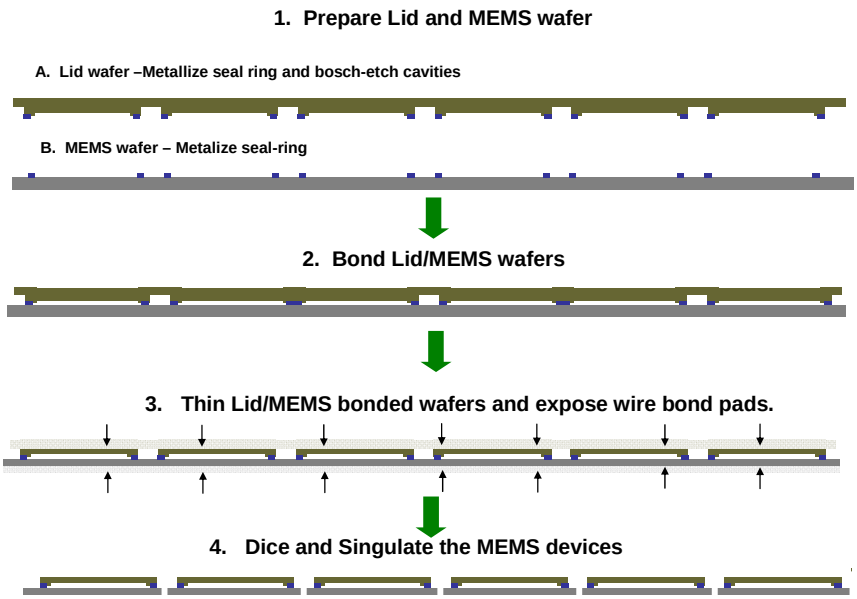


Figure 4: Wafer-level process steps

A. Lid and MEMS wafers Preparation

1. MEMS Wafers

The MEMS wafers used in this study were of >10KΩ-cm resistivity, 150 mm diameter and 675 μm thick containing AlN-based microresonator devices with Pirani gauges [11]. The Pirani gauges were included to measure in-situ vacuum pressure of the packaged devices and they were fabricated using the same process flow as the microsensors. The Signal/Power/Ground interconnections to the wire-bond pads exit the cavity by passing underneath the sealring and are isolated from the sealring metallization by an insulating AlN layer. After the MEMS wafers were fabricated, the sealring and wire-bond pad metallization was deposited. The sealring is 80 μm wide. The RF bond pads were 105 μm long and 75 μm wide coplanar transmission lines on 300 μm pitch and separated from the center pad with a gap of 40 μm. the other signal/power/ground pads are 100 μm square on 150 μm pitch. The metal-stack used in forming these patterns consisted of 20 nm Ti, 100 nm Pt and 500 nm Au. We have used both sputtered and evaporated metal films with success. The metal-stack was patterned with a sealring and wire bond pads using standard photoresist and metal lift-off techniques. After the sealring is patterned on the front side, a backside image is created

using evaporated metal lift-off technique to form the features necessary for alignment during the bonding operation. The last process step performed immediately prior to wafer bonding is the MEMS release step using XeF2 for removal of a polysilicon release layer.

2. Lid Wafers

The lid wafers used were >10Kohm-cm resistivity, <100> silicon, 150 mm diameter and 675 µm thick. The lid sealring pattern was formed using lift-off photolithography with an evaporated metal-stack of 20 nm Ti, 100 nm Pt, 440 nm Au, 500 nm Ge, and 100 nm Au. The lid metal width was sized to be smaller than the MEMS die sealring metal to ensure that it always makes full contact with the MEMS die metal sealring given alignment tolerance variation. Various geometries were tried, and a good hermetic seal was obtained using a 40 µm Lid sealring bonded to an 80 µm wide MEMS metal sealring.

As shown in Figure 2, this technology required two cavity depths in the lid – a 20 µm deep cavity in the center of the lid (over the MEMS) and a 120 µm deep cavity on the edge (over the wirebond pads). These cavities were formed by Bosch etching (Deep Reactive Ion etching). The lid after cavity formation is schematically illustrated in Figure 5a and the Scanning Electron Microscope (SEM) views of the finished lid is shown in Figure 5b.

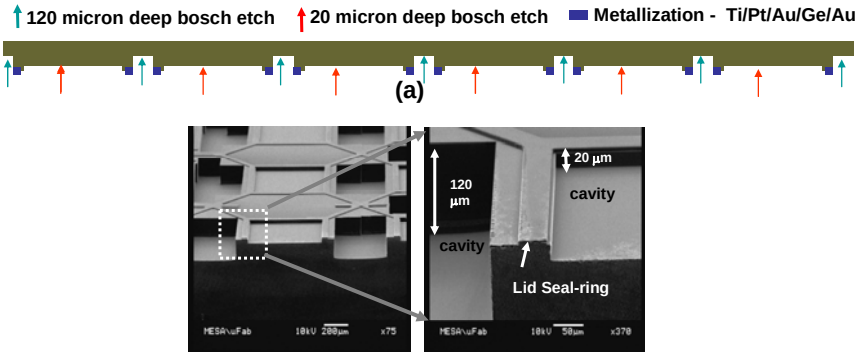


Figure 5: (a) Schematic drawing of the wafer with different depth Bosch-etched cavities. (b) SEM Micrographs of the finished section of the lid wafer showing 20 µm deep cavity in Lid area and 120 µm deep cavity in I/O pad area.

Deep reactive ion etching (DRIE) allows highly anisotropic, high-aspect ratio, deep etching of features in silicon wafers. Fabrication of the lid wafers incorporated a two-step lithography process that enabled two cavity structures of different depths. A photoresist hard mask and a conventional photoresist mask were used to fabricate the two structures.

Following metallization of the sealring metal-stack on the wafer, 5 μm of AZ-4330 photoresist was used to define the lid area as well as I/O pad area. The resist was then hard baked at 180C. In second lithography step, 3.5 μm of AZ-4330 photoresist was used to define the I/O pad area openings, which are the deeper of the two features. The wafer was then exposed to the initial DRIE and the I/O pad openings were etched to a 100μm depth. The conventional resist is then stripped using acetone so the hard baked resist remains in place. The wafer was then exposed to the second DRIE etch and etched to the depth of the 20 μm in the center lid area. During this etch cycle, the I/O pad area continued to etch for additional 20 μm, which gives a total depth 120 μm. The hard baked resist is removed using an oxygen ash process. When etching was completed, the center lid area 20 μm deep opening and the I/O pad area had 120 μm deep opening as shown in Figure 5b.

B. Wafer Bonding

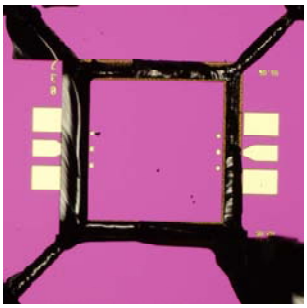
Past investigators [12-15] have used different varieties of wafer bonding materials and processes. These bonding techniques fall under one of the three broad categories, namely surface bonding (e.g. fusion and anodic bonding), metallic bonding (e.g. eutectic bonding) and insulation layer bonding (e.g. glass-frit bonding). For this technology, eutectic bonding of the MEMS wafer to the lid wafer is the best choice because (i) it will meet the alignment accuracy requirements, (ii) it will mitigate surface topology from lateral feedthroughs, and (iii) it will provide hermetic sealing at low cost. We have chosen Au-Ge eutectic bonding to demonstrate our technology because of our experience at Sandia in using this material in previous projects. The other likely eutectic bonding materials that could also have been chosen are Au-Si[16] and Au-Sn[16,17].

Immediately prior to aligning and bonding, the die and lid wafers were exposed to a short oxygen plasma treatment to reduce surface moisture and other contaminants. The alignment of the MEMS and lid wafers for bonding was done using EVG-620 alignment system. The wafer stack was aligned in a fixture, which was later transferred to the bonding chamber in the EVG520 bonder. The bonding was done at a slightly higher temperature than the Au-Ge eutectic temperature of 363^{o}C for 5 minutes in either vacuum (1E-4 mBar pressure) or in nitrogen environment with a bonding force of 3kN, which equated to 2.1 MPa pressure. After bonding, the temperature was ramped down to 200^{o}C in the bonder and then cooled to room temperature in ambient.

The bonding was characterized by shear testing the pieces (15mm x 15mm) of the bonded wafers. The shear force required to break the sample and inspection of the broken surfaces helped in optimizing the bonding conditions. As shown in Figure 7, if bonds are strong, the break in the shear test often occurred in silicon

near the sealring usually from the lid side. Another key characteristic of a strong bond was good metal alloy reflow with minimal or no squeeze-out from the bond line.

Inspection of lid wafer seal-ring after Shear test.



Silicon around seal-ring broke indicating a strong bond

Figure 7: Shear test sample showing a good bond, where silicon broke around the bond line.

C. Thinning of Bonded Wafers and Device Singulation

Thinning is an essential step in the process in this packaging technology as shown in Figure 2. Thinning of the lid is necessary for opening the bond pads access for interconnection to next-level assembly. We have thinned both MEMS and lid wafers to get a packaged device of thickness of < 200 μm to meet modern form-factor requirements. Since our lab equipment for thinning was not set-up for manufacturing, the turn-around time needed for thinning whole wafers was very long. In order to shorten the process development time, we used 1 cm to 3 cm square samples of MEMS/Lid bonded wafers. Even these small sample sizes yielded hundreds of devices per sample for process characterization. After the process development was completed, we have duplicated the process steps on full wafers at a commercial wafer thinning facility as shown in Figure 3a.

Prior to thinning, the samples were mounted on the lapping plate using wax as the bonding material. We followed the thinning step sequence as shown in Figure 2. Our initial experiments showed that thinning had to be done in several steps starting with coarse grinding followed by finer grinding. If this current sequence was not followed, the thinned device had micro-cracks, which will eventually result in the device breaking during handling. The MEMS side was thinned to 100 μm with a nearly scratch-free and crack-free surface. The typical thinning sequence for the MEMS side was (i) very coarse grinding with 9 to 15 μm slurry to remove ~500 μm of silicon, (ii) fine grinding with 3 μm slurry to remove ~35 μm of silicon, and (iii) very fine grinding with 1 and 0.5 μm slurry to remove the last ~10 μm of silicon. Next, the lid side was similarly thinned to 120 μm exposing the wire-bond pads. The typical thinning sequence used for the lid side was (i) fine grinding with 6 μm/3 μm slurries to remove 450 to 500 μm of silicon, and (ii) very fine grinding with 1 μm/0.5 μm slurries to remove the last 50 to100 μm of silicon. The grinding sequences as presented above have not been optimized for reducing grinding time or lowering the cost; however, this sequence

has consistently given high yields. After the bonded wafers were thinned, the samples were demounted from the grinding plate and cleaned using acetone and isopropanol.

The wafer was mounted on UV tape and sawed to singulate the resonators. The devices were then demounted and cleaned in acetone and isopropanol.

D. Next-Level Integration

These devices can be integrated into the next-level assembly either by wire-bonding or by surface mounting. Figure 8a shows the demonstration of a part wire-bonded to a Flex circuit board. As demonstrated, the devices can be wire-bonded without further processing. The surface mountable version is currently being developed by attaching solder balls to the pads as drawn in Figure 8b.

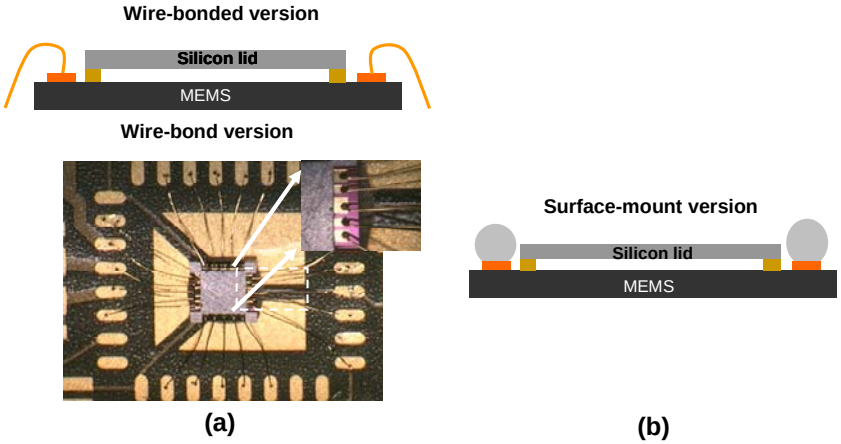


Figure 8: (a) Wire-bonded version. (b) Surface mount version.

III. Results

A. Pressure Testing

Because of the miniature (7 nL) volume of space between the device and the lid in these packages, we cannot reliably test the hermeticity using the standard gross and fine leak test techniques. Thus, the hermeticity of the package was tested with *in-situ* pirani gauges and resonator devices. The small-signal resistance of the pirani gauge changes from 10 kΩ to 25kΩ as the pressure varies from atmosphere to vacuum, and the Q of a 20 MHz resonator increases from ~1800 to ~2400 between high and low pressure. Based on measurements from these devices, it appears that the pressure inside of the package is in the 1-10 Torr range, which is consistent with previously reported[9] examples of miniature packages without getters. The results from our preliminary proof-of-concept demonstration experiments show that the wafer-level packaging provides the hermeticity in the package-lid assembly with yields of above > 50%. We have identified yield limiting failure modes to be related to the defects generated by photolithography and by inadequate cleaning. Higher pressures than as would be

expected in a vacuum environment are observed due to internal vaporization of absorbed surface contamination from the process chemicals. Further improvement in this pressure will require refinement of the pre-bonding cleaning and conditioning, and may also require the use of getters.

B. RF Performance

The RF performance of the package was tested by measuring a 0.6 mm-long coplanar waveguide transmission line (width = 75 µm, gap = 40 µm)that traversed the width of the package and was connected to test pads by two 20 µm-wide, 0.6 µm-thick traces passing underneath the 80 µm thick sealring insulated by aluminum nitride insulator. The measured and simulated performance is compared to an equivalent circuit model of the underpass in Figure 9. The measured performance is consistent with a shunt capacitance of 250fF and a series resistance of 3Ω per feedthrough. The low-frequency insertion loss of 0.3dB per feedthrough is limited by the series resistance, which may be improved by using thicker traces and improving the contact resistance between the trace and lower resistivity metals for the underpass.

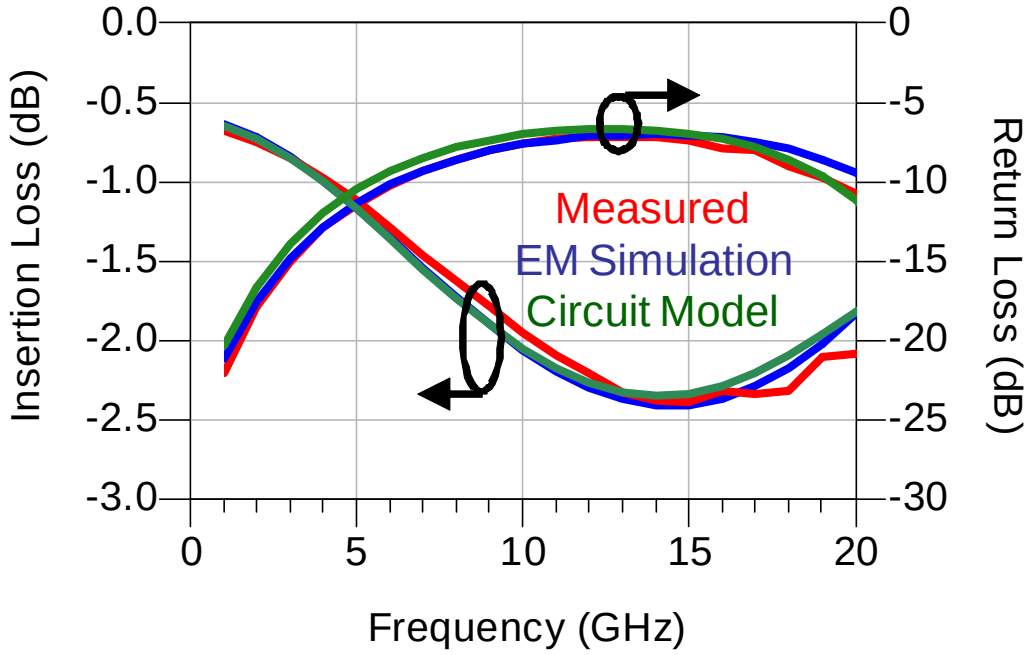


Figure 9: Measured, simulated, and circuit modeled insertion loss and return loss for a 0.6 mm-long transmission line connected to test pads outside of the package through two 0.6µm-thick, 20µm-wide tungsten feedthroughs passing underneath the 80µm-wide metal sealring.

IV. Preliminary Cost Analysis

Our cost analysis has shown that packaging cost of these devices when mass-produced with high yields will be $0.10 to $0.90 per device. Encouraged by these results, the next

steps in the development of these packages will be to continue with the refinement of our cleaning and bonding processes, full development of surface mountable packages and scaling to manufacturing

V. Conclusions

We report a new wafer-level packaging technology for miniature MEMS in a hermetic micro-environment. The unique and new feature of this technology is that it requires low cost wafer-level processes like eutectic bonding, Bosch etching and mechanical lapping and thinning steps as compared to more expensive process steps that will be required in other alternative wafer-level technologies involving thru-silicon vias or membrane lids. We have demonstrated this technology by packaging Silicon- based AlN microsensors in packages of size 1.3 x 1.3 mm^2 and 200 micrometer thick.

The technology involves first preparing the lid and MEMS wafers separately with the sealring metal stack of Ti/Pt/Au on the MEMS wafers and Ti/Pt/Au/Ge/Au on the lid wafers. On the MEMS wafers, the Signal/Power/Ground interconnections to the wire-bond pads are isolated from the sealring metallization by an insulating AlN layer. Prior to bonding the lid wafers were Bosch-etched in the wire-bond pad area by 120 μm and in the center hermetic lid area by 20 μm. The MEMS and the lid wafers were then aligned and bonded in vacuum or in a nitrogen environment at or above the Au-Ge Eutectic temperature, 363^{o}C. The bonded wafers were then thinned and polished first on the MEMS side and then on the lid side. The MEMS side was thinned to 100 μm with a nearly scratch-free and crack-free surface. The lid side was similarly thinned to 120 μm exposing the wire-bond pads. After thinning, a 100 μm thick lid remained protecting the MEMS features and providing a 20 μm high hermetic micro-environment. Thinned MEMS/Lid wafer-level assemblies were then sawed into singulated devices. These devices can be integrated into the next-level assembly either by wire-bonding or by surface mounting.

The wafer-level packaging approach developed in this project demonstrated RF feed throughs with <0.3 dB insertion loss to 2 GHz. The pressure monitoring Pirani structures built inside the hermetic lids have demonstrated the ability to detect any leaks in the hermetic packages. In our preliminary development experiments, we have demonstrated >50% hermetic yields and have identified yield limiting failure modes to be caused by the photolithography defects and by inadequate cleaning.

Our initial cost analysis has shown that when mass-produced the packaging of these devices will cost $0.10 to $0.90. We are currently developing large-scale manufacturing processes with reduced defects.

References

[1] Chanchani, Rajen, Keith Treece and Paul Dressendorfer**,** "A New mBGA Multichip Module Technology," Published in International Journal of Microelectronics and Packaging, September, 1995, vol. 18, no. 3, p 185-92. Also in Proceedings of ISHM Annual Meeting, Boston, November, 1994 p 196-201.

[2] Chanchani, Rajen, “mini Ball Grid Array (mBGA) Assembly on Low Cost MCM-L Boards,” Proceedings of the Electronic Components and Technology Conference, May, 1997, San Jose, p 656-63.
[3] Riley, George, “Wafer-level hermetic cavity packaging,” Advanced packaging, 13, May 2004, pp 21-24.
[4] Evans, Daniel D., Jr., “Advances in MEMS Packaging,” Advanced Packaging, 13, April, 2004, pp 1-5.
[5] Iannacci, J et al, “Parasitic Effects Reduction for Wafer-level Packaging of RF-MEMS,” Proceedings of Design, Test, Integration and Packaging of MEMS/MOEMS, Stresa, Italy, 26-28, April, 2006. ISBN:2-916187-03-0.
[6] Choa, Sung-Hoon, “Reliability study of hermetic wafer level MEMS packaging with through-wafer interconnect,” Microsystem Technologies (2009) 15, pp 677-686.
[7] Premchandran, C. S. et al, “Design, fabrication, and testing of wafer level vacuum package for MEMS device,” Proceedings of 56th Electronic Components and Technology Conference, San Diego, CA, May, 2006, pp 1136-1140.
[8] US Patent Number 7,851,925 B2, Issued December 14, 2010.
[9] Chae, Junseok, Giachino, Joseph M., and Najafi, Khalil, “Fabrication and Characterization of a wafer-level MEMS Vacuum package with vertical feedthroughs,” Journal of Microelectromechanical Systems, 17, No. 1 February 2008.
[10] Monajemi, Pejman et al, “Wfer-level MEMS packaging via thermally released metal-organic memberanes,” Journal of Micromechanical Microengineering, 16, (2006), pp 742-750.
[11] Olsson, R. H. III et al, “Post-CMOS compatible Auminum Nitride MEMS filters and resonant sensors,” Proceedings of IEEE Frequency Control Symposium, Geneva, Switzerland, , pp 412-419, June 2007.
[12] Chanchani, Rajen, “3D Integration Technologies – An Overview,” Chapter 1, *Materials For Advanced Packaging*, edited by Daniel Lu, C.P. Wong, Published by Springer, 2009, pp 16-28. ISBN 978-0-387-78218-8.
[13] Topol, A. W. et al, IBM J. Res. & Dev., 50, No. 4/5, July/September, 2006, pp 491-506.
[14] Lee, C. C. et al,”Advanced Bonding/Joining techniques,” Chapter 2, *Materials For Advanced Packaging*, edited by Daniel Lu, C.P. Wong, Published by Springer, 2009, pp 51-76. ISBN 978-0-387-78218-8.
[15] Kohl, Paul A. et al,” Advanced Chip-to-substrate Connection,” ,” Chapter 3, *Materials For Advanced Packaging*, edited by Daniel Lu, C.P. Wong, Published by Springer, 2009, pp 77-112. ISBN 978-0-387-78218-8.
[16] Pecht, Michael, Book – *Integrated circuit, hybrid, and multichip module package design guidelines: a focus on reliability*. Wiley-IEEE, 1994, Technology and Engineering. Page 376.
[17] Zhou, Tao et al, “An/Sn Solder Alloy and its Applications in Electronic packaging,” http://www.coininginc.com/files/admin/english_gold_tin_paper.pdf