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Radiation Effects in 3D Integrated SOI SRAM Circuits

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Abstract:

Radiation effects are presented for the first time for 3D vertically integrated 3 x 64-kb SOI SRAM circuits fabricated using Lincoln 3DIC technology. Ionizing dose, tier-to-tier single event upset cross-section, and angle effects are discussed.

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I. INTRODUCTION

3D integrated circuits are an emerging technology to continue improving system performance beyond the end of Moore's Law [1]. This approach can significantly increase integration density, reduce interconnection length and enable integration of heterogeneous materials, technologies and functionality components in a monolithically integrated process. Lincoln Laboratory has developed a wafer-based 3D technology that enables stacking of multiple IC wafers (or tiers) [2]. This approach is well suited for high-density stacking of heterogeneous technologies because the substrates from the stacked tiers are removed, and oxide-through vias are used for short electrical interconnects. Several designs have been demonstrated including a large-area 8 x 8 mm^2 high-3D-via-count 1024 x 1024 visible imager [3], a 64 x 64 laser-radar focal plane based on single-photon-sensitive avalanche photodiodes [4], a 10Gb/s/pin low power interconnect for 3DICs [5], and an imaging array with InP diode and Si CMOS readout tiers [6]. We reported earlier that total ionizing dose (TID) effects in n-channel FETs (nFETs) in the bottom tier were similar to those on standard single tier wafers [7]. Less positive charge build-up was observed for wide nFETs on the upper tiers, which was associated with the absence of silicon material below the BOX.

This paper reports for the first time on the radiation effects in SOI SRAM circuits operating at 1.25 V and densely vertically integrated on three tiers. TID effects and low-to-high energy proton irradiation data are discussed. We found that the proton irradiation effects in the 3D SRAM circuits are similar to those on a single tier 2D SRAM. The other tiers can be effectively modeled as a modified backend of line (BEOL) stack. We also demonstrate that the current 3DIC process is tolerant to TID. 3DICs are promising candidates for space applications.

II. 3D FABRICATION PROCESS

The three-tier Integrated Circuits (ICs) characterized in this work were fabricated in the third DARPA-sponsored 3D multiproject run (3DM3). The process begins with fabricating three individual tiers of fully depleted SOI (FDSOI) circuit tiers, with a 150-nm FET gate length, 40-nm-thick SOI active layer and a 400-nm buried oxide (BOX), a dual threshold CMOS, Co-silicided polygates with a silicide block layer, and three metal interconnect layers. 3D integration begins with oxide-oxide bonding of tier-1 and tier-2 wafers. The tier-2 substrate is then removed by grinding and wet chemical etching, stopping on the tier-2 SOI buried oxide layer. Electrical interconnection is formed by through-oxide vias to tier-2, 3D vias from tier-1 to tier-2, and a tier-2 back metal layer. The process is then repeated with tier3. 3D-IC with eleven interconnect-metal layers and dense unrestricted 1.75-μm-diameter 3D vias interconnecting stacked circuit layers. The SRAM active circuitry is confined within in a 21-μm-thick layer above the SOI substrate.

Upon completion of single tier fabrication and again after 3D integration, an extensive series of tests is performed to characterize transistor and circuit performance to monitor the effect of wafer integration. Id-Vg characteristics for tiers 1, 2, & 3 are essentially unchanged by the 3D process, although FETs on each tier have somewhat different electrical characteristics. Id-Vg curves will be shown in the full paper.

III. CIRCUIT DESCRIPTION AND RADIATION TESTING EXPERIMENTS

The baseline 64-kb SRAM core is organized as a 512-row by 128-column array, includes fully-static CMOS decoders, and an address re-encoder for testability and variable timing. Data are accessed via 4-bit buses, using 14-bit addressing. The SRAM cell has 6 transistors with n-channel FET pass-gates, conventional layout, *i.e.*, with no body ties. It is not optimized for speed or power, and it is primarily used for circuit validation and fabrication debugging. The 3D SOI SRAM consists of three instantiations of the 64-kb SRAM core, multiplexed to operate as a single memory. The total memory size is 192-kb, with tier selection controlled by two additional pads. Figure 1 shows that the SRAMs on tier 3, tier 2 and tier 1 are located 2,600 nm, 9,900 nm and 20,350 nm below the passivation surface. The SRAMs on tier 2 and 3 are inverted compared to that on tier 1. The tier-to-tier circuit alignment is a function of the wafer-to-wafer alignment during tier integration, and it is nominally +/- 0.75 μm. Both 3D and 2D SOI SRAM circuits were packaged in a 40-pin dual in-line package. The 2D SRAM is a single tier SOI tier 1-like SRAM circuit of the baseline 64kb SRAM core. Circuits were irradiated under constant biasing of 1.25 V, with a back substrate voltage at

0-V and no lid on the package. Note that the 3D W-filled vias are located a minimum of ~ 230-µm from the SRAM bit cells; that is much longer than the range of low-energy secondaries generated by proton/silicon nuclear interactions. However standard W-contacts and vias are used throughout the SRAM circuit and are located less than 0.5 µm away from the cell FET active region.

Circuits were irradiated at the TRIUMF Proton Irradiation Facility in Vancouver, Canada [8]. This facility provides mono-energetic proton beams from 65 to 500 MeV with energies down to 20 MeV obtained by degrading the low energy beam. Proton fluxes up to 10^{11} $cm^{-2}s^{-1}$ can be achieved with uniform beams up to 7.5 cm diameter. The SRAM was tested before and after radiation increments using an FPGA board remotely controlled from a laptop. A checkerboard pattern of "0" and "1" was written and read right before irradiation. Then, the memory was read right after irradiation as soon as the proton beam was turned off. Because of the memory size and the small sensitive volume of the FDSOI cell transistors (defined by the area under the gate, *i.e.*, 900-nm x 150-nm x 40-nm for the cell), proton fluences ~ $1x10^{11}$ cm^{-2} were required to measure a statistically meaningful number upsets without accumulating too much TID. This is because standard unhardened FDSOI technology is sensitive to ionizing radiation because of charge trapped in the BOX below the active SOI layer [9]. Because of the front-to-back capacitive coupling, significant device parametric shifts can be observed unless the BOX has been treated to mitigate these effects. The I_{DD} supply current is measured before and after irradiation to evaluate TID effects.

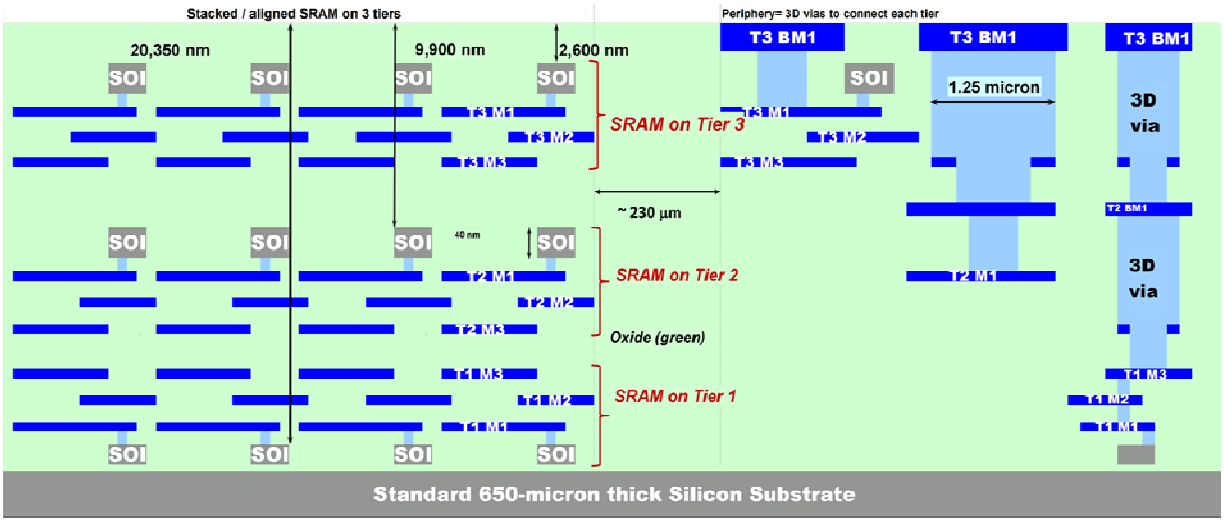

Figure 1: Illustration of MITLL 3D SRAM Circuit. The 3D vias are small enough to be useful in large numbers inside circuits, but for this application they were only needed in the periphery. "BM" stands for Back Metal layer ("Back") because it on the back of the SOI.

IV. RESULTS AND DISCUSSION

TID effects: The worst TID accumulation occurs for proton energies of 500 MeV. This may be due to a higher charge yield for the very high energy proton irradiation [10]. Figure 2 shows the variation in supply current versus total dose for proton energies of 500 MeV.

The 2D SRAM with a standard BOX has an I_{DD} current that increases starting at 30 krad (Si), while it remains unchanged for 2D SRAM with a modified BOX. The modified BOX fabrication process is effective at mitigating TID effects. The I_{DD} current of the 3DSOI SRAM also remains unchanged with total dose. This result indicates that the transistors on all of the three tiers are tolerant to total ionizing dose effects. This is explained because a) the tier1 wafer had a modified BOX, and as shown in previous work, transistors on tiers 2 and 3 are much less sensitive to total dose effects than that of FETs on a standard single tier wafer [7]. These results illustrate that the TID hardness of the 3D SRAM is better than 100 krad(Si).

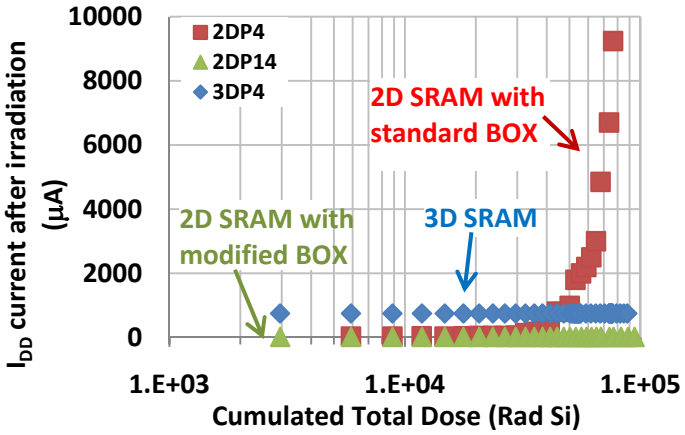

Figure 3: 2D 64-kb and 3D 192-kb SOI SRAM I_{DD} supply current versus total dose for 500 MeV protons.

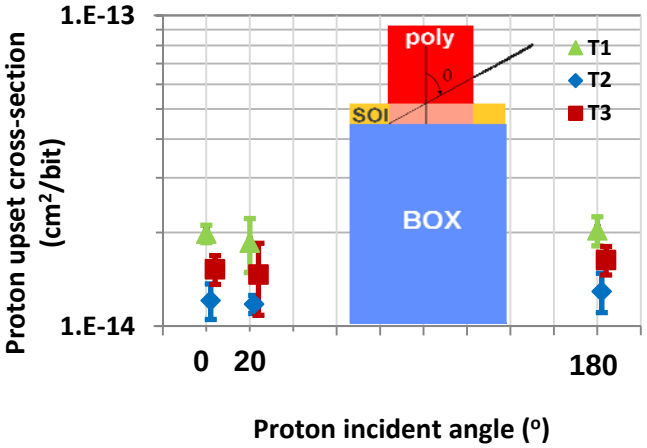

Figure 2: Median cross-section versus proton incident angle, θ, in the plane of the gate length (illustrated on the right) for a typical 3DSOI SRAM. The error bars are the standard deviation of repeated measurements.

SRAM cross-section: The 3D SRAMs were irradiated under various θ angles in the plane of the gate length (see Figure 3). For these angles one does not expect to see much variation in the charge collection volume, so 3D effects are expected to dominate. Figure 3 shows the proton upset cross-section in cm^2/bit for each tier and proton incident angles of 0, 20 and 180°. Note that at 180°, the 500-MeV protons are going through the board and the package.

Results show that the median upset cross-section is lower on tier 2 compared to that on tiers 1 and 3 regardless of the proton incoming angle. Since the FETs on tiers 2 and 3 are inverted compared to that on tier 1, we conclude that the lower cross-section on tier 2 is not caused by the 3D integration process. Removal of the silicon substrate on tier 2 and 3 does not significantly impact the upset cross-section either. We found that the difference in upset cross-section between tiers is consistent with the variation in the nFET widths and gate lengths observed wafer-to-wafer and lot-to-lot in the FDSOI process. As stated in section II, the 3D integration process did not change the FETs electrical characteristics. However, these characteristics were slightly different prior to 3D integration. The cross-section values measured for the 3D SRAM are within the range of cross-section values measured for 2D SRAM indicating that the upset events occurring on one tier are uncorrelated with the events occurring on another tier.

The change in the upset cross-section with the proton incident angle is within one standard deviation of repeated measurements. For a proton incident angle of 0 and 180° and on all three tiers, the data follow a normal distribution, and the standard deviation is equal to the root square of the mean of the data. Consequently, the proton upsets are independent from each other, and there are no significant tier-to-tier effects. The error bars on tiers 1 and 3 for a 20° incident angle are larger than expected for a normal distribution. This result is not well understood at this time, but it could indicate some tier-to-tier effects do happen, although these effects should have also been seen on tier 2.

These results indicate that, in the 3D SRAM, proton-silicon reactions are the dominant mechanisms responsible for the upset events measured on each tier. Consistent with the results published in [11] for an older single tier FDSOI technology (L = 0.2 µm), the proton upset sensitivity is driven by the sensitive volume defined by the cell nFET gate width, length and the SOI thickness (*e.g.*, 0.0054 μm^3 in this work), and there is no significant change in the upset cross-section between front to back irradiation.

Figure 4a. shows the physical location of the upsets for the SRAM on each tier and for 500-MeV protons (0^{o}). The bitmaps were slightly offset in the + x direction to improve the visibility of coincident upsets. These bitmaps confirm that the upsets are randomly distributed across the 3 x 64-kb memory size. Also, the upsets on each tier are independent from each other. Figure 4b. shows the upset cross-section as a function of the proton energy for the 3D SRAM. Tier-to-tier variation is similar to what was measured at 500 MeV. There are no indications of direct proton ionization effects in these data (*i.e.*, a sharp increase in SEU cross section at low proton energies). However, to observe direct proton ionization effects, finer steps in proton energy may be required at very low energies. Indeed, SRIM simulations show that the incident proton energy would need to be < 2 MeV for the Bragg peak to fall within the active SOI regions of the 3D SRAM circuit [12]. Additional experiments are planned with neutrons on the same 3D SRAM as well modified designs to investigate further any particular differences between the 2D and 3D SRAM designs.

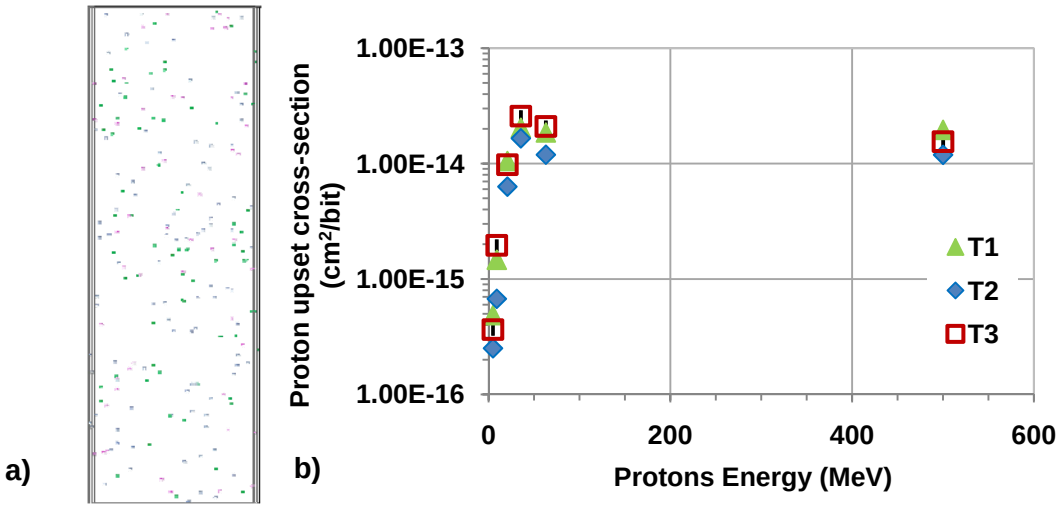

Figure 4: (a) Bitmaps showing the physical location of single event upsets induced by 500 MeV protons on tier 1 in blue, tier 2 in pink and tier 3 in yellow. The upsets are randomly distributed. (b) Upset cross-section as a function of the proton energy for a 3D SOI SRAM.

V. CONCLUSION

Radiation effects are presented for the first time for vertically integrated 3 x 64-kb SOI SRAM circuits. The 3D integration process is an effective novel approach to stacking high performance ICs with a high density. The 3D SRAMs are shown to be tolerant to ionizing radiation up to a total dose of at least 100 krad (Si). We found that the proton irradiation effects in the 3D SRAM circuits are similar to that on a single tier 2D SRAM. The other tiers can be effectively modeled as a modified BEOL stack. Thus, this work demonstrates that radiation-hardened vertically integrated 3D circuits can be fabricated making them suitable for space and military applications.

VI. REFERENCES

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