

Thin Gold to Gold Bonding for Flip Chip Applications

Lauren E. S. Rohwer and Dahwey Chu, *Senior Member, IEEE*
 Sandia National Laboratories
 P.O. Box 5800, MS-0892, Albuquerque, New Mexico 87185
 leshea@sandia.gov, 505-844-6627

Abstract

We have demonstrated a solderless flip chip bonding process that utilizes electroless nickel / palladium, immersion gold pad metallization. This mask-less process enables higher interconnect densities than can be achieved with standard solder bump reflow. The thin (100nm) immersion gold surfaces were coated with dodecanethiol self-assembled monolayers. Strong gold to gold bonds were formed at 185°C with shear strengths that exceed Mil-Std 883 requirements. Gold stud bumps are also promising for flip chip applications, and can be bonded at 150°C when the gold surfaces are properly pre-treated - dilute piranha solution, argon plasma, and dodecanethiol SAM treatments work equally well.

Introduction

This study was motivated by the need for a flip chip bonding process that enables bonding of devices with higher interconnect densities and finer pitches than can be bonded with solder bumps. We explored two standard under bump metallization technologies: electroless nickel immersion gold (ENIG) and electroless nickel, electroless palladium, immersion gold (ENEPIG) as bonding materials. These electroless plating processes are typically maskless. The ability to bond ENIG/ENEPIG pads enables advancements such as direct flip chip interconnects using ENIG/ENEPIG bump metallization.

Thermosonic gold wire bonding to ENIG [1,2] and ENEPIG [3,4] pads having 100nm immersion gold is accomplished routinely for printed circuit technology. In fact, ENIG and ENEPIG are now low-cost, maskless alternatives to ~400nm to 1µm thick, soft gold electrolytic metallization [2]. In studies of thermosonic gold wire bonding to ENIG [5] and ENEPIG [6] metallization, plasma cleaning was found to be essential for achieving consistent adhesion with reduced bonding temperatures [2,5] and having a wider wire bonding process window. The process window refers to the range of bond power and temperature over which strong wire bonds are formed. Typically, argon or argon-oxygen plasmas are employed. The plasma power, exposure time, and hold time prior to bonding are the key parameters. A short duration (1 to 3 minutes) exposure to a 100W plasma has been found to be sufficient to remove the organic contaminants from the gold surface. Wire bonding is typically done within 1 to 8 hours of plasma cleaning.

Previous work on gold to gold flipchip bonding has employed thicker gold layers on the flip chip bond pads. Gold bumps ranging from 2µm to 50µm tall have been used to integrate optoelectronic devices [7,8]. These studies report that surface activation with argon plasma enables strong bonds at 150°C. Plasma treatment also enabled bonding of 600nm gold films to 150nm gold films at 100°C to 150°C [9]. As with gold thermosonic wire bonding, 100W argon or

argon-oxygen plasmas have been found to be effective at reducing the temperature for gold to gold flip chip bonding.

Other studies of gold to gold flip chip bonding of thick gold have concluded that when the gold is coated with dodecanethiol self-assembled monolayers (SAMs), the bonding temperature can be reduced [10,11]. Dodecanethiol was reported to act as a lubricant and a passivation layer. With treated gold surfaces, gold to gold bonding can be done at lower temperatures than are possible with untreated gold. Moreover, X-ray photoelectron spectroscopy studies have shown that gold surfaces coated with dodecanethiol SAMs have less oxygen and carbon contaminants than uncoated gold surfaces [12]. This finding helps explain why dodecanethiol coated copper bond pads can be wire bonded after longer storage times than uncoated bond pads [13]. There is no reason to suspect that dodecanethiol will result in stronger gold to gold bonds considering that it desorbs at ~117°C, which is below the typical bonding temperature of 160°C [8].

Using the results of these previous studies as a guide, our goal is to develop a flip chip bonding process for 100 nm immersion gold layers. In this paper, we discuss our preliminary findings of bonding experiments with gold stud bumps, ENIG bumps and ENEPIG bumps.

Experimental Procedure

Our experiments used several different flip chip bump test samples. The first type of bumped test flip chip die consist of ~1cm square silicon die with an 8x8 array of gold stud bumps (Figure 1). These 8x8 arrays were made by wire bonding 25µm gold wire on to 100µm square pads with 1µm thick gold on a 200nm thick titanium adhesion layer.

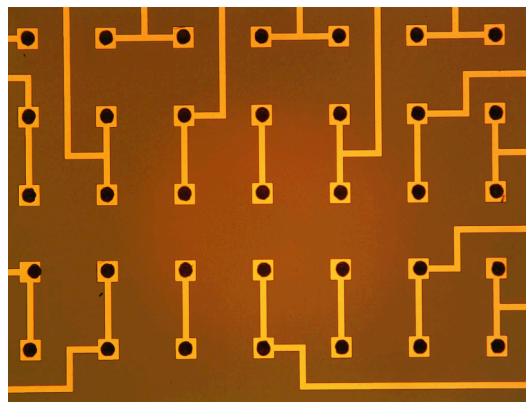


Figure 1. Optical microscope image of gold stud bumps (dark circles) on square gold pads

The second and third type of bumped test flip chip die consist of 24x40 arrays of ENIG or ENEPIG bump metallization on aluminum pads. The ENIG/ENEPIG

metallization on 150mm wafers were made by Pac Tech USA Inc. (Figure 2). The aluminum pad size on the test die was 100 μ m and octagonal in shape. The pad passivation openings are ~80 μ m and octagonal in shape on 400 μ m pitch in the x direction and 200 μ m pitch in the y direction. The ENIG bump metallization consists of 5 μ m, 10 μ m, 15 μ m, 20 μ m, or 25 μ m thick nickel and 100nm thick of gold. The ENEPIG bump arrays have the same thicknesses of nickel and gold as the ENIG pads, plus a 0.35 μ m thick layer of palladium beneath the gold. Figures 3 and 4 show the cross section of an ENEPIG bump. The ENIG or ENEPIG bumped arrays were bonded together (ENEG to ENIG, ENEG to ENEPIG, ENEPIG to ENEPIG) or were bonded to 10mm x 10mm silicon substrates coated with a blanket film of 1 μ m thick evaporated gold on a 200nm titanium adhesion layer (ENEG to gold, ENEPIG to gold).

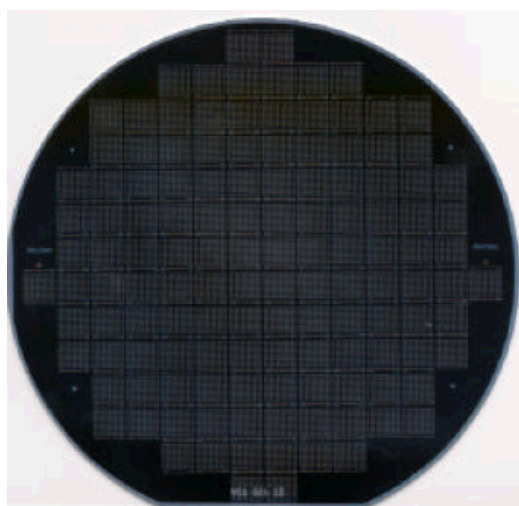


Figure 2. ENIG or ENEPIG bumped wafer [14].

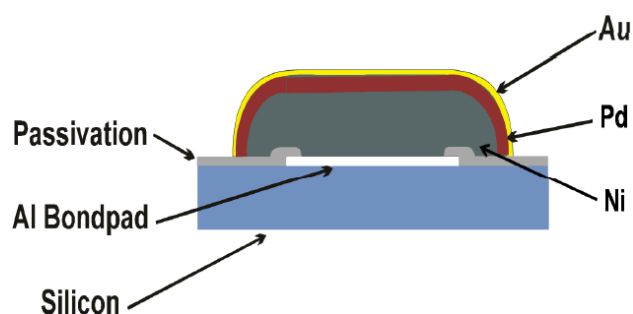


Figure 3. Cross section of ENEPIG bump [15].

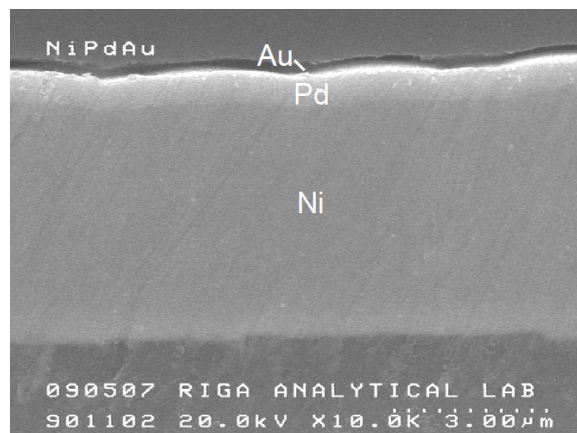


Figure 4. SEM image of an ENEPIG bump in cross section [15].

The gold surfaces of the test die were either coated with dodecanethiol SAMs; argon plasma cleaned for 5 minutes (375W, 15 psi); or cleaned in a dilute piranha solution (5:1:1 solution of deionized water, H₂SO₄, and 30% H₂O₂) for 5 minutes. Before SAM coating, the gold was cleaned in dilute piranha for 5 minutes, rinsed in water, air-jet dried, then immersed in a 1mM solution of dodecanethiol in ethanol for 24 hours, rinsed in ethanol, and air-jet dried. The time till bonding ranged from 0 to 8 days for the SAM coated parts.

The bonds were made using a Finetech Lambda flip chip bonder at 150-155°C for 30-45 seconds under 20N of force; and 185°C for 20 minutes under 25N or 200N of force for the gold stud bump and the ENIG / ENEPIG arrays, respectively. The bonds were sheared using a Dage 4000 shear tester.

Results and Discussion

Gold stud bump bonding.

Three surface treatments (dilute piranha clean, argon plasma clean, and dodecanethiol SAM coating) were used for the gold stud bump bonding experiments. The bonding was done immediately after the surface treatment. The 25 μ m thick gold stud bumps formed strong bonds at 150°C -155°C, whose shear strengths were independent of the surface treatment. The average shear strength was ~1.2kg. The bonding temperatures are comparable to those reported in previous studies of argon plasma cleaned gold bumps [7-9]. The bonds were formed in 30-45 seconds under moderate force (18N-20N).

ENIG / ENEPIG arrays bonded to gold films.

Our next experiments involved bonding the ENIG/ENEPIG arrays having 100nm thick immersion gold on the pad surfaces to 1 μ m thick blanket gold films on silicon substrates. Figure 5(a) shows an SEM image of the ENIG pads. Higher magnification images of the pad surfaces are shown in Figure 5(b) and (c).

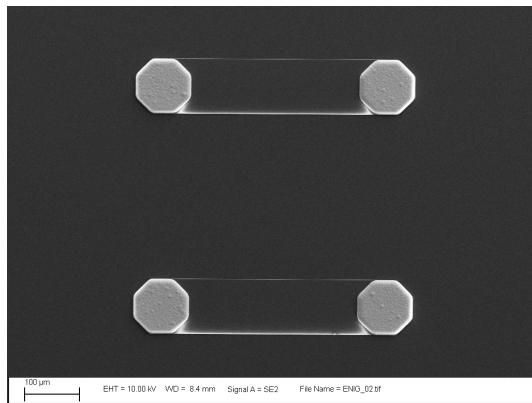
The arrays and substrates were coated with dodecanethiol SAMs and bonded at 185°C under 25N and 200N of force. The lighter force was not sufficient to form strong bonds that meet the Mil-Std 883 die shear strength requirement of 1kg.

Strong bonds were formed when the arrays were bonded under 200N at 185°C for 20 minutes.

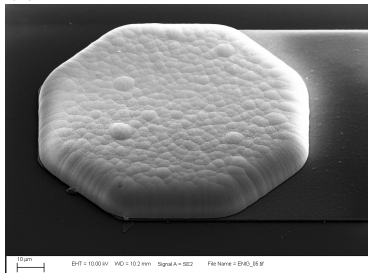
The shear strength data from the ENIG / ENEPIG array bonding experiments did not point to any improvement in bondability due to the presence of a SAM coating. In fact, there is a large variation in shear strengths that is not correlated to the hold time prior to bonding.

ENIG/ENEPIG arrays bonded together.

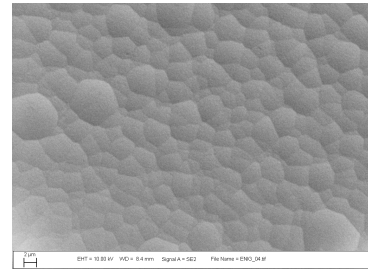
Preliminary experiments have shown that SAM coated ENIG/ENEPIG arrays bond in at 185°C, and 200N when the bonding time was increased from 20 to 30 min.



(a)



(b)



(c)

Figure 5. SEM images of (a) ENIG pads, (b) pad surface, and (c) morphology of the grains.

Conclusions

This study shows the feasibility of ENIG and ENEPIG bumps for solderless flip chip bonding. The ENIG/ENEPIG pad arrays with 100 nm thick immersion gold films bonded to 1 μm thick gold films at 185°C. These arrays were coated with dodecanethiol self-assembled monolayers. Gold stud bump arrays formed strong bonds at 150°C to 155°C regardless of the surface treatment used (dodecanethiol

SAM coated, argon plasma cleaned, or dilute piranha cleaned). An advantage of SAM coating the gold surfaces is that the hold time or storage time prior to bonding can be extended, compared to that of argon plasma cleaned gold surfaces. Our future work will focus on comparing the SAM coating and plasma cleaning treatments for thin gold to gold flip chip bonding in more detail.

Acknowledgments

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. We thank Alicia Baca, Sharon Benson-Lucero, Javier Gallegos, Suzi Grine-Jones, Ken McGuire, and Ben Thurston for their contributions.

References

1. Kim, J. K. and Au, B. P. L., "Effects of metallization characteristics on gold wire bondability of organic printed circuit boards," *Journal of Electronic Materials*, Vol. 30, No. 8, (2001), pp. 1001-1011.
2. Chan, Y. H., Kim, J-K., Liu, D., Liu, P.C.K., Cheung, Y-M., Ng, M. W., "Process Windows for Low-Temperature Au Wire Bonding," *Journal of Electronic Materials*, Vol. 22, No. 2, (2004), pp. 146-155.
3. Johnson, R.W., Palmer, M.J., Bozack, M.J., Isaacs-Smith, T., "Thermosonic gold wire bonding to laminate substrates with palladium surface finishes," *IEEE Transactions on Electronics Packaging Manufacturing*, Vol. 22, No.1, (1999), pp.7-15.
4. Ng, B. T., Ganesh, V. P., Lee, C., "Optimization of gold wire bonding on electroless nickel immersion gold for high temperature applications," *Electronics Packaging Technology Conference, 2006, EPTC '06*, pp. 277-282.
5. Chan, Y. H., Kim, J-K., Liu, D., Liu, P. C. K., Cheung, Y-M., Ng, M. W., "Effect of plasma treatment of Au-Ni-Cu bond pads on process windows of Au wire bonding," *IEEE Transactions on Advanced Packaging*, Vol. 28, No. 4, (2005), pp. 674- 684.
6. Oezkoek, M., Ramos, G., Metzger, D., Roberts, H., "Benefits of pure palladium for ENIG and ENEPIG surface finishes," *Electronic System-Integration Technology Conference (ESTC), 2010* pp.1-6.
7. Takigawa, R., Higurashi, E., Suga, T., Sawada, R., "Low-temperature bonding of laser diode chips on Si substrate with oxygen and hydrogen atmospheric-pressure plasma activation," *2009 Conference on Electronic Packaging Technology & High Density Packaging (ICEPT-HDP)*, pp. 475-477.
8. Higurashi, E., Chino, D., Suga, T., Sawada, R., "Au-Au surface-activated bonding and its application to optical microsensors with 3-D structure," *IEEE J. Sel. Top. Quant. Electron.*, Vol. 15, No. 5 (2009), pp. 1500-1505.
9. Higurashi, E., Imamura, T., Suga, T., Sawada, R., "Low-temperature bonding of laser diode chips onto silicon substrates using plasma activation of Au films," *IEEE Photonics Technology Letters*, Vol. 19, No. 24 (2007), pp. 1994-1996.

10. Ang, X.F., Li, F.Y., Tan, W.L., Chen, Z., Wong, C.C., "Self-assembled monolayers for reduced temperature direct metal thermocompression bonding," *Appl. Phys. Lett.*, Vol. 91, (2007), pp. 061913(1)-061913(3).
11. Chin, L.C., Ang, X.F., Wei, J., Chen, Z., Wong, C.C., "Enhancing direct metal bonding with self-assembled monolayers," *Thin Solid Films*, Vol. 504, (2006), pp. 367-370.
12. Laiho, T., Leiro, J.A., "Influence of initial oxygen on the formation of thiol layers," *Appl. Surf. Sci.*, Vol. 252, (2006), pp. 6304-6312.
13. Whelan, C.M., Kinsella, M., Carbonell, L., Ho, H.M., Maex, K., "Corrosion inhibition by self-assembled monolayers for enhanced wire bonding on Cu surfaces," *Micro. Engr.*, Vol. 70, (2003), pp. 551-557.
14. Pac Tech USA Inc. Test Chip 2.3 Brochure, <http://www.pactech-usa.com>
15. Teutsch T., "ENIG vs. ENEP(G) Under Bump Metallization for Lead-free WL-CSP Solder Bumps – a Comparison of Intermetallic Properties Using High Speed Pull Test," *IMAPS International Conference on Device Packaging*, 2008.