SAND2011-2734C

Evaluation of the Leon3 Soft-Core Processor within a Xilinx Radiation Hardened Field Programmable Gate Array

XRTC Conference

April 2011

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Acknowledgements

- Xilinx and the Xilinx Radiation Test Consortium (XRTC):
  - Providing the use of beam time to conduct experiments.
- Aeroflex Gaisler:
  - Providing design considerations for testing.

Outline

- Rationale
- Background
- Test Setup
- Results
- Conclusion

Rationale

- Evaluate the radiation environment performance of the Leon3 soft-core processor in a radiation hardened SRAM-based Field Programmable Gate Array (FPGA).
- Comparison of two cores:
  - Open-source Leon3 core
  - Fault-tolerant (FT) Leon3 core

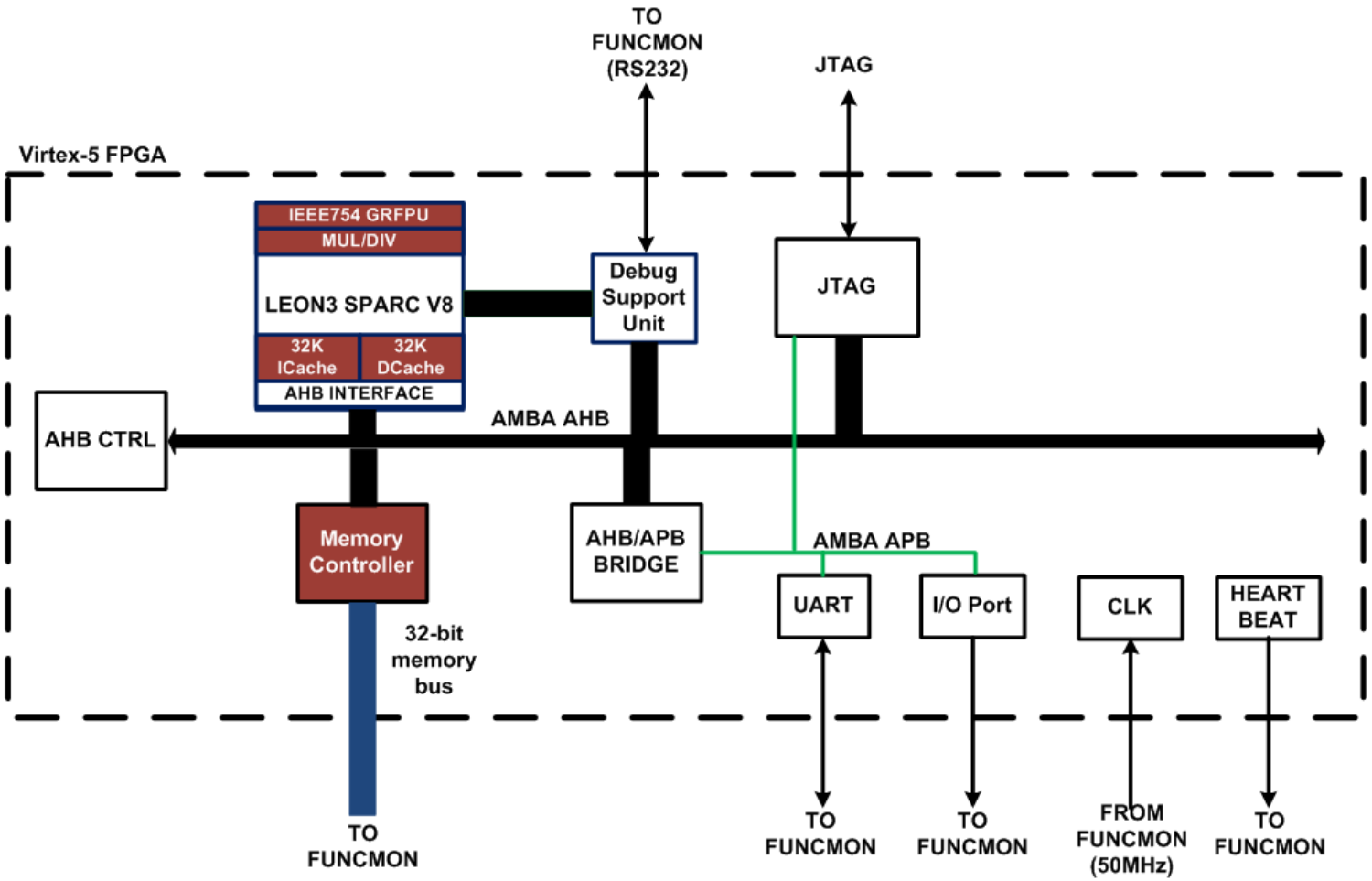
Leon3 Background

- Aeroflex-Gaisler 32-bit SPARC v8 Soft-Core processor.
- Two versions offered:
  1) Open-source, unmitigated core
     - Highly configurable
     - Full source code available under the GNU GPL license
  2) Licensed core
     - Referenced also as fault-tolerant.
       - Designed to be fault-tolerant within one-time programmable (OTP) FPGAs, i.e. Actel RTAX.
       - Leon3FT Radiation test data is available on the RTAX.
       - Focused on the protection of on-chip RAM blocks.
     - Similar version also provided for use in SRAM-based FPGAs.
       - Source code is not available.
       - Preconfigured Netlist.
       - Can be customized by requesting changes to Aeroflex-Gaisler.
       - Limited radiation testing has been conducted to assess radiation hardness of this core within SRAM-based FPGAs.

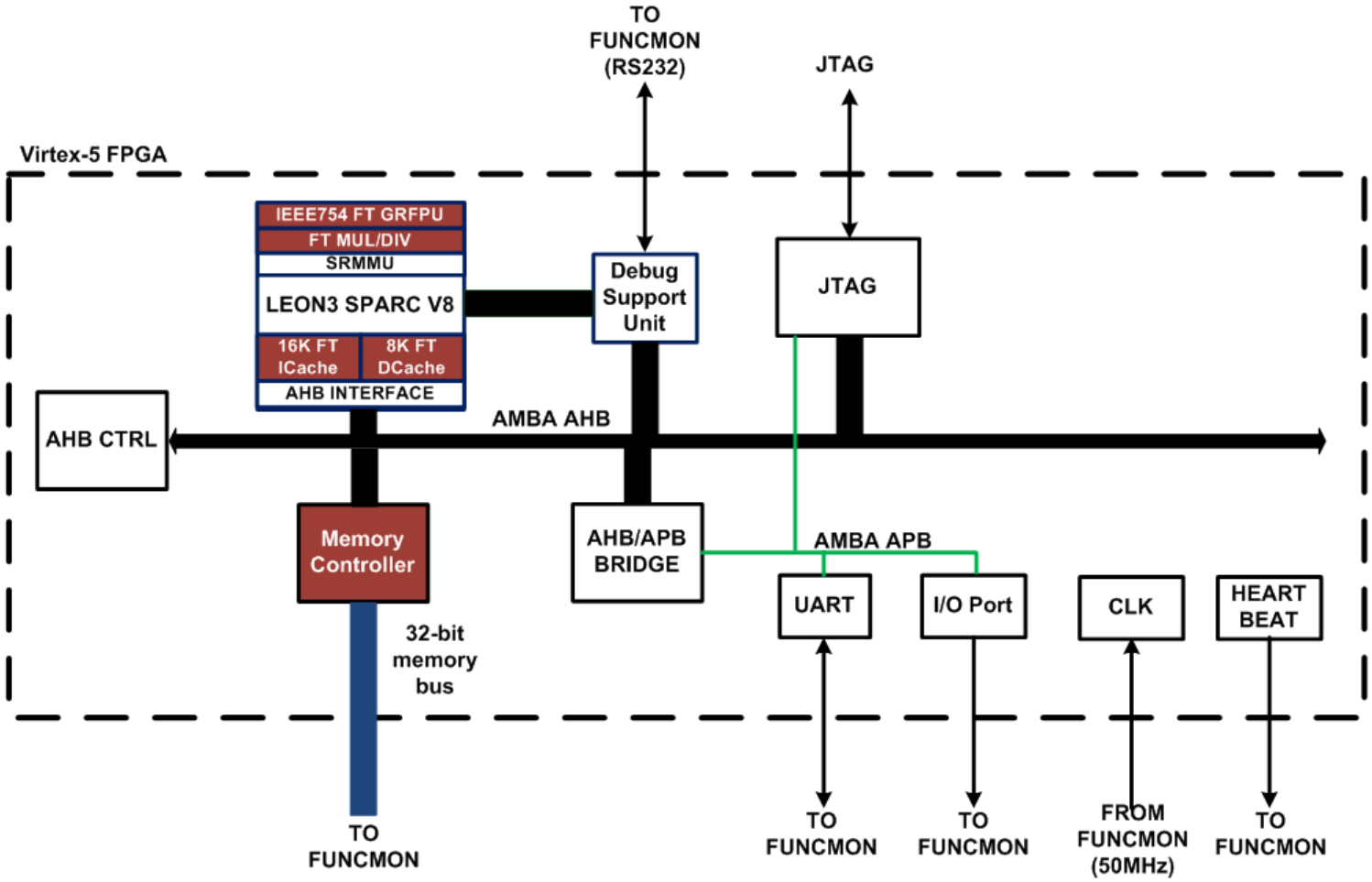
Hardware Test Setup

- Xilinx FX130T XQR5V Radiation Hardened by design FPGA used for testing.
  - Rely on the XQR to protect configuration bits, flip-flops, and look-up-tables (LUTs).
  - Remove digital signal processors (DSPs), digital clock manager (DCMs), and phased lock loops (PLLs) to reduce the number of possible single event upsets (SEUs) to the designs.
- Rely on Licensed Leon3 to protect BRAM, i.e. cache, integer unit (IU) and floating-point unit (FPU) register files.

Open-Source Leon3



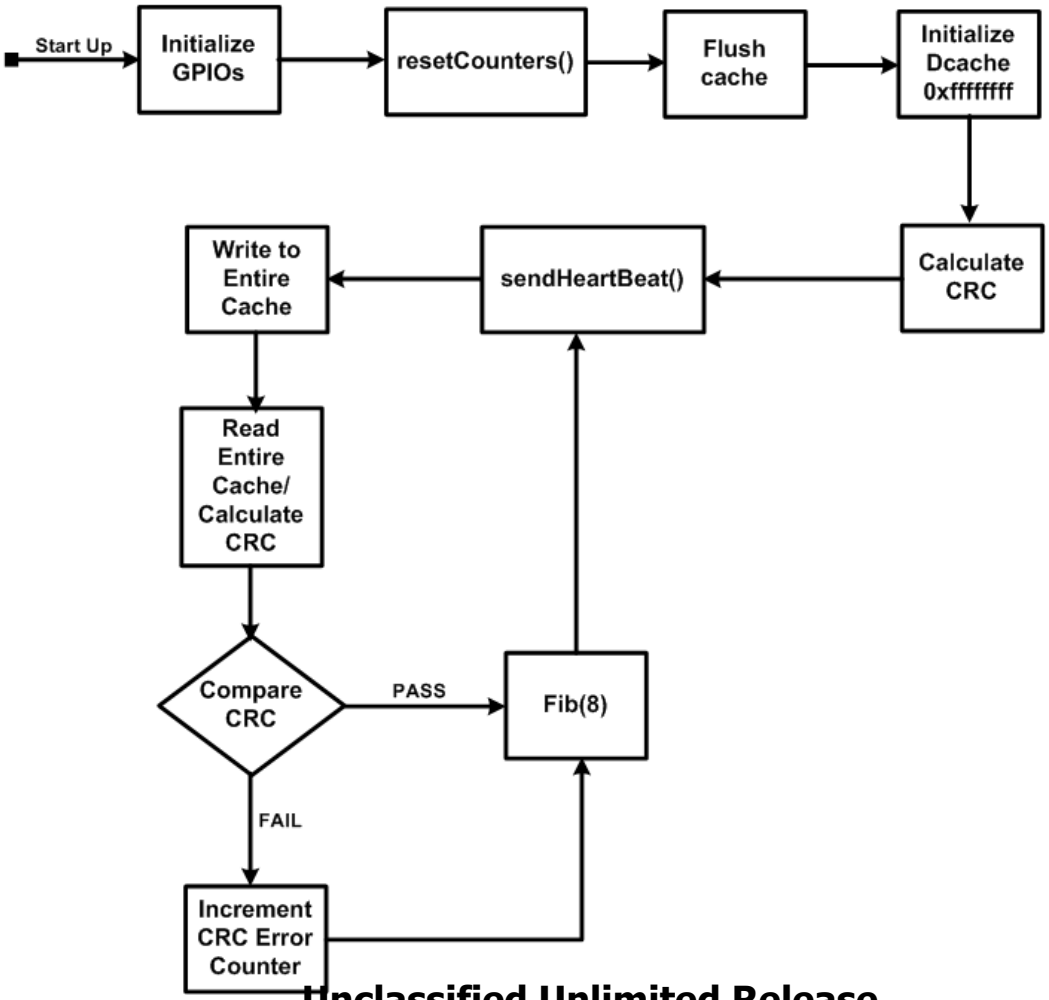
Licensed Leon3



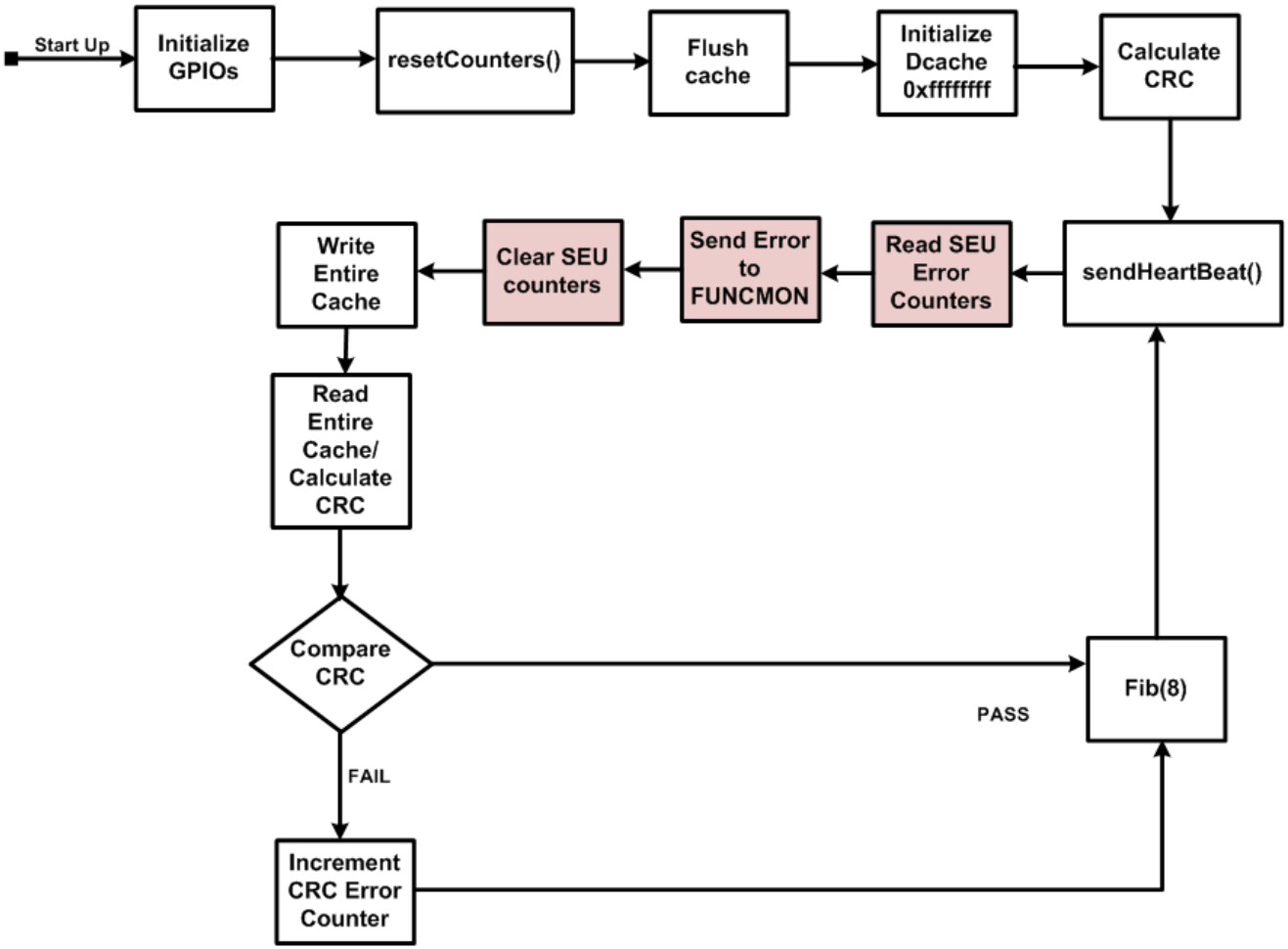
Software Test Setup

- Executable code stored off-chip to avoid corruption.
- Testing included cache testing, register file testing and FPU testing.
- Recommendation by Jiri Gaisler to add software scrubber.
  - Recursive function used to spill out all register windows to the stack (external memory) and corrects them in the process.
  - Helps to avoid error build up due to high flux during testing.
  - Necessary in design since no OS used and single-threaded application.
  - Adds easy way to test full register window.
- GRMON used to download executable, run and reset processor, and monitor unhandled traps:
  - Connects to the DSU through UART.
  - JTAG unused due to configuration scrubber.

Open-Source Leon3 Software: Cache, Register File Testing



Licensed Leon3 Software: Cache, Register File Testing



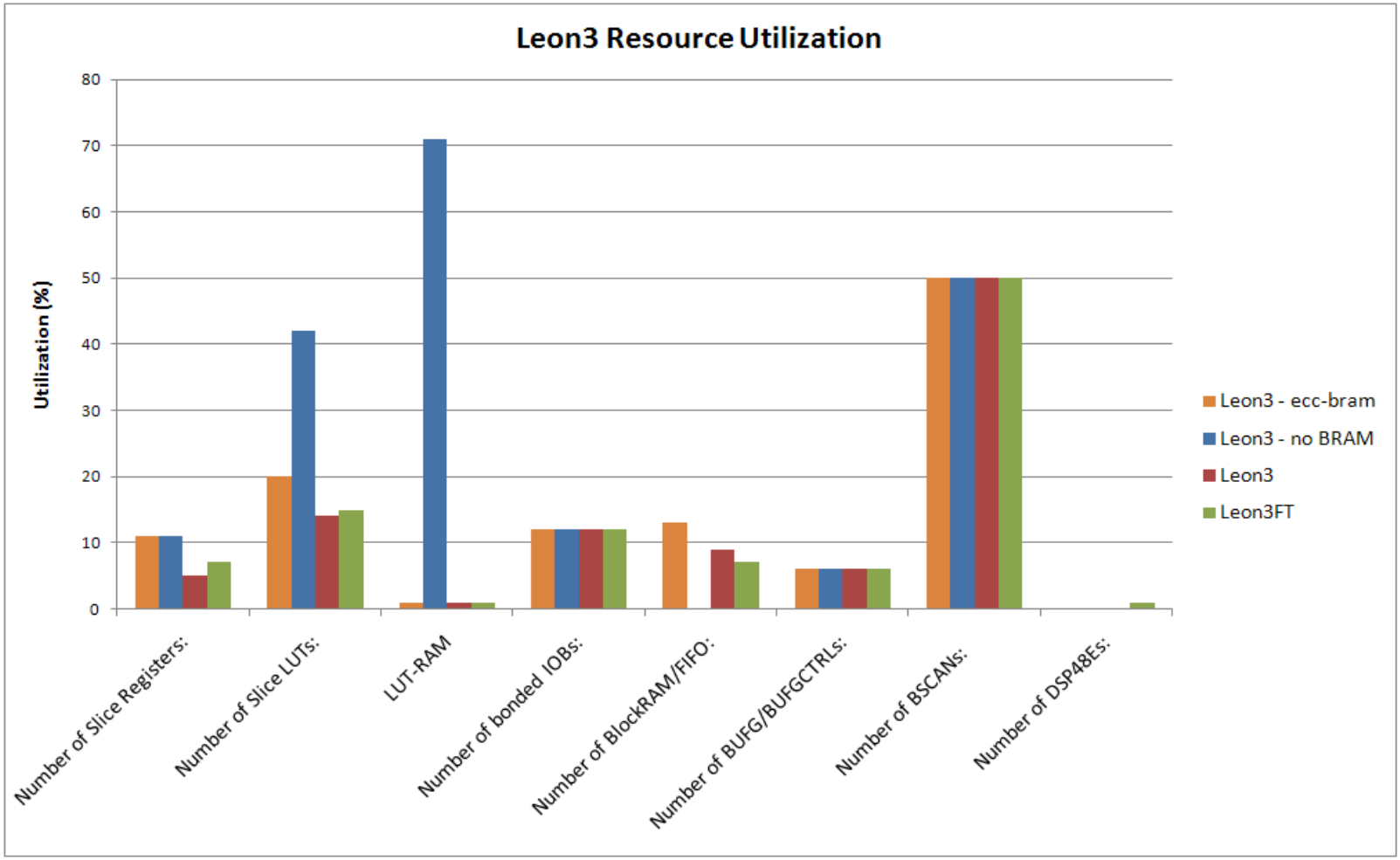
Experiments Tested

- Three various Leon3 designs were tested in the beam:
  - Unmitigated open-source Leon3:
    - Use results as base-line when comparing licensed and mitigated open-source designs.
  - Licensed Leon3:
    - Assess radiation hardness of this core.
  - Mitigated open-source Leon3:
    - Attempting to improve mitigation in open-source Leon3.
      1) ECC BRAM used.
      2) Remove BRAM and only use LUT-RAM for cache and register files.

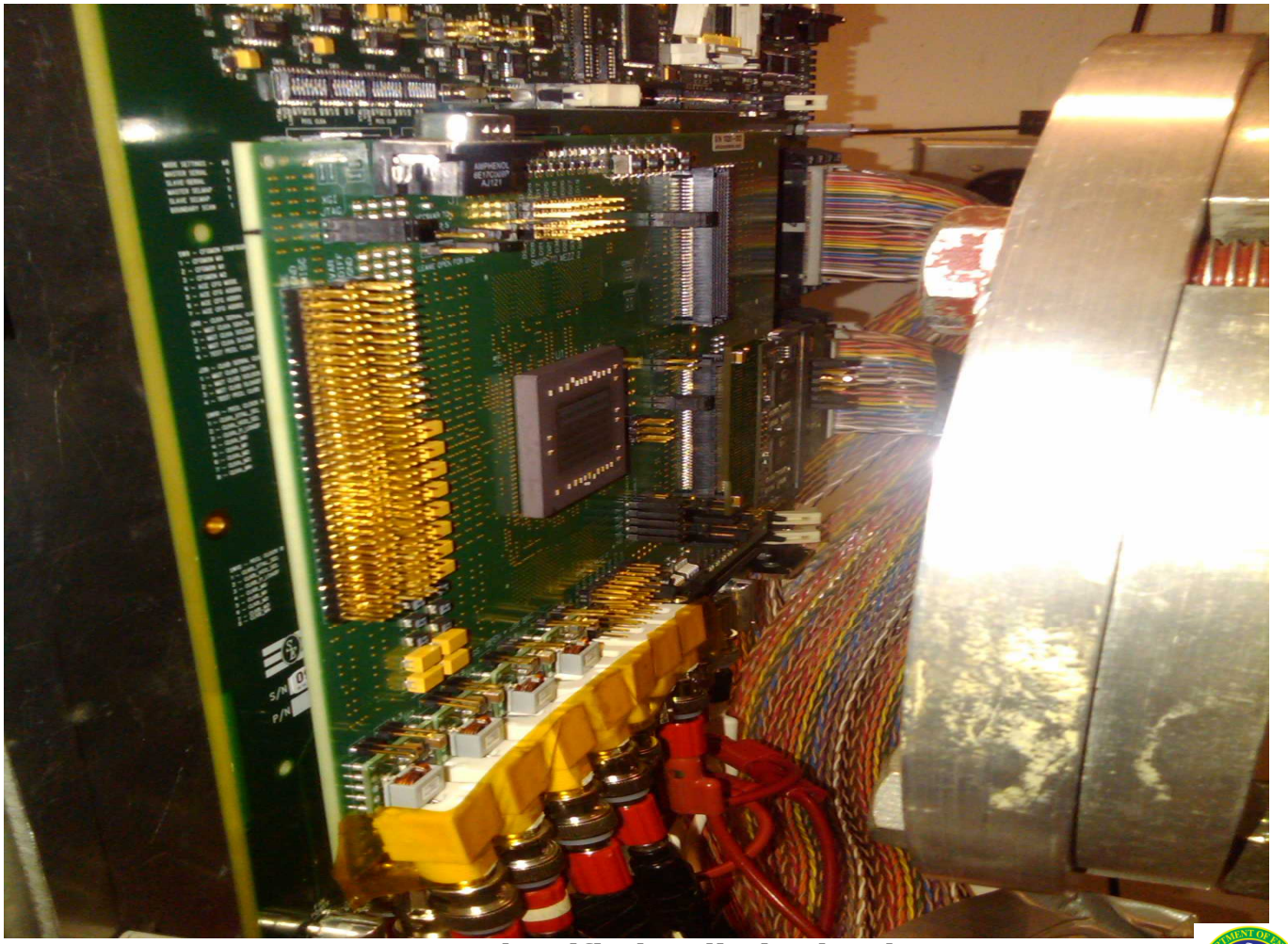
Mitigated Open-Source Leon3: Considerations

- ECC BRAM design:
  - 64-bit Simple Dual Port (SDP) provided in V5.
  - 32-bits unused in design.
  - Unused bits can accumulate errors leading to invalid detection, i.e. actual user data may be uncorrupted.
- LUT-RAM only used design:
  - 71% LUT-RAM used
  - Only 1% used for unmitigated open-source Leon3 and Licensed Leon3.
    - 9% BRAM used in open-source Leon3
    - 7% BRAM used in Licensed Leon3 – smaller cache

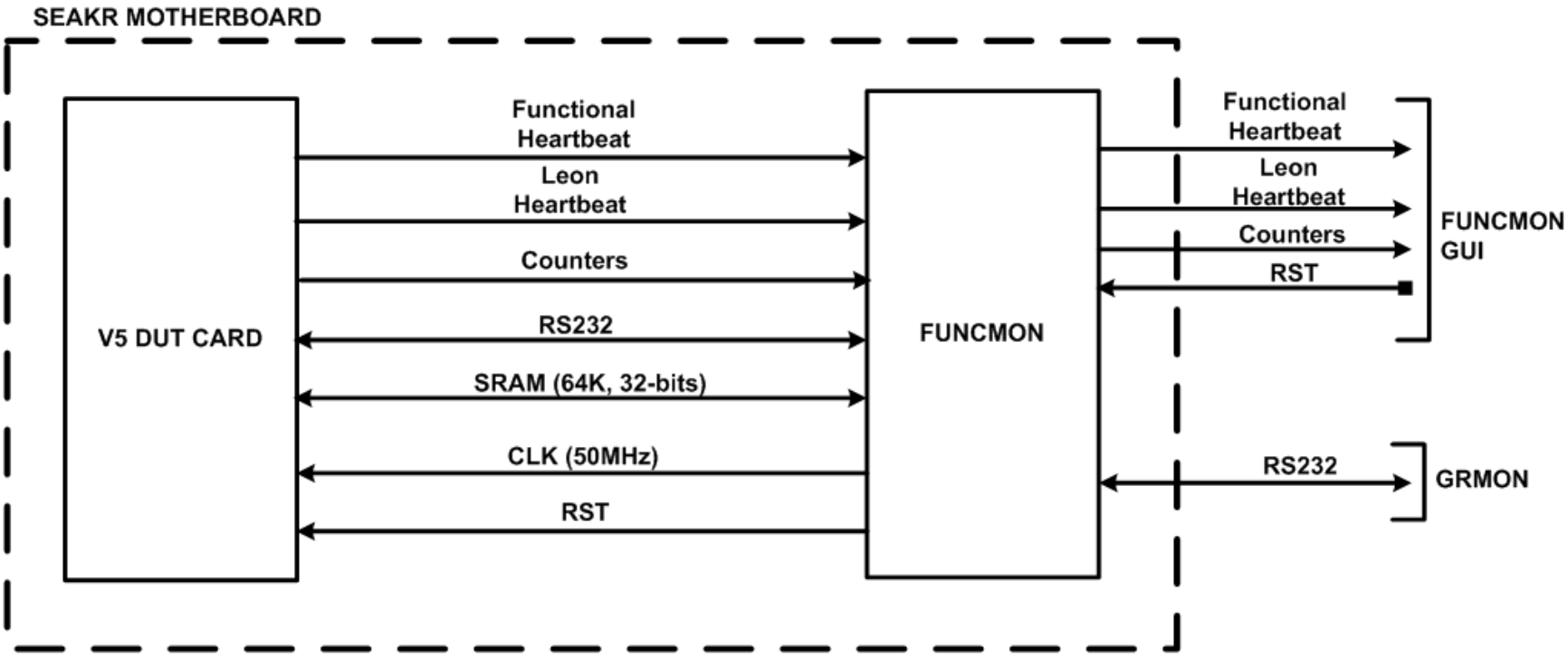
Resource Utilization



DUT Test Setup

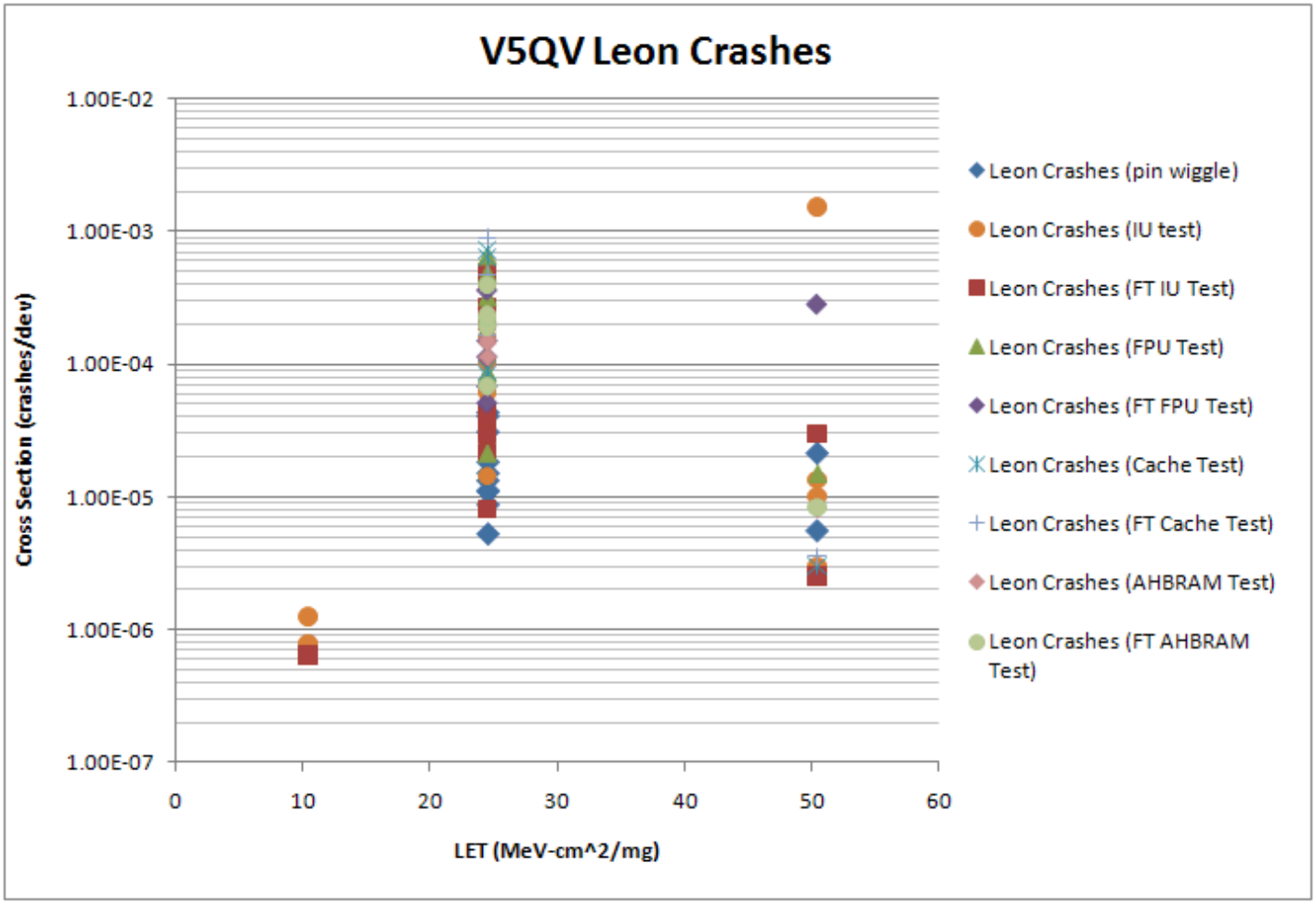


DUT Test Setup Block Diagram



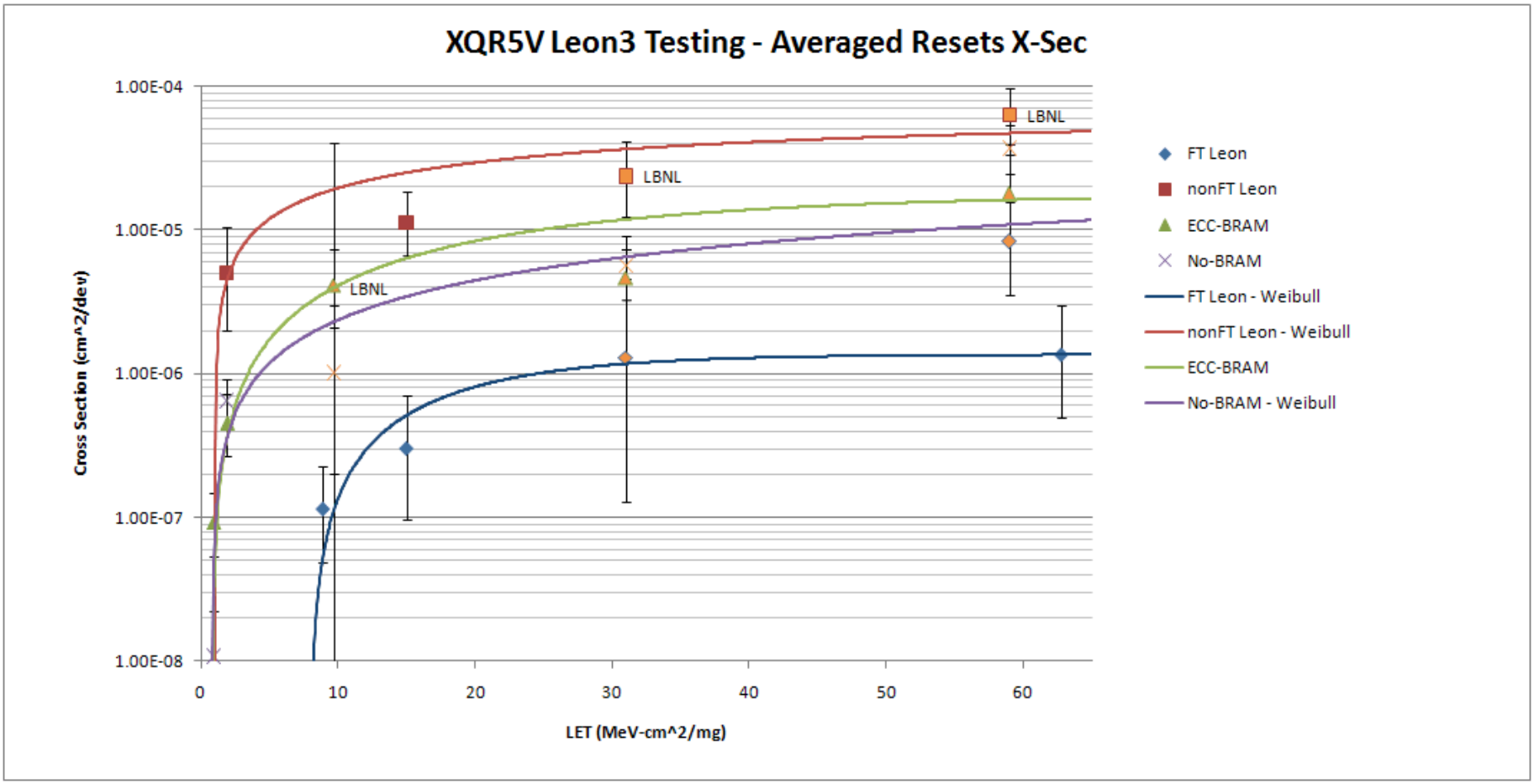
*External configuration scrubber used, but not shown here.

Initial Data Collected: FEB2010/MAY2010



*no software-scrubber present

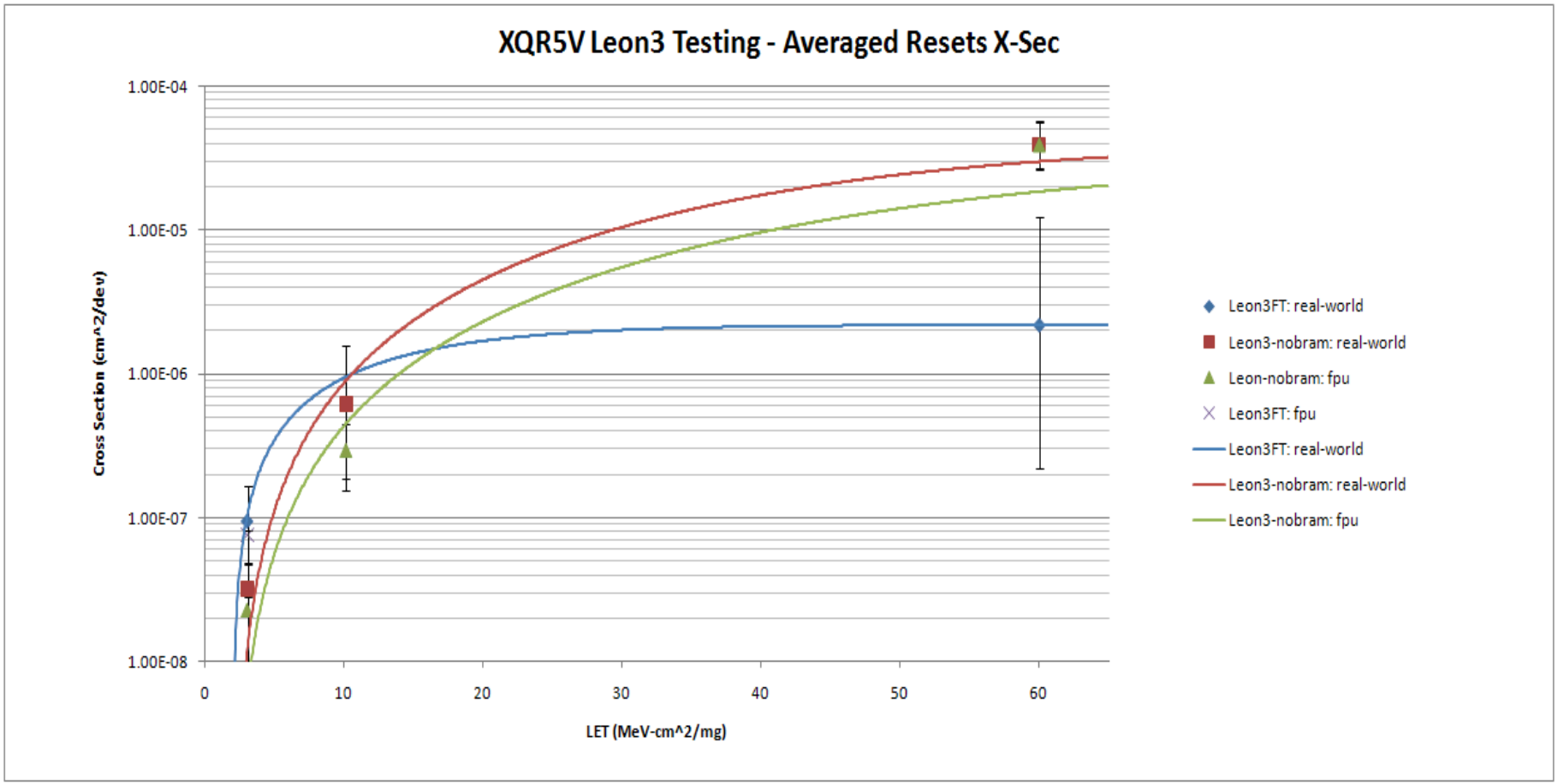
Software Improvements: SEP2010/OCT2010/DEC2010



Additional Software Testing

- Included additional software tests to see how the performance of the Leon3 changed.
  - Executed a "Real-World" application:
    - Application used on MicroBlaze for MISSE.
    - Includes floating-point operations.
  - Floating-Point Application:
    - Used to perform floating point operations.
- Software applications executed on the Leon3FT and the LUT-RAM only design due to time allocated for testing.

Additional Software Testing Results: TAMU MAR2011



CREME96 Heavy Ion Error Rates

- **Solar-Quiet Conditions:**
  - **GCR Solar-min**
- **Spacecraft location:**
  - **Near-Earth Interplanetary/Geosynchronous Orbit**
- **Shielding:**
  - **100mils, Aluminum**

Error Rates Using Current Software

Test	Upset Rate (resets/day)	Upset Rate (years/reset)
FT LEON3	IU/Cache: 7.01218e-6 RW: 3.609e-5	IU/CACHE: 391 RW: 75.9
Unmitigated LEON3	IU/CACHE: 1.69414e-3	IU/CACHE: 1.6
Mitigated Leon3: ECC-BRAM	IU/CACHE: 2.54481e-4	IU/CACHE: 11
Mitigated Leon3: NO-BRAM	IU/CACHE: 1.89166e-4 RW: 8.277e-5 FPU: 4.6366e-5	IU/CACHE: 14.4 RW: 33 FPU: 59
Aeroflex-Gaisler UT699* **(errors/device-day)**	IUTEST: 1.7e-4 errors/device-day RW: 1e-4 errors/device-day Benchmarking: 5.1e-5 errors/device-day	IUTEST: 16 years/error RW: 27 years/error Benchmarking: 54 years/error

*"Single Event Effects Qualification Summary for the UT699 Leon3FT Processor" – Craig Hafer

Additional Testing/Improvements Required

- An operating system (OS) would allow us to remove the software scrubber and characterize the Leon3 with an OS.
- Replace psuedo-external memory (FUNCMON) with QDR memory.
  - May improve Leon execution.
    - Occasionally unwanted external memory writes were seen.
    - Unable to reset processor due to corrupted executable.
  - Allows addition of an OS.
- More test data on various software applications including benchmarking applications.
- Need to improve the way executable code is loaded and run.
  - Communication to GRMON/DSU would occasionally get hit in the beam.
  - Would shorten run time since we could not communicate with Leon to reset or continue execution.
  - Steve Elzinga from Xilinx helped to create a DATA2MEM type design.
  - Would allow us to remove DSU from design and avoid using GRMON to communicate with processor.

Conclusion

- Licensed Leon3 had a much lower error rate than other three designs.
  - ~391 yrs/reset vs. every ~2 years with the unmitigated Leon3.
- Able to provide some simple mitigation to the open-source Leon3.
  - Using ECC-BRAM increased the number to ~11years/reset.
  - Using LUT-RAM increased the number to ~14 years/reset.
- Keep in mind that these error rates are specific to the software design used.
- Traps were dominate software error seen during testing.
  - Mainly a result from multi-bit errors.
- Software scrubber helped to avoid error build up during testing.

References

1. Aeroflex Gaisler, “GRLIB IP Core User’s Manual”, v.1.0.21, August 2009.
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5. SPARC International Inc., “The SPARC Architecture Manual, Version 8”, rev SAV080S19308, 1992.
6. Xilinx, “LogiCORE IP Block Memory Generator v4.2”, DS512, July 2010.
7. C. Hafer, “Single Event Effects Qualification Summary for the UT699 Leon 3FT Processor”, 2008.
8. G. Swift, “MAPLD 06 Seminar – Radiation Effects and Field Programmable Gate Arrays”, Xilinx Corporation, September 2006.