

Structural Simulation Toolkit (SST)

Interfacing Coarse-Grain (SST/Macro) & Fine-Grain (SST/Micro) Simulation Spaces for Exascale SuperComputer Development

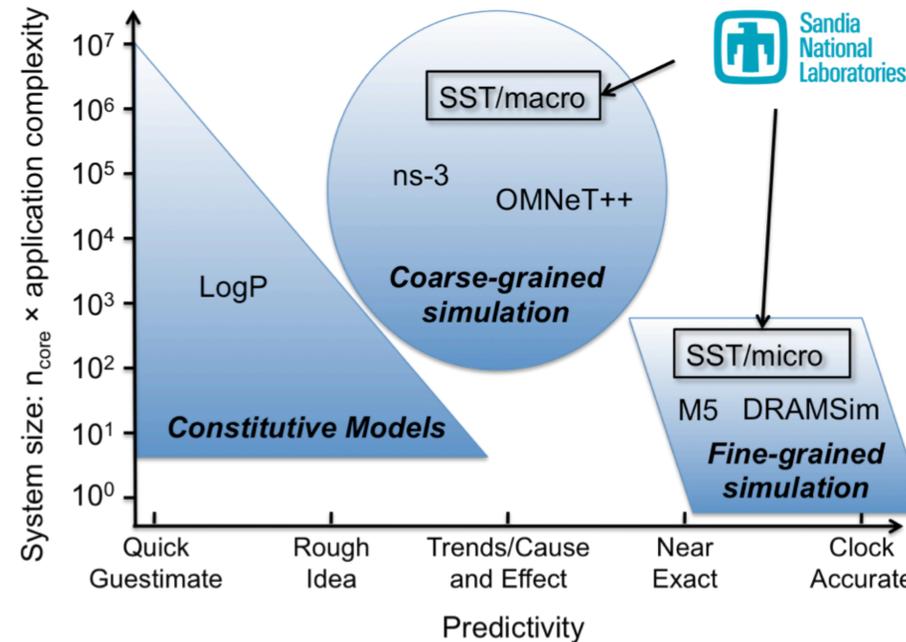
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MOTIVATION

- Computer Architectural Simulators provide a development environment in which hardware designs can be *simulated* to provide insight into how computer systems would behave
- Fine-Grain Simulators rely on performing detailed modeling of architectural components that impose superlinear increasing time and simulation complexity in order to obtain a cycle accurate measurement
- Coarse-Grain Simulators forego the detailed modeling of architectural components in favor of *coarse* estimations to provide a faster, and more scalable simulation time.
- The nature of computing is beginning to change dramatically:
 - billions of processors, threads, faults
- Accurately modeling exascale computers with reasonable performance and scalability require being able to communicate simulation state from a coarse -grain simulation to a fine-grain simulation without having to rollback or checkpoint

OBJECTIVES

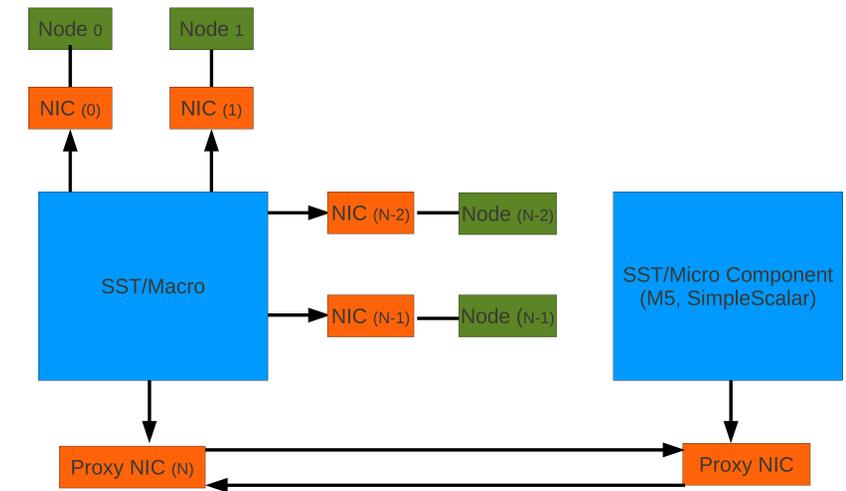
- Interface SST/Macro with the SST/Core Parallel Framework
- Simulate using both SST/Macro and SST micro components
- Develop an Event-Translation Scheme to allow for communicating between
- Determine how to appropriately transfer *system state*



METHOD

Interfacing SST/Macro and SST requires understanding how to represent SST/Macro as a visible *component* SST/Core

- SST/Core Framework interconnects different *component* objects
- Encapsulating specific event types + data information to provide meaningful communication between different *Core* components
- Allowing for simulation control handling when transferring control from SST/Macro to SST
- Encapsulating SST/Macro network communication with ST/Core component handling



FUTURE WORK

- Developing a more flexible interface that
- Develop a fine-grain *cache storage* for storing execution state/time for previously finer-grain executed code

