SAND2011-5376C

Quantum Information S&T

AQUARIUS

Silicon enhancement mode nanostructures for quantum computing

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Sandia National Laboratories

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LDRD LABORATORY DIRECTED RESEARCH & DEVELOPMENT

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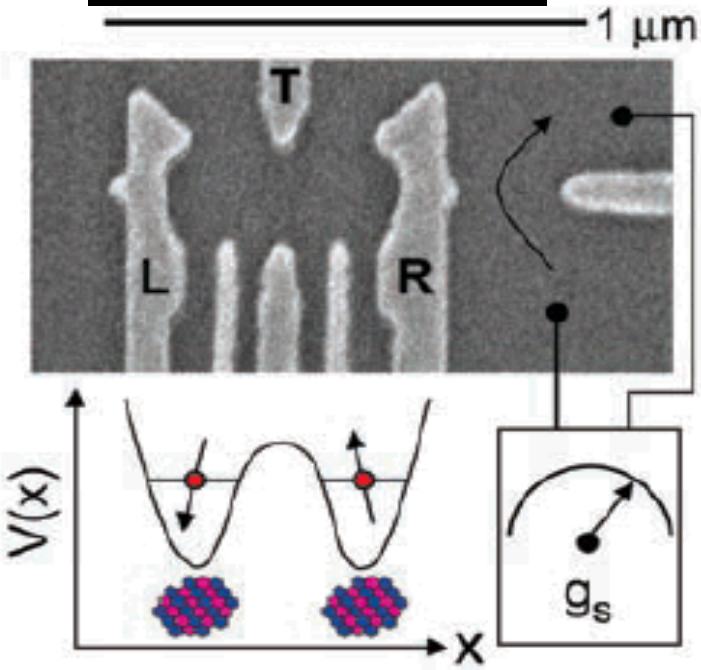
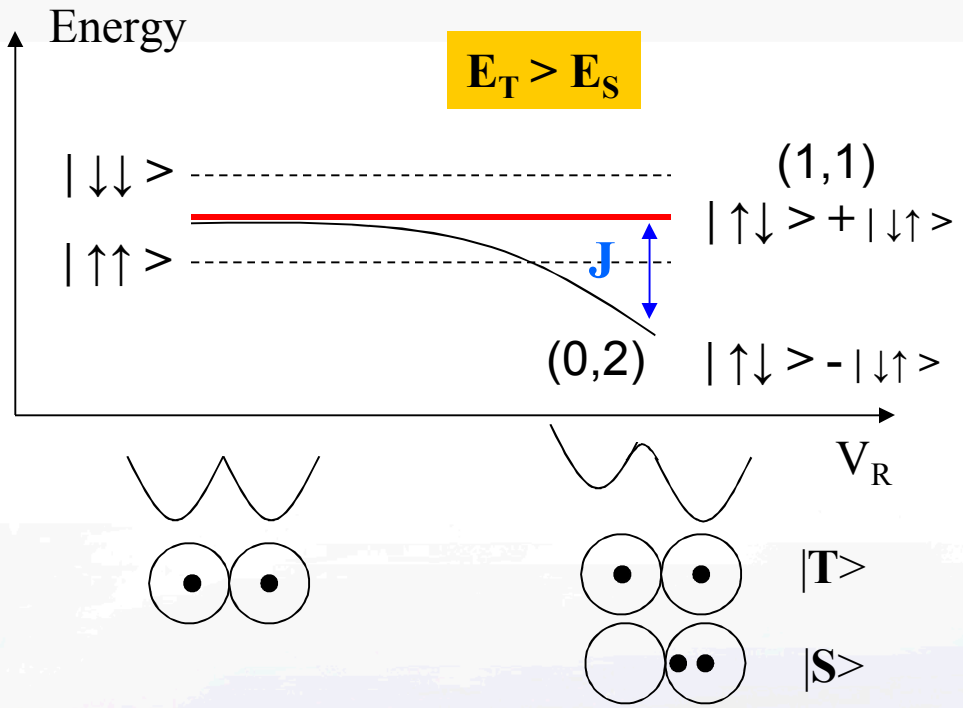
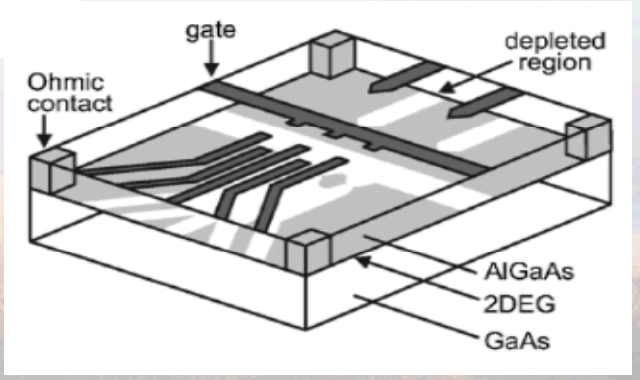
One inspiration for semiconductor quantum computing

Petta, Science, 2005

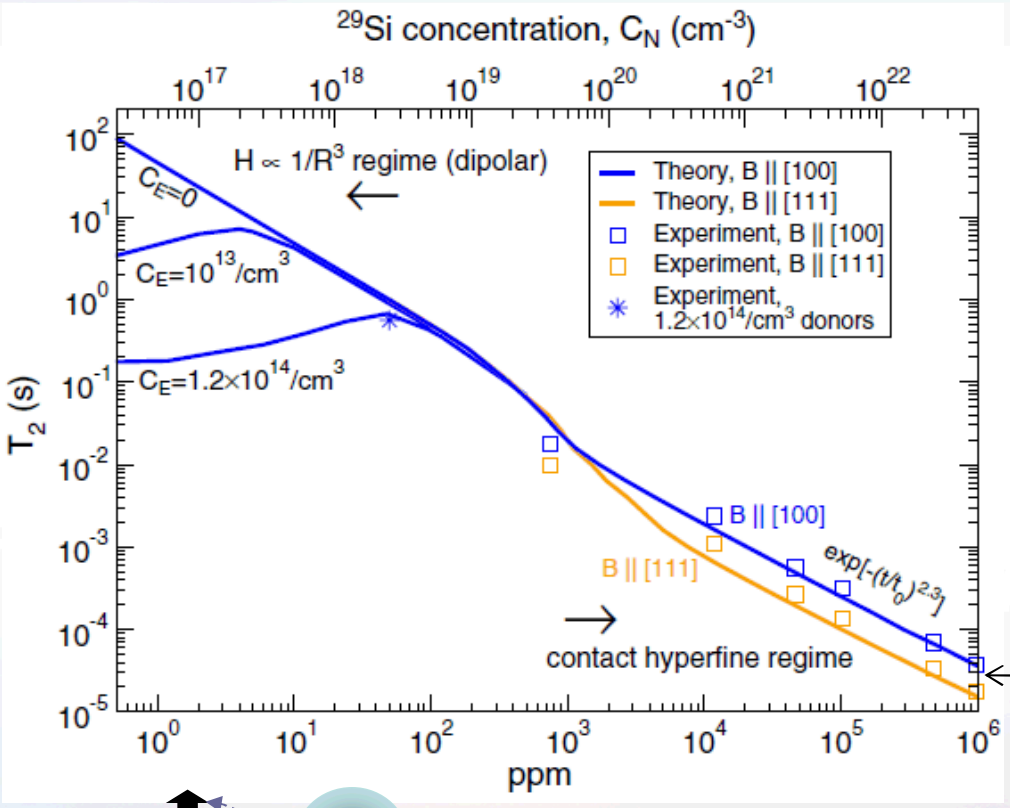




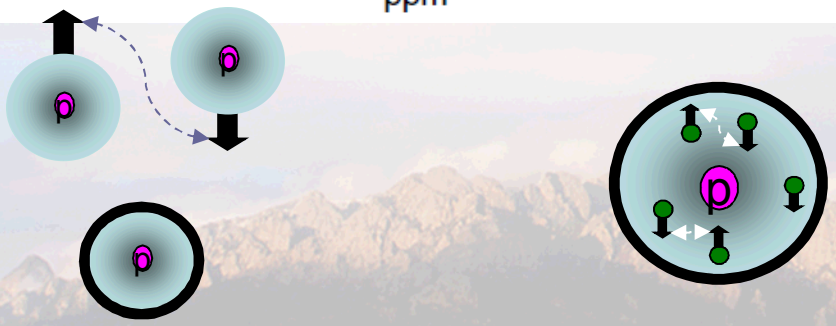
Elements:
- Two level system
  - m=0 subspace of 2 electrons
- Electrically tunable (tunnel coupling)
- Charge sense



Motivation for Silicon Qubits



GaAs (30 us)



- GaAs has non-zero nuclear spin isotopes shorten T_2
- Si isotope enrichment removes nuclear spin, long T_2
- Nuclear spins can be useful for rotations between S & T0 but off/on is better and it limits T_2
- Recent device progress in electron spin manipulation (spin read-out & evidence of coherence)
  - UNSW (donors)
  - UCLA (MOS)
  - HRL (SiGe mod. doped)
  - U. Wisconsin (SiGe mod. doped)

Witzel et al, PRL 105, 187602 (2010)

Does T_2 need to be really long? ($p \sim 10^{-4}$?)

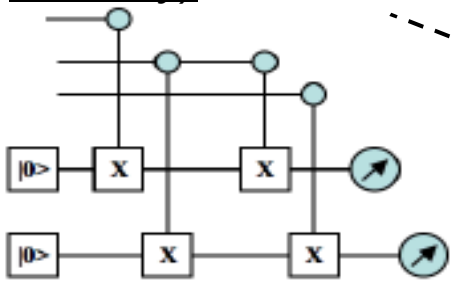
Some conclusions from logical memory

- Scheduling conflicts lead to more idles (e.g., electronics & DD itself)
- if T_2 error is non-negligible gates requirements are more strict
- Circuit would shows benefit at $p \sim 5 \times 10^{-4}$ assuming negligible idle error
- Marginal with present GaAs T_2

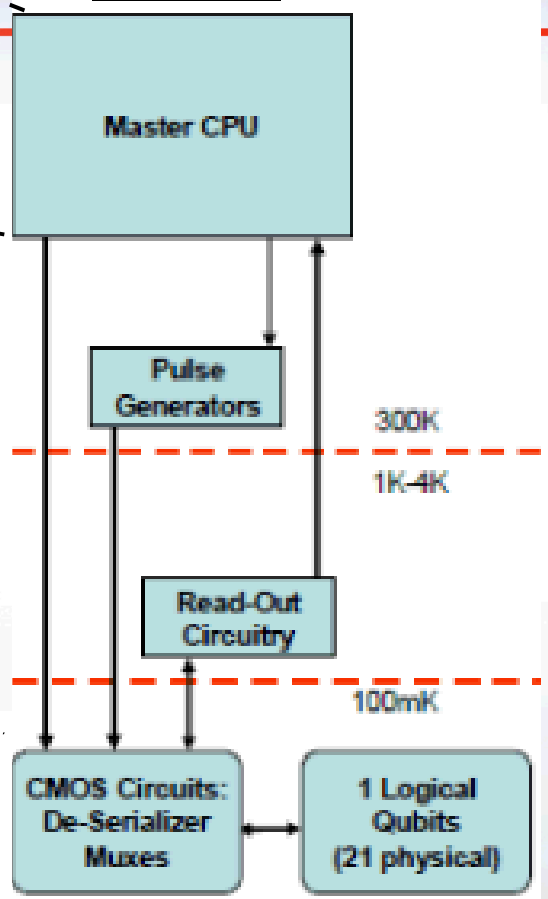
Levy et al. SPAA (2009)
Levy et al. arXiv:1105.0682 (2011)

DQD qubit encodings might work for adiabatic approach (both Si & GaAs)

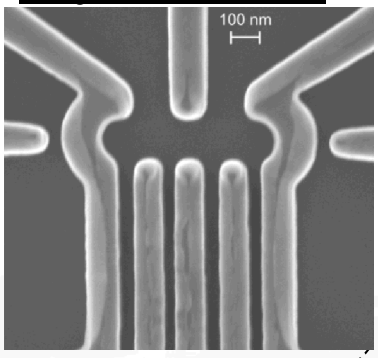
Quantum Circuit (Logical Memory)

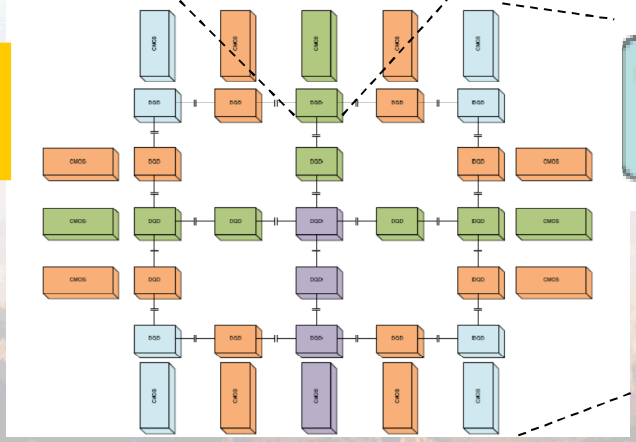


Classical-Quantum Interface



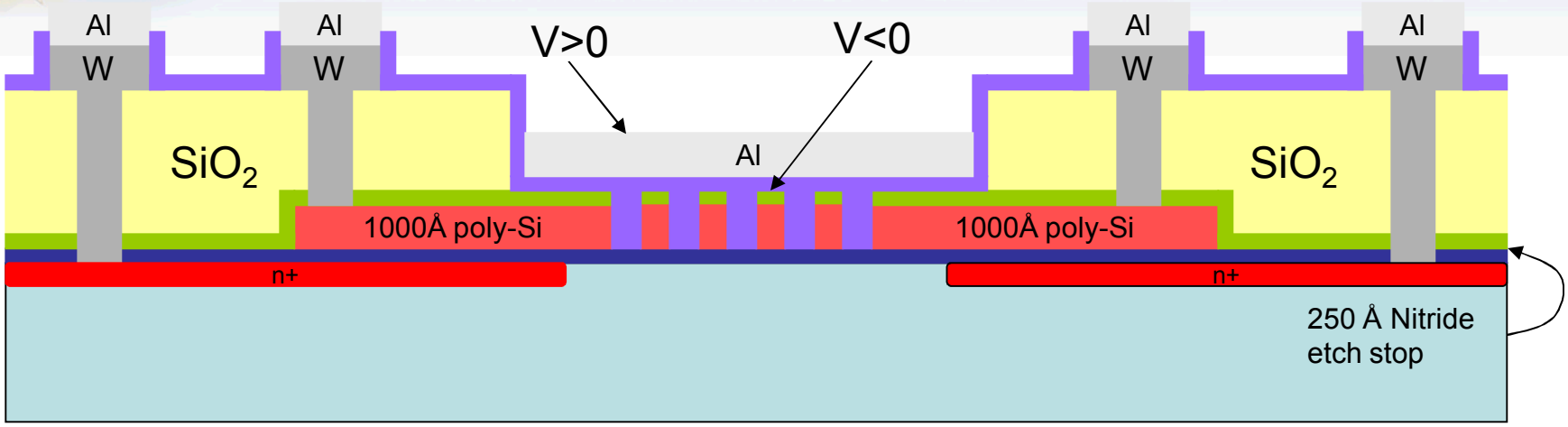
Physical Qubit





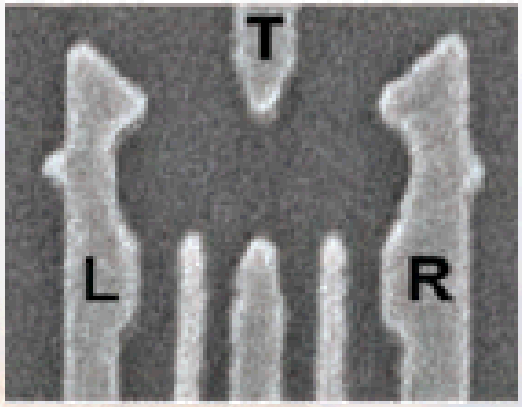
Chip Level Circuit (21 qubits)

Enhancement Mode Si Quantum Dots



- Many silicon approaches
- SNL looking at enhancement mode & Si foundry approach
- This talk: MOS & SiGe/sSi

GaAs design to Si?

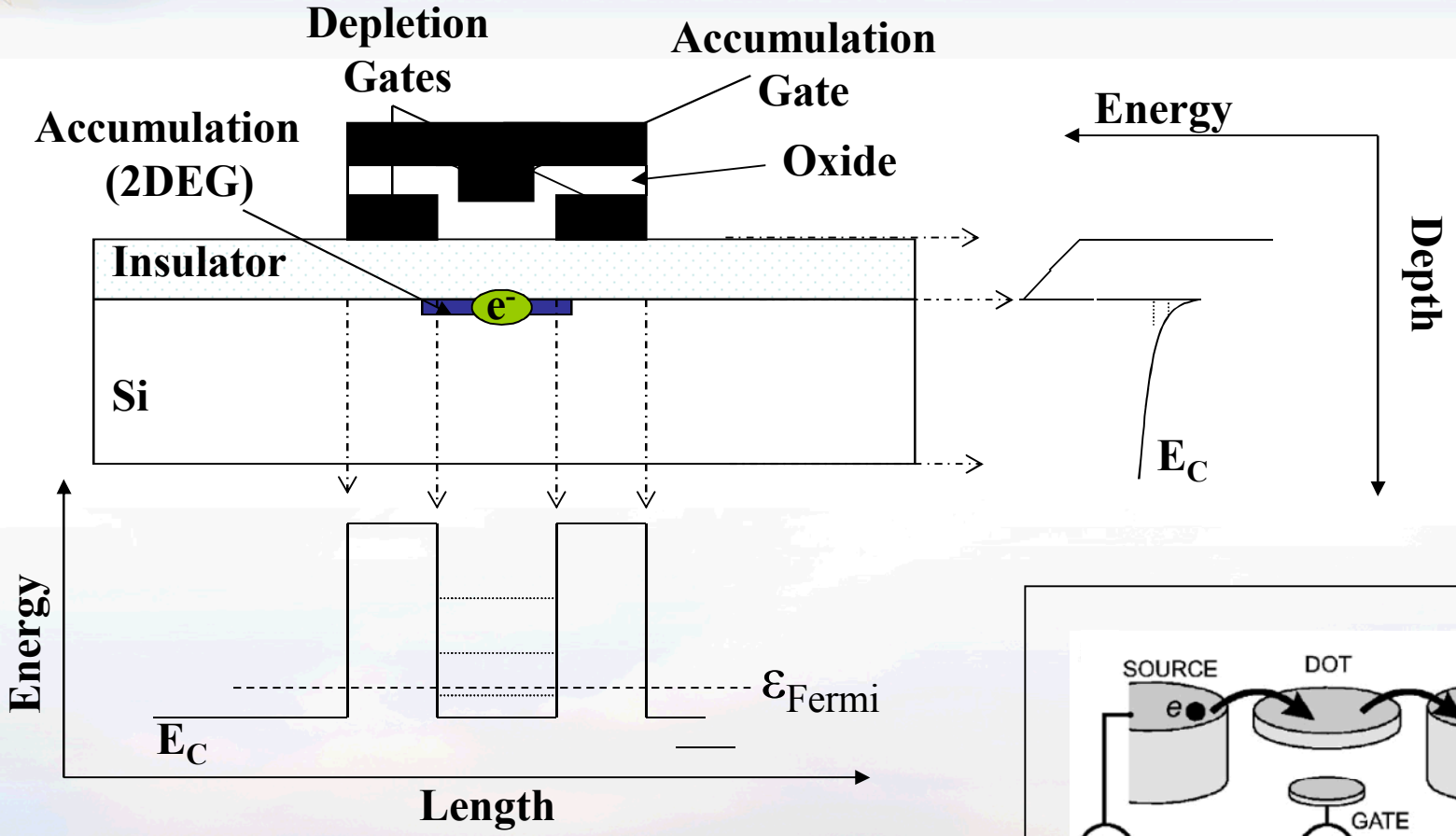


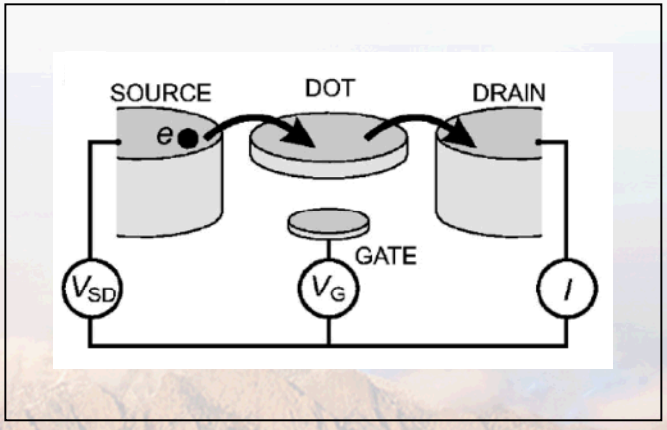
Petta et al. [2005]

<u>Motivations</u>

1. Platform is modular design for both donors and SiGe/sSi
2. Tunable parameters (density, valley splitting, g-factor?)
3. No dopants
4. Start with MOS:
   - well understood material system
   - overlapped interests for other Si approaches
5. CMOS compatible (MOS)

Enhancement mode quantum dot concept

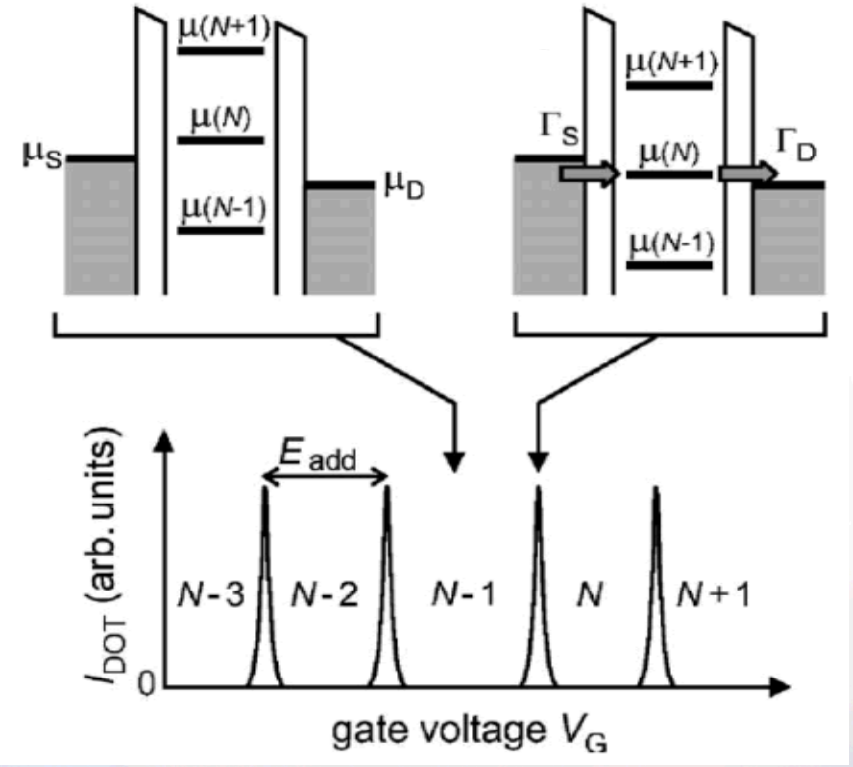




- Structure provides 3D confinement

Coulomb blockade

Periodic resonances understood by evenly spaced chemical potential energy levels

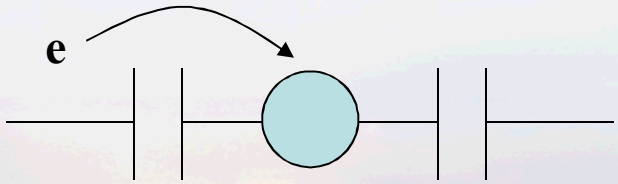


$$V = \frac{q}{C}$$

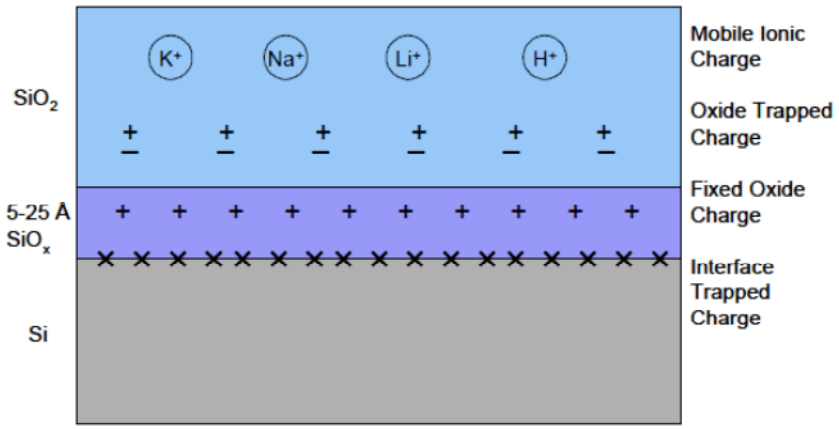
- Equally spaced energy levels related to charging energy of capacitance
- Periodic current resonances produces – “Coulomb blockade”
- Low temperatures required (T << 4K)

$$C_{sum} \sim 16\ \text{aF}$$

$$\Delta V = \frac{q}{C} \sim 1\ \text{mV}$$



Early challenge to MOS QDs

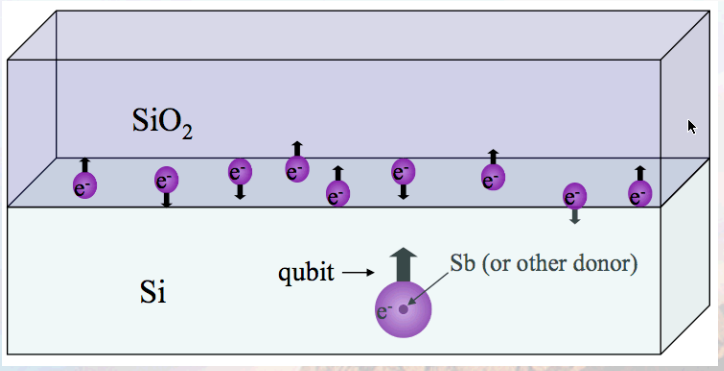


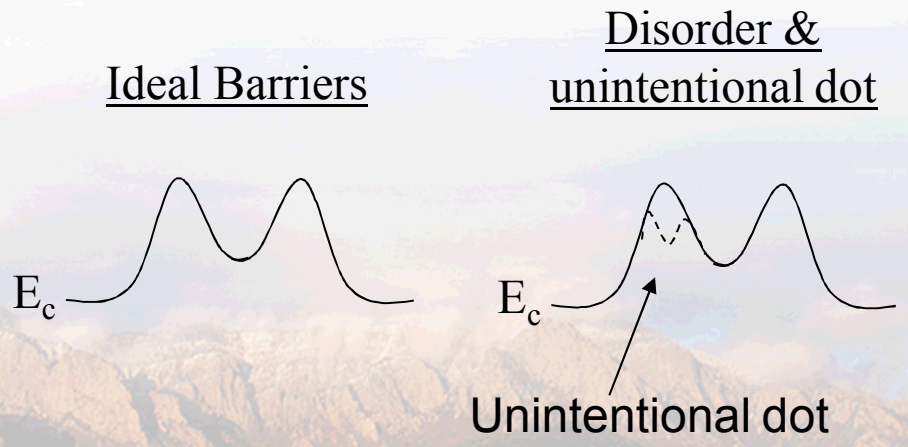
Charge defects & effective mass

1. Uncertain confinement potential
2. Unintentional dots
3. Fluctuators (TLS)

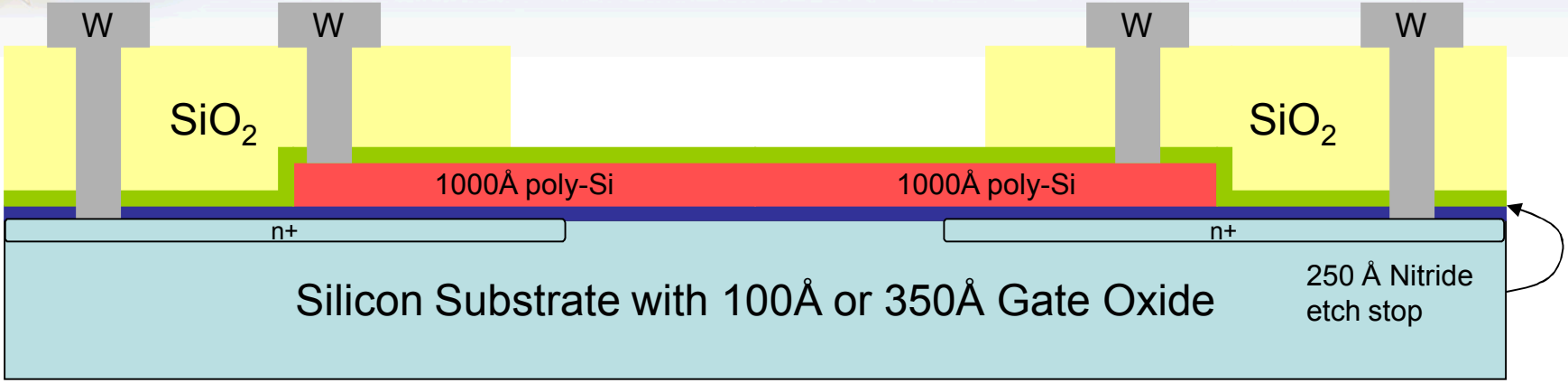
Magnetic defects

1. Non-uniform magnetic field
2. Time varying magnetic field (if not polarizable)





How is device made: "Front-end"

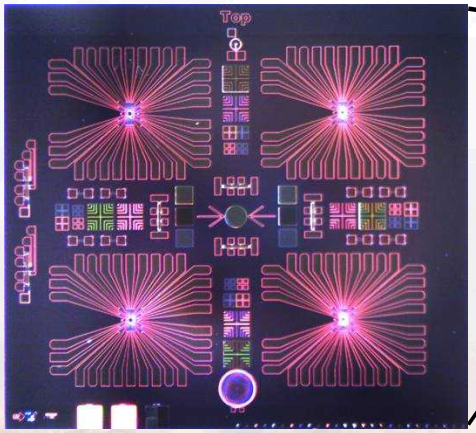


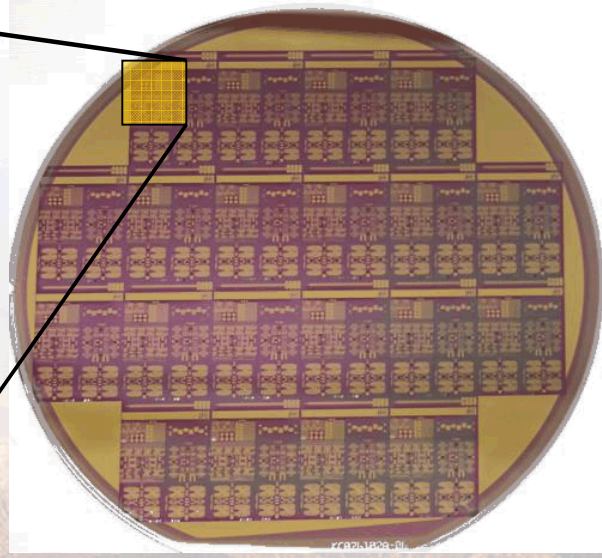
MOS Stack from Si fab

QDs possible with 0.18 ❍m litho

EDMR for external community

7,500 – 15,000 mobility, high resistivity substrates





T. Pluym

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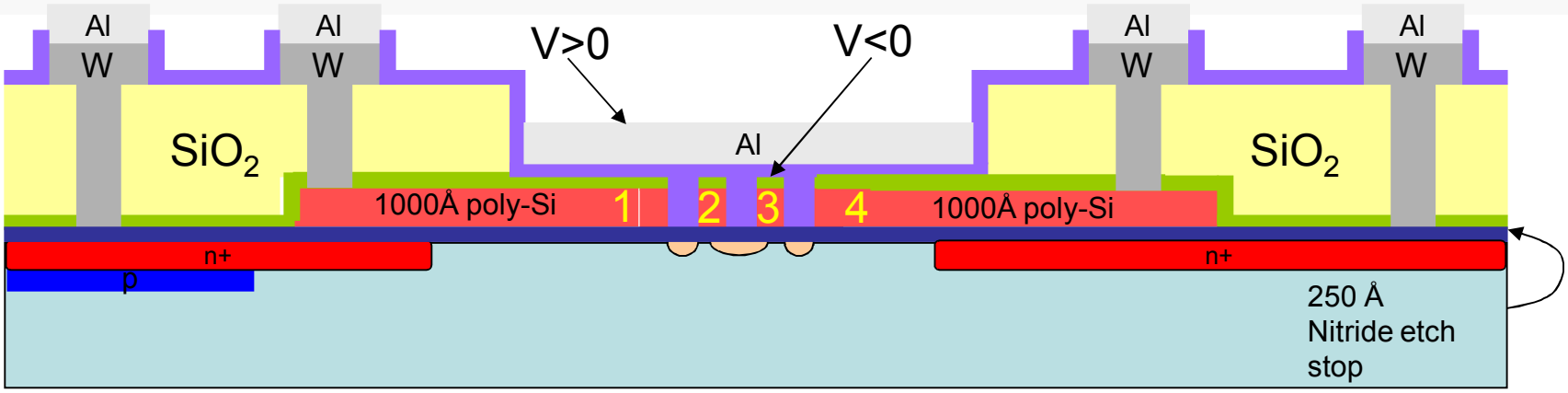
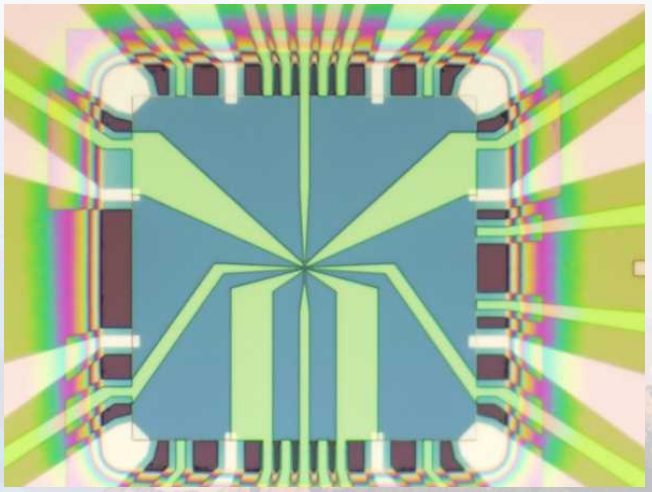
Back-end processing

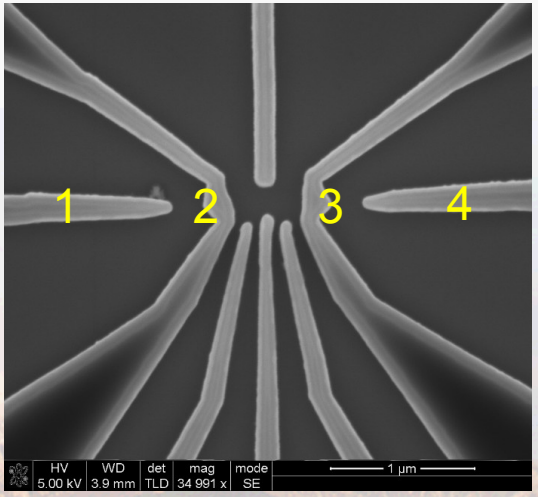


GaAs design to Si



Micro-fab facility
E-beam lithography
Poly-silicon etch
Aluminum oxide
Top Al gate

Low parasitic RF die



T. Pluym, B. Silva, J. Dominguez, N. Bishop

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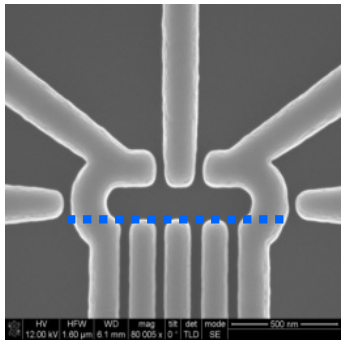
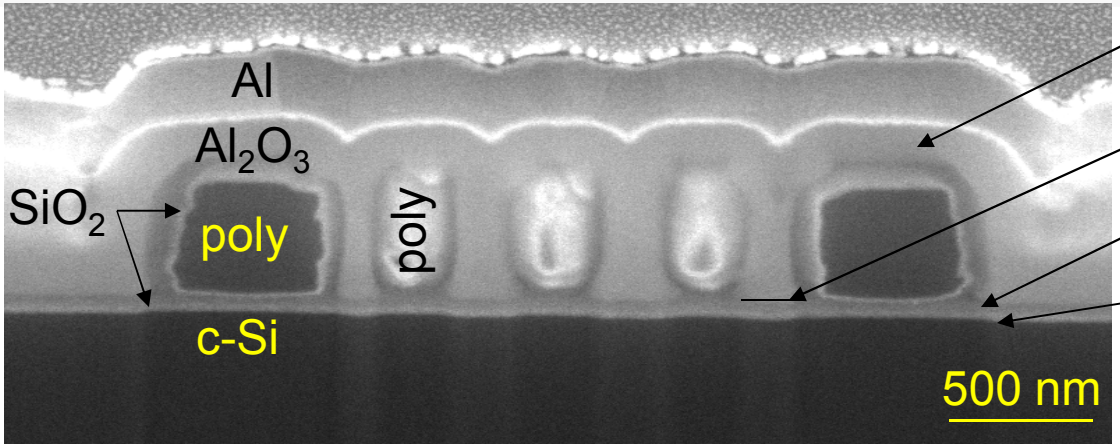
Immediate Challenge: Charge Defects





$Q_{ox}(Al_2O_3) < 0$

$Q_{mobile} = ?$

$Q_{interface} = ?$

$Q_f(SiO_2) > 0$

$D_{it}(SiO_2) > 0$

	Si Fab		QD Fab
mobility:	~15,000 ($cm^2V^{-1}s^{-1}$)	=>	~200
D_{it} :	~10^{10} $eV^{-1}cm^{-2}$	=>	~10^{12}
Q_{eff} :	~10^{11} cm^{-2}	=>	~10^{12}

G. Ten Eyck

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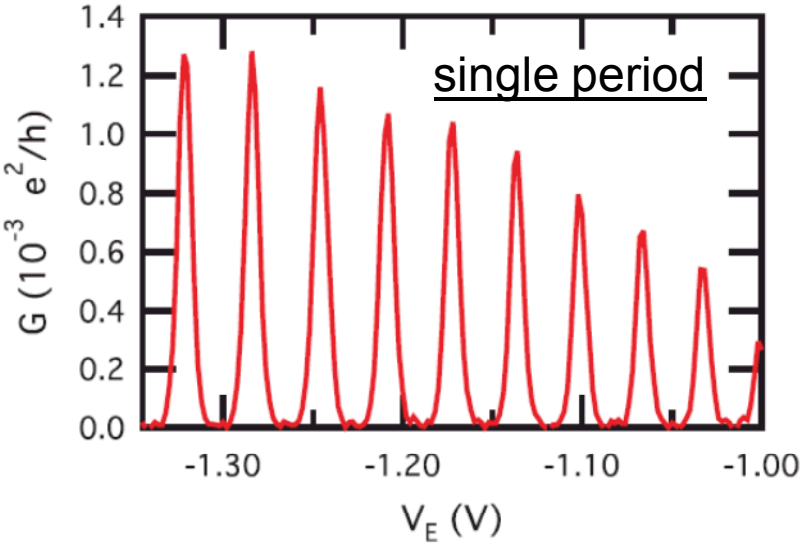
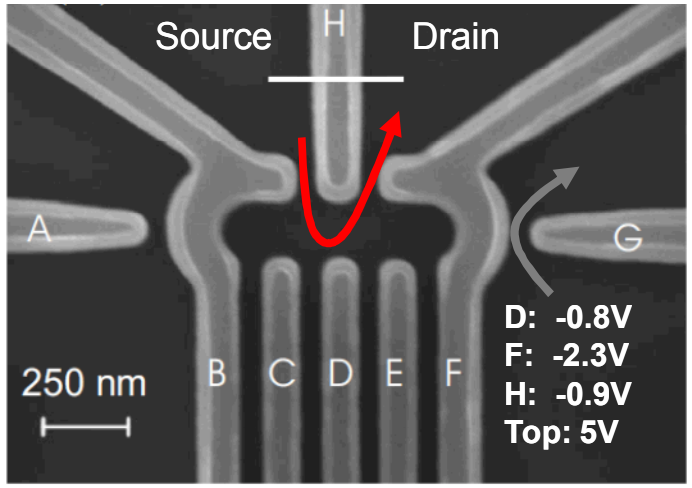
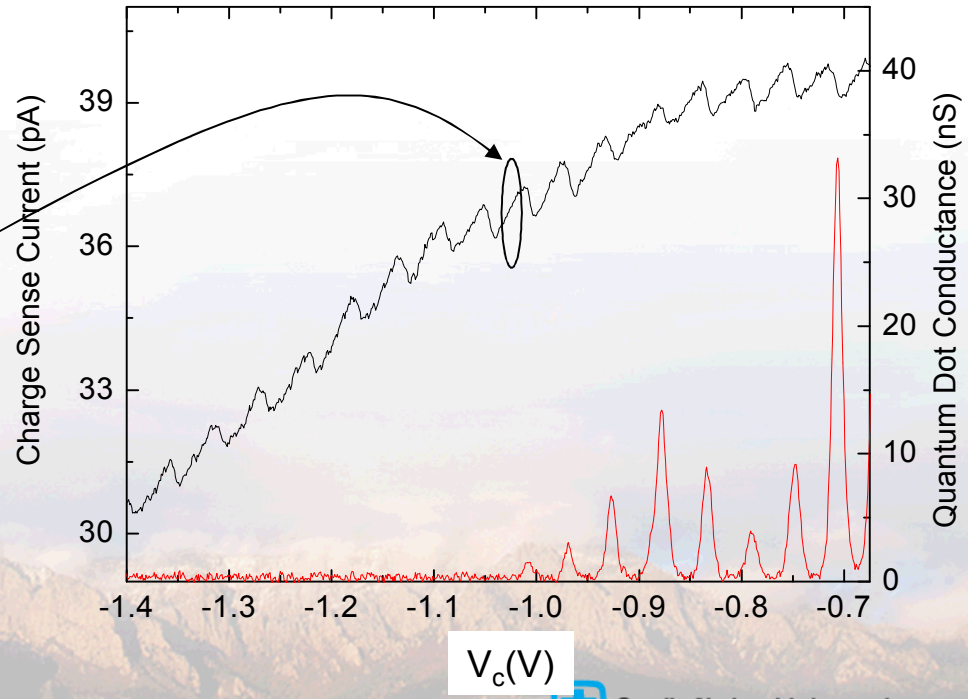
Sandia quantum dot platform



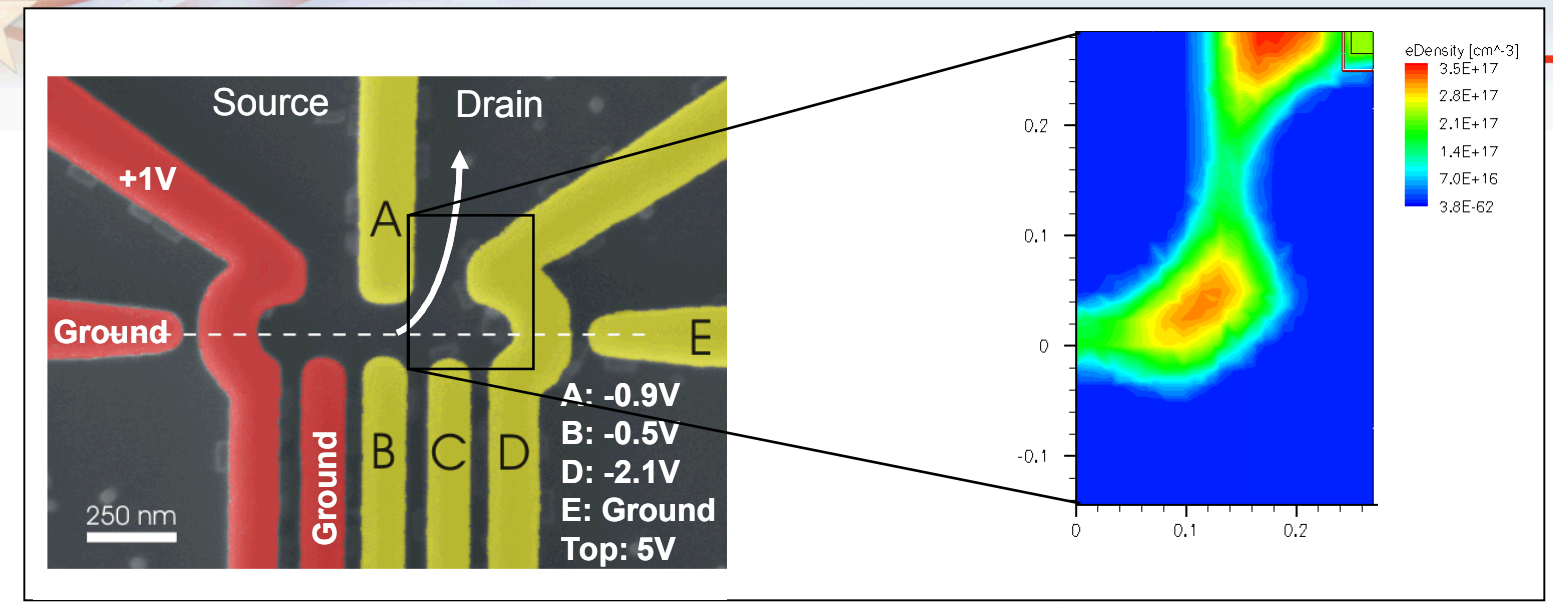


Improved processes (test stack):
Mobility: 8,000 ($cm^2V^{-1}s^{-1}$) [T~4K]
D_{it} : 2.9 x 10^{10} $eV^{-1}cm^{-2}$
Q_{ox} : 1.1 x 10^{11} cm^{-2}
~ 1 charges per QD (r = 12 nm)

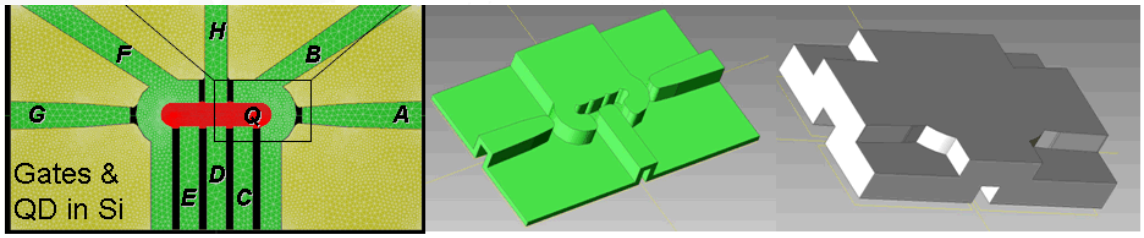


Nordberg et al., PRB (2009)

Lithographic dot verification



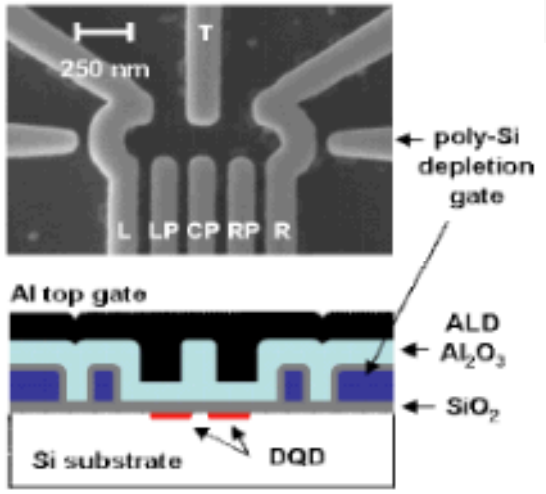
Gate	experiment [aF]	Model [aF]
A	6	6.2
B	3.2	3.3
C	3.3	3.4
D	7.2	7.3
Top	14.6	14.4



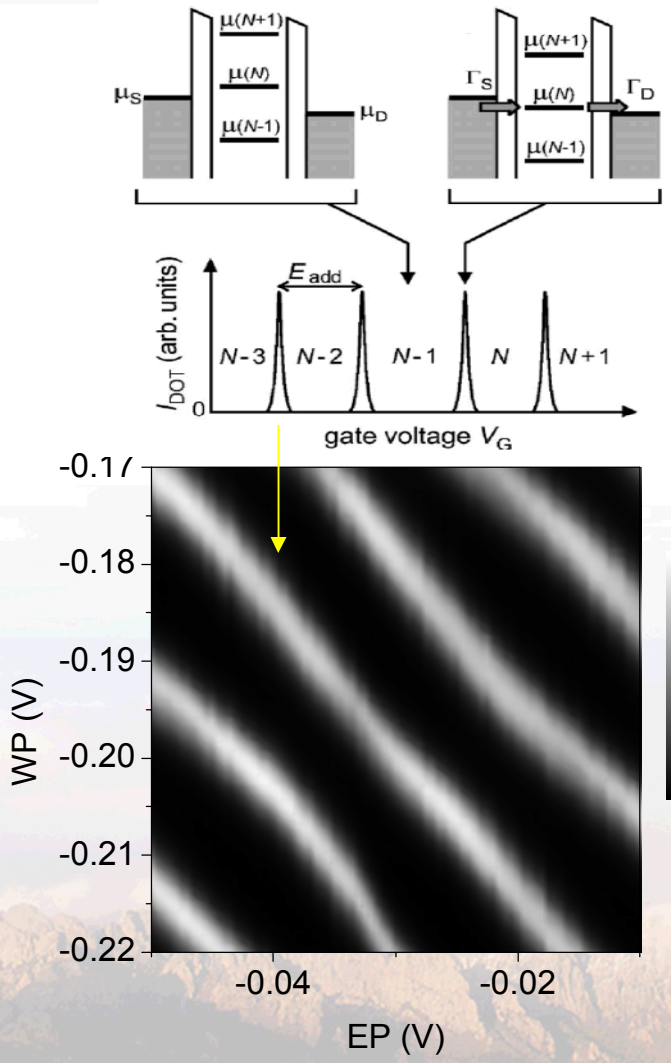
- Measured capacitances are consistent with lithographically formed dots
- Signal is consistent with 3D capacitance estimates for coupling

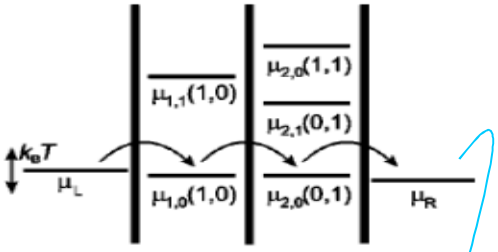
Stalford et al., IEEE T. Nanotechnology

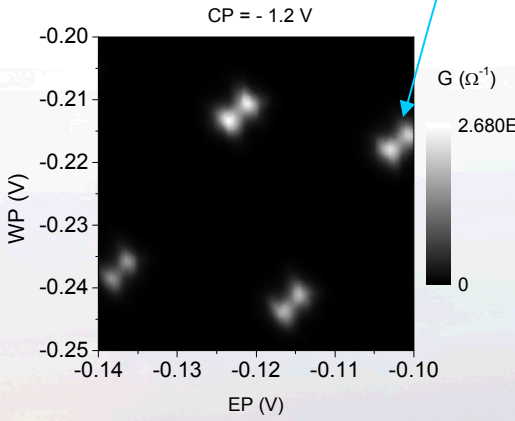
Reconfigurable Dot with Gates



TG = 5.0V
T = -0.3V
CP = -1.2V
R = -2.0V



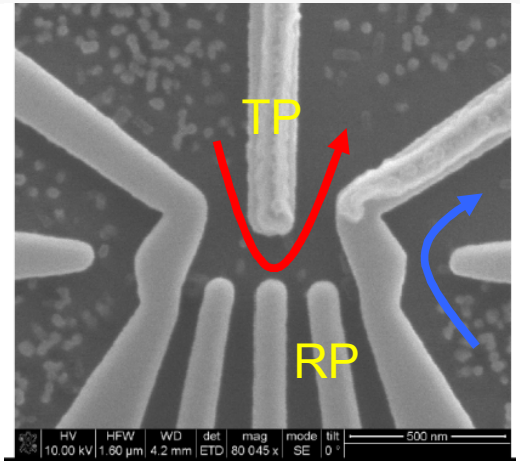




L. Tracy, et al.
APL 2010

Next step: reduce electron number

Smaller area design for fewer electrons



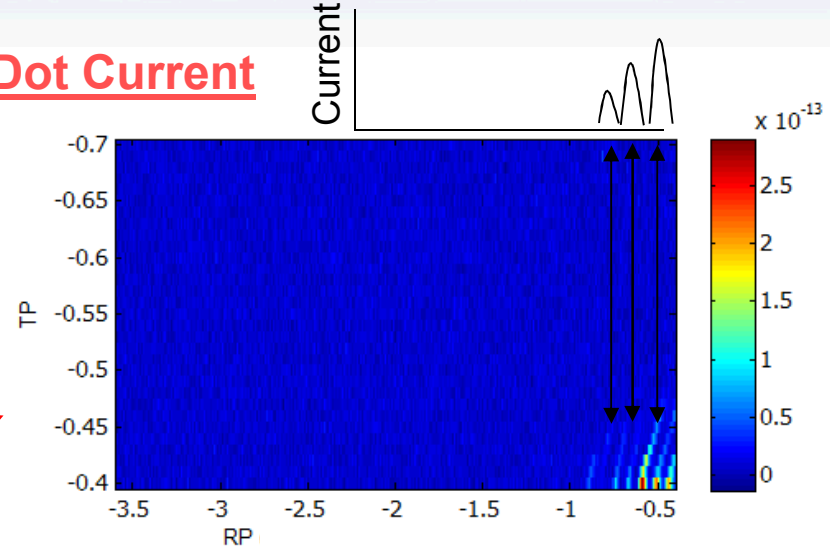
Transport drops below noise limit

Charge sensor detects many more transitions

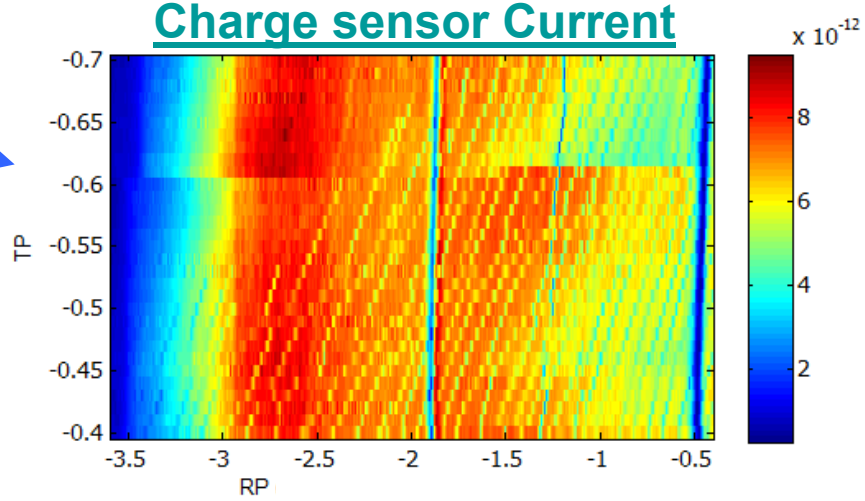
Charge sensor susceptible to metastable behavior of QD (are we at N ~ 1?)

- tunneling rate characterization w/ sensor
- this device started to drift
- semi-classical modeling => N~30-40

Dot Current



Charge sensor Current



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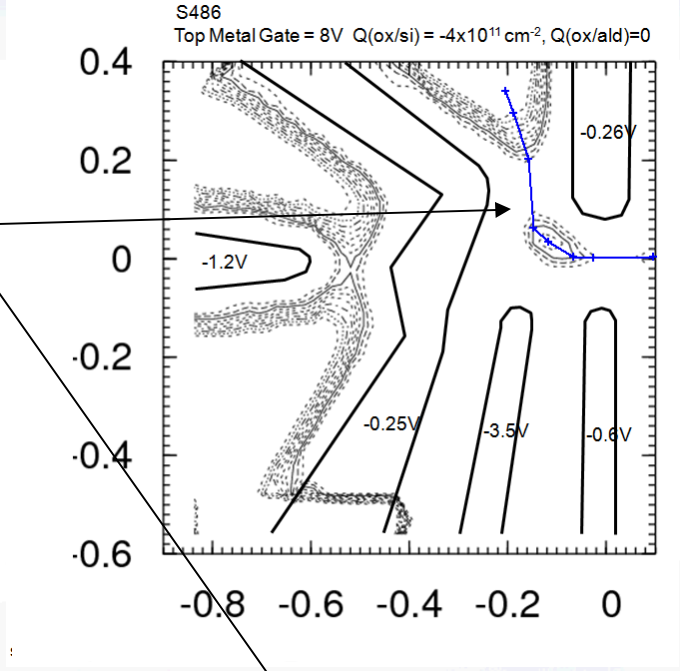
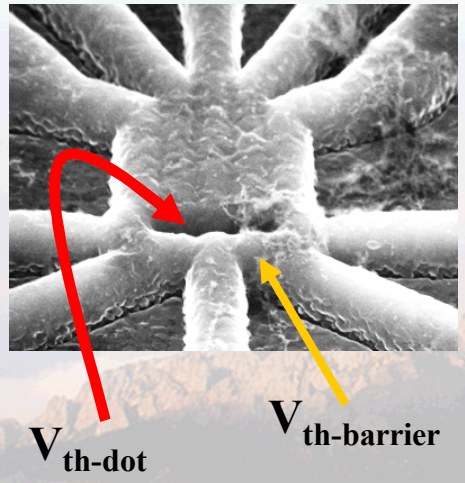
Challenges to achieving few electron

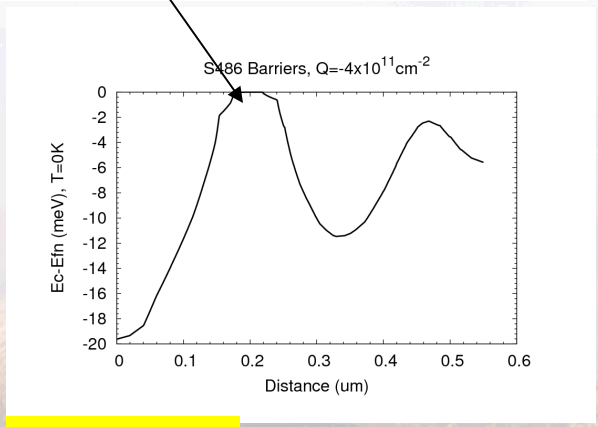
Challenge: More negative bias to reduce $N_{electron}$
ALSO results in wider tunnel barriers

C_{top} agree with simulation (+/-20%) at 32 electrons



Approach: open tunnel barrier





R. Young

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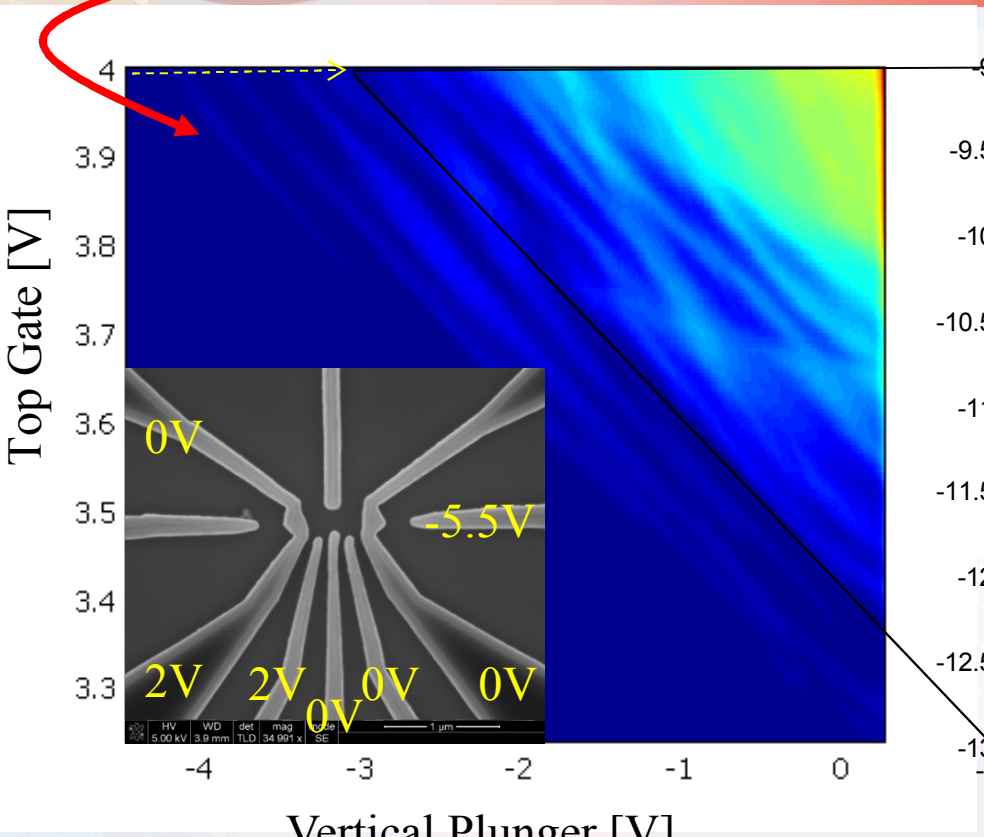
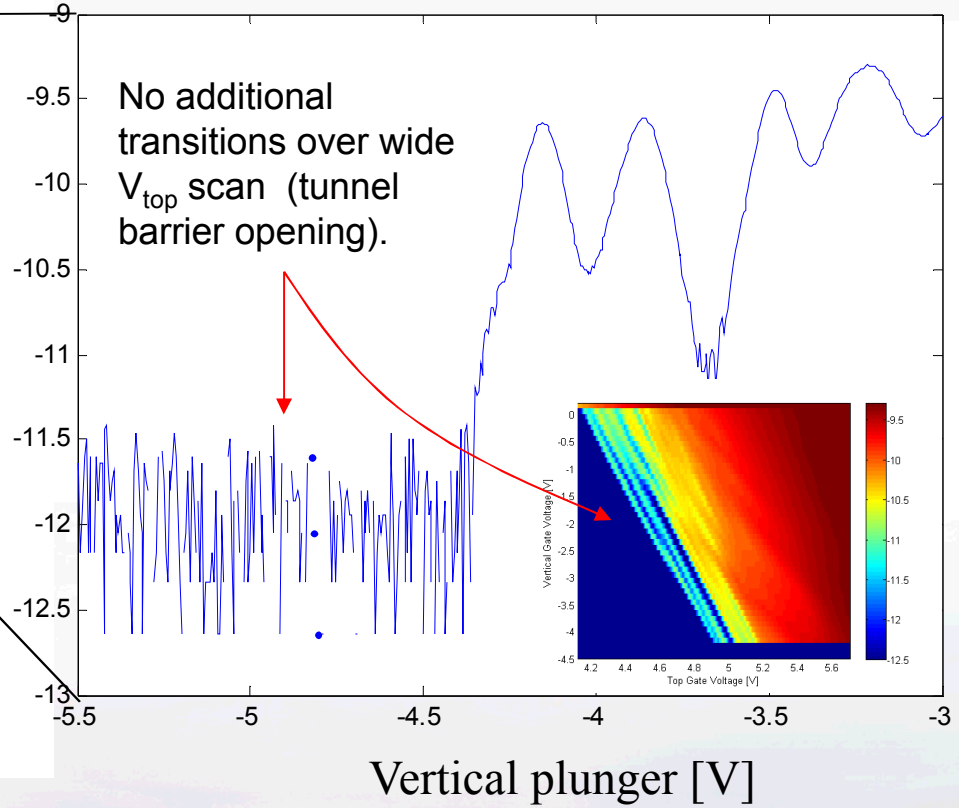
Wider tunnel barrier

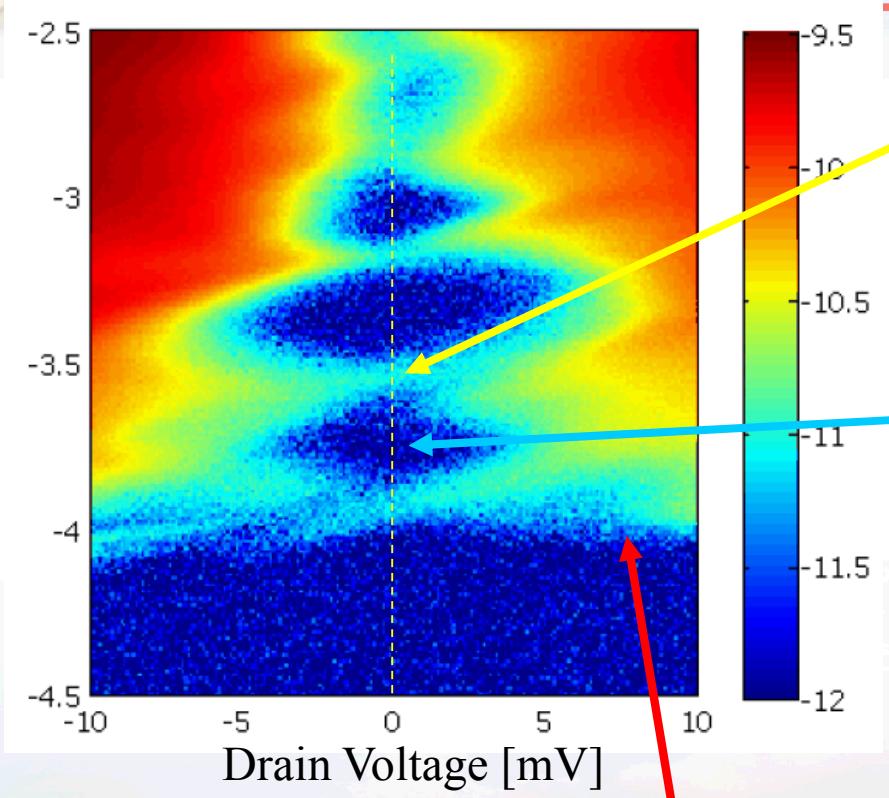
Last "visible" transition

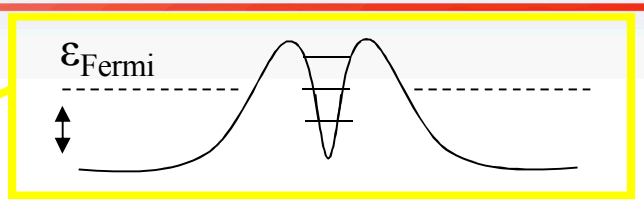


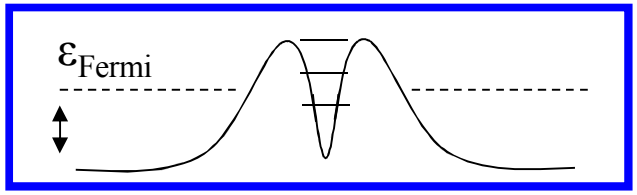


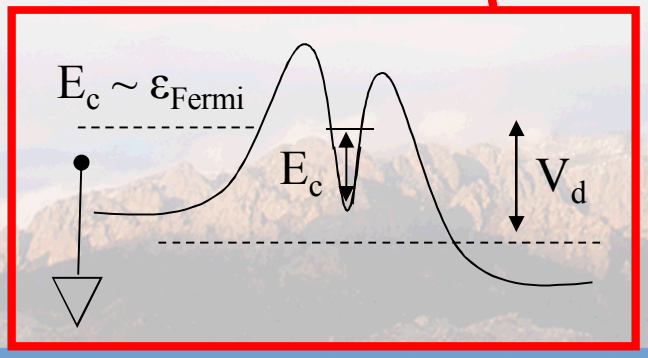
- Edge of transport through dot observed
- Several possible reasons
  - tunnel barrier is gradually turning off (often the case)
  - Last electron
- This case is not gradual and no additional transitions are observed over reasonably large V_{top} scan

Indicators of last electron









- No transitions observed at high V_{sd} beyond -4V on plunger
- V_{sd} can be set that all levels in dot can empty
- Edge of opening corresponds to line-up of energy level with Fermi energy
- Ideal case, well depth is no greater than Fermi energy
- Largest charging energy approximately equal to Fermi energy (5-6 meV)
  - This sample examined up to ~2*Fermi energy
- Three measurements suggestive of N=1
  - Other groups have used this as a test of N=1

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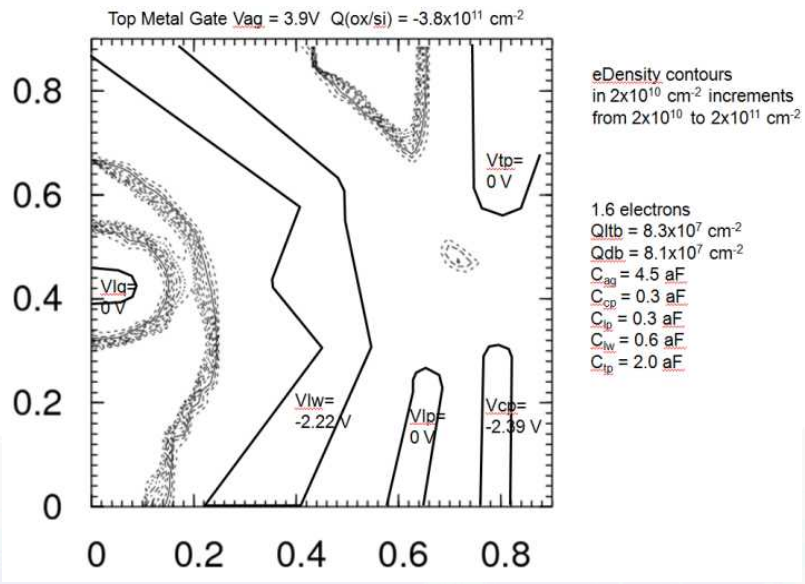
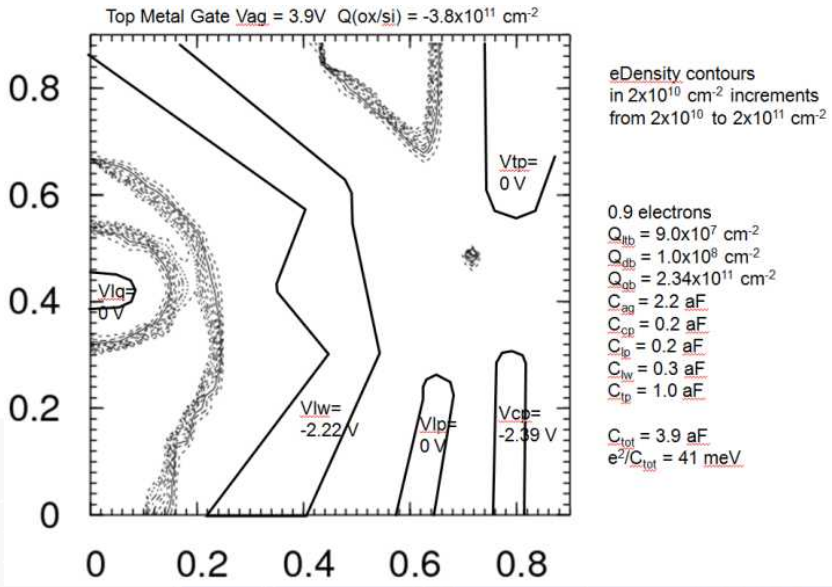
Last electron modeling

Semiclassical



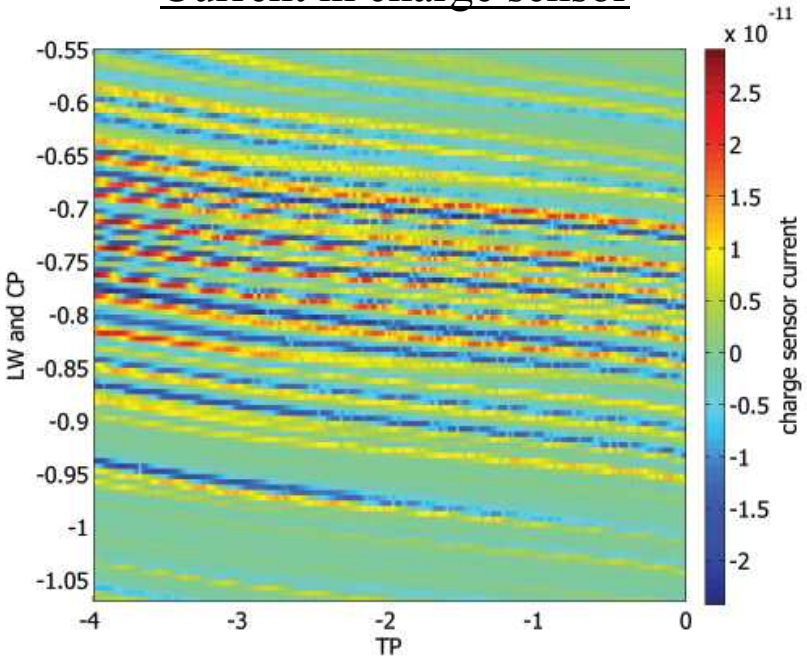
CI modification to TCAD



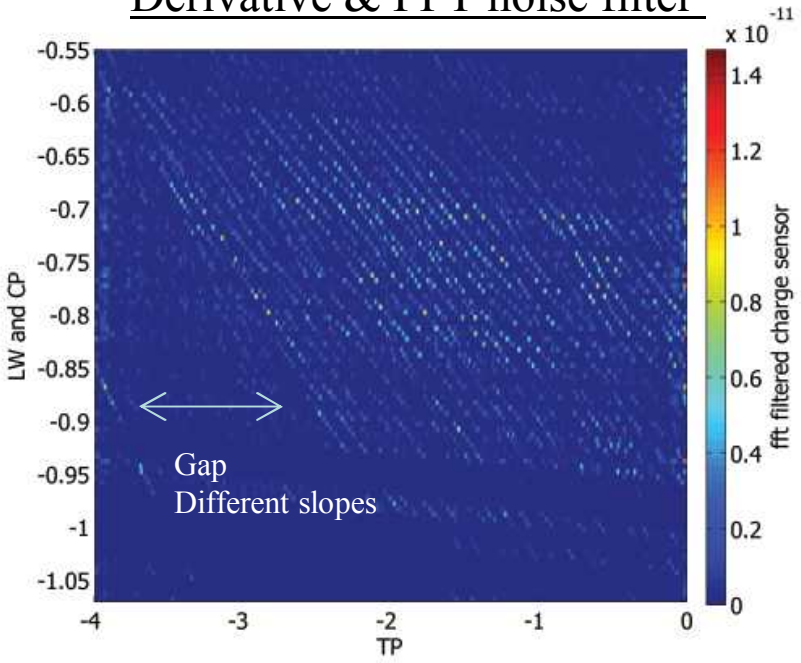
- Configuration interaction loop integrated with commercial TCAD package
  - Rapid convergence with effective mass calculation after single charge reconfiguration step
  - CI model predicts approximately 2x smaller
- Top gate and vertical plunger capacitances in good agreement with model
  - $C_{top\text{-}meas}$ ~ 2.6 aF ($C_{top\text{-}sim\text{-}N=1}$ = 2.2 aF)

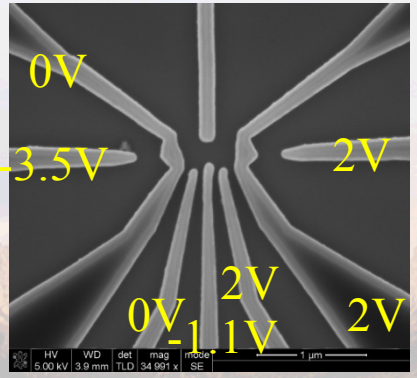
Charge Sensing to few electron (similar design)

Current in charge sensor



Derivative & FFT noise filter





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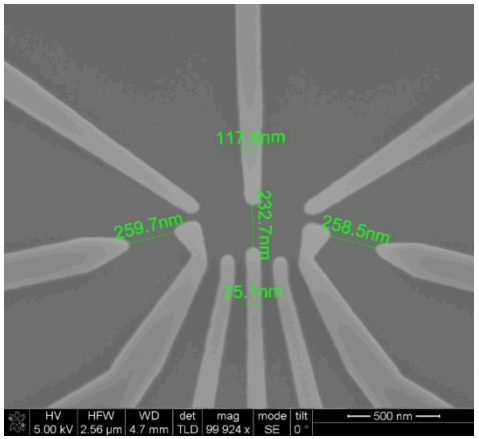
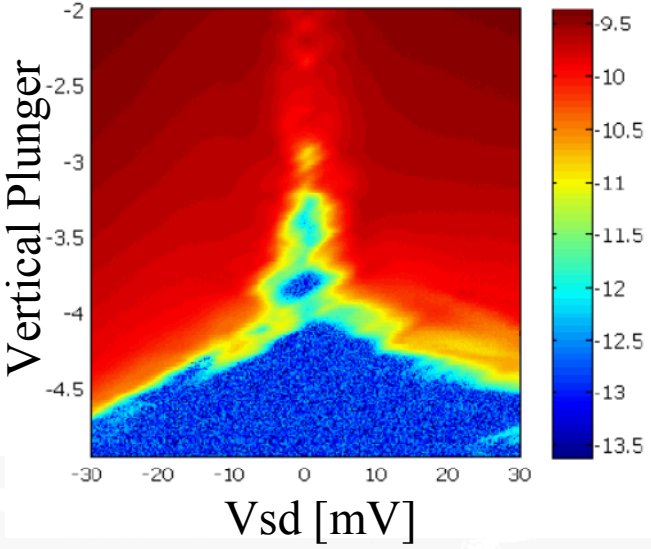
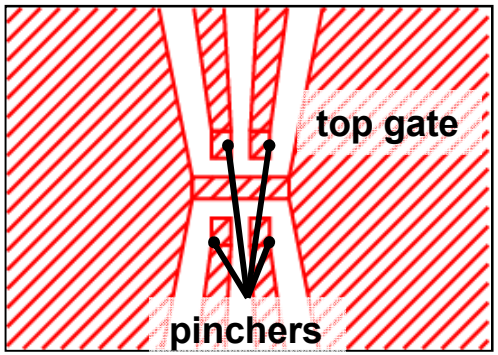
Last electron in MOS?

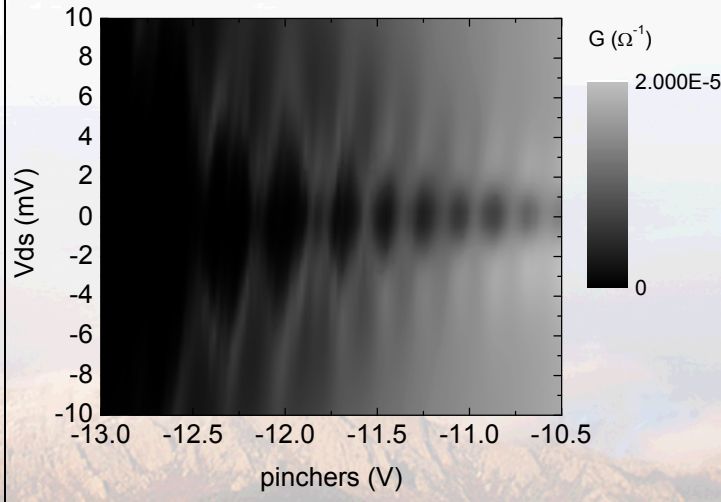






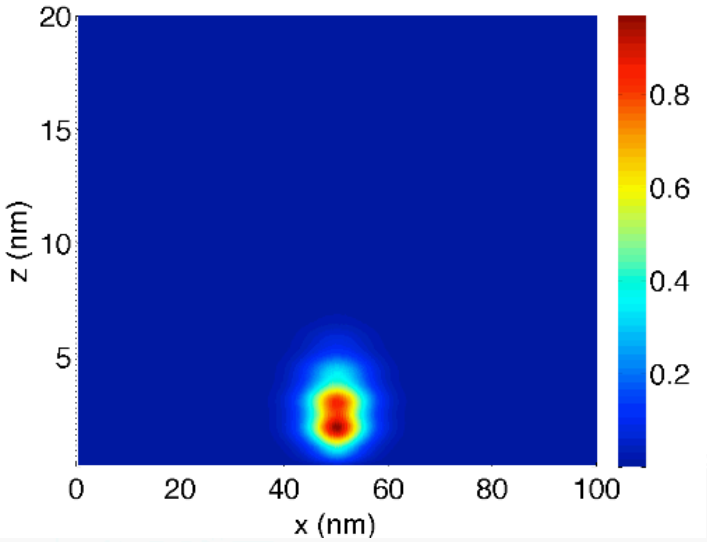
(K. Eng & L. Tracy)

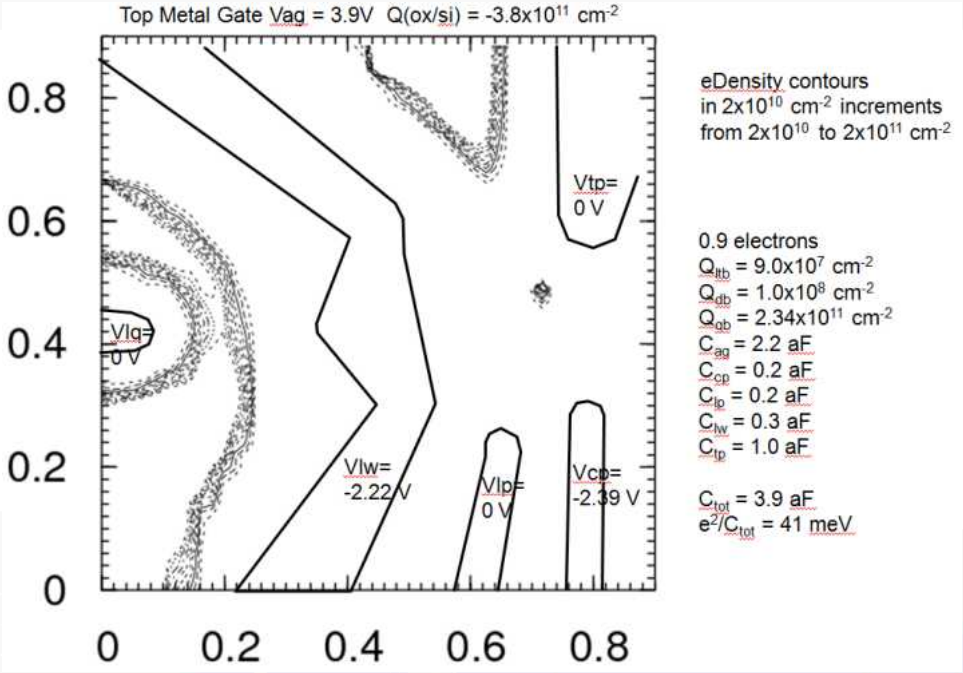
Vtg = 4 V
Wg = -75 V
T = 0.25 K



- Common in MOS for charging energy to rapidly increase as N => 1
- Charge sensing also detects outlier(s)
- Large area devices produce small dot charging energies?

Last electron modeling





D_{it} or Q_{ox} ($cm^{-2}eV^{-1}$) or (cm^{-2})

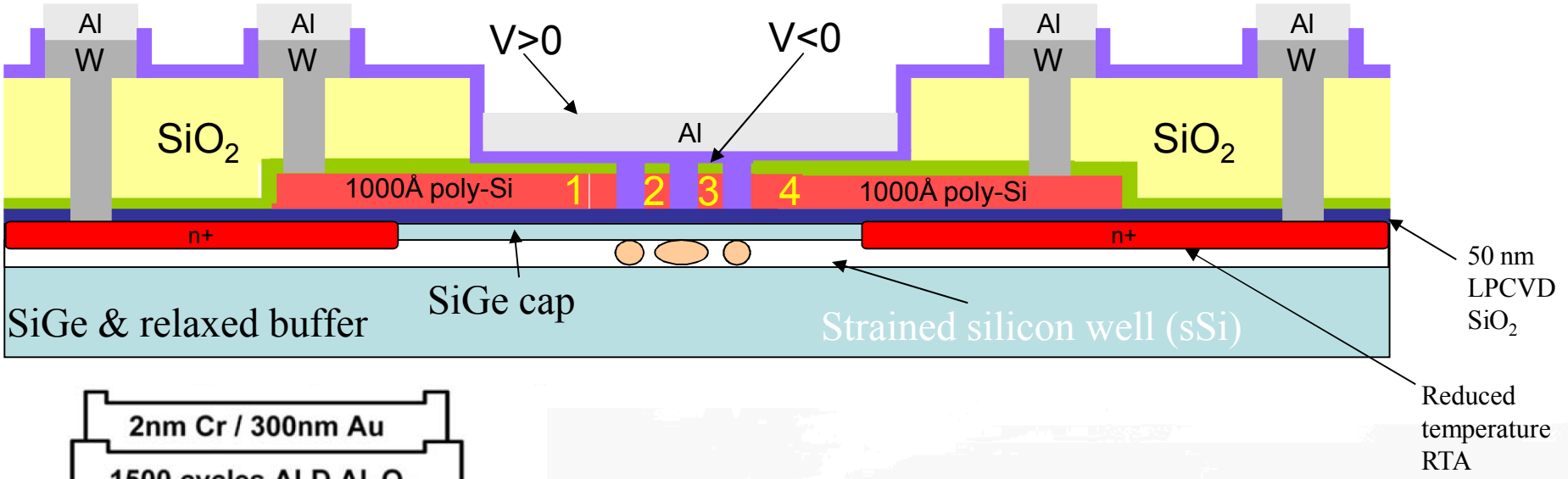
$1x10^{10}$ → 0.04 per QD

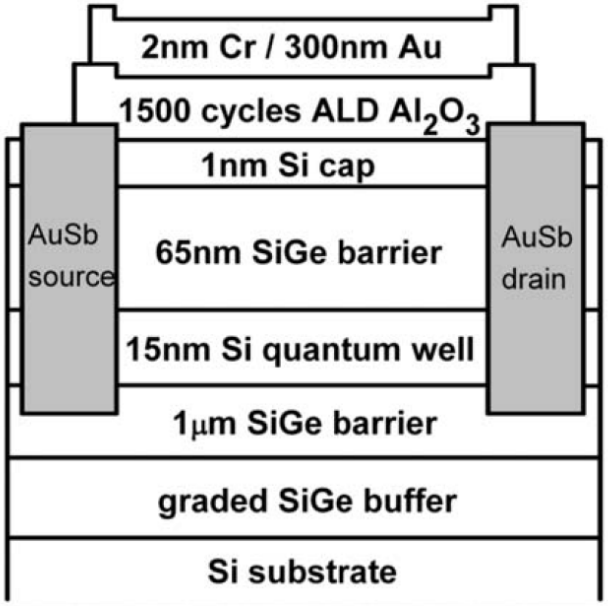
$1x10^{11}$ → 0.4 per QD

$1x10^{12}$ → 4 per QD

- Single positive charge at SiO2 interface can strongly localize electron & large binding E
- Last transitions jump in charging energy? Operate in closed shell N>1?
- But electrostatic dot is also predicted to be very small in some cases
  - Similar sizes predicted (~20 nm x 20 nm)

Enhancement Mode SiGe/sSi: High Mobility & Modular Change to MOS Flow



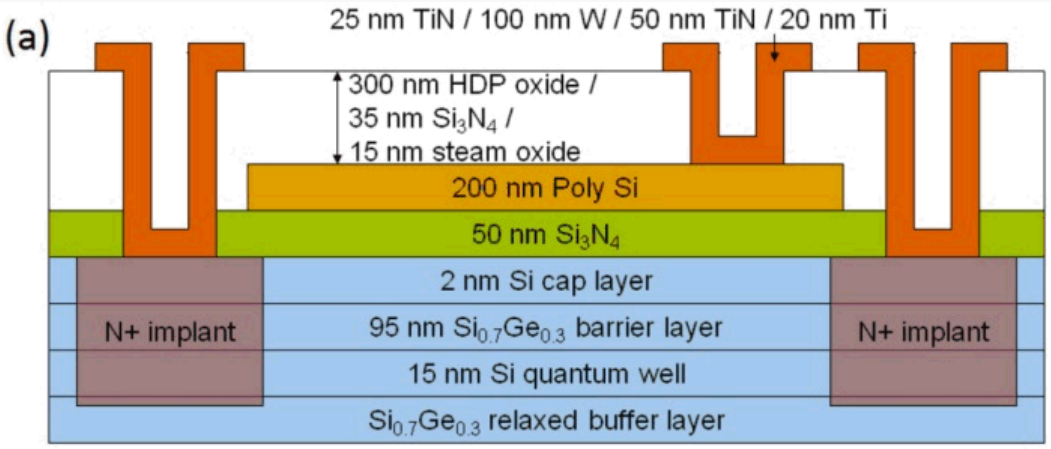


Undoped SiGe Heterostructure

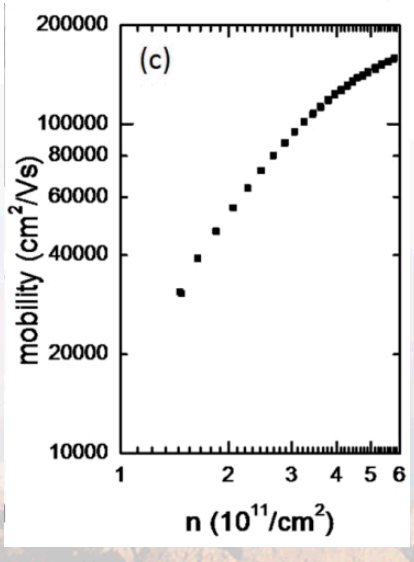
Lu et. al., APL **94**, 182102 (2009)

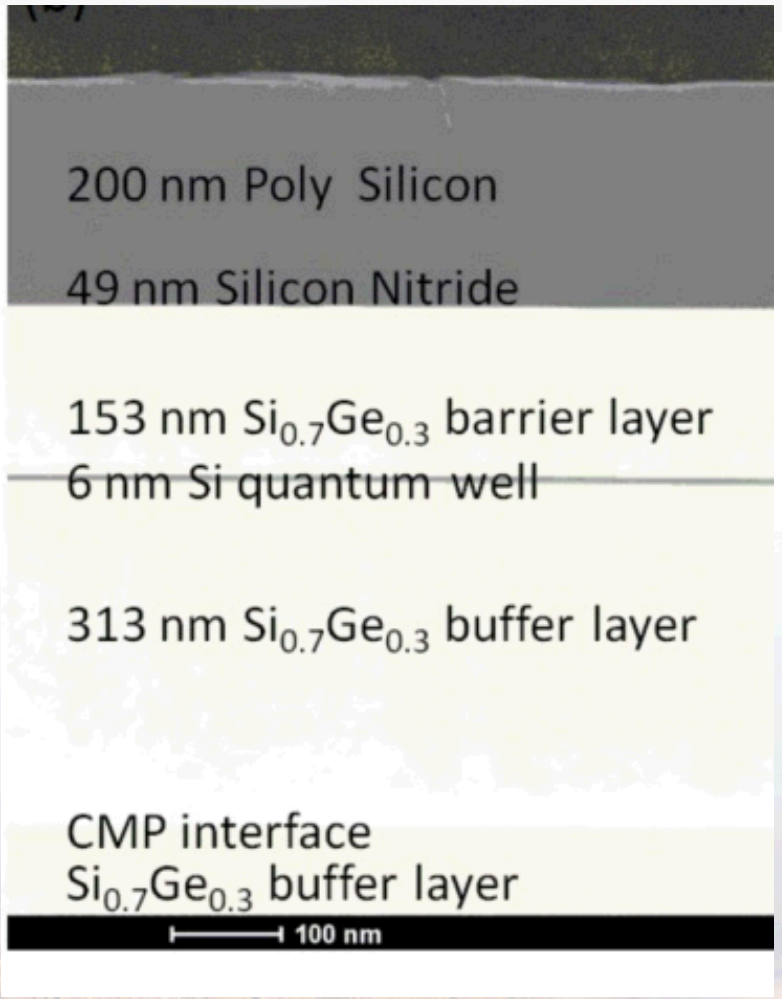
Mobility ~1.6x10^6 cm^2/Vs

Back to the fab: SiGe/sSi

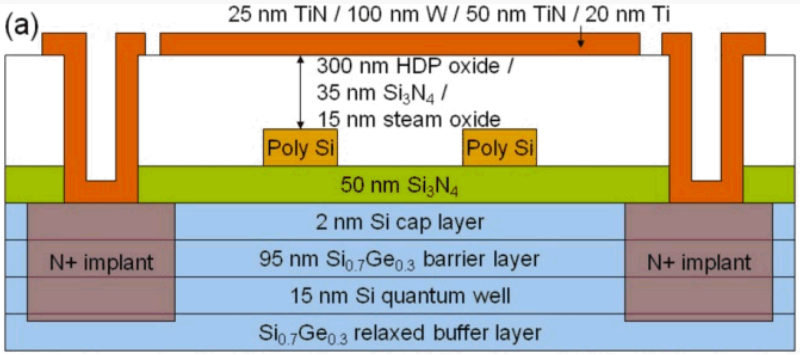


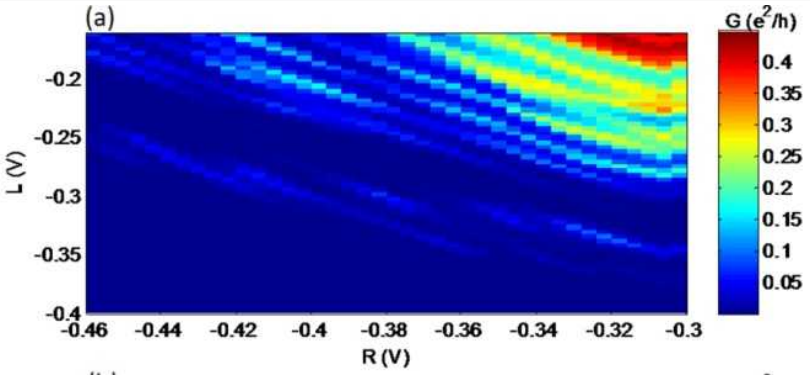
- Modifications:
  1. Substrate
  2. Gate dielectric
  3. Implant & anneals
- Questions:
  1. Ge/Si diffusion
  2. Surface pinning
  3. Mobilty

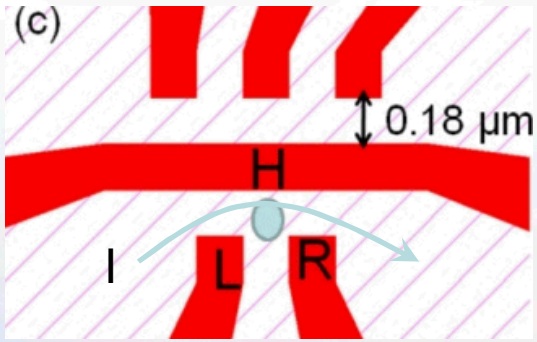


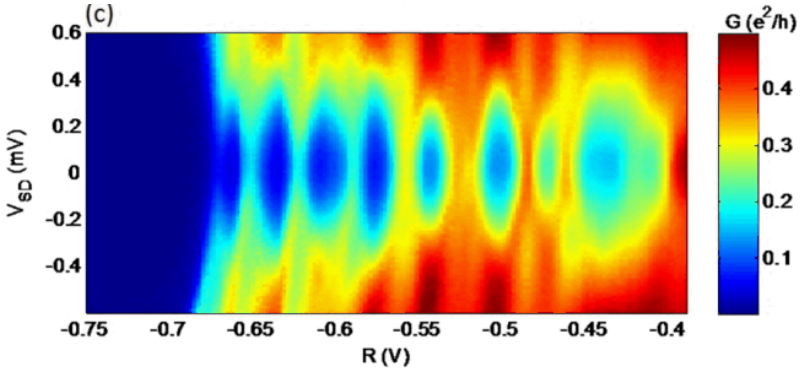


Transport through SiGe/sSi dot





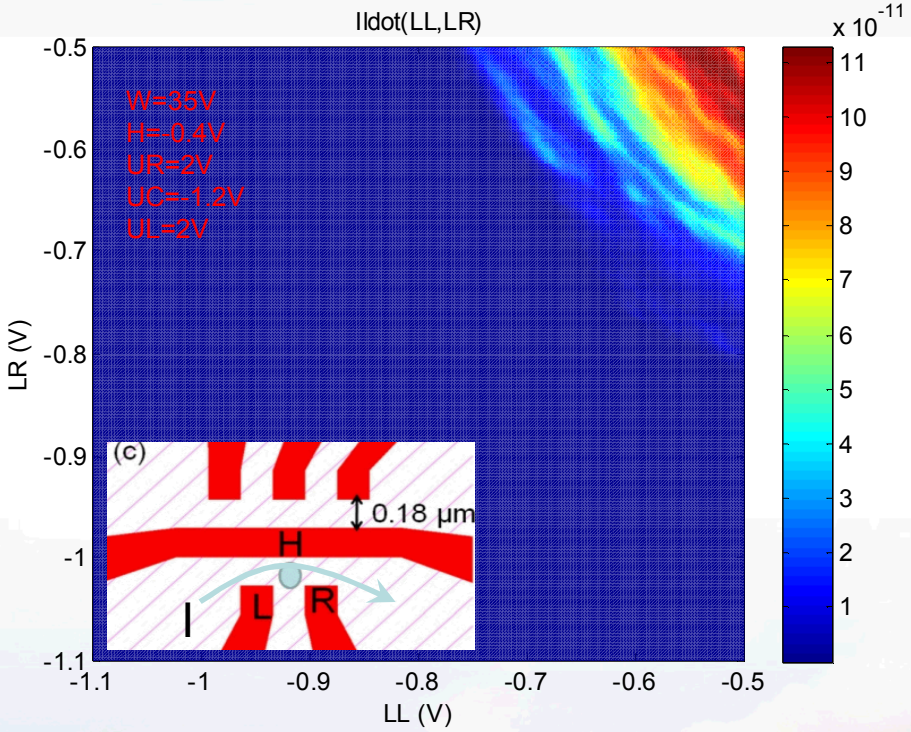


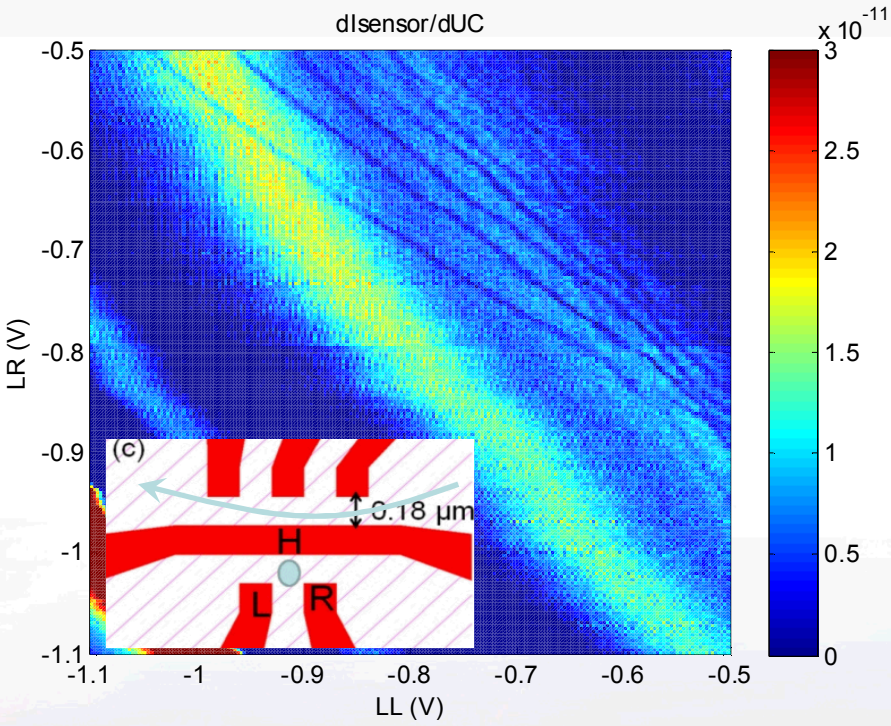


- Double top gated quantum dot w/ DUV lithography
- Relatively regular CB observed w/ small charging energy

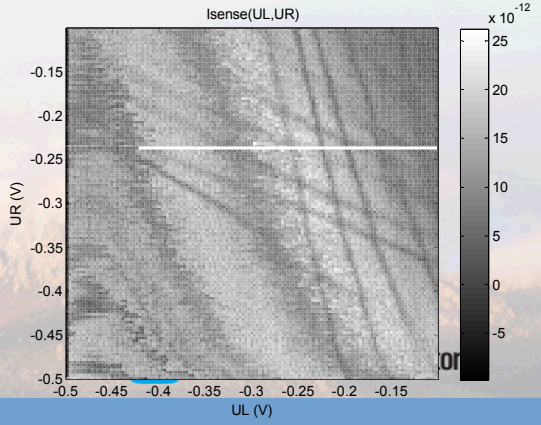
Lu et al, (in preparation)

Charge sensing: last transition

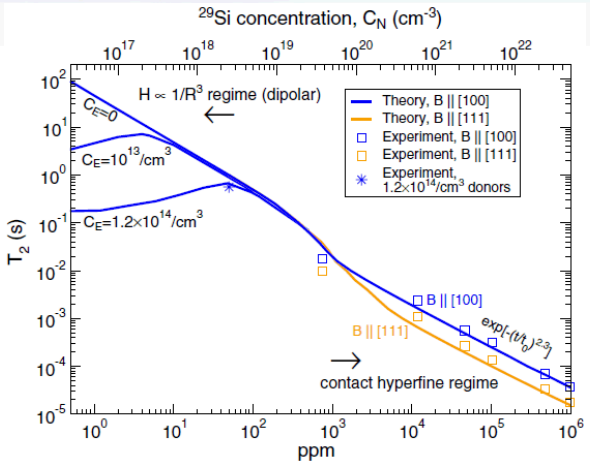


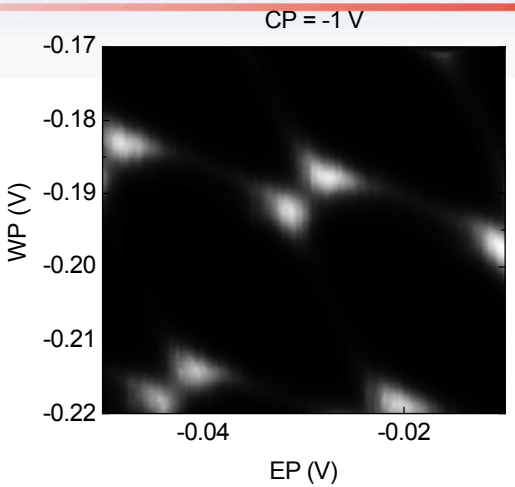


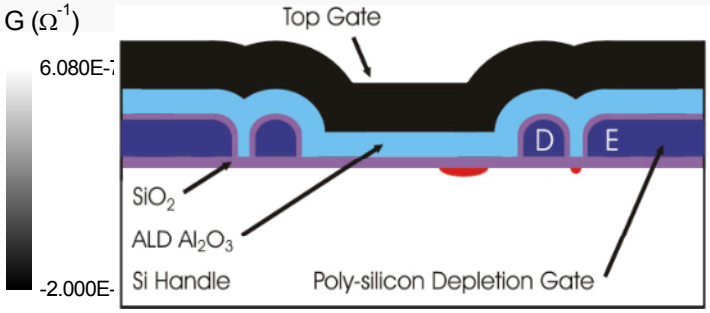
- Opposite channel used as charge sensor
- Last transition in region of high sensitivity of sensor
  - looks like the last electron
- Problem: charge stability

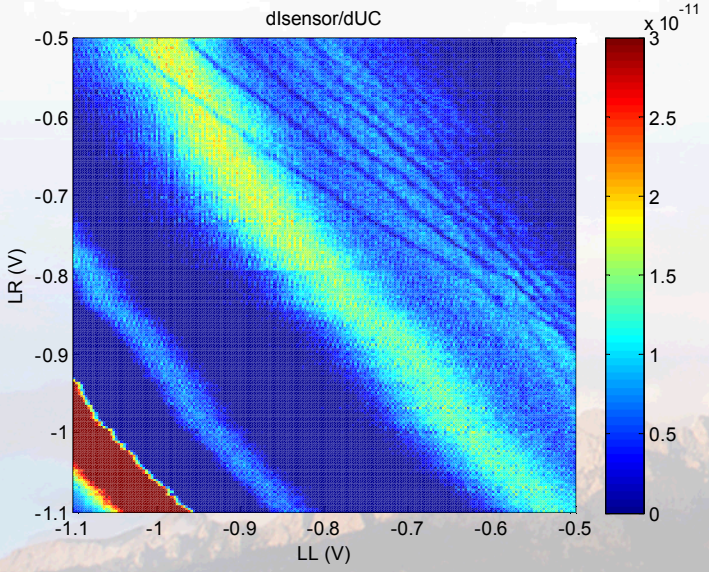


Summary









- Decoherence times can be long in Si
  - Relationship to impurities and enrichment well understood
  - Relationship to surfaces is still open
  - DD , DCG and OC show promise to reach logical circuit requirements
- Lateral, Si DQD platforms demonstrated
  - Low damage for MOS (Q_f ~ 10^{11} cm^{-2} , D_{it} ~ 10^{10} cm^{-2} eV^{-1}, mobility ~ 8000)
  - 150,000 mobility for SiGe/sSi
  - MOS because of infrastructure, donors and learning
  - SiGe/sSi because of more ideal system
- Double quantum dot & charge sensing of few (last) electron
- Lots still to do:
  - Few electron charge sensed DQD (S/T)

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