SAND2011-6885C

Robustness and Versatility of Thin Films on Low Temperature Cofired Ceramic (LTCC)

Wolf, J. A.[1*], Peterson, K. A.[2], Vianco, P. T.[2], Johnson, M. H.[1], Goldammer, S.[1]

[1] NNSA's Kansas City Plant, Kansas City, MO USA
*Phone: 816-997-2127 Email: awolf@kcp.com
[2]Sandia National Laboratories, Albuquerque, NM, USA,

Abstract

Thin film multilayers have previously been introduced on multilayer low temperature cofired ceramic (LTCC). The ruggedness of a multipurpose Ti-Cu-Pt-Au stack has continued to benefit fabrication and reliability in state-of-the-art modules. Space optimization is described, preserving miniaturization of critical spaces and component pads. Additional soldering details are also presented, including trends with solder-stop materials. Feature compensation becomes a simple step in the normal manufacturing flow which enables exact targeting of desired feature sizes. In addition, fine details of the manufacturing process, including ion milling, will be discussed. We will discuss full long-term aging results and structural details that reinforce the reliability and function. Different thin film materials for specific applications can be exploited for additional capabilities such as filters and other integral components. Cross sections verify the results shown. This successful integration of thin films on LTCC points to higher frequencies which require finer lines and spaces. Advancements of these applications become possible due to the associated progression of smaller skin depth and thinner metallic material.

This work prepared by The Kansas City Plant for the United States Department of Energy under Contract No. DE-NA0000622. The Kansas City Plant is operated by Honeywell Federal Manufacturing & Technologies, LLC.

Key Words: LTCC, thin film, PVD

1. Introduction

Thin film multilayers have previously been introduced on low temperature cofired ceramic (LTCC) multilayer electronic modules. [1] This paper expands upon our earlier report of success with a multi-functional multilayer thin film system on LTCC [2] providing additional characterization and capabilities. Long-term aging of soldered pads has been completed, demonstrating ruggedness sufficient for multichip modules (MCM). An engineering decision to use thicker gold (not part of this report) has resulted in superior performance for wire and ribbon bonds. A very conservative line pitch has been used to date, and we discuss factors involved in improving the miniaturization of minimum feature sizes. Specifically, space optimization – which was a spin-off benefit to us – is demonstrated, allowing components to be mounted closer to critical elements and in a smaller space. We provide additional detail regarding ion milling and look ahead to the possibilities of laser definition of features on LTCC. An edge monitor contains many features to assure quality is maintained as implementation proceeds. Finally, the combination of thin film with fired parts undergoing green state machining of LTCC tape has provided some benefits that can also be incorporated into prototype MCMs.

The decision to use thin films was not made lightly-many trade-offs were considered. An example of a thin film line (explained below) is shown in the SEM photo in Figure 1.

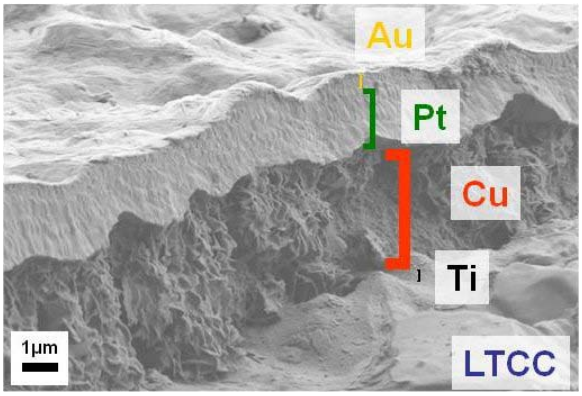

Figure 1. A view of the edge of a multilayer thin film line on LTCC reveals some of the layers.

The appearance shows that the different layers etch somewhat differently in that the copper seems to be set back from the overlying Pt and Au layers. Cu also has developed a complicated surface structure presumed to be from ion milling.

2. Background

Low temperature cofired ceramic multichip modules are common, due to the commercial availability of tapes and associated thick film inks. Our implementation exposed concerns for long term performance and yield using thick film only compositions. Thin film layers were used to boost the manufacturability and reliability of MCMs – especially in the area of solderability and aging behavior. We experienced multiple post-fired steps on each side of a double-sided prototype in order to thicken the solderable thick film against liquid phase and solid state intermetallic compound formation. The refiring was driving sub-LTCC surface structural changes that were causing weakness. This weakness was revealed in cross-sectioning and not actual prototypes. A major challenge was to deal with critical surface topography at vias, since elevation changes or moats could compromise the coverage of the thin film. Solder penetration at a via proved catastrophic for early thin film development stages.

The development of thin film on LTCC was initiated in order to address and improve the following aspects:

- Reliability – Long term performance of soldered connections
- Durability – Continued good performance through testing and in the field.
- Conductivity (DC and RF) – Materials selection for good RF properties.
- Good line width tolerance – Line is full thickness all the way to the edge, unlike thick film.
- Good line edge tolerance – Photolithographic definition exceeds the capabilities of screen printing due to mesh/emulsion in screen printing.
- Wire bond connectivity – Improved bond ability and adhesion values, including aging.
- Solder connectivity – Improved and sustained ability to wet the surface.
- Miniaturization – Capability to use better edge definition for smaller features.
- Reworkability – Primarily due to durability and persistence of solderability.
- Good aging performance – Soldered and wire bonded connections as well as associated components.

The films we have used were added with physical vapor deposition by evaporation. The adhesion is assisted by a first layer of Ti. The RF conductivity is assured by a thick Cu layer. Atop the copper is a Pt layer that acts as a barrier against diffusion in both directions (Cu and Sn) and enables solder connectivity. Finally, a Au layer assures wire bondability and preserves solderability. The gold is thin enough to mitigate embrittlement when incorporated into the solder by dissolution. A schematic cross-sectional view of such a multilayer thin film stack is shown in Figure 2.

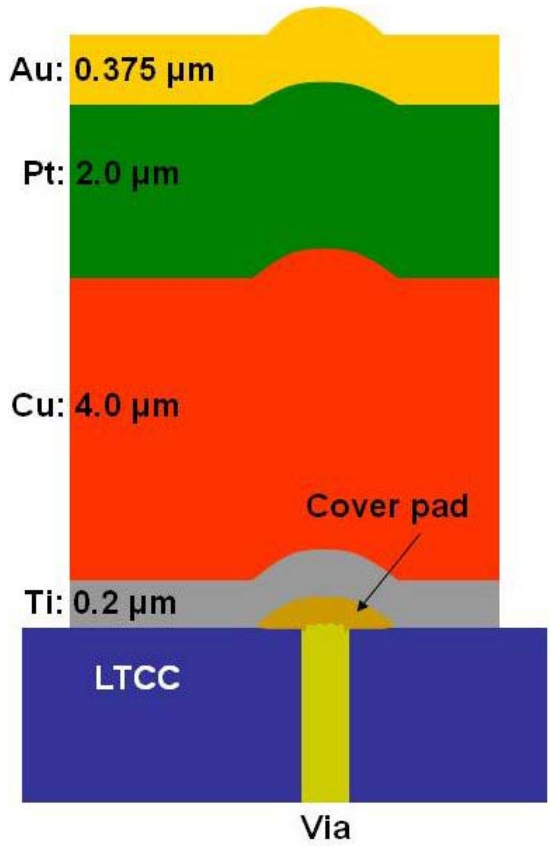

Figure 2. Schematic (color coded) cross section of thin film layers illustrating coverage of a thick film barrier pad over a filled via (not to scale).

Details of an actual structure which were obtained using a focused ion beam (FIB) apparatus are also shown in Figure 3. It was necessary inside the FIB apparatus to coat the area with Pt and then a photoresist prior to performing the cut, which provided uniformity to the cross sectioning technique.

The FIB cross section reveals interesting details of the polycrystalline thin film growth and ion mill patterning. Grain structure is visible in the Cu, Pt and Au layers. In many instances the grain growth continues epitaxially across material interfaces, such that 'continuous' grains are visible through all three

layers. Subtle shifts of the grain walls at the Pt/Au interface help identify the location of this interface and distinguish the two layers.

In Figure 3 the angle of the ion milled edge of the thin film multilayer is indicative of the ion mill process. Two ion mill angles were used repeatedly to achieve good edge and line definition, 45º from normal for bulk ion milling and 18º from normal to sharply define the edge. This optimized milling sequence inhibits the formation of a 'foot' or edge at the base of the multilayer stack. Such a foot can be partially masked by the tall geometry of the line edge and is undesirable. A very unusual structure is seen at the edge of specifically only the Cu layer, both in the actual cross section, farther back in the same picture along the edge of the thin film layer, as well as in Figure 1. The structure to a depth of approximately half of the layer thickness (about 2µm) is broken up into fine interlocking slivers or splinters. This structure is fine enough to be extremely sensitive to the accelerating potential used in scanning electron microscope imaging, being more transparent at higher voltages. The reason for this appearance has not been determined yet, with both scattered milling and slight wet under-etching as possibilities. However, the final structure inadvertently allows for a very robust and solid thin film edge with high resistance to Sn migration around the protruding Pt ledge into the Cu, as is discussed in Section 3.

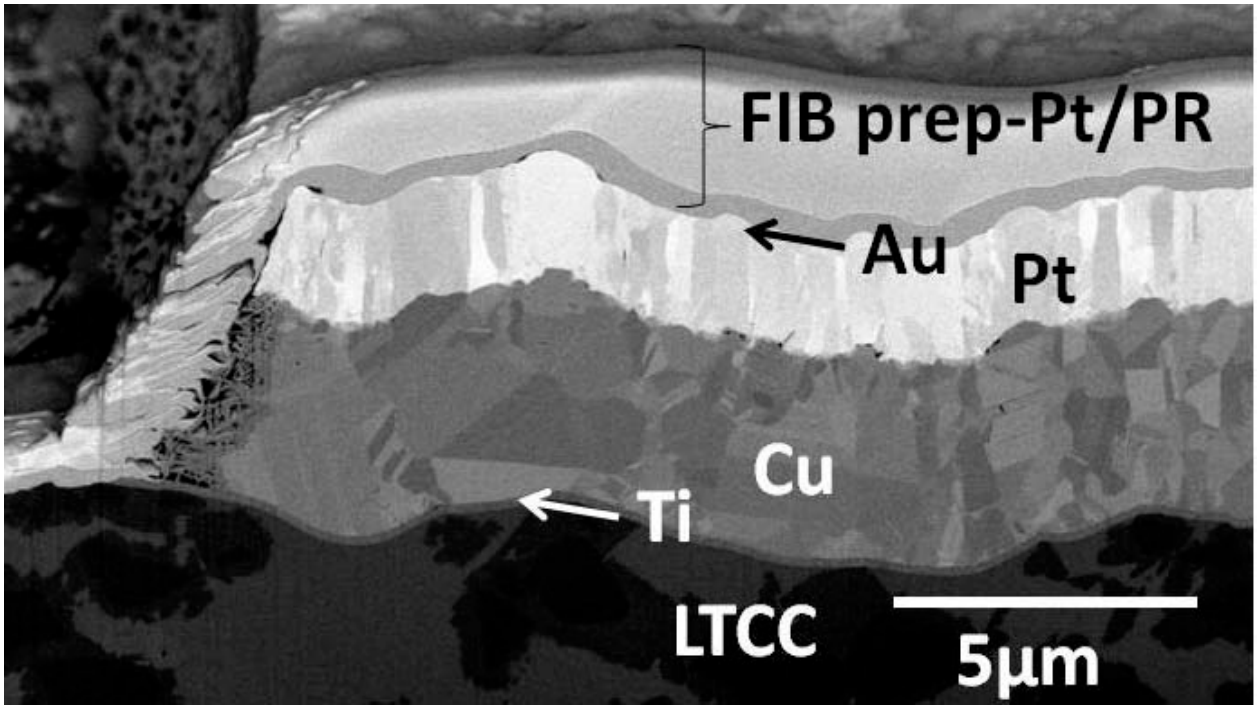

Figure 3. FIB cross section of line edge.

3. Fine features

Feature size is commonly a function of film thickness, etch (or deposition) properties, and photoresist thickness. In our case, due to the total thickness of the thin film multilayer, a thicker photoresist is necessary in masking defined circuit areas from the ion milling. Thinner photoresist can be eroded partially or completely, interfering with the circuit definition. Ion milling has proven to be superior for pad definition over both physical masking during deposition and photoresist lift-off techniques (patterning prior to deposition). However, the necessary photoresist minimum thickness, for patterning a 6.5 micrometer thick metal stack, has an effect on minimum feature size. Despite this, we are still able to resolve lines and spaces down to 2 mils on prototypes (Figure 4). Four mil lines and spaces are reliably patterned in quantity. Literature reports of thin film lines below 2 mils involve thinner films and thinner associated photoresist films.

Despite being able to resolve small features, initial results using physical masks allowed the Sn to attack the exposed Cu edge, as shown in Figure 5. In this Figure, the cross section is depicted in part a), while the Cu, Sn and Pt energy dispersive results are shown in parts b), c) and d) respectively. Note that the arrows point to the approximate same location, where the Sn signal is seen to wrap around the Pt layer, while the Cu is totally dissolved to a distance of about 25µm. Dissolution distances upwards of 50µm were observed, increasing the risk of Sn

migration into Au via fill material and a resulting electrical failure (loss of continuity). Thus, for

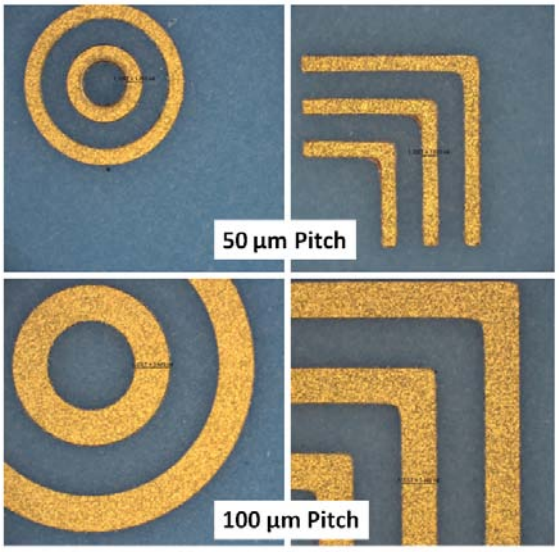

Figure 4. Achieved resolution examples of 2mils (50µm) for prototypes and 4mils (100µm) for reliable production.

patterning with physical masks, where the edge is not as sharply defined, a solder stop was necessary as edge protection against such a failure. The solder stop material, in turn, would negate any benefits in miniaturization that were gained by the fine feature sizes down to 4mils, necessitating a comparatively large area of solder stop material between adjacent thin film pads.

The use of ion milling to create the desired pattern, however, has created robust edges that

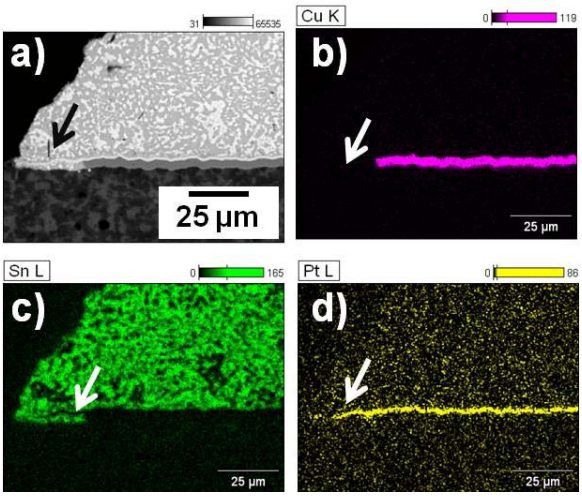

Figure 5. SEM (a) and X-ray energy dispersive analysis, b) Cu, c) Sn and d) Pt, of a sideline breach in an early development thin film.

virtually eliminate any risk due to Sn migration into the Cu. As stated above, the ion milling process leaves a small protruding ledge of Pt that is characterized by the milling angle and that demonstrates relatively sharp corners. These act as a migration stop for the Sn, keeping the edge of the Cu pristine (Figure 6, left half). Only in a very few instances has a Sn migration been observed around such an edge, and typically only after long term aging treatments (Figure 6, right half, after ten days at 135ºC). In those cases where migration has occurred, however, the small amount of Sn that is able to migrate around the sharp corner has limited the effect to only a few micrometers (even after long term aging), eliminating the risk.

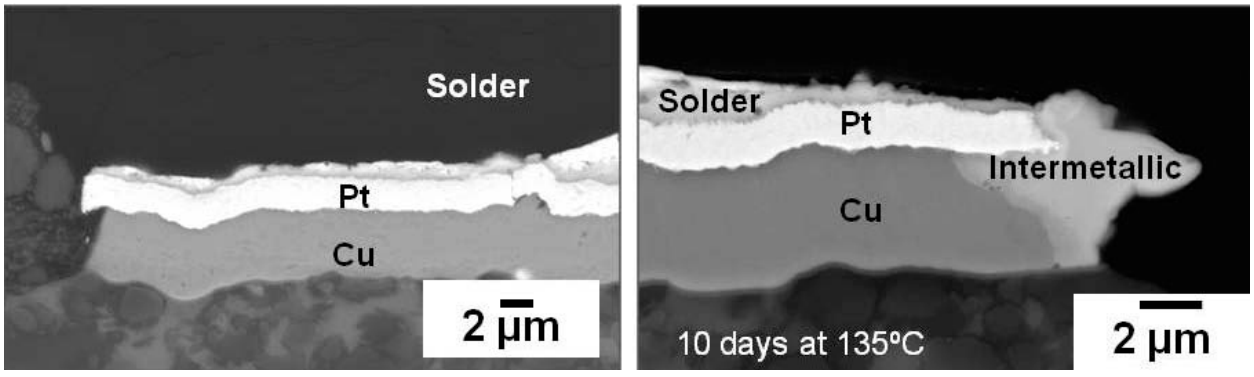

Figure 6. The edge structure affects the solder attack of the Cu portion.

Thus the ion milling of the thin film has made it possible to back the solder stop away from the pad edges such that the pads are not defined by the solder stop – similar to the practice in PWBs. The full gains of the 4mil fine features achieved with ion milling can be put into practice.

The origin of this etchback is still not understood, as was previously mentioned. The fact that it removes the Cu to approximately half of the Cu layer thickness, with the deepest recess being at the top just beneath the Pt, the fact that Cu is removed that is not in direct line-of-sight of the Ar ions during milling (Figure 6), independent of the milling angle, and the fact that a smooth Cu wall can be achieved would support indirect dry etching due to scattering of Ar ions close to the line edge. The splinter-like appearance as seen in Figure 3 supports a slight wet etching preferentially along grain boundaries during photo resist stripping. However, neither of the two explanations is conclusive and further investigation is necessary.

4. Space optimization

The elimination of the solder stop or other dielectric material due to the ruggedness of the ion milled thin film edges allows for much denser packing of surface mount parts. Where wire bonding is desired the bond pads can be located within 4mils of each other, and 4mil lines and spaces features can be achieved to match typical wire bond pad spacings on chips without resorting to either fan-outs or staggered pad rows. Even solder pads can be located much closer to each other with thin film as compared to thick film. Figure 7 shows the two solder pad cases for '0402' surface mount devices. The solder pads in the

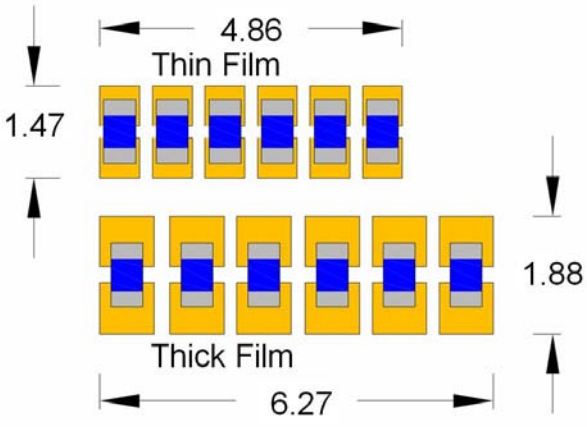

Figure 7. Size reduction for 0402 devices due to implementation of thin film on LTCC. Top row is thin film, bottom row thick film solution. Dimensions are in mm.

bottom row (indicated in yellow) demonstrate the closest spacing for thick film parts utilizing triple print solderable thick film for reworkability and defined by a dielectric to avoid edge vulnerabilities. The solder pads in the top row (also indicated in yellow) demonstrate 8mil spacing for thin film for surface mount ease. As mentioned above, edge vulnerabilities have been eliminated by the characteristics and geometry of the thin film material. The solder stop or dielectric material is pulled back in a manner more common with PWB and only serves the function to protect open areas of the circuit from inadvertent contact with solder. When utilizing full miniaturization the spaces could be further reduced to 4mils, reducing the length of the array shown by an additional 0.5mm to a total of only 4.36mm. The full array area is reduced from 11.79mm^2 (thick film) to 7.14mm^2 (thin film with 4mil spacing), a reduction by almost 40%.

5. Interaction of thin films with green machining.

Thin films have also provided a reliable solution to EMI required by circuits. Evaluation of full tape thickness feature (FTTF) seal frames to accomplish faraday shield structures has been presented. With improvements to the FTTF itself, the behavior of the thin film is sufficient to provide crack-free assemblies. Such assemblies are currently being tested for long term effects. A slightly different method of achieving effectively the same faraday shield structure with solid conducting walls is to combine the green machining of a prelaminated structure with sense-mode milling, which electrically detects the ground plane and limits the plunge depth. The creation of this wide trench with angled side walls and the exposed thick film ground plane at the bottom lends itself to coating with the solderable thin film material. The robust thin film material can be deposited along the bottom, walls and onto the top shoulder of the trench, without the necessity of any protection. The seal frame can be mounted directly atop the thin film in the bottom of the trench without using the FTTF (Figure 8).

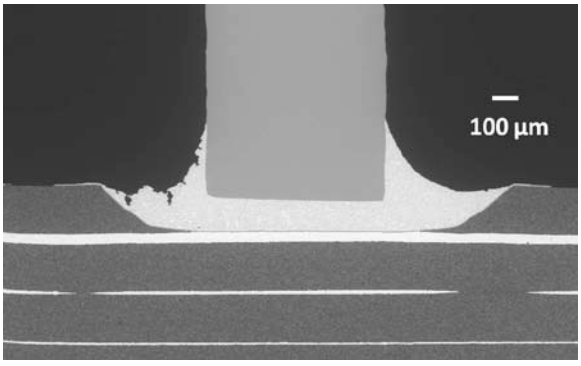

Figure 8. Cross section of seal frame soldered with SnPb into a wide green-machined trench coated with thin film (after aging).

The seal frame is placed in a less-conventional manner, locating it directly onto the ground plane level. The bottom of the seal frame through the thin film and ground plane make a continuous faraday cage with outstanding isolation characteristics. Initial aging tests of this structure have indicated a high reliability and hermeticity to fine leak levels over multiple hundred heat cycles.

In fact, the cross section showed in Figure 8 is of a part that has undergone accelerated aging over multiple hundred heat cycles. The area to the left of the central seal frame wall in the figure was exposed to air, while the area to the right was hermetically sealed with an inert gas. After these cycles prior to cross sectioning the part still passed a fine leak test (better than 10^{-6} ccm atm/s). Notice that the left side of the solder that was exposed to air shows typical aging characteristics of SnPb solder, which eventually lead to failures. However, the right side that remained exposed only to the inert gas still looks pristine and does not show the typical signs of aging. The appearance is still very much like a similar cross section of an as-fabricated part prior to aging. The outstanding isolation characteristics become clear in that the typical aging of SnPb solder must affect the total distance from the air-exposed side down into the SnPb fillet, under the seal frame and up through the inert-gas exposed SnPb fillet before effectively becoming a leak.

6. Long term aging

Both solid state and liquid state aging studies were performed to establish the ruggedness of the thin film material on LTCC. The methodology for determining the aging characteristics included shear testing of soldered surface mount devices, pull testing of solder pins, and cross sectioning.

The parameter space for the solid state aging ranged over various temperatures and times up to 170ºC and 100 days. Even after 100 days at 100ºC the thin film layers remain intact, as seen in Figure 9. The extent of intermetallic growth at the solder-Pt interface and, with that, the Pt consumption is only moderate.

Serious degradation of the thin film structure starts to appear after aging at 170ºC for 25 days (Figure 9). Significant amounts of Pt have been consumed into the intermetallic compound, and initial breaches have formed where the solder is able to penetrate into the underlying Cu layer and start a reaction. After 100 days at 170ºC the Pt and Cu layers are both completely consumed towards the formation of a Cu-Pt-Sn intermetallic (Figure 9). However, even under these extreme aging conditions there was no loss of integrity at the interface to the LTCC. Pin pull test data show that the effect of this extreme solid state aging does not cause a catastrophic loss of adhesion.

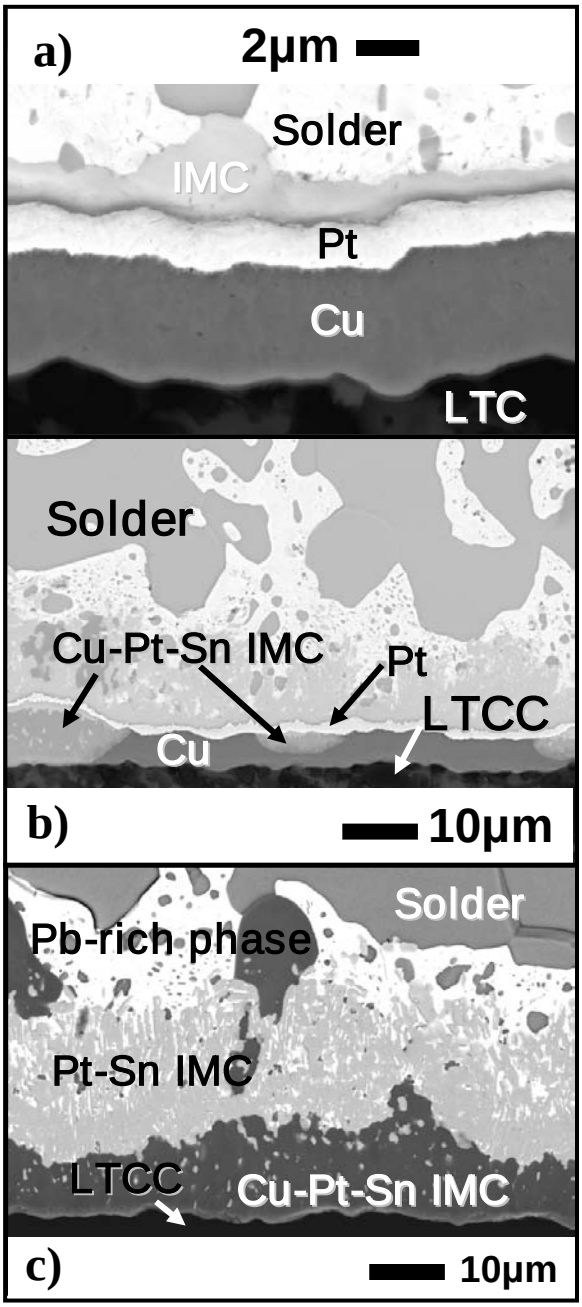

Figure 9. Long term aging results. a) 100 days at 100ºC, b) 25 days at 170ºC, c) 100 days at 170ºC.

The liquid state aging was performed in two fashions, the first being multiple traditional solder reflow cycles. Wetting and spreading of the solder was excellent, and the robustness of the thin film edge was demonstrated, as discussed previously.

The second method was to effect both aging and temperature shock simultaneously by immersing entire parts into a SnPb solder bath maintained at 290ºC for up to 15 five-second-intervals. Pin pull test data displayed the excellent pull strength of the thin film material even after the most rigorous liquid state aging treatments.

7. Summary

Thin film metallization on LTCC has been developed and characterized, leading to reliable interconnections and well-characterized long term aging in soldered connections. Unique defined edge conditions have been responsible for a layer that can be defined by dry etching and does not require definition by solder stop. The structure within the layer has also been explored using FIB and SEM examination. Space optimization resulting from fine feature resolution shows promise as even conservative miniaturization parameters result in a 40% reduction of area required for surface-mounted components. Multichip modules using metal seal frames and lids are more easily made in a reliable manner using an all-thin-film approach for in-module faraday enclosures for electromagnetic isolation improvements. Ion milling is effective at producing good line/space combinations with good conductor edges. The overall system of this thin film multilayer on LTCC yields high reliability and robustness. Future efforts are envisioned to further improve these and related aspects of thin films on LTCC.

Thin film multilayers have provided a complete solution to a range of high performance circuit needs. One of the criticisms of this approach has been the cost. Particularly with a small number of post-firings it would be expected that the screen printing, drying and firing is far simpler than the PVD in a vacuum, photoresist definition, and etching – dry etching in an ion mill in our case. However, with a number of post-fired steps, each must be well-aligned to the others and to the circuit itself. In a business climate where labor is far more expensive than even raw materials and the reliability is the most important metric, the premium for thin film has more than paid for itself.

8. Acknowledgements

The authors wish to acknowledge valuable assistance from Bill Price, Jack Tippit, Jim Hickson, Mike Girardi, Gary Zender, Dave Stockdale, and many others.

The Kansas City Plant is operated and managed by Honeywell Federal Manufacturing and Technologies for the United States Department of Energy under contract No. DE-AC04-01AL66850.

Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

References

[1] J. Müller, D. Schwanke, T. Haas, E. Feurer, B. Schweizer, A. Klaassen, "Improved design options and microwave performance by combining thin film with LTCC," Workshop Proceedings WS8, 33rd European Microwave Conference, Oct. 6, 2003, Munich.

[2] J.A. Wolf and K.A. Peterson, "Thin films on LTCC for Connectivity and Conductivity," 7th International Conference and Exhibition on Ceramic Interconnect and Ceramic Microsystems Technologies (CICMT), San Diego, USA, pp. 139-145, April 5-7, 2011.