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Monolithic Smart Structures at the Nexus of Conformal Electronics and 3D Hyperintegration

IMAPS ATW and Symposium on 3D and Conformable Printed Electronic Packaging

February 23, 2012

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Outline

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  - Nanosats and hosts
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  - 3D Hyperintegration
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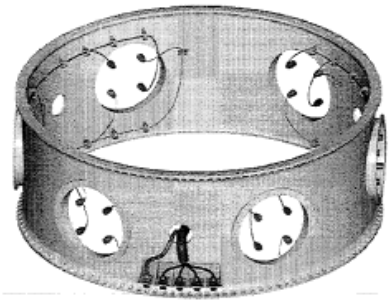
Motivation

- Recent study indicates cost per kg to low Earth orbit (LEO) averages $10k US across launch vehicle classes[1]
- Public and private enterprises seeking affordable access to space have pioneered small satellite ("nanosat") and scientific instrument payloads.
- Relatively limited functionality
- Many nanosats are secondary payloads on a host platform; facilitated by new infrastructure such as the EELV Secondary Payload Adapter (US AFRL, late 1990's)[2]

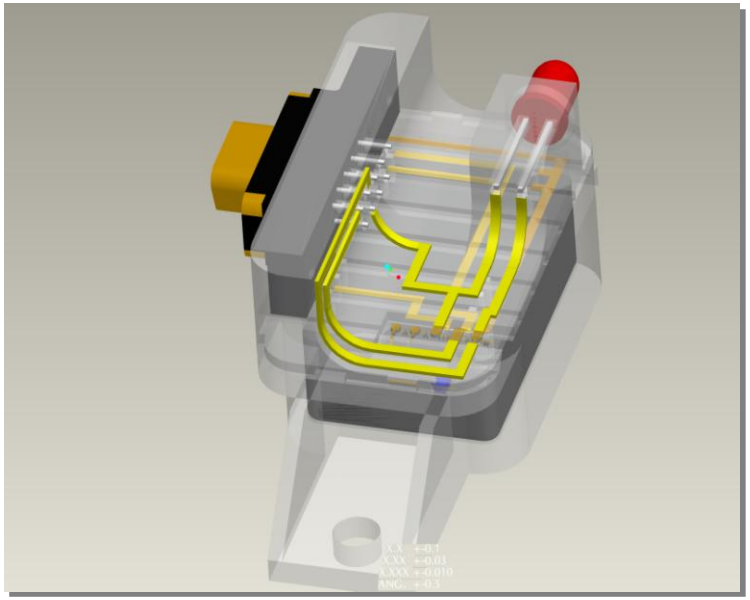


Compactness and volumetric packing efficiency of secondary payloads can be optimized to (1) fly more of them to distribute costs and (2) simplify nanosat architecture. Smart structures may offer a solution.

[1]Futron Corp., 2002.
[2]Goodwin and Wegner, AIAA, 2001.

Characteristics of a Smart Structure

- **Monolithic**
  - **Complex geometry (can't be machined) for innovative use of volume and lower mass relative to multipart assemblies**
  - **Structural, electronic, optical, and thermal management components may be encapsulated within.**
- **Incorporates multiple, functionally-graded matrix materials for engineered properties such as stiffness, resonant modes, or refractive index.**
- **Fabricated by tools that enable *bounded customization***
  - **Dimensions may be created by point cloud or coordinate data of installation space.**
  - **Fabrication process may be interrupted to incorporate design changes late in production.**



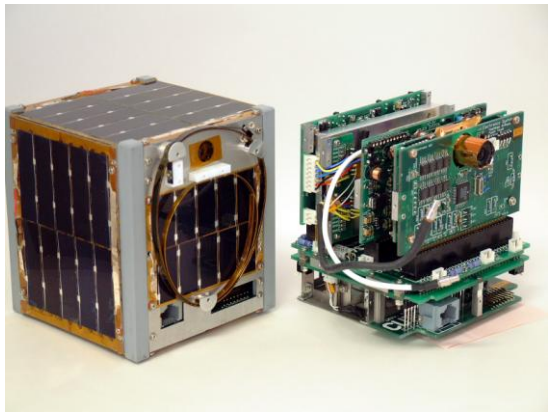
Smart structures such as these are created by the combination of layer-additive solid freeform fabrication (SFF or 3D printing), functional component encapsulation, and direct write (DW) media dispensing.

Nanosats and Host Payload Configurations

- **Nanosat: describes a small satellite less than 110 lbm**
- **CubeSat® commercial nanosat platform**
  - **Specification developed by Stanford and Cal Poly in late '90s**
  - **10 cm cube (1 L)**
  - **COTS electronics**
- **Multiple CubeSat launchers (P-PODs) are carried on a host payload**

P-POD

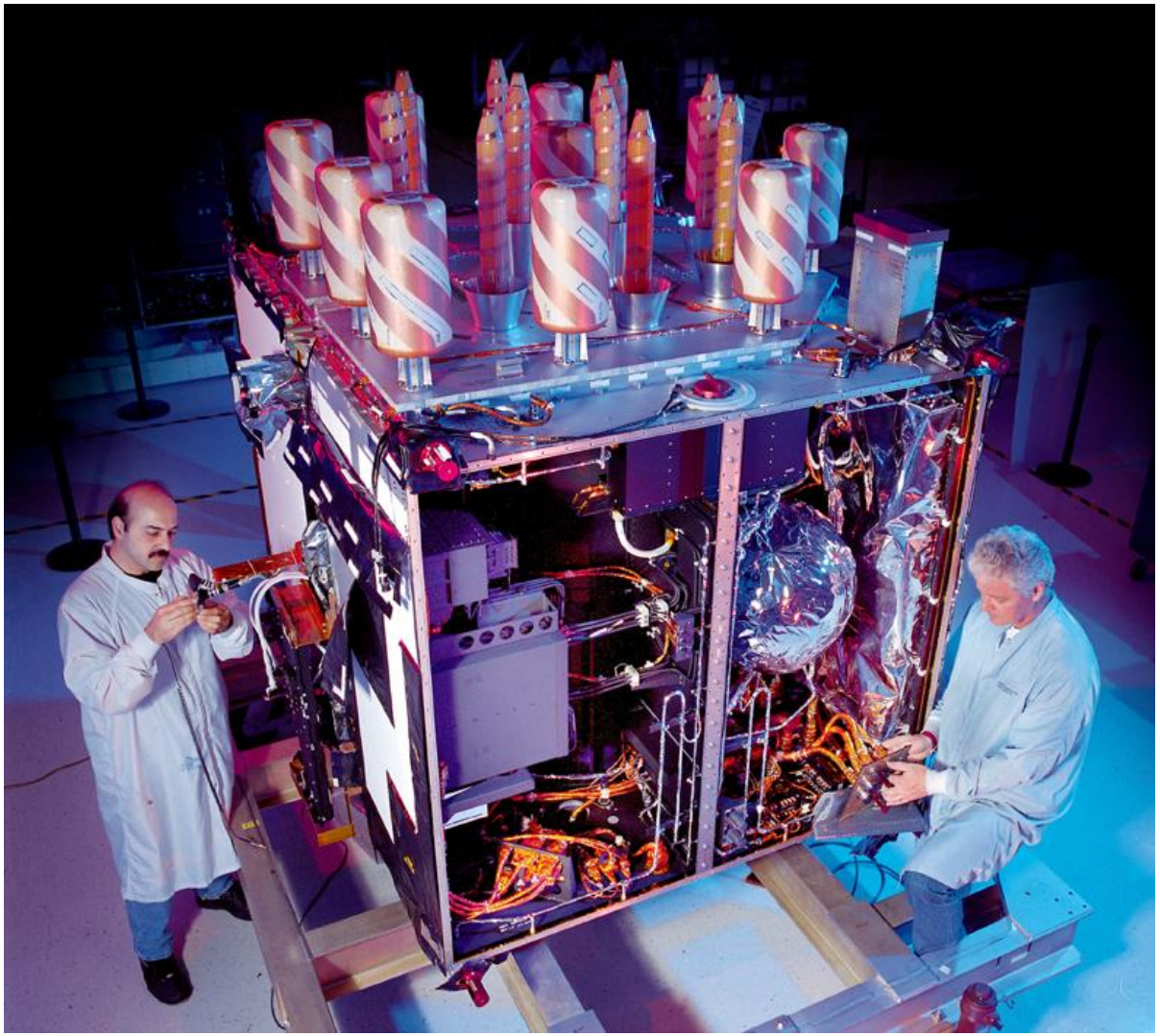
ESA ALMASat-1



References:
http://www.wired.com/geekdad/2011/12/a-rocket-for-christmas/
http://en.wikipedia.org/wiki/CubeSat

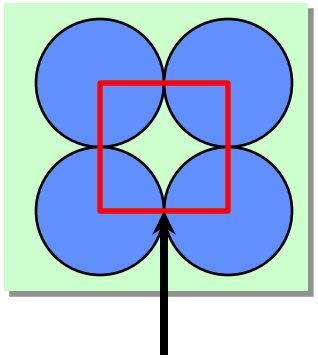
Photos:
www.cubesatkit.com
www.space.t.u-tokyo.ac.jp
www.spacedaily.com

Volumetric Packing in a Host Payload: GPS III Satellite (Lockheed Martin Corp.)



Host Payloads and Volumetric Packing Efficiency

- Ratio of the volume occupied by functional components to the enclosed volume of the system
- Simple 2D analogy: crystal unit cell packing efficiency
- High packing efficiency:
  - Mass-produced durable goods
  - Evolutionary biological systems
- Host payload volumetric packing efficiency is low because:
  - Need access for tools and human hands
  - Low-volume production with plenty of re-work



Unit cell enclosed area

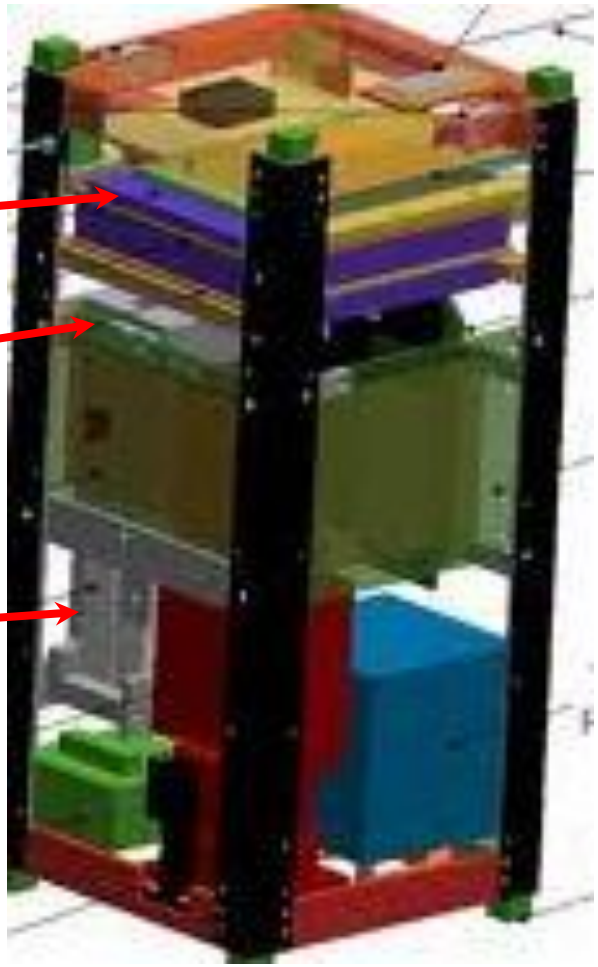
$$\eta_v = \frac{\pi r^2}{(2r)^2} = 78.54\%$$

Figure: www.jamonconj.com
Photo: www.cars.about.com

Ref: http://departments.kings.edu/chemlab/animation/packgeo.html

Space System Electronics

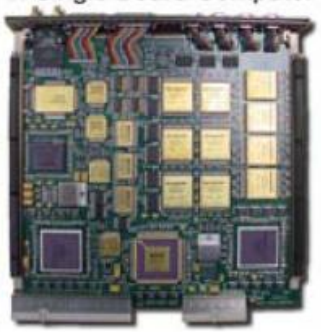
- Navigation pointing and control (NP&C)
  - Sensors (ex. star finder, sun sensor)
  - Reaction wheels/gyroscopes for slow turns (electric motors)
  - RF transceivers/transponders
- Command and data handling (C&DH)
  - Solid state memory (hundreds of ICs)
  - Flight computer/microprocessor
  - Interconnect backplane
  - DAC
  - Communications interface
- Power
  - Batteries
  - Solar arrays
  - DC-DC converters/power electronics



References:
http://mars.jpl.nasa.gov/mro/mission/spacecraft/parts/command/
http://www.jhuapl.edu/techdigest/TD/td1902/stott.pdf
http://klabs.org/DEI/Processor/PowerPC/rad750/papers/LROCDHAIAA092008.pdf
http://mars.jpl.nasa.gov/mro/mission/spacecraft/parts/gnc/controldevices/

Lunar Recon Orbiter C&DH (NASA/GSFC)

1. Single Board Computer



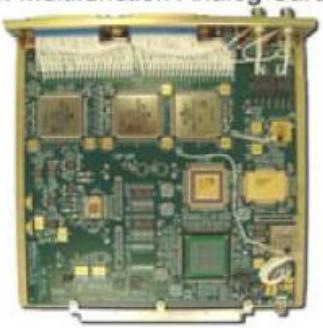
3. Low Voltage Power Converter

5. Housekeeping Input/Output Card

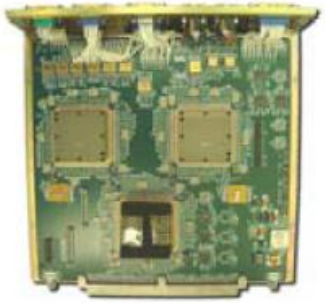
7. Ka-Band Communication Card

2. Data Storage Board

4. Multifunction Analog Card



6. S-Band Communication Card



8. Backplane

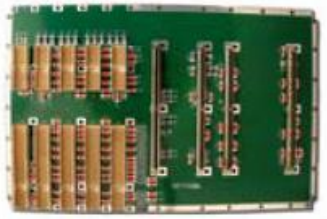
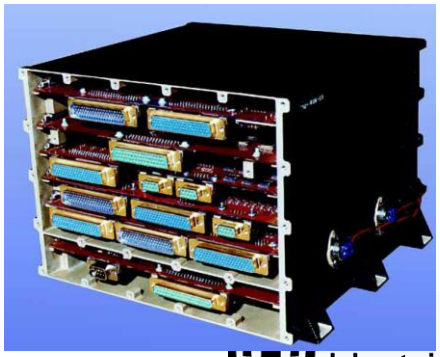


Figure 2. C&DH Sub-assemblies.

Photo: JHU APL

16 x 11.5 x 9.75 in., 46 lbm

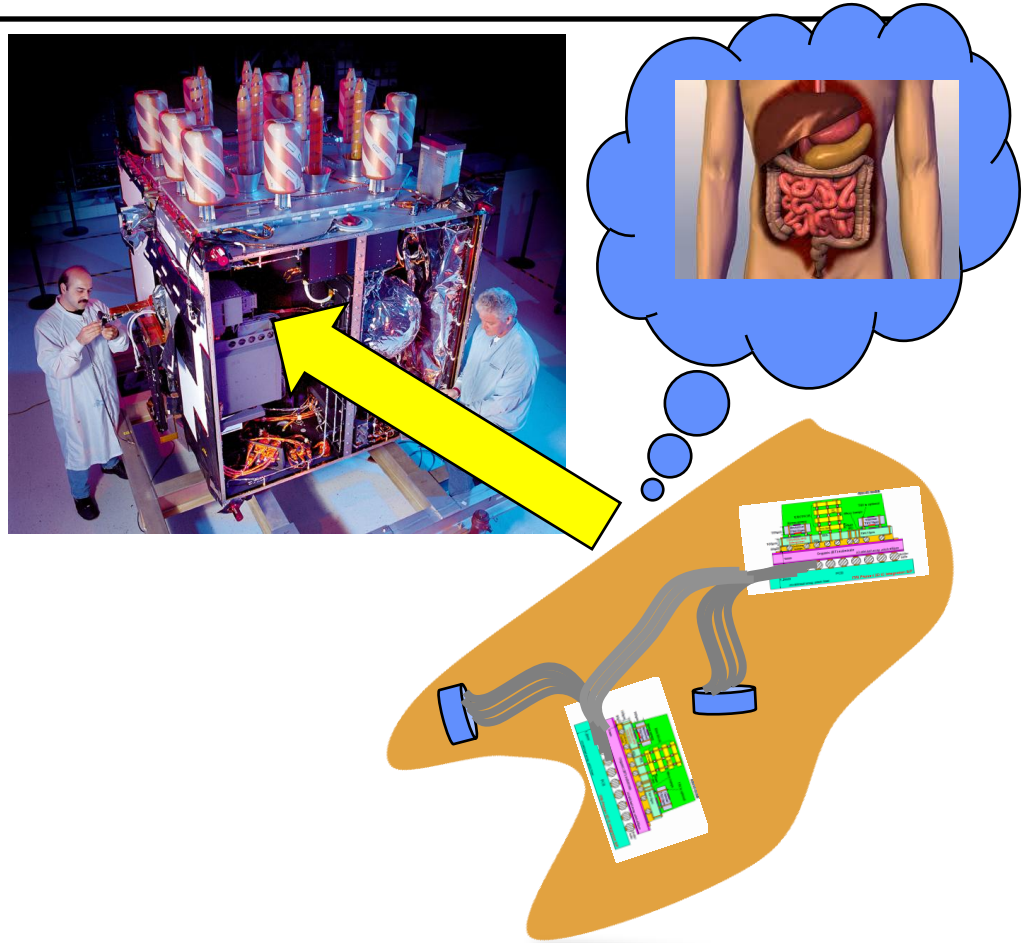


Focus is on the nanosat electronic modules; don't try to replace these in the host!

Laboratories

Value Proposition:
3D Monolithic Smart Structures

- Make nanosat electronic modules smaller by reducing packaging.
- Move modules (C&DH) to the host.
- Nanosat becomes a smaller, simple fly-by-wire system
- Boost volumetric packing efficiency
  - More secondary payloads for a given mass allotment
  - Distribute costs over a larger user group.
- Host monolithic smart structure integration process
  - Calculate or scan free volumes late in host payload integration
  - Print smart structures and snap-fit into free volumes



Conformal 3D monolithic smart structures snap directly into mapped empty volumes.

Enabling Technologies: Rapid Prototyping of High Density Circuitry (RPHDC)

- **Stereolithography (SL)**
  - **A UV laser selectively cures a photopolymer resin to print solid objects layer-by-layer**
  - **1-mil minimum layer thickness, 3-mil lateral resolution**
- **Process interrupts and functional component encapsulation**
- **Direct Write (DW) media dispensing**
  - **Automatic dispensing on 3D surfaces**
  - **~50 µm min. line width and getting smaller**
  - **Laser curing**
  - **Chemically inert with matrix material**
- **Low temperature ultrasonic consolidation of aluminum (Solidica®)**

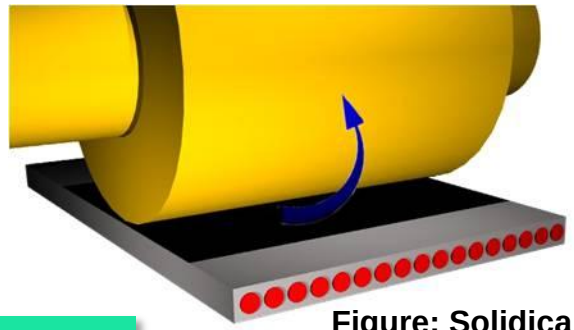


Figure: Solidica Corp.

RPHDC merges these processes to fabricate 3D monolithic smart structures.

Enabling Technologies: 3D Hyperintegration

- 3D system-in-package (SiP) features
  - Vertical stacking of thinned ASIC dice
  - Through silicon via (TSV) interconnect
- Advantages
  - More ASICs in a smaller volume
  - Shorter interconnect, less electrical parasitics and thermal resistance
- How to configure for smart structures
  - Structural matrix material serves as the encapsulation.
  - Eliminate PWAs in favor of 3D SiPs
  - Interconnect SiPs with:
    - Encapsulated mechanical sockets
    - Solderless DW interconnect directly to substrate lands
  - Optimize orientation of SiPs for
    - Maximum volumetric packing efficiency
    - High stiffness

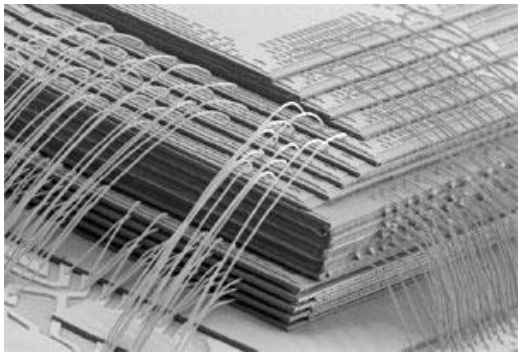


Photo: Amkor Corp.

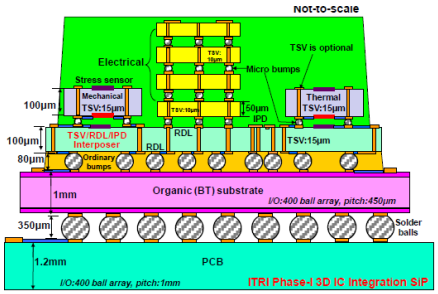


Figure: John Lau

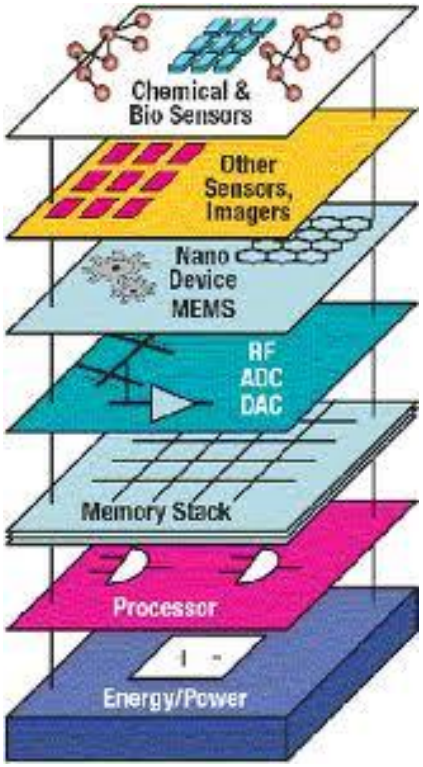


Figure: James Lu

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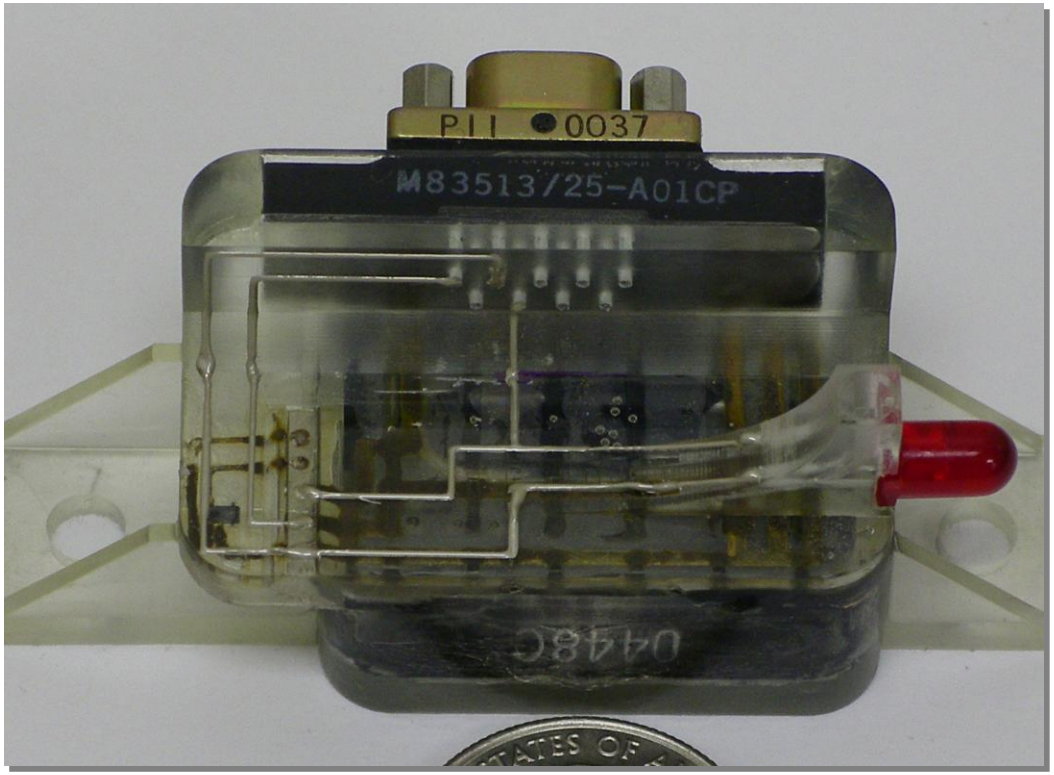
Recent Results: DC-DC Converter Smart Structure*

- **Functional**
  - **Average trace resistance: 800 mΩ/in**
  - **One inch of AWG 26 gauge braided Al wire: 200 mΩ**
  - **System drew approximately 16 mA at 28 volts (~450mW)**
- **Thermal Cycling**
  - **50 cycles of temperature varying between –40 and +85ºC under ambient atmospheric pressure**
  - **Rate: 15ºC per minute, 5 minute soak at temperature limits**
  - **LED failure noted**
  - **Delamination at interface**



*Palmer *et al.*, ASME 2005.

Functional solderless 3D DW interconnect was verified.

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Challenges

- **Technical**
  - **High SL resin viscosities lead to long settling times and long builds**
  - **Polymer outgassing (TML, CVCM targets) and degradation**
  - **Trace and contact resistance of DW interconnect**
  - **CTE mismatches**
  - **CAD tools cannot render mechanical elements and electrical networks (with circuit verification and simulation) in a common 3D space**
- **Programmatic**
  - **Space systems community manages risk by relying on proven legacy hardware**
  - **May conflict with accepted design standards (e.g. MIL-STD-1553 for serial data bus)**

Summary and Conclusions

- **Volumetric packing efficiency of secondary payloads can be optimized to reduce the cost of access to space and simplify nanosat architecture.**
- **3D monolithic smart structures are a possible solution.**
- **RPHDC and 3D Hyperintegration technology combine to create conformal smart structures that install in free volumes on the host payload.**
- **Functional solderless 3D DW interconnect within a smart structure is possible.**

Acknowledgements

- Sandia National Laboratories staff members Don Davis, Phil Gallegos, Bart Chavez, Pin Yang
- Sandia Laboratory Directed Research and Development (LDRD) Program, Project 52527
- The authors thank Dr. Ryan Wicker and Mr. Frank Medina of The University of Texas at El Paso W. M. Keck Border Biomedical Manufacturing and Engineering Laboratory using equipment purchased through Grant #11804 from the W. M. Keck Foundation. Additional UTEP support is provided through Sandia National Laboratories LDRD Research Contract #504004.
- Jeff Summers of MicroSat Systems, Inc., Littleton, Colorado
- USAFRL, Kirtland AFB, New Mexico
- Utah State University
- nScrypt, L.L.C.

Thank you!

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