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Self-Scrubber Design Methodology

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  - Providing the use of beam time to conduct experiments.

Outline

- Overview
- Block Diagram
- Xilinx Primitives
- Design Description
- Control Data Flow
- Test Setup
- Preliminary Results

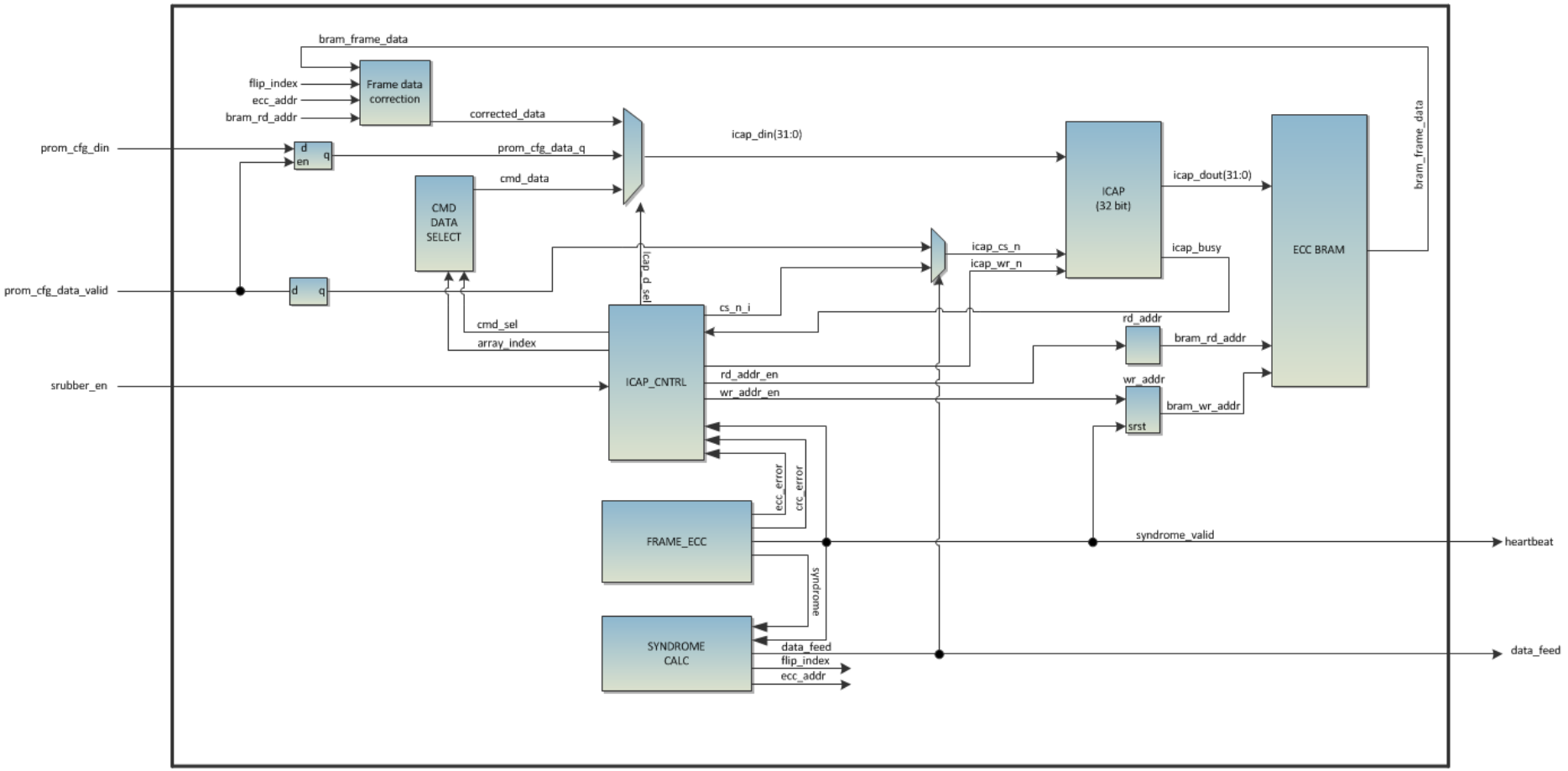
Overview

- The goal of this activity was to generate a small, lightweight IP to detect and fix SEUs within the configuration memory of the Virtex-5QV
- To reduce dependency on external devices, the scrubber logic would be implemented within the same device that was being scrubbed (hence, the name “self-scrubber”)
- Future generation architectures may load Xilinx configurations over a network, which removes the need for any local configuration memory

Overview (cont)

- The self-scrubber accesses the configuration memory of the Virtex-5 through the ICAP port
- The FRAME_ECC primitive performs continuous readback of the configuration memory, error detection for up to two bits per frame, and also provides the location of error for single bit upsets
  - Single bit errors are corrected by the self-scrubber using the error location from FRAME_ECC
  - Double-bit errors require a full scrub, currently performed by reloading the entire bitfile (without pulsing PROG)

Block Diagram



Xilinx Primitives

- FRAME_ECC_VIRTEX5
  - RDBK_CRC runs in background until error is detected
    - DESYNC command must be sent to enable RDBK_CRC
    - Writing SYNC to ICAP port stops RDBK_CRC
  - SYNDROME_VALID
    - Used as heartbeat
    - Used to register SYNDROME and ECC_ERROR
    - Enables syndrome calculation for error correction
  - SYNDROME is single error correct and double error detect (SECDEC)

Xilinx Primitives (cont)

- ICAP_VIRTEX5
  - Provides access to configuration memory
  - Used 32-bit data bus
  - Similar to SelectMAP port except input and output data buses
- ECC_BRAM
  - BRAM is soft so only used to store frame data
    - Very short storage time to limit error accumulation

Design Description

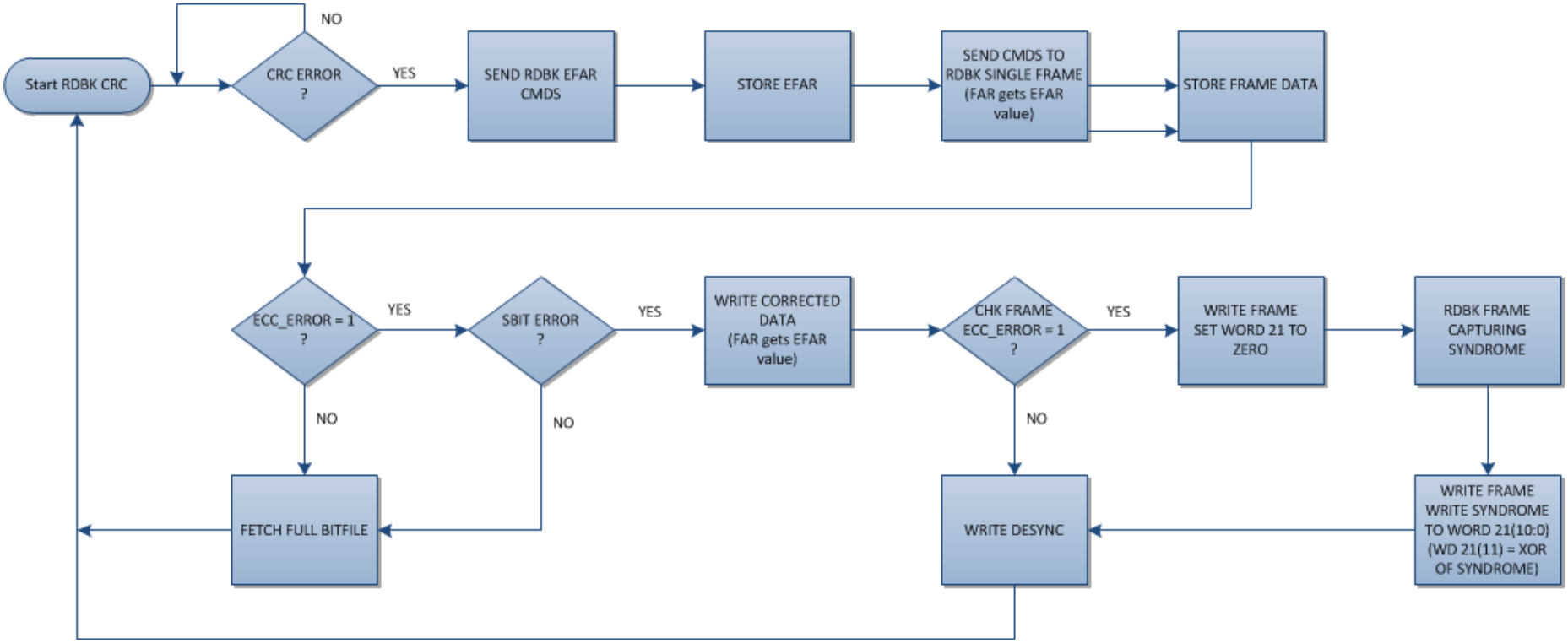
- **Frame Data Correction**
  - **Allows data to pass until bram_rd_addr equals ecc_addr and then flips bit at flip_index**
- **CMD Data Select**
  - **Configuration commands are stored as arrays of constants (not in BRAM)**
  - **ICAP CONTROL selects array and indexes through command set**
    - **Read EFAR, read frame, write frame, …**

Design Description (cont)

- SYNDROME CALCULATION
  - Enabled by ICAP CONTROL
  - On syndrome_valid:
    - Determines single- or double-bit error
    - Finds location of error within the frame

- ICAP CONTROL
  - Sits idle until readback CRC finds an error
  - Writes commands to configuration controller
  - Controls timing of ICAP port reads and writes
  - Controls reading and writing BRAM

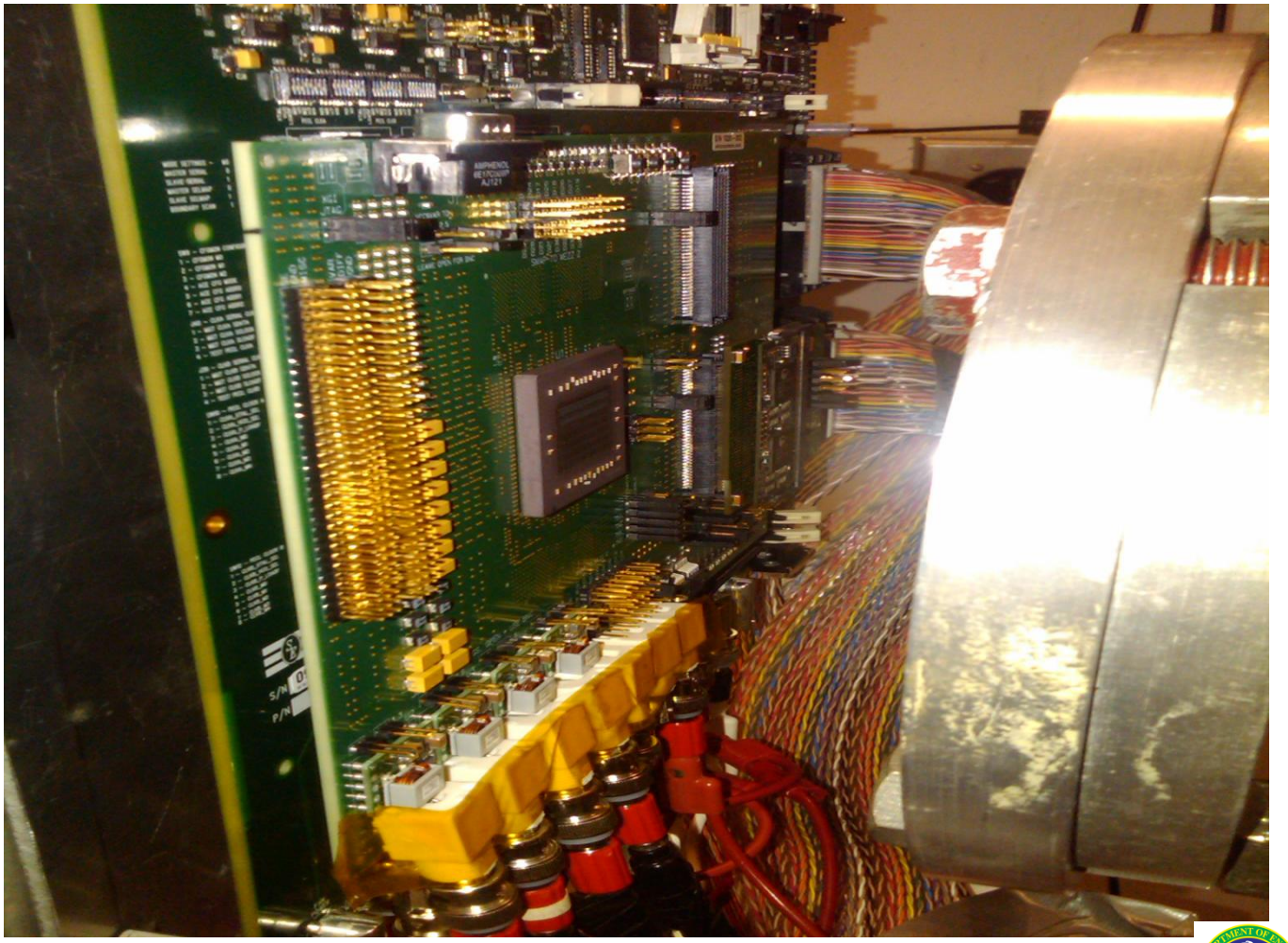
Control Flow



Resource Utilization

Logic Resource	Used	Available	%
# Slice Registers	398	81,920	0.5
# Slice LUTs	712	81,920	0.9
# BRAM	1	298	0.3

DUT Test Setup



Preliminary Test Results

- All single bit errors were corrected
  - Initial results show about 6 to 1 single bit errors to double bit errors
- The actual number of double bit errors may be lower due to double bit errors in extended block frames
  - These frames are checked but not correctable because they are not available in original bitstream
  - Thus, double-bit errors are not corrected in these frames
- Frames with more than 2 errors were counted as stuck (DRP) bits – corrected for future beam tests
  - Captured frames with 3 errors using Chipscope

Future Improvements

- Append extended block data to bitfile
  - Allows scrubbing multi-bit errors in these frames
- Add ability to fetch only a single frame to fix a frame with a multi-bit error instead of the entire bitfile