SAND2012-1420C

Development of Ultra Dense Edge Interconnects for Die to Die Connections Based on Immersion Solder Bridging

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Abstract

A high density 2-D integration process that involves linking multiple die along their edges using a linear array of solder bridges was explored. Solder bridging is a versatile approach that is compatible with a range of interconnect geometries and metallizations. We have demonstrated this approach using copper plated nodules that were fabricated on the surface of the die and extend beyond the edge of the die. These nodules were 25 microns (μm) thick with 10, 20, and 50 μm widths. The formation of solder bridges was accomplished using immersion soldering, where the entire part was dipped into a molten solder bath. Due to surface energy effects, the solder selectively wets and flows along all wettable metal surfaces to form a strong solder bond. The solder can even flow across gaps (15 microns).

Introduction

The ability to link devices along their edges with an array of interconnects opens up the possibility for new device architectures and functionalities. This 2-d integration approach presents many challenges such as edge interconnect fabrication and edge bonding. The first demonstrations of edge interconnect fabrication utilized copper "nodules", which protruded from within the die; the so-called embedded nodule approach [1-9]. Embedding the nodules requires adding a number of additional processing steps. These steps include techniques to isolate the nodules from the substrate. The integration of these embedded nodules with CMOS circuit interconnect requires further processing to add another via and metal layer for interconnects. These additional processing steps would include multiple oxide depositions, CMP (chemical mechanical polish) operations to achieve planarity, deposition of multiple metals, and photo and etch operations. Figure 1 shows the cross section of two die with embedded nodules.

In contrast our approach, utilizes surface nodules which are easier to implement. In this paper we describe the processes to form the surface nodules and to singulate without damaging these nodules. These nodules are formed by electro-plating copper metallization on top of the last dielectric layer. For integration to the CMOS circuit interconnect, the nodules are directly plated on the final metal layer. This eliminates the need for additional processing for interconnects between last metal and nodules. Finally, processes for precision alignment and die-to-die edge interconnect joining were developed. Figure 2 shows the cross section of the surface nodule between two die.

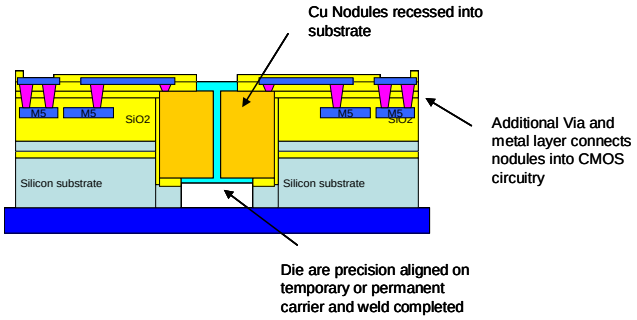


Figure 1 – Cross section of two die with embedded nodules.

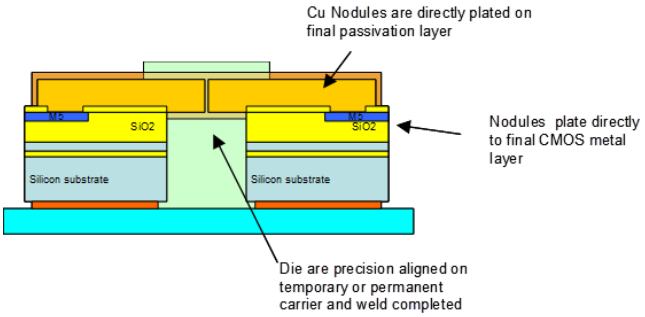


Figure 2 – Cross section of two die with surface nodules.

Nodule Formation

An initial mask set was designed to facilitate process development of surface nodules which included last metal, pad vias, nodule plate, back side Bosch etch. The size of the test chip was 10 mm x 10 mm in size. The design variation studies covers:

- Nodule formation in widths 10 μm, 20 μm, and 50 μm
- Nodule extension beyond the Bosch etch edge range from 7.5 μm to 10 μm, in 0.5 μm increments allowing nodule plate distances from none up to 5um.
- Large 500 μm corner support plates were placed in each corner as structural support for die to die placement. These were designed with 10 μm overlap of Bosch etch lines in the vertical side of the die and with no overlap of Bosch etch lines in die horizontal sides. This allowed for both nodule overlap of die edge as well as nodule recess from die etch in Bosch etch studies. Saw options include flush and recessed nodule placement.

The test vehicle chosen for development was a standard monitor grade n-type, 675 µm Si wafer upon which 8 µm of plasma enhanced tetraethylorthosilicate (PETEOS) SiO_2 was deposited on the front (to simulate a multi-level CMOS or optical device stack), and another 8 µm of PETEOS SiO_2 was deposited on the back to serve as a temporary hard mask for Bosch singulation. A hard mask was preferred for reduced sensitivity to thermal issues in singulation. The matched front/back oxide thicknesses on these test wafers minimized any stress-induced wafer curvature.

Nodule Photolithography and Plating - For integration with singulation, the first processing step used was a hard mask contact exposure. A standard 10 µm AZ9260 resist was used to pattern the 8 µm oxide mask**.**

Prior plating, a thin Ti/Cu (300 Å/ 3000 Å) seed metal layer was deposited. Just before electroplating, a short, low bias, low-temperature oxygen descum process was used to clean the surface of the exposed copper. A dense and relatively smooth Cu electroplating process was developed to form controlled-height molded nodules using a pulse plating process with relatively low current density. This resulted in a thickness non-uniformity range of approximately 10% across a 150 mm wafer. Surface nodules were formed with plated copper metallization 25 µm thick. After the surface metallization process, the processed wafer was partially scribed using a wafer sawed. Final singulation with overhanging surface metal nodules was accomplished with a Bosch etch.

The thick resist was then removed with *N*-Methyl-2-pyrrolidone (NMP) or acetone, followed by an Isopropyl Alcohol (IPA) rinse and nitrogen spin dry. The seed metal layer was removed in an acid processing tool using a two-step etch process: a Cu etch step using a Diluted Sulfuric Peroxide (DSP) chemistry and a Ti etch step using a dilute NH_4OH/ H_2O_2/ H_2O mixture (SC1) chemistry.

Die Singulation Bosch Etch and Dice - For etch singulation of test devices, the test wafer was bonded to a handle wafer using Crystalbond™ CB509 with the nodule side face-down. Low-void filling of the 25 µm nodule topography was achieved. Next, back etching on the carrier through the 675 µm test wafer with Bosch etch was accomplished without significant die shifts or buckling.

A serious limitation of this type of singulation process integration was the aspect ratio sensitivity of the etch of the 8 µm oxide stack following the formation of a 100 µm wide, 675 µm deep trench by the Bosch etch. The fraction of ions lost to ion shadowing effects at nearly 7:1 aspect makes etching through the 8 µm oxide "simulated device stack" with practical rate and selectivity to Si substrate very challenging. With re-optimization of the oxide etch process, a pure dry-etch singulation was achieved.

For the initial test vehicle wafer release, a work-around was demonstrated which involves partial sawing, centered on the previously Bosch-etched streets, approximately 525 µm deep and 750 µm wide. This has the effect of greatly reducing the effective aspect ratio and ion/neutral shadowing of the trench oxide, thus easing the Inductively Coupled Plasma Reactive Ion Etching (ICP RIE) oxide etch. The downsides of this approach were increased defect from the saw chip-out, and reduced mechanical robustness of the chip edges. Spray-on resist was employed to partially mitigate the particle problem.

Initial work showed that beyond the point of oxide etch punch-through, the Crystalbond™ CB509 was heated sufficiently by the plasma etch to soften, and individual die were found to have shifted by 10-100 µm relative to one another. Still, only a few die exhibited greater than 100 µm out-of-plane shifts. The adhesive was adequate in retaining the die through the completion of singulation. Blackening of the Crystalbond™ CB509 material in the streets was also noted. This suggested some deterioration under exposure to sustained high temperature (estimated 100-110º C) conditions, as well as plasma reactive species and ion bombardment during the over-etch. Despite the Crystalbond™ CB509 damage, a room-temperature acetone bath dissolved the adhesive and released the die within several hours. Individual die were picked out by grabbing top and bottom surfaces with tweezers, then dried in N_2, and further cleaned of residue with 5-minute dips in a NMP bath heated to 80º C, the last minute of which included ultrasonic agitation. Preliminary Energy dispersive X-ray spectroscopy (EDAX) data analysis from die nodules confirmed the predominant presence of a surface copper oxide, with only a very slight evidence of carbon contamination. Glacial acetic acid was used to brighten the Cu nodules visually.

Over 80% successful die release was realized on processed test wafers. Figure 3 depicts a test die corner. This corner includes an L-shaped 500 µm wide "mechanical" nodule for alignment and protection of the narrow "electrical" nodules.

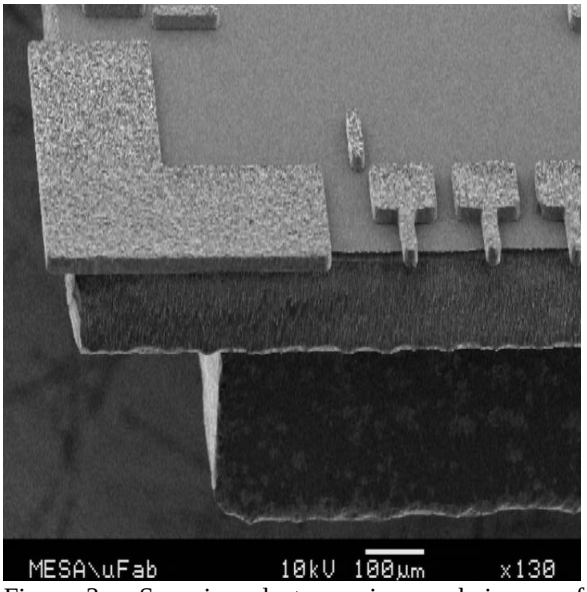


Figure 3 – Scanning electron micrograph image of the corner region of released test vehicle die using partial saw cut to enable front oxide etch.

Nodule Placement and Alignment

Precision Die Placement and Alignment- For precision die to die edge placement, a Finetech Lambda placement system with placement accuracy of +/- 1.5 μm was used. In a typical process, the die was placed face-up on the stage and picked-up by a 1 cm x 1 cm tool that was mounted to a pick-up arm and held in place by vacuum. A beam-splitting prism enables simultaneous imaging of the pick-up tool and the stage. The die-to-tool alignment was accomplished by moving the stage beneath the pick-up tool until the images were aligned. Typically, a corner of the die was aligned to a corner of the pick-up tool. Once the die was picked-up, a silicon carrier (2"x2") was placed onto the stage. The carrier was laminated with a partially-cured die attach film (Adwil LE series) that was tacky at room temperature. The carrier has Bosch-etched, T-shaped (pad and nodule) alignment features to which the die was aligned. After alignment, the die was placed onto the carrier. The second die was aligned to the first die using corner nodules as the primary alignment marks as shown in Figure 4. Figure 4 represents the alignment of two images: the backside of the die on the pick-up tool and the front side of the die on the carrier. The second die was placed onto the carrier. Typical alignment accuracy is shown in Figure 5. The nodules labeled +0 were in contact, creating a die-to-die connection. Note that this connection was achieved without the aid of tweezers.

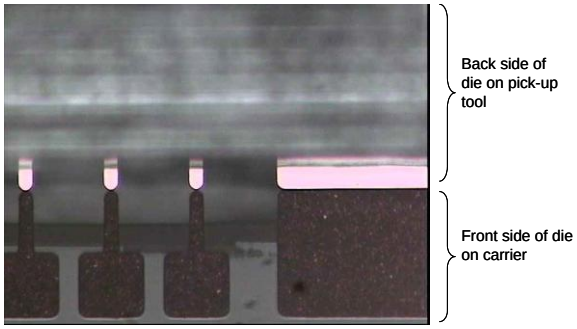


Figure 4 - Prior to die placement, the backside of the die on the pick-up tool was aligned to the front side of the die on the carrier. The overhanging nodules serve as alignment features.

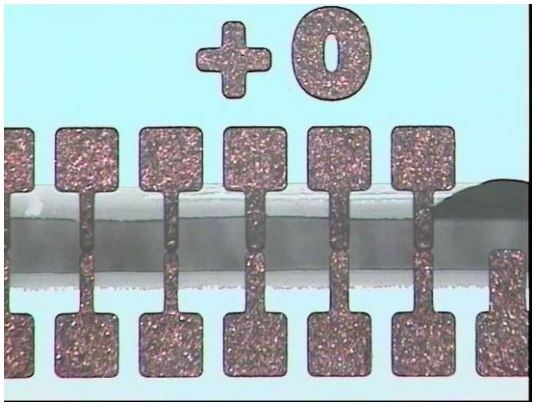


Figure 5 - This image shows a section of two die, placed close enough to achieve nodule-to-nodule contact.

After placement, the die were fixed in place with an ultraviolet (UV) curable optical adhesive. In a typical process, the UV adhesive was dispensed onto a silicon or glass carrier and the die was placed onto the adhesive. Placement accuracies of +/- 1.5 μm were consistently achieved. The adhesive around the edge of the die was UV cured (365 nm wavelength) to tack the die in place. Once all die were placed, the adhesive cure was completed in an oven at 125^{o} C for 15 minutes. Die shifting was not a problem. The measured variation in the gap between the die before and after curing was only 0.5-1 μm.

Die-to-Die Interconnect with Immersion Solder

Immersion solder **-** Immersion soldering and wave soldering are related techniques with proven manufacturability. They can be scaled up to accommodate large PC boards or wafers, or scaled down for individual components or die. Immersion soldering can be implemented into advanced packaging process flows with relative ease and at low cost, enabling more advanced integration. For example, a recent publication [10] reported the use of wafer level immersion soldering to produce thinner solder bumps (13 μm) than could be achieved using screen printing (75-125 μm). Using an immersion solder bump process, thin solder bumping could be attained at wafer level or at the die level. These results encouraged us to explore immersion soldering surface nodules interconnect.

The goal was to demonstrate and control solder bridging. Whether a solder bridge forms depends on the size and shape of the nodule interconnect, the volume of solder, how well the solder flows, and the size of the gap the solder must bridge. Different interconnect geometries were employed to explore these issues.

Test die **-** All of the experiments were performed using individual die or multiple die mounted onto silicon or glass carriers. Two types of test die were used in these experiments The first type used the surface nodule concept. These test die have electroplated copper nodules of varying widths and lengths on their surfaces. The nodules were designed to overhang the edge of the die by varying lengths after Bosch etching. The second set of die have circular (~150 μm diameter), electroless Ni-Au pads on their surfaces. These die came from wafers that were fabricated for a different project. A precision dicing process developed previously at Sandia was used for die singulation. Some wafers were diced as close as possible to the pads or through the pads.

Solder **-** The solder formulation was 60Sn-40Pb. The Sn-Pb solder block was melted in a stainless steel crucible on a hotplate. The volume of solder in the bath was ~80 cm^3. Experiments were done at solder temperatures ranging from 230-270 ^{o} C.

Immersion soldering procedure**.** **-** Die with copper nodules were cleaned in a 2M solution of H_2SO_4 in DI-H_2O for 10-15 minutes. After cleaning, the samples were rinsed in DI-H_2O then dried in air. Next, the sample was

placed onto a hot plate and pre-heated to 120° C. A water soluble flux, Kester 2331-ZX, was brushed onto the sample. After applying the flux, the sample was immersed in the solder bath for a few seconds then removed. The sample was then lightly brushed with a solution containing 10 volume % Hydrex in DI-H_2O to remove flux residues.

Results and Discussion

The goals of these experiments were to determine how the solder wets to copper surfaces; to control the thickness of the solder deposited; to form solder bridges across die, but not across adjacent features; and to optimize the immersion soldering process.

Solder wettability **-** As expected, the Sn-Pb solder had excellent wettability to electroplated copper and electroless Ni-Au surfaces, but no wettability to as-deposited aluminum. This aluminum non-wettability can be a processing advantage. For example, aluminum wire bond pads would not need to be masked for immersion soldering.

Solder thickness control **-** The effects of solder temperature and flux on the formation of solder bridges were studied using die with copper nodules. We found that the thickness of the solder deposited on the metal surfaces depended on the temperature of the bath. If the temperature was too low the solder does not properly flow from the die as it was being removed from the bath. The result was non-uniform solder deposition. The solder deposited onto the copper nodules at 200° C was non-uniform and formed bridges between adjacent pads and nodules. Increasing the temperature to at least 215° C improved the quality of the solder deposition significantly. At this temperature and at temperatures as high as 265° C the solder viscosity was optimal for the immersion process.

Solder masking materials like Kapton tape can be incorporated into the immersion soldering process to mask exposed metallization like wire bond pads. The advantages of Kapton tape for this application include excellent thermal stability at the solder bath temperatures and ease of removal. After immersion, the Kapton tape can be peeled off of the die without causing any of the metal features to delaminate and without leaving any residue.

Flux was another important parameter for solder deposition uniformity since it attacks the metal oxides that cause poor solder wetting. We have achieved good results with a high activity, neutral pH, water soluble organic flux used in wave soldering. These fluxes can leave behind dendritic flux residues if not cleaned thoroughly after soldering. These residues can be removed with heated DI-H_2O (54-66° C) or with a DI-H_2O diluted cleaning agent. In thwas work, a 10 volume % solution of Hydrex AC in DI-H_2O was found to effectively remove flux residues.

Overhanging nodules Solder bridging **-** Preliminary results were quite promising. An optical microscope image of a corner of a test die after solder immersion is shown in Figure 6. There was excellent solder coverage over all exposed metallization, and no unwanted bridging between adjacent nodules or pads. A portion of the copper was masked off with Kapton tape.

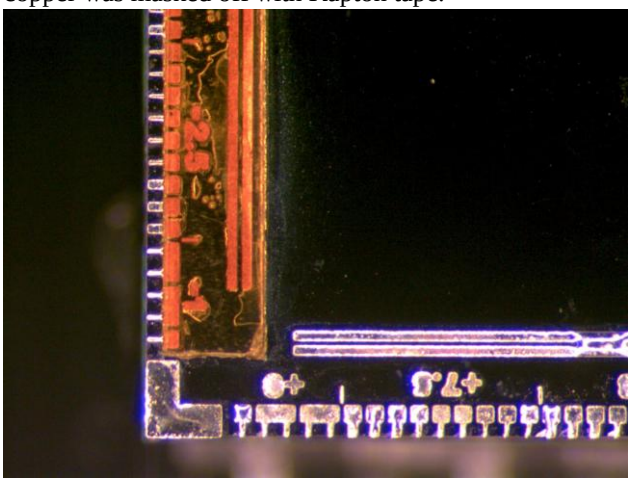
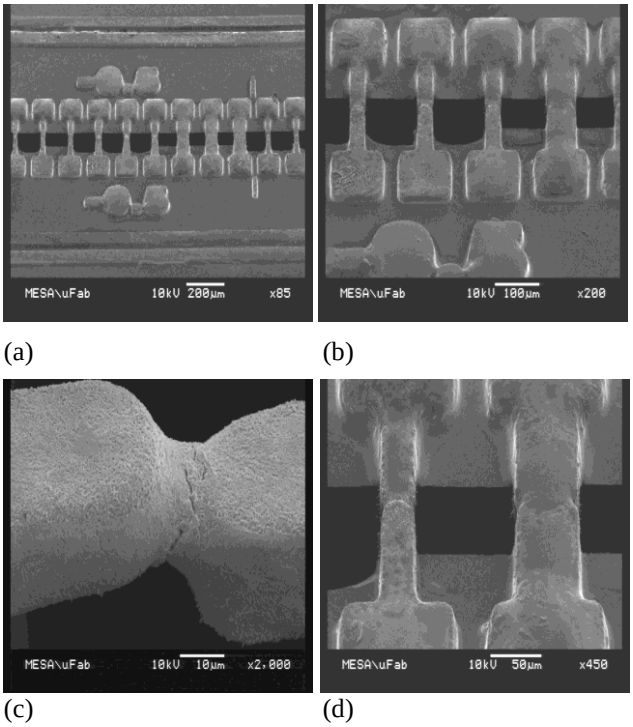


Figure 6 - Optical microscope image of a test die after immersion in Sn-Pb solder. Kapton tape was used to mask off a portion of the copper metallization.

An image of nodules overhanging the edges of two finely placed die is shown in Figure 5 after solder immersion. Nodule-to-nodule bridging was accomplished along the entire edge of each die and there was no unwanted bridging between adjacent nodules. Results like those shown in Figure 7 have been achieved consistently with immersion soldering.

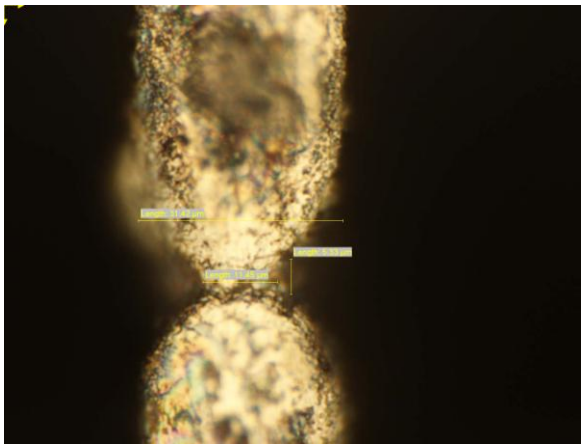


(a) (b)

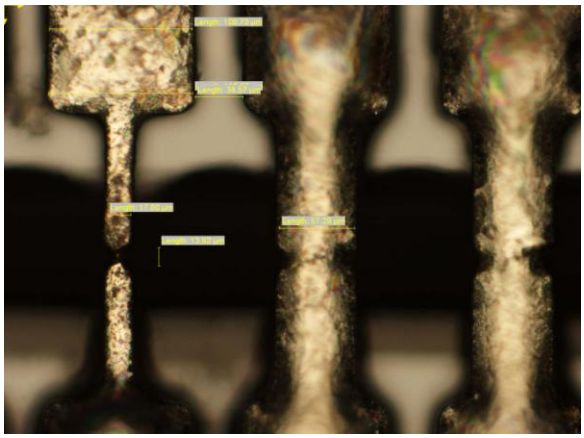
(c) (d)

Figure 7 - Scanning electron micrograph image of solder bridges that join the nodules of adjacent die to form a bridged interconnect (a). Higher magnification images of the solder bridges appear in (b) and (c). In (d), the solder can bridge nodules that have some z-axis misalignment.

The effect of nodule geometry on solder bridging is illustrated in Figure 8a – the width of the nodule is 31 μm, where it is bridging across is 5 μm (nodule-to-nodule gap), the width of the bridge is 11 μm. In Figure 8b – for the right set of nodules, the top pad width is 101 μm, the nodule width where it narrows down is 17 μm, the gap between the top and bottom nodule is 14 μm; for the middle pad, the spacing between the middle pad and the right pad at the is 36 μm, where the middle nodule bridges to the bottom middle nodule the width is 57 μm . As the nodule width decreases and the gap increases, solder bridging becomes more difficult. Higher magnification optical images with nodule and gap dimensions were shown in Figure 9a and Figure 9b.

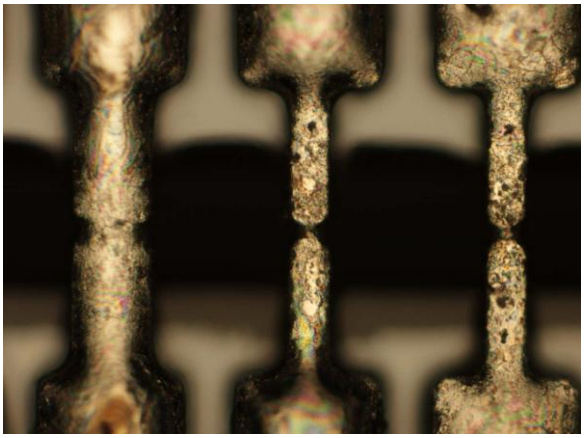


(a)

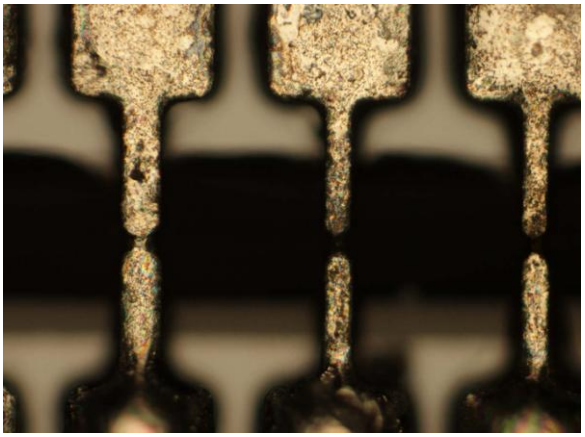


(b)

Figure 8 - Optical microscope images of nodules along the edges of two die after immersion solder. (a) As the nodule width decreases and the gap increases, solder bridging becomes more difficult. (b) At a certain gap size, the solder will not bridge thin nodules.



(a)



(b)

Figure 9 - Higher magnification optical images with nodule and gap dimensions shown. (a) The effect of nodule dimensions on solder bridging was clearly seen in this image. A gap of ~15 μm was not bridgeable when the nodules were too thin. (b) Tapered solder bridges.

Effect of geometry on solder bridging - After the experimental parameters were optimized, the combined effect of geometry and gap size on solder bridging was investigated. These experiments revealed that bridging depends more on geometry than the gap size, due to surface tension considerations. For instance, solder can bridge 50 μm gaps between circular pads, but cannot bridge 15 μm gaps between the copper nodules. Although such large gaps were not envisioned for surface interconnects packaged devices, the results were important to consider when designing edge surface interconnects. The bridging results that were obtained from these experiments guided the selection of nodule dimensions for a subsequent demonstration using actual devices. Figure 10 shows a die pair after immersion soldering. Scanning electron micrograph images of the bridges were shown in Figure 11a. Figure 11b shows a high magnification of the solder bridge.

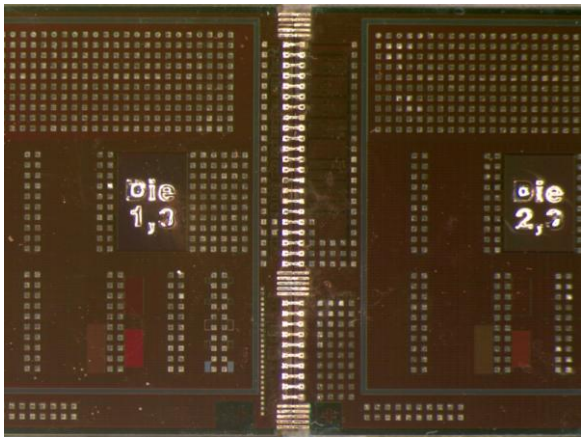
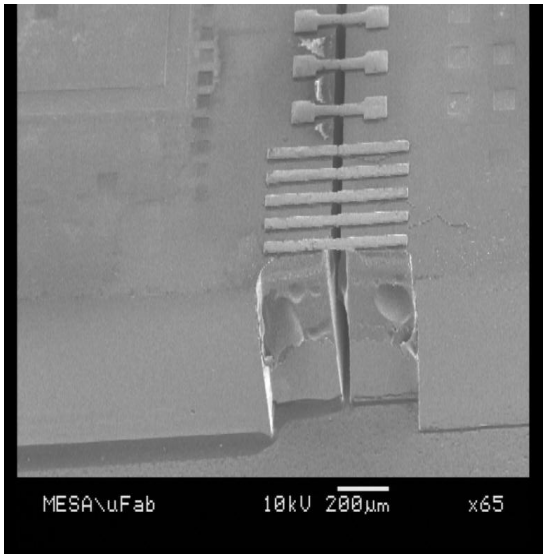
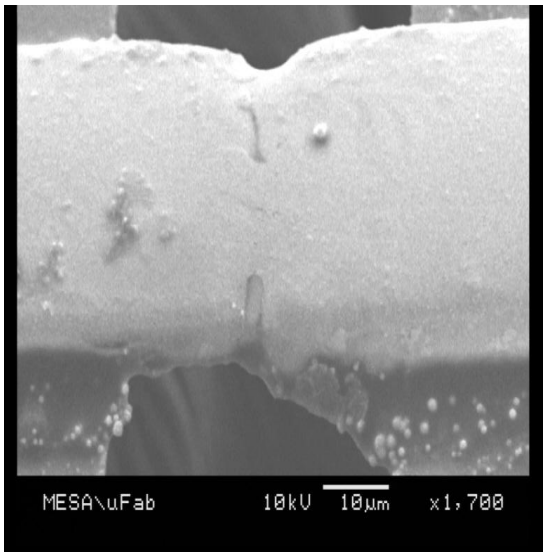


Figure 10 - Optical microscope image of two surface interconnected devices. The nodules overhanging the edge of each die were joined using immersion soldering.



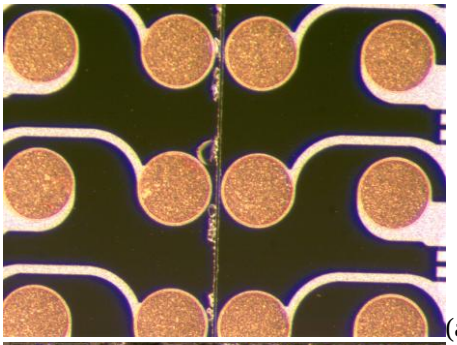
(a)



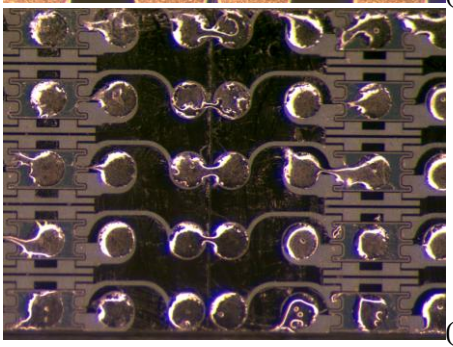
(b)

Figure 11 – (a) Scanning electron micrograph image of solder bridges between devices. (b) A single solder bridge at high magnification.

Solder bridging - Circular pads - For the circular pad bridging experiment, wafers were diced close to the die edges, but not through the pads. The die were then placed onto carriers as described previously. The pads were ~50 µm apart (see Figure 12 a & b). In a second experiment, the die from the same wafer were diced through the pads (see Fig. 12 c & d) so when the die are placed edge to edge the pads are in contact.



(a)



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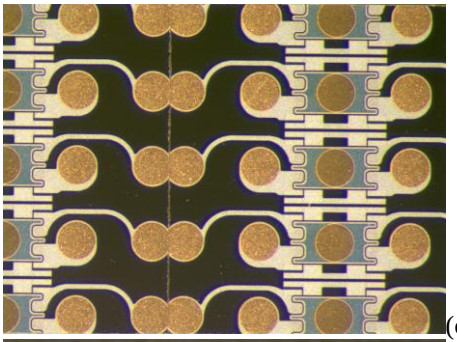

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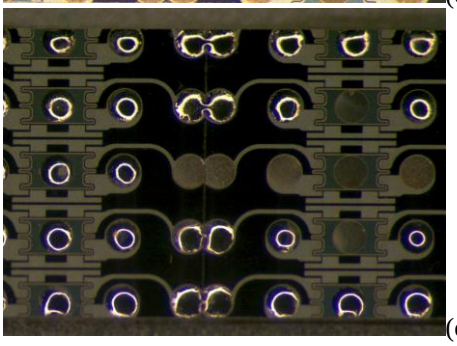
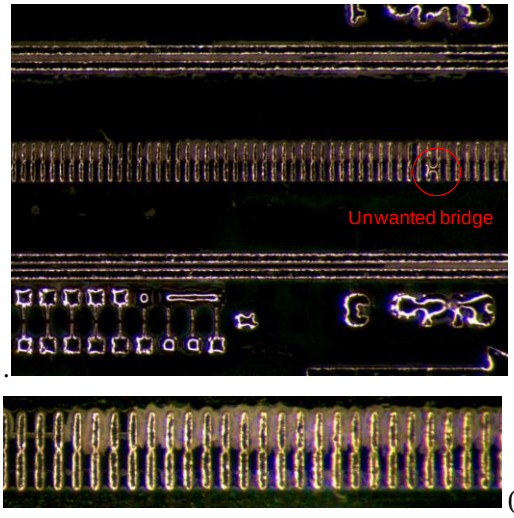


(d)

Figure 12 - Solder bridging across 50 micron gaps is possible as shown in these images of Ni-Au pads (a) before and (b) after immersion soldering. The pad diameter is: 150 µm. When the pads are placed in contact (c), solder bridging is easily accomplished (d).

High-density surface interconnects **-** Immersion soldering of high-density, 20 µm wide nodules was shown to be feasible. In Figure 13 (a), die with edges having 20 µm nodules separated by 20 µm were shown after precision placement and immersion solder bridging. The majority of interconnects were bridged, with only about 13 areas where the solder has bridged across adjacent nodules. One of these unwanted bridges is shown in the figure. The higher magnification image of the bridged nodules appears in Figure 13 (b).



(a)

(b)

Figure 13 - (a) Die pair having 20 µm wide nodules separated by 20 µm after precision placement and immersion soldering. (b) Higher magnification of soldered immersion bridge.

Experiments were also done using 10 µm nodules. Successfully bridging such small nodules proved to be more challenging, but not out of the question. Further refinement of the immersion soldering process, it may be possible to avoid the result shown in Figure 14. The solder has wet the nodules on die 1, but has bridged each nodule to its neighboring nodules. This did not occur on die 2.

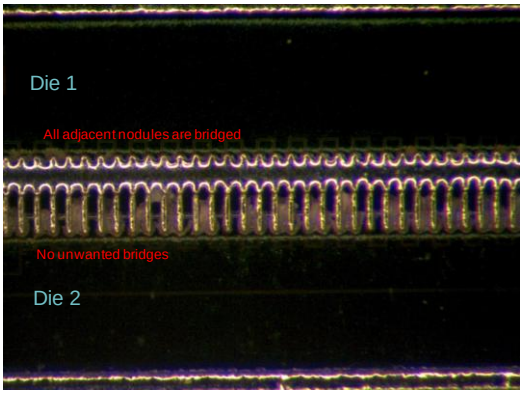


Figure 14 - Die pair having 10 µm wide nodules separated by 20 µm after precision placement and immersion soldering. Solder has bridged all of the nodules along the edge of die 1. Die 2 shows solder wetting of the nodules, but no unwanted bridging of adjacent nodules.

Conclusion

Experimental results have shown the feasibility of immersion soldering for edge surface interconnect packaging. The method was applicable to overhanging nodules. Solder bridges can be made between features that were located at the die edge, but do not overhang the edge, thus enabling simpler fabrication processes for future applications of edge surface nodule interconnect. Immersion soldering appears to be a viable technology for surface nodule interconnect and has shown to be applicable to a range of geometries and dimensions.

Among the advantages of immersion soldering was reworkability. Unwanted bridges can be repaired in most circumstances by one or two additional immersions. The scalability of immersion soldering was another advantage.

Acknowledgments

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000. We thank Arun Rodrigues, Paul Davids, Chris Derose, Rohan Kekatpure, Tony Lentine, Will Zortman. Jeff Lantz, Mike Shaw, Alex Hsia, Doug Greth, Robert Jarecki, Carlos Sanchez, Subhash Shinde, Andrew Starbuck, Robert Timon, Doug Trotter, Ralph Young, Steve Limmer, Graham Yelton, Mike Watts, Sharon Benson-Lucero, and Ken McGuire for their contributions.

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