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Fabrication of Lattice Mismatched Multijunction Photovoltaic Cells Using 3D Integration Concepts

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ABSTRACT

We present the experimental procedure to create lattice mismatched multijunction photovoltaic (PV) cells using 3D integration concepts. Lattice mismatched multijunction photovoltaic (PV) cells with decoupled electrical outputs could achieve higher efficiencies than current-matched monolithic devices. Growing lattice mismatched materials as a monolithic structure generates defects and decreases performance. We propose using methods from the integrated circuits and microsystems arena to produce the PV cell. The fabricated device consists of an ultrathin (6 μm) series connected InGaP/GaAs PV cell mechanically stacked on top of an electrically independent silicon cell. The InGaP/GaAs PV cell was processed to produce a small cell (750 μm) with back-contacts where all of the contacts sit at the same level. The dual junction and the silicon (c-Si) cell are electrically decoupled and the power from both cells is accessible through pads on the c-Si PV cell. Through this approach, we were able to fabricate a functional double junction PV cell mechanically attached to a c-Si PV cell with independent connections.

INTRODUCTION

Multijunction PV cells have proved to be the most efficient way to directly transform solar energy into electricity. Under concentration, laboratory cells have been able to reach efficiencies above 43% [1].

Historically, multijunction cells are grown monolithically one junction on top of another. Even though conventional monolithic solar cells have achieved the highest efficiency, they have to be grown in substrates with similar lattice parameters and the current that flows across the cell is restricted to the junction that generates the least current.

In multijunction PV cells, it is desired to collect photons with the highest bandgap cell possible for the specific energy of the photon. For example, high energy light should be absorbed with the high energy bandgap cell, letting the lower energy light pass through to the subsequent lower energy cells. However, current matching restricts the thicknesses of the cells by requiring some higher energy cells to pass some of the high energy photons that they would otherwise absorb to the subsequent junctions so all junctions generate equal current. This current matching requirement results in suboptimal operation of the multijunction cell.

Some thin film tandem cells have seen the advantage of decoupling. One notable example is a four terminal (micro crystalline/amorphous silicon) solar cell avoiding restrictions on current matching [2]. Other researchers have used crystalline substrates where the spectrum is split by optical means and spread into electrically decoupled cells [3,4]. Extensive simulation work has shown the advantages of doing heterogeneous integration of cells to achieve higher efficiencies when the current outputs of the different junctions are not matched [5,6]. In this article, we present the experimental procedure to create a mechanically stacked multijunction cell using 3D integration concepts.

SIMULATIONS

The individual cell IV characteristics for the c-Si, GaAs, and InGaP PV cells were calculated using the ideal balance equations [7,8]. The combined 'module' IV characteristics of series and parallel cell combinations were calculated using the appropriate circuit equations, depending on the series and parallel configurations. The product of the voltage and current at the maximum power point (MPP) point, normalized to the power of the incoming light, gave the efficiency.

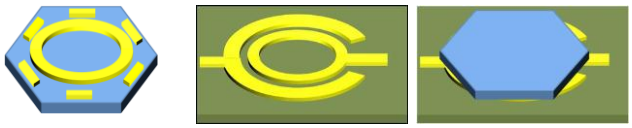
In the experimental cell structure with c-Si, GaAs, and InGaP, the c-Si cell limits the current of the other two. For 3 μm thick III-V cells and a 675 μm thick silicon cell, the sum of the individual efficiencies for the AM1.5 standard spectra at 1 sun is 44%, with the individual cells contributing 6.2%, 13.6%, and 24.2% respectively. A series connected cell with those three junctions and given thicknesses has a theoretical efficiency of 28.8%, again limited by the current in the c-Si cell (optimized thicknesses lead to 41%). However, by creating a voltage matched interconnection between the cells, near ideal efficiencies can be achieved [5,6]. Using a parallel combination of 12 series connected c-Si cells, 9 series connected GaAs cells, and 6 series connected InGaP cells yields an efficiency of 43.4%, or 98.7% of the ideal case of 44.0% when all cells are individually operated at their MPP.

FABRICATION

We have fabricated multijunction prototype cells that take advantage of techniques developed for 3D integration of integrated circuits. This approach of using tools from the microsystems and integrated circuits to create ultrathin and small solar cells is known as Microsystems Enabled

Photovoltaics [9,10]. The cells processed are small (< 1 mm in diameter) and ultrathin (< 20 µm). Our group has been able to prove 15% efficient, 14 µm thick c-Si PV [11] and ultrathin and flexible c-Si PV sheets [12], as well as back contacted GaAs PV cells [13].

The fabricated stack is composed of a series connected dual junction InGaP/GaAs PV cell and an electrically independent c-Si PV cell. Fig. 1 shows a diagram of the concept: a) illustrates an ultrathin dual junction InGaP/GaAs PV cell created through epitaxial lift-off with backside contacts and metal traces; b) illustrates the c-Si PV cell which also acts as a receiving substrate. The c-Si receiving substrate has metal traces and indium solder bumps. The III-V PV cell and the c-Si substrate are assembled together and a solder reflow is performed by heating the assembly. When the indium bumps melt, connections are formed between the InGaP/GaAs PV cells and the Si receiving substrate. In this way, all junction connections are accessible from the c-Si receiving substrate.



a) InGaP/GaAs solar cell with connections

b) Si receiving substrate with connections

c) Assembled cell with connections on the Si side

Fig. 1 Diagram showing a mechanically stacked cell.

InGaP/GaAs solar cell

The dual junction cell is an inverted cell structure grown on a GaAs wafer. The structure and layer thicknesses are represented in Fig. 2.

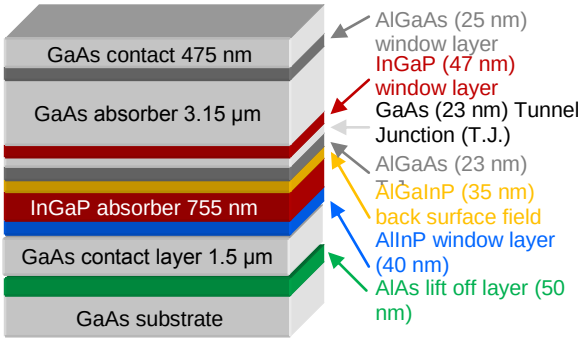


Fig. 2 Stack of materials for InGaP/GaAs PV cell.

To fabricate leveled back contacts, a series of steps were completed using standard microsystems tools. A total of five photolithography masks were used to create the patterns required for the cell. Each step uses one mask and a photolithography procedure that transfers the pattern of the mask onto photoresist.

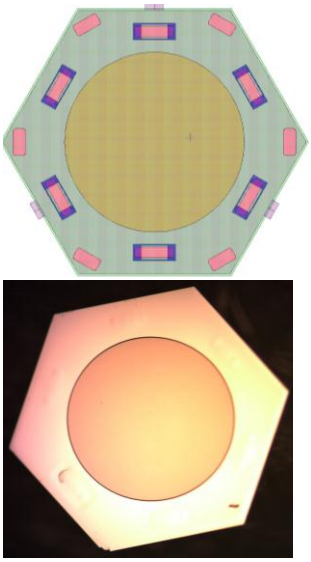
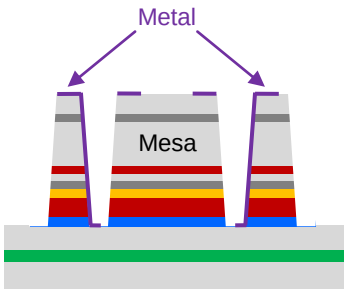


Fig. 4 is a cross section diagram showing some of the steps required for the processing.

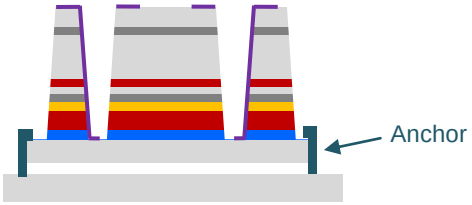
1) *Contact and mesa photolithography etch*. This step defines the contact windows and the size the mesa. The etch goes all the way to the 1.5 µm thick GaAs layer by applying a succession of selective etches of 1:4:45 H_3PO_4:H_2O_2:H_2O and 7:1 H_3PO_4:HCl.

2) *Metal Pad.* A photolithography step was used to define the size and shape of all metal pads contacting both p and n sides. Then the metal was evaporated. We used a stack of Cr/Au with thicknesses of 20 and 200 nm respectively. A lift-off method was used submerging the wafer in heated NMP for 10 min. The metal layer stayed in contact with the GaAs top layer (475 nm) and the bottom layer (1.5 µm) from Fig. 2.

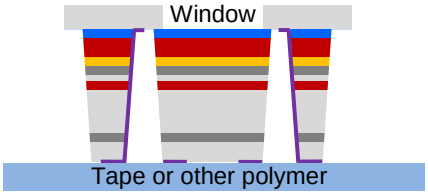
3) *Trench etch.* This step etches the 1.5 µm of GaAs to create a trench that accesses the AlAs lift-off layer for later release. Another photolithography step was used to define the pattern and a wet etch using 1:4:45 H_3PO_4:H_2O_2:H_2O was used to do this step.



Steps 1 and 2 Contact and mesa etch with metallization



Steps 3 and 4: trench etch, anchoring, and pre-release



Steps 5: Cell transfer, window etch and final release

Fig. 3 Cross section of the process flow to create the double junction back contacted PV cell.

4) *Anchor and pre-release.* Before doing lift-off, we used a PMGI structure that anchored the structure to the GaAs substrate. In this way, the cells stay in place when detached from the substrate. For this, we applied SF15 PMGI polymer on the wafer and patterned using conventional photolithography. After this step, the cells were submerged in HF in order to detach the cell from the substrate.

5) Cell transfer, window etch and final release. After etching the AlAs layer (pre-release), the cells were transferred into tape. The tape was then covered with photoresist and a window for optical access was patterned and etched into the GaAs contact layer. Finally, cells are released from the tape and put into IPA filled vials.

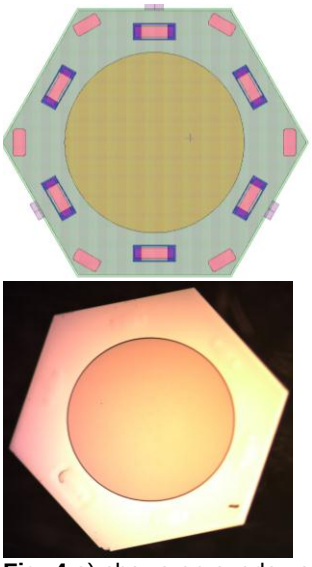


Fig. 4 a) shows an overlay of the photolithography masks. Each color describes one mask layer. Fig. 4 b) is a microscope image of the back side of a dual junction cell. The distance between the sides of the hexagon is 750 µm. Fig. 4 c) is a microscope image of the front side of the dual junction cell. The circle defining the optical access window is 504.6 µm in diameter and is 1.5 µm deep. Fig. 4 d) shows the detail on the conformal metal that runs from the bottom of the trench to the top of the mesa to level both p and n contacts.

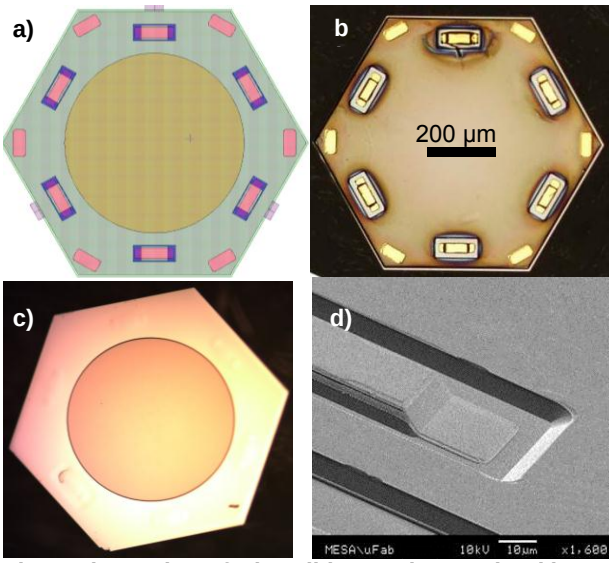


Fig. 4 a) Overlay of photolithography masks. b) Back of dual junction cell. c) Front of dual junction. d) Detail on leveled contact.

c-Si Cell Substrate

For the fabrication of the c-Si PV cell and receiving substrate, a series of 6 photolithography steps were used in the process. The process began with standard six-inch

SOI n-type, 50 um device layer, 21-28 Ω-cm silicon wafers with a 10 nm thermally grown dry oxide. The process follows these steps:

1) *P implantation.* The first mask delineates the p contact windows on a 2.2 µm thick photoresist layer. The regions are doped p with a boron implantation. The dose used was 3 $X10^{15}$ cm^{-2}, the energy was 45 keV and the wafers were tilted 7° during this step to avoid tunneling.
2) *N implantation.* The second mask delineates the n contact windows on a 2.2 µm thick photoresist layer. The regions are doped n with a phosphorus implantation. The dose used was $3X10^{15}$ cm^{-2}, the energy was 120 keV and 7° tilt on the wafer was used.
3) *Via creation.* After an activation anneal for the implantation, the oxide was stripped. This was followed by deposition of a 125 nm thick silicon nitride layer. The third mask then delineates vias that are etched in the 125 nm nitride layer and the thin oxide layer. The vias provide access to the implanted areas.
4) *Metal contacts and pads.* 200 nm of Al/Cu is deposited. The metal is patterned and etched using the fourth mask and an RIE metal etch.
5) *Alignment etch and pad exposure.* A 4 µm thick oxide layer is deposited and then patterned by the fifth mask and an RIE etch to create a guiding key for the III-V cell to fit in and access to the metal pads.
6) *Indium bump.* The last mask is used to define the location of the indium bumps which are created by electroplating.

Fig. **5** a) shows the overlay of the photolithography masks used to create the c-Si PV cell (receiving substrate) where each color describes one mask. Fig. 5b) is a microscope image of the front side of the c-Si PV cell.

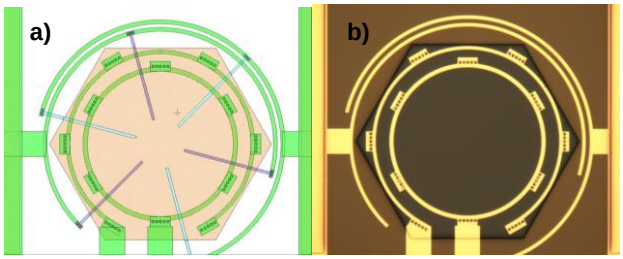
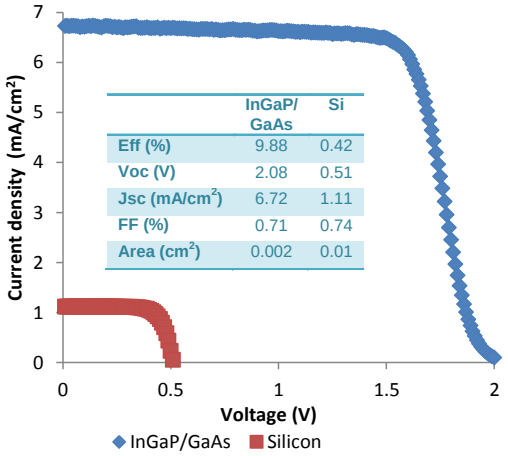


Fig. 5 a) Overlay of the photolithographical masks for c-Si substrate. b) Microscope image of the front of the c-Si PV cell.

ASSEMBLY AND TESTING

After completing both the Si substrate and the InGaP/GaAs PV cell, the III-V dual junction PV cell is placed inside of the keyed hexagonal hole in the receiving c-Si substrate. This is done by picking individual cells using vacuum tweezers. The dual junction has the back side facing the front side of the c-Si so the gold in the pads of the III-V cell can make contact with the indium bumps on the receiving substrate. Once both cells are aligned under the microscope, the stack is placed on a hot plate at 180°C for 10 min while a probe exerts force to push the stack together. After cooling, the bond between the back contacts of the InGaP PV cell and the indium bumps provides independent electrical connections between the III-V PV cell and the c-Si PV cell as well as mechanical attachment.

A Spectrolab model XT-10 class AAA solar simulator with a 1 kW, short arc, xenon lamp was used for testing. The spectrum was normalized to 1000 W/m^2 using a c-Si reference cell for both measurements. The pads were then contacted by probes using the 4 wire method (force-sense) to reduce the effects of the resistance of the cables and connectors to do one sun calibrated measurements. The test was done at 25°C. Fig. 6 shows the current density curve vs. voltage curve for both cells when the stack is complete.



	InGaP/ GaAs	Si
Eff (%)	9.88	0.42
Voc (V)	2.08	0.51
Jsc (mA/cm²)	6.72	1.11
FF (%)	0.71	0.74
Area (cm²)	0.002	0.01

Fig. 6 J-V curve of both stacked cells.

CONCLUSIONS

We showed the experimental procedure to create a mechanically stacked multijunction PV cell composed of a dual junction InGaP/GaAs PV cell and a c-Si substrate/cell. The InGaP/GaAs PV cell received a unique processing that allowed for an all leveled back contacted PV cell. The dual junction was small (750 µm) and ultrathin (6 µm). The electrical output of the dual junction cell was interconnected with metal traces on the c-Si receiving substrate through indium solder bumps to transfer the power of the dual junction onto pads in the c-Si PV cell. The simulation worked showed the benefits of

releasing the constraints of lattice matching and current matching to optimally absorb the solar spectrum.

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