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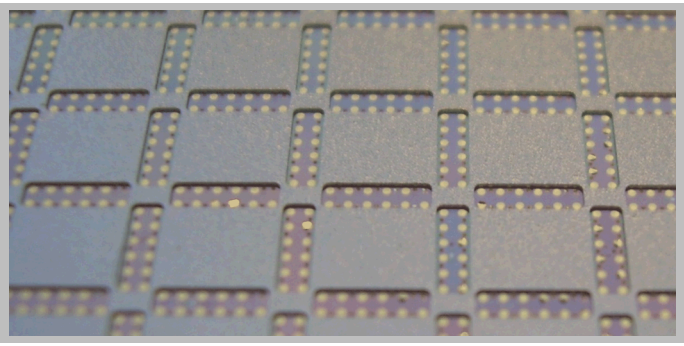

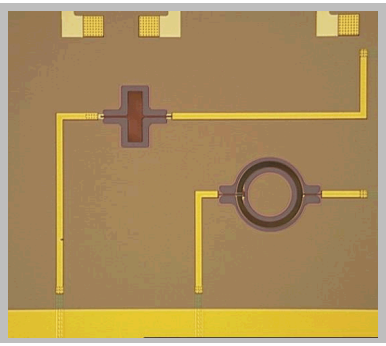

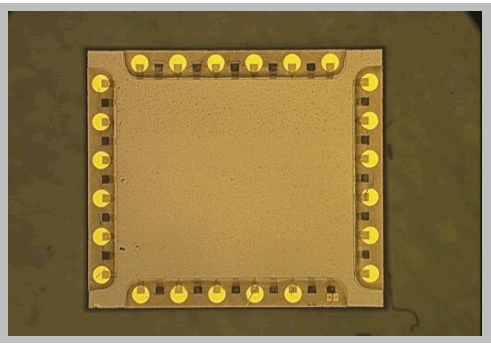

Hermetic Wafer-Level Packaging for RF MEMs: Effects on Resonator Performance

M. David Henry, , K. Douglas Greth, Janet Nguyen, Christopher D. Nordquist, Randy Shul, Mike Wiwi, Thomas A. Plut, Travis Young and Roy H. Olsson III

U.S. DEPARTMENT OF ENERGY | NNSA

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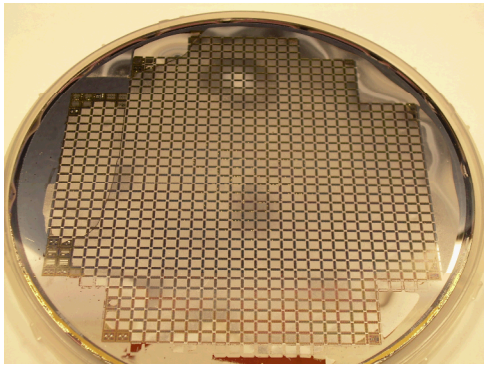
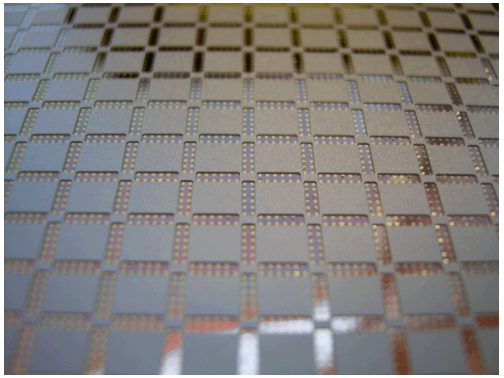
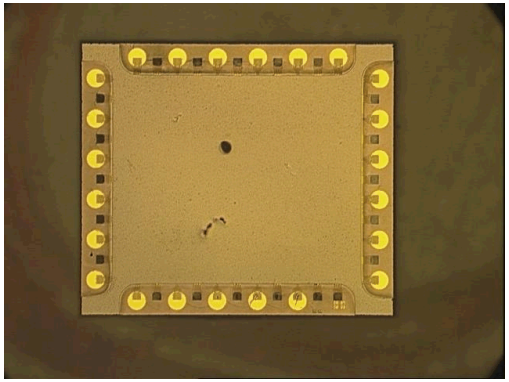
Overview

- WLP Integration of AlN Micro Resonators
- Eutectic Bonding Problems Encountered
- Lid Wafer Back Etch
- Hermetic Cavity Testing







Wafer-Level Packaging

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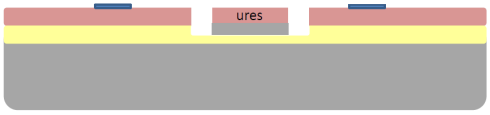
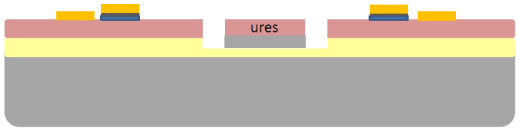
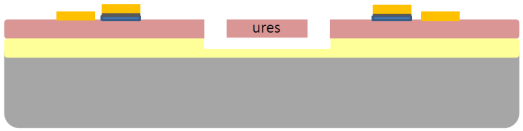
Die Wafer from CMOS foundry



Au pad / bond ring patterning



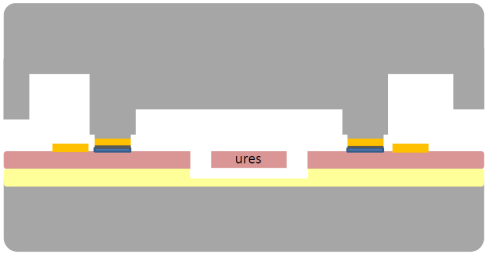
XeF2 release of suspended resonators



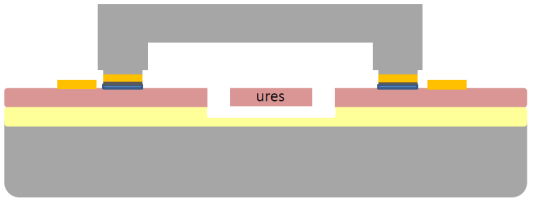
Advantage of WLP : Release of resonators on a wafer scale, hermetic encapsulation on a wafer scale, inexpensive lid technology (silicon) .
WLP is essential for achieving small form-factor and cost reduction for MEMs devices.

Lid Wafer from CMOS foundry

Au-aSi Eutectic Bond



Lid Back Etch



Eutectic Bonding – Au-Ge Bonding

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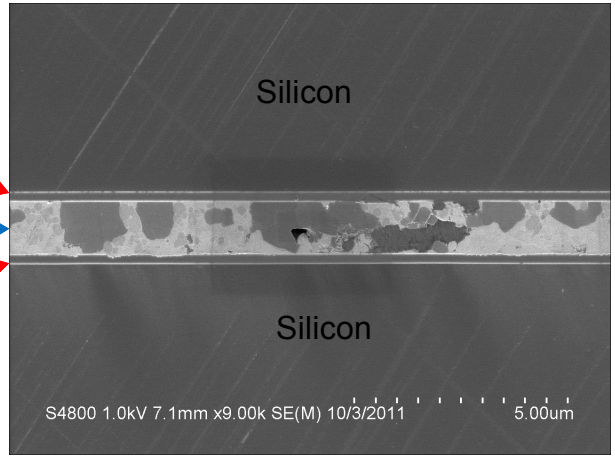
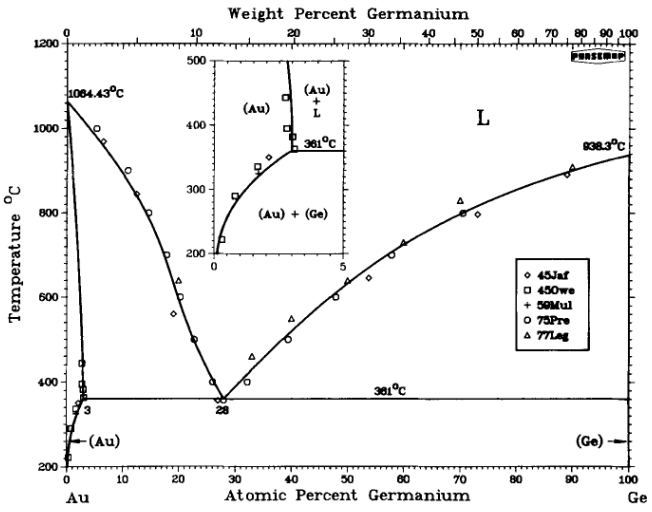
Problems encountered using Au-Ge bond

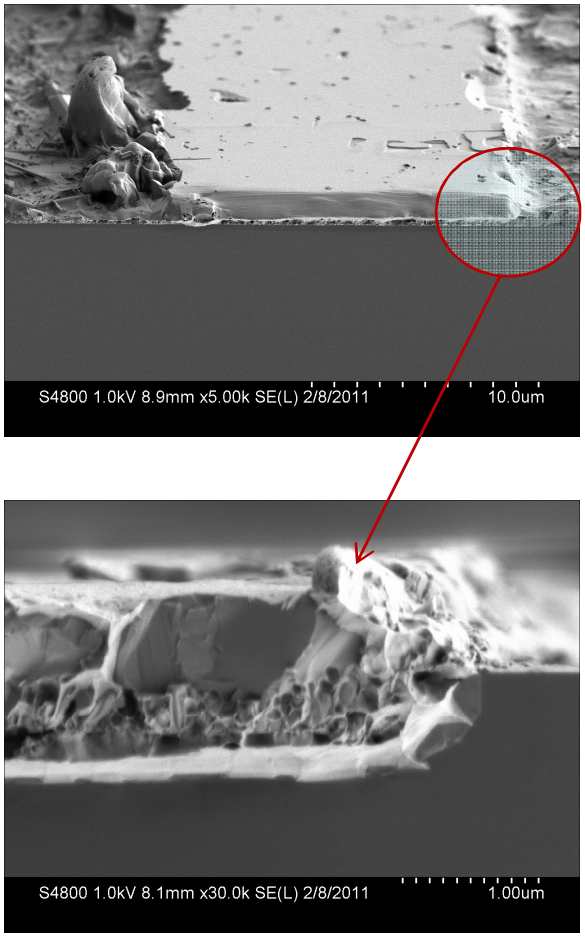
- Pt used as a barrier for the eutectic – Si can migrate through during the elevated bond temperatures
- Au-Ge eutectics required longer bonding times than Au-aSi.



For this bond, the temperature was 400 C and 40 minutes. Although the eutectic chemistry was optimized, precipitates still formed.



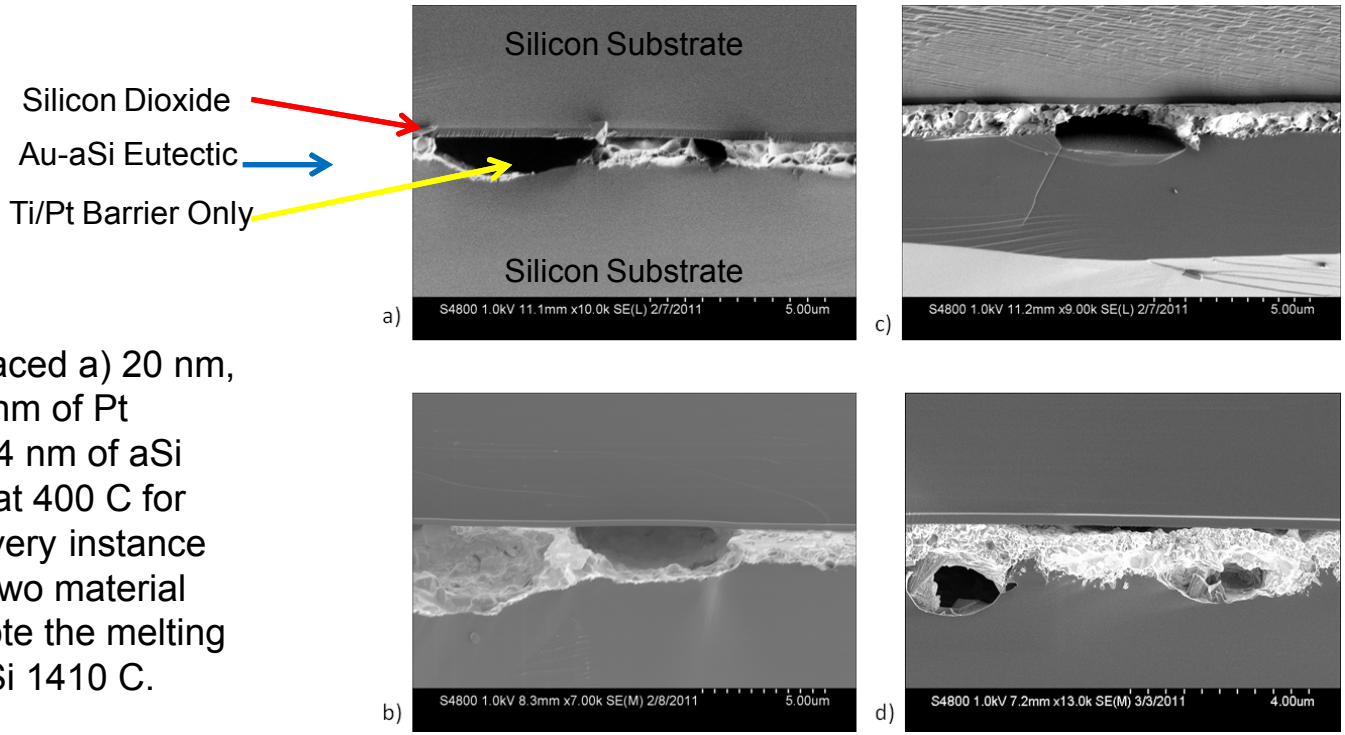
H. Okamoto and T.B. Massalski, 1984.



Failed Ge-Au eutectic bond for a microresonator package. Eutectic sequestered Si from the substrate.

Eutectic Bonding – Pt Barrier

Pt prevents Au from diffusing into the silicon substrate. However, Si substrate is free to diffuse into the Pt at lower temperatures, making a Pt silicide. During bonding the Si then forms a eutectic leaving voids in the Si substrate.

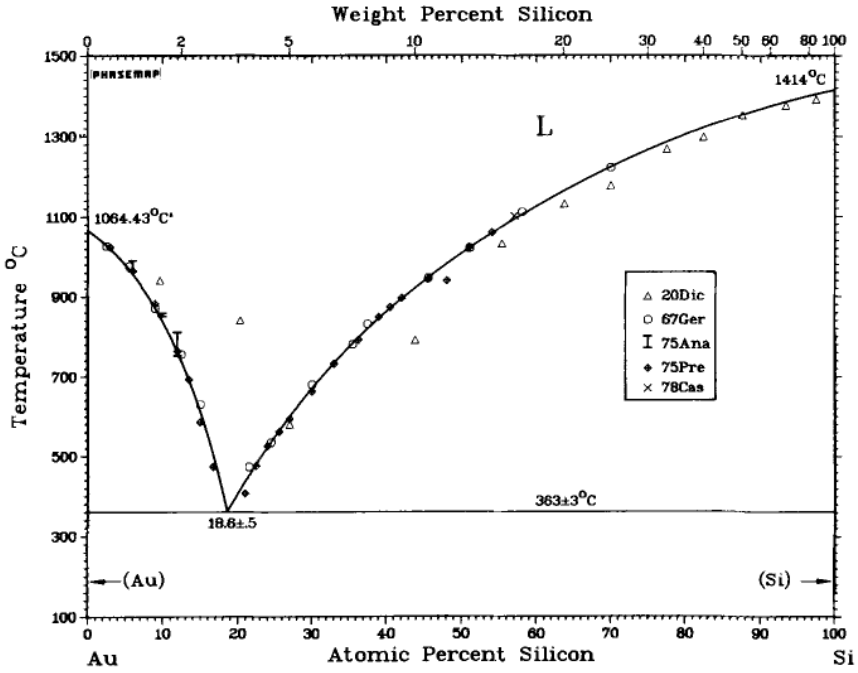


To test the effect of Pt, we placed a) 20 nm, b) 50 nm, c) 100 nm, d) 200 nm of Pt between 200 nm of Au and 64 nm of aSi and then bonded the wafers at 400 C for 30 min at 2 kN of force. In every instance the Pt failed to separate the two material and eutectic was formed. Note the melting temp of Au is ~ 1060 C and Si 1410 C.

Henry et al., *Platinum diffusion barrier breakdown in a-Si/Au eutectic wafer bonding*, In Submission, 2012.

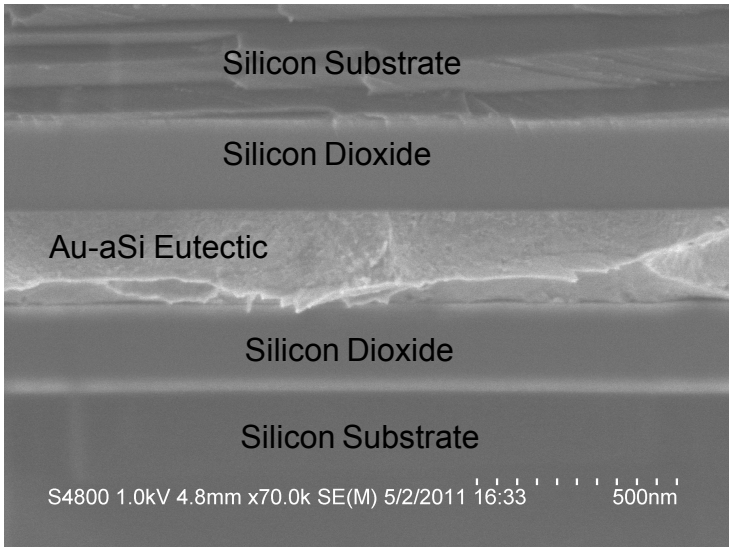
Eutectic Bonding – Au-aSi Bonding

The process described here utilized 136 nm of a-Si with 500 nm of Au to achieve the correct stoichiometry at ~19% at. Si. The bond is made at 400 C for 25 minutes, after 25 minutes at 125 C, to ensure complete reaction through the layers.

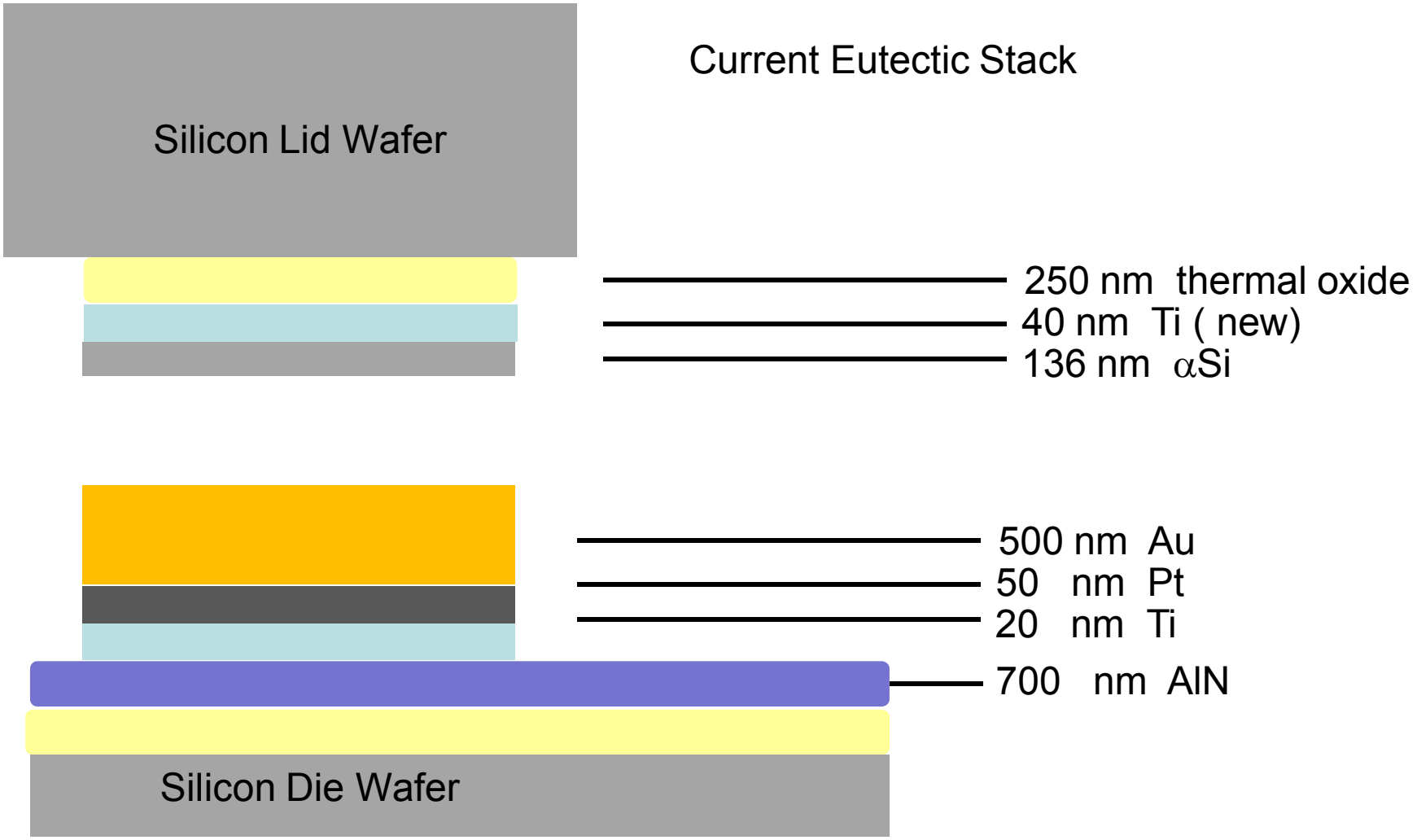


H. Okamoto and T. B. Massalski, 1983.

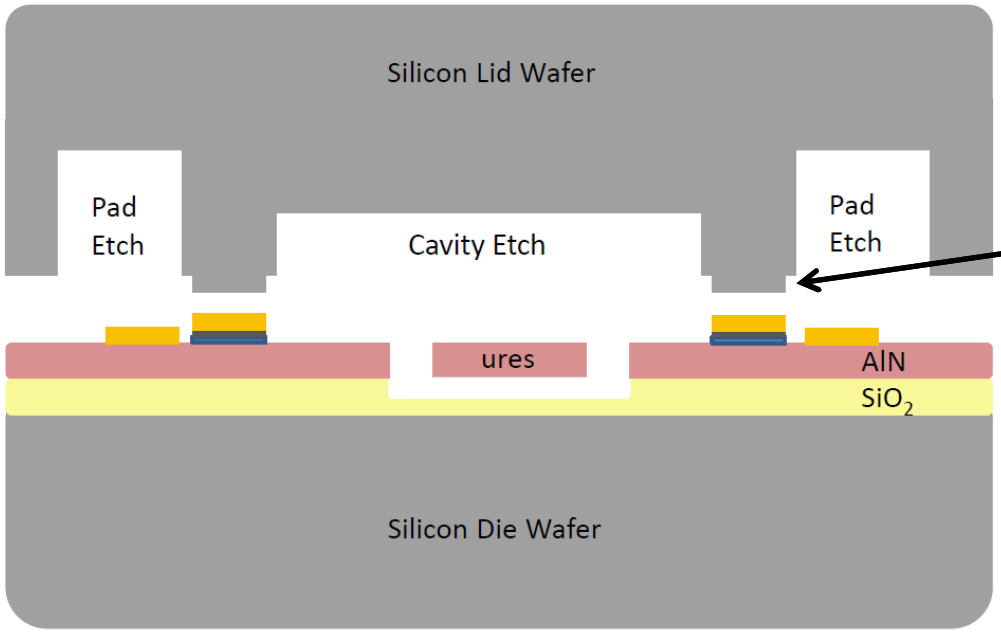
To prevent the substrate from being sequestered, 250 nm of SiO_2 was used on the Lid and 750 nm of AlN was used on the Die. Below is a SEM of Au-aSi (200 nm/ 64 nm) eutectic confined between oxide layers.



Eutectic Bonding – Au-aSi Bonding



Lid Wafer Back-Etch

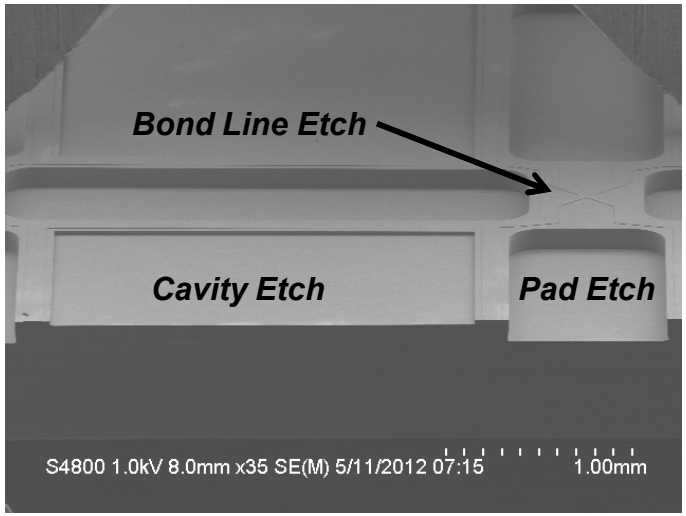


Final cross-section.

Bond line etch	1-3 um
Pad etch	100 um
Cavity etch	20 um
Lid back etch	550 um

Lid Wafer Back-Etch

Once the lid wafer is bonded to the die wafer, we then back etch the lid wafer to create the silicon cap for the resonator. Prior to etches, a thermal oxide is grown to 250 nm and 136 nm of aSi is deposited.

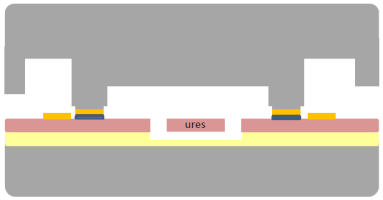


a) Bond Line Etch
1-3 um

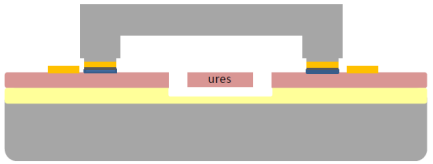
b) Pad Etch
100 um

c) Cavity Etch
20 um

d) Au-aSi bond



e) Lid-Back Etch
~550 um



Lid Wafer Back-Etch

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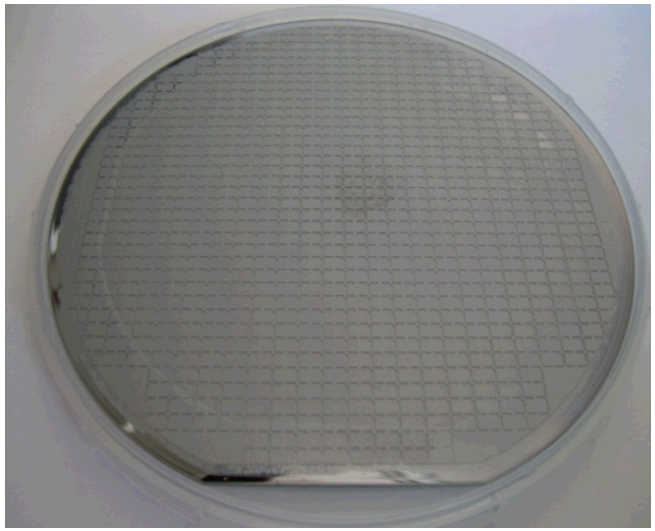
Uniformity of the back etch- Die loss at edge of wafer due to over etching of lids

- Cannot be explained by plasma non-uniformity : *Assume a 10% edge heavy uniform etch -> front side etch of 120 um and back side etch of 550 um : 67 um deeper on the edge than center.*
- Hypothesis: Due to increase in silicon loading of etch when punching into pad etch

Silicon loading experiment

- Plasma bonded wafer to produce Si-Si wafer stack so silicon load does not change during punch through
- Bonding conditions: 1min HF 100:1 clean / DI
  10 min SC-1 clean / DI / SRD
  3 min O2 plasma activation and bond
  Bond 200 C for 4 hours and 2 kN
- Result: lid heights 95=+/-5 um after back etch
  Substrate etch 54 +/- 9 um



Importance: even if the plasma uniformly etches, a silicon loading effect will be persistent problem for yield.

Lid Wafer Back-Etch

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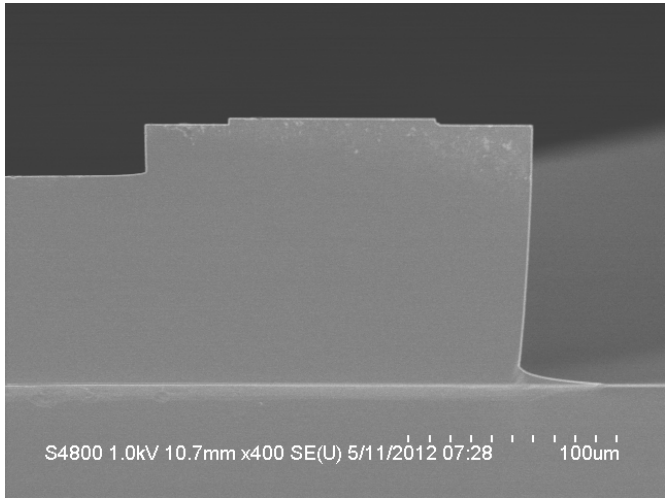
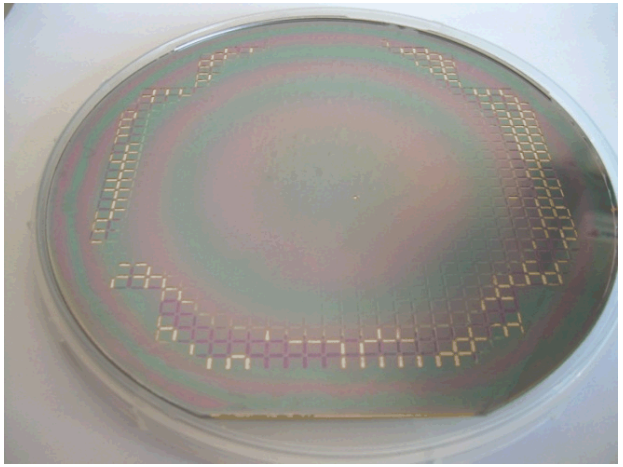
Uniformity of the back etch : Potential Solutions

- Lid back etch uniformity variation using oxide ring to slow the etch on the edges
  - Problem is tuning the amount of oxide needed takes effort

- Lid back etch landing on BOX of SOI
  - Problem is BOX stress can crack lid wafer during etch back





Lid Wafer Back-Etch

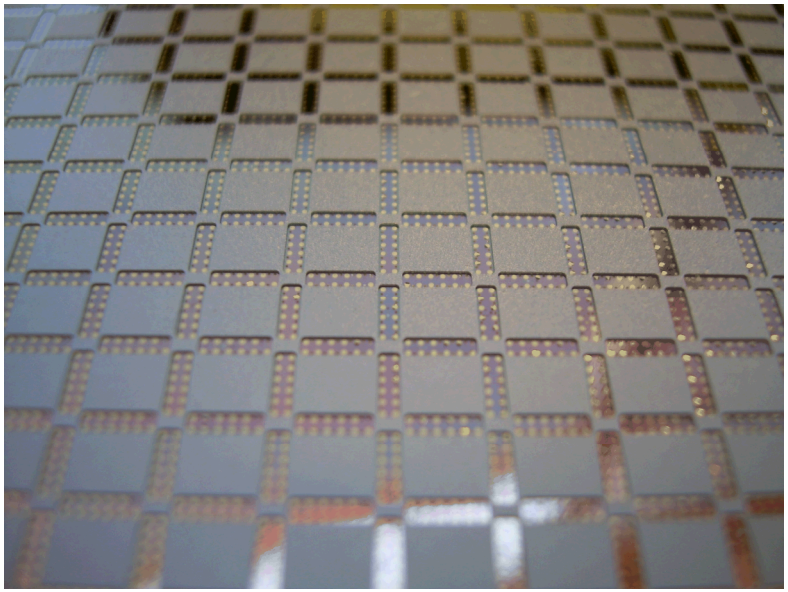
Sandia National Laboratories

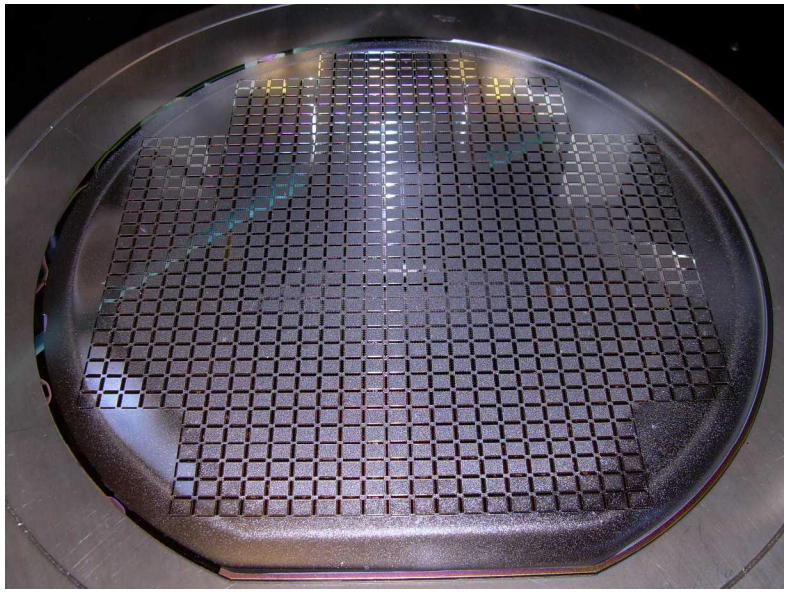
Uniformity of the back etch :

Current Method

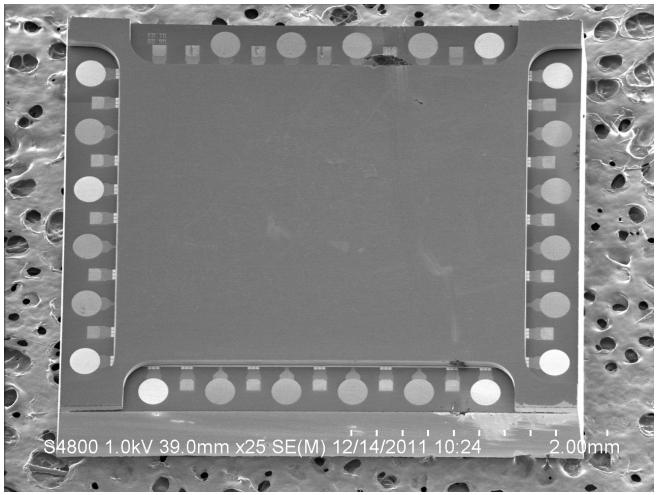
- Modification of the Lid sequence (etch bond line, pad, cavity then grow oxide and deposit aSi layer). The etch was tuned for SF_6 only and higher pressure for the lid-back etch. Etch uniformity improved as well as selectivity to oxide.

Lid Wafer Back-Etch



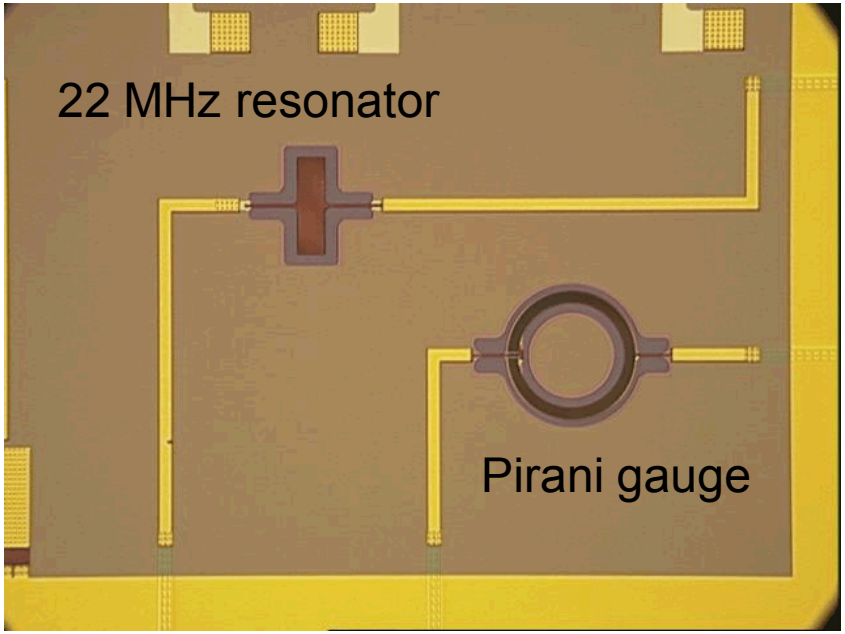


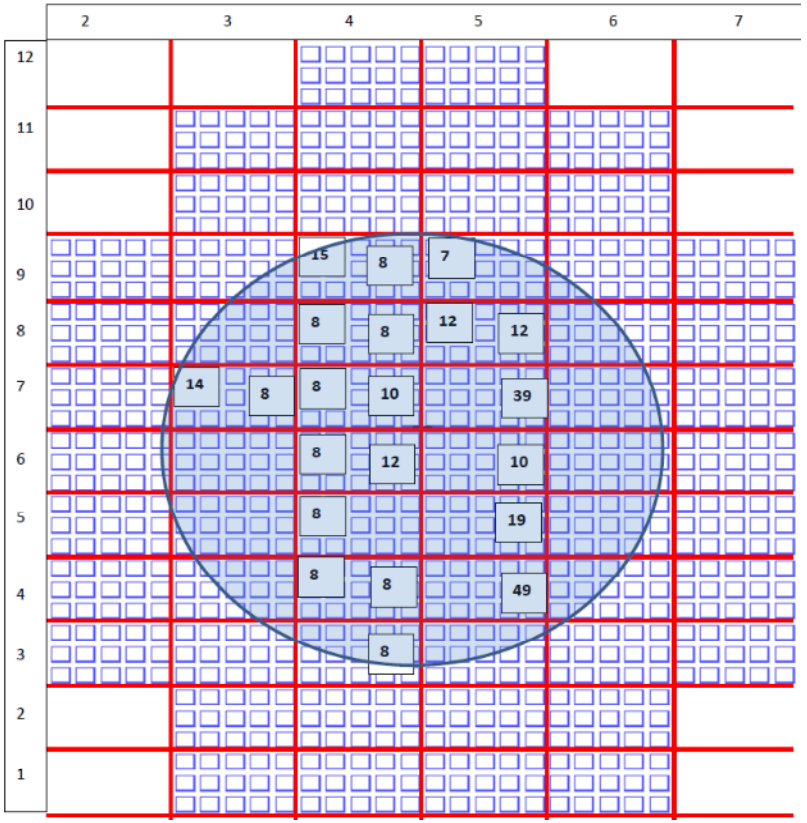
Final product wafer and die.



Hermetic Cavity Testing

Measurement of pirani gauges and 22 MHz resonator:



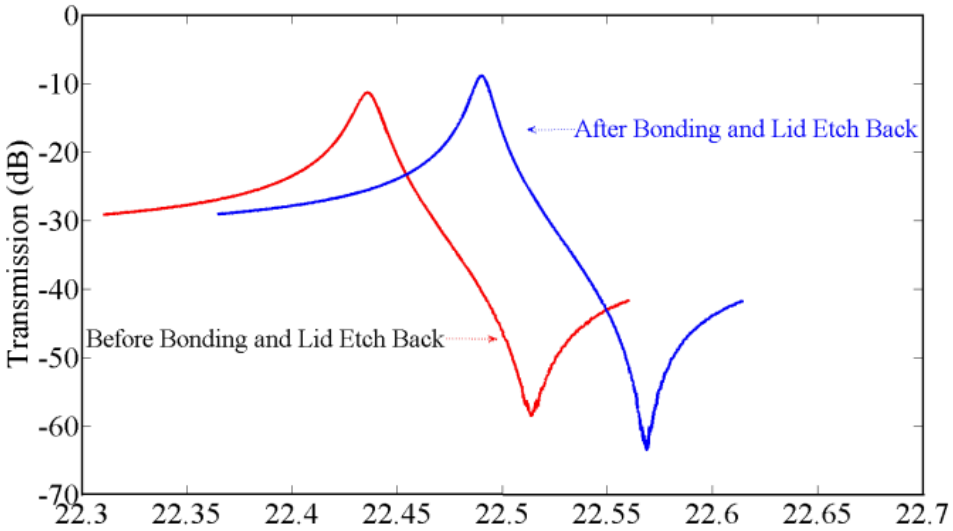


Yield map from a 6” wafer. Red is the reticle and blue are die. Boxed values are Pirani measurements.

Note – Per reticle, one die has a 22 MHz resonator and Pirani gauge and a second die has Pirani gauge only .

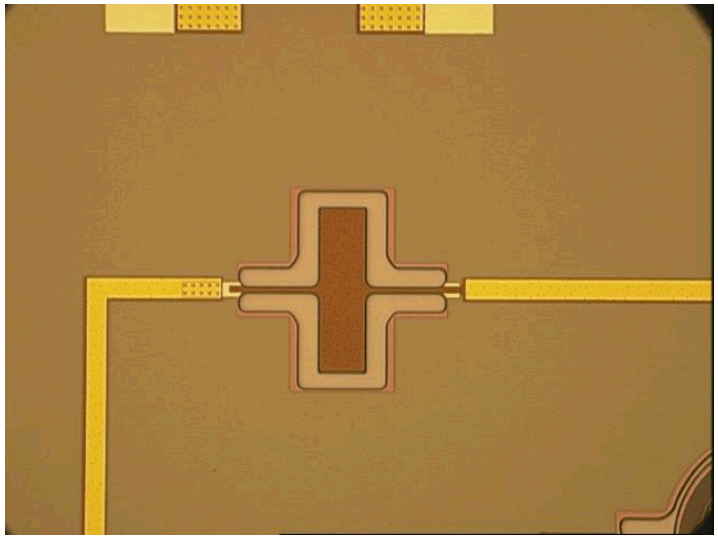
Hermetic Cavity Testing

Effect of bonding/lid etch back/ vacuum on the resonators:



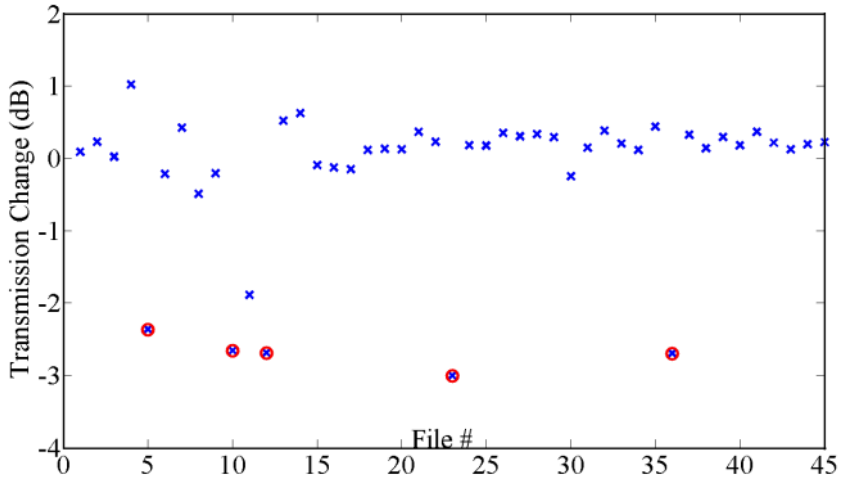
Noted improvements on Q and insertion loss expected due to vacuum.

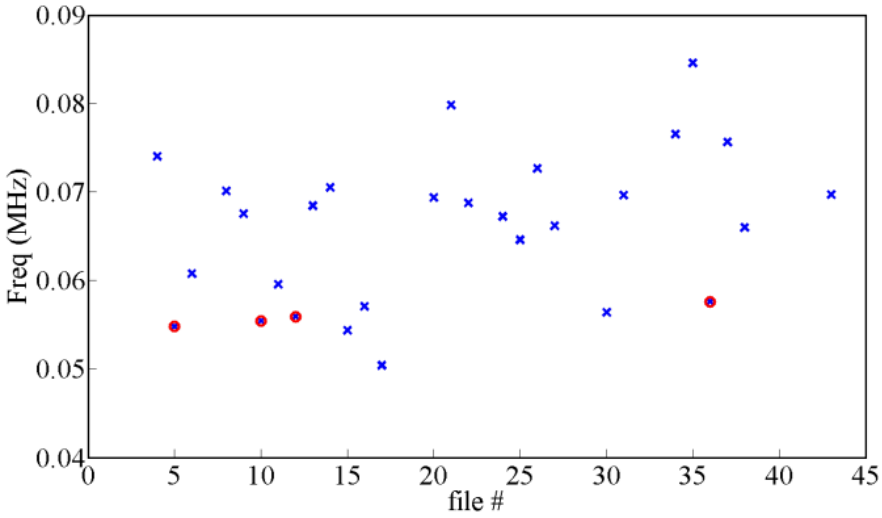
Noted shift in frequency which was not anticipated.

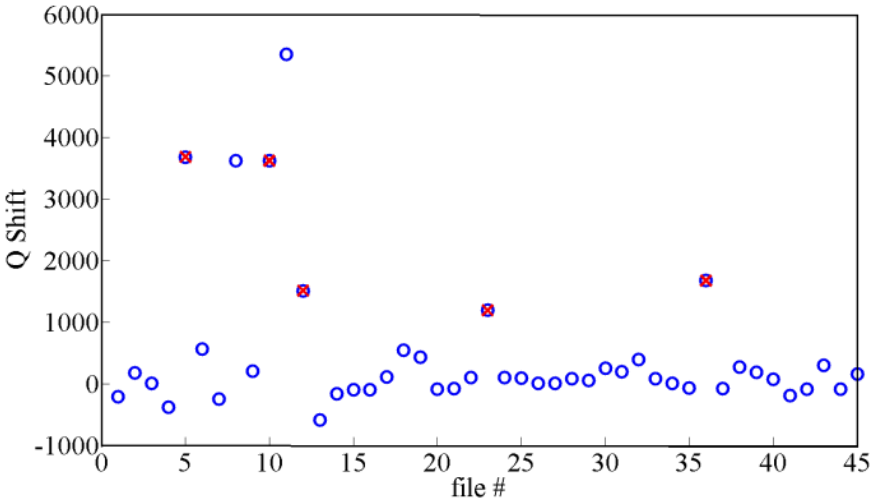


Hermetic Cavity Testing

Effect of bonding/lid etch back/ vacuum on the resonators (die under vacuum in red):







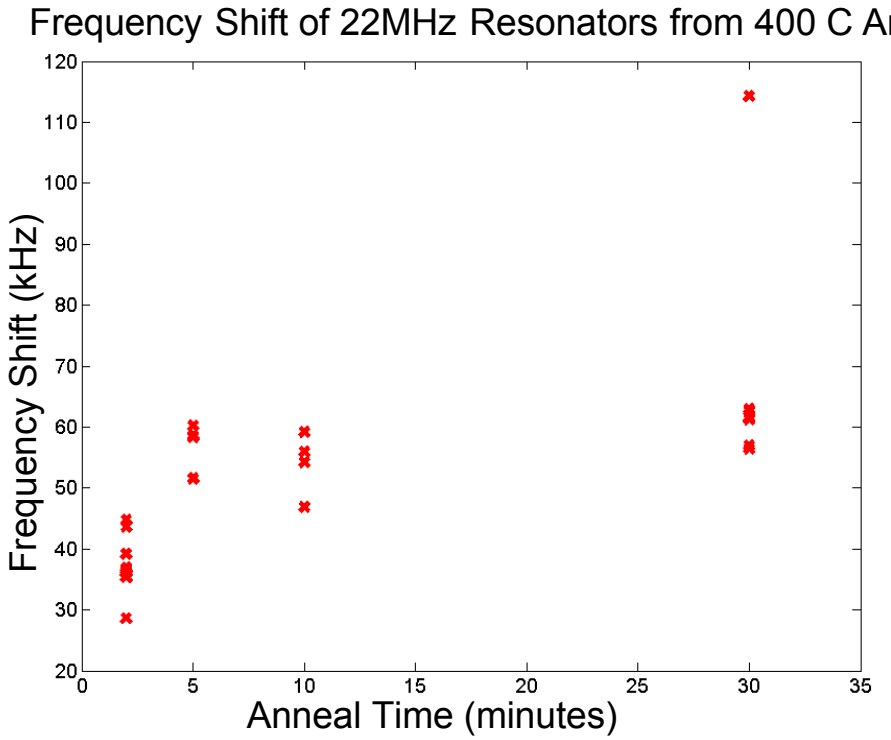
In all cases, frequency upshifted.

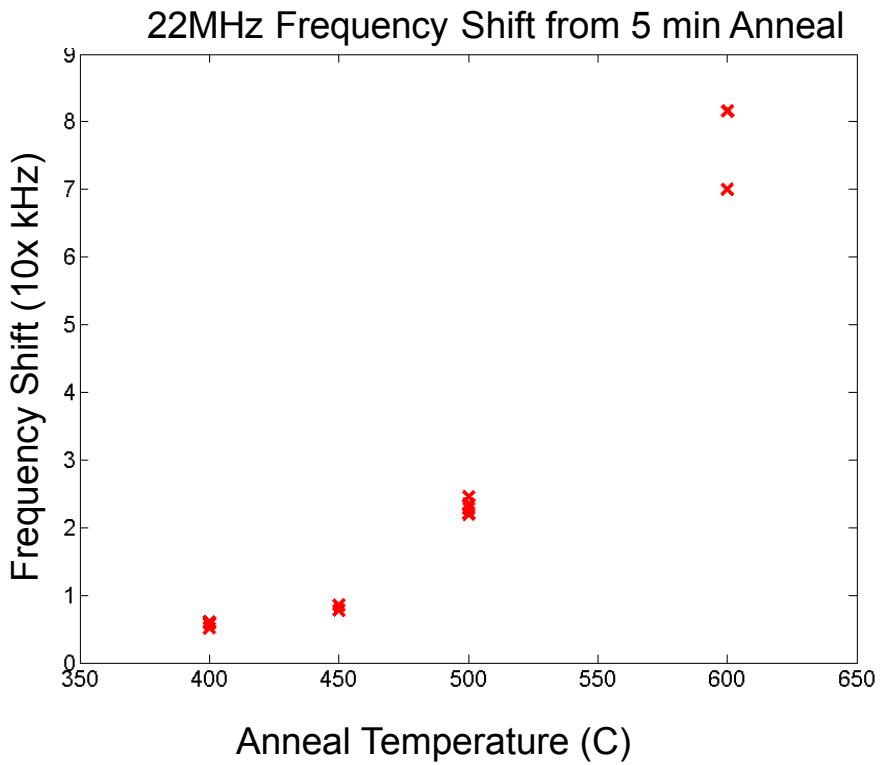
In cases of vacuum, insertion loss decreased by 2.5 dB.

As vacuum increased, the resonator Q increased.

Hermetic Cavity Testing

Experiment – Cleaved die wafer (not packaged) and RTA in Ar/Vac:





Effect saturates out in 5 minutes.

Frequency upshifts but damage is done to Al contacts above 500 C.

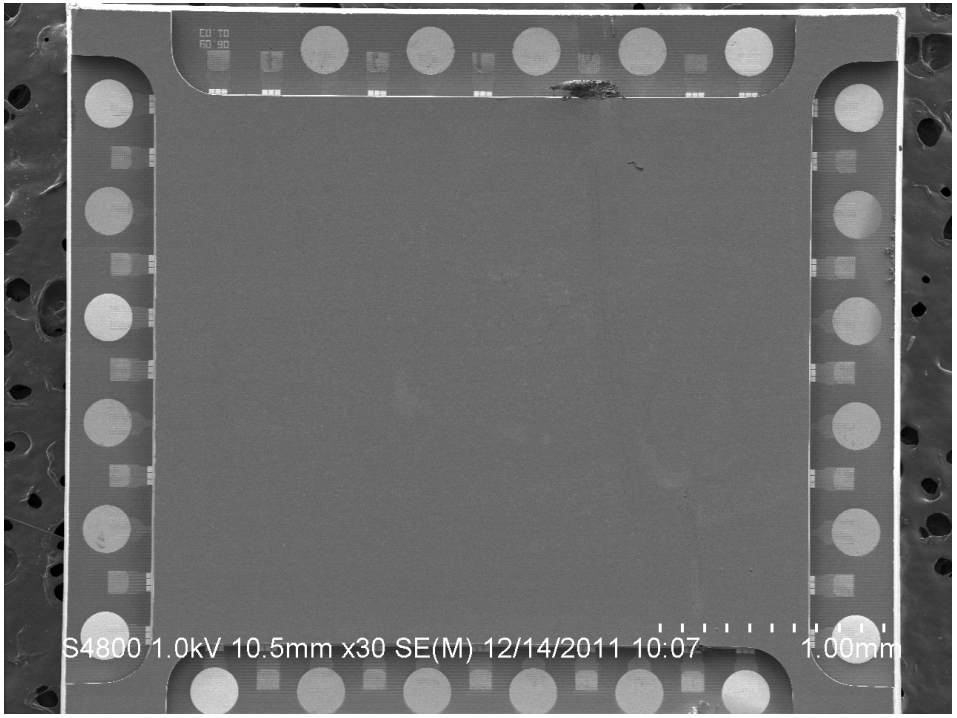
Summary

- Described a (mostly) silicon hermetic packaging system.
- Improved on the eutectic bonding using Au-aSi and appropriate diffusion barriers.
- Utilized a plasma etch to create 100 um thick silicon lids bonded to the die wafer pre-dicing.
- Verified hermetic cavities for the resonators and noted:
  - Frequency shift due to bonding temperatures
  - Q improvement with increased vacuum
  - Insertion loss decrease with vacuum
  - Frequency shift dependence on temperature and bonding time

Questions

Many Thanks to the Sandia National Labs Micro Resonator Team

Peggy Clews
Tom Friedman
Anathea Ortega
Jim Stevens
Teri Romanic
Chris Ford
Todd Bauer
Rajen Chanchani
Tracy Peterson
Jayne Bendure
Dale Hetherington
Dave Sandison



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