SAND2012-9044C

Front End Compatible Through Silicon Via Fabrication

Subhash L. Shinde,
Todd M. Bauer, Robert L. Jarecki, Jordan E. Massad,
and
Dale L. Hetherington

Sandia National Laboratories
Albuquerque, NM 87185
slshind@sandia.gov

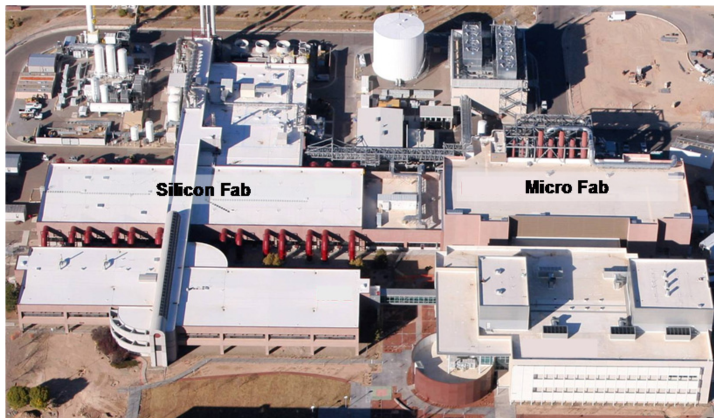
Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy under contract DE-AC04-94AL85000.

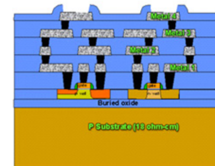
National Nuclear Security Administration

Sandia National Laboratories

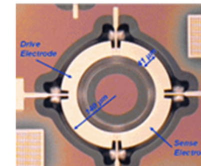
Sandia National Laboratories MESAFab

- **MESA – Microsystems and Engineering Sciences Applications**
- **MESA Silicon Fab**
  - **33,000 ft^2 Class 1 Clean Room for silicon wafer processing.**
  - **Full flow CMOS and MEMS and other associated technologies.**
- **MESA MicroFab**
  - **16,000 ft^2 Class 10 and 100 Clean Room for compound semiconductor material processing, silicon/quartz/alumina/LTCC/metal substrate processing, etc.**
  - **Compound semiconductor devices and other technologies, unique prototypes.**

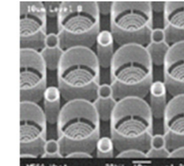




Rad-Hard CMOS SOI Technology

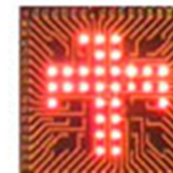


RF MEMS

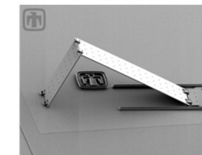


MEMS Molded Tungsten

SUMMiT



III-V



microoptics

- *Diverse Product Mix – from IC production to highly customized prototyping with flexible processing capabilities*.
- ***We are ideally suited for leveraging 3D integration to bring together dissimilar technologies.***

NNSA National Nuclear Security Administration

Sandia National Laboratories

Advantages of FEOL TSV Integration

Front-end-of-line (FEOL) Through Silicon Vias:
TSV fabricated before or immediately after device fabrication.

- TSVs formed before metal routing layers
  - Eliminates 'real estate' need for fab'ing post vias
  - High vertical interconnects density (aspect ratio >20, pitch $\leq$20 μm, diameter ~2 μm)
  - Reduces design complexity.
- High yield
- Uniform feature size & via isolation
- Reproducible electrical & mechanical properties
- High reliability
- Facilitates incorporation into 3D structures.

TSV Process Flow

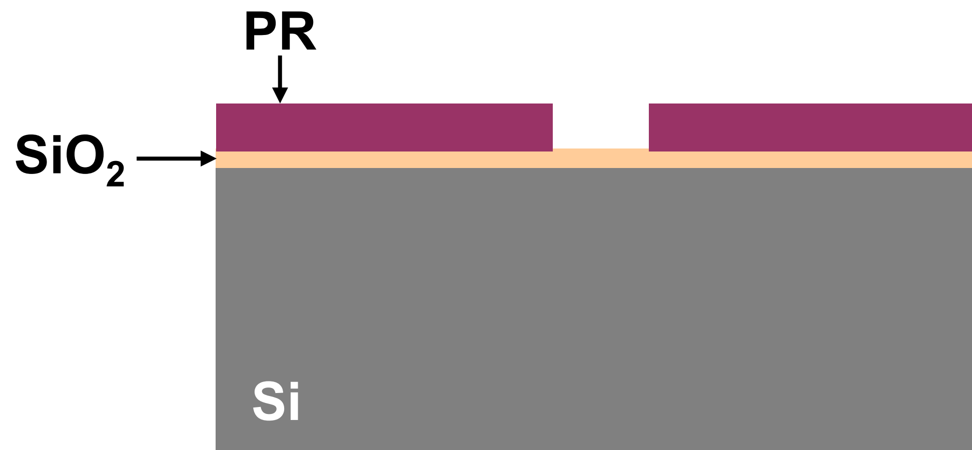
1. Deposit SiO_2 for etch mask and polish stop.
2. Pattern and etch vias.
3. Isolate via holes by lining them with dielectric.
4. Thermally deposit silicon to fill via holes.
5. Remove silicon overburden by CMP.
6. Remove SiO_2 hardmask.
7. Form silicon nitride barrier.
   - *COMMENCE NORMAL FEOL PROCESSING*
8. After normal IMD0 deposition and planarization, pattern and etch contacts to expose vias.
9. Remove silicon in via.
10. Deposit tungsten by CVD to fill via.
11. Remove overburden of tungsten by CMP.
    - *COMMENCE NORMAL BEOL PROCESSING*

Silicon Dioxide Film Deposition

- Functions as etch mask, CMP stop.
- FEOL compatible low temperature oxide, ~ 0.15 µm thick.
  - Provides process margin for poly Si CMP.
- Deposited oxide preferred rather than thermal oxide that will be formed as dielectric isolation.
  - Loss of device silicon during oxidation is unacceptable for CMOS fabbed on thin epitaxial Si or SOI with thin device Si.

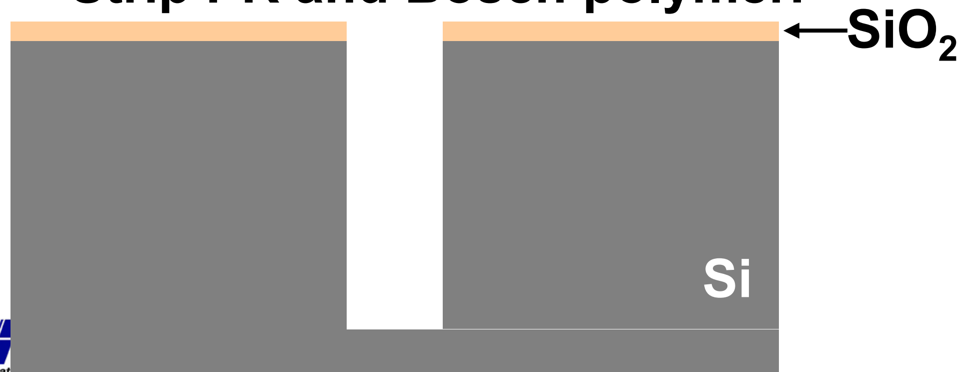
Via Patterning

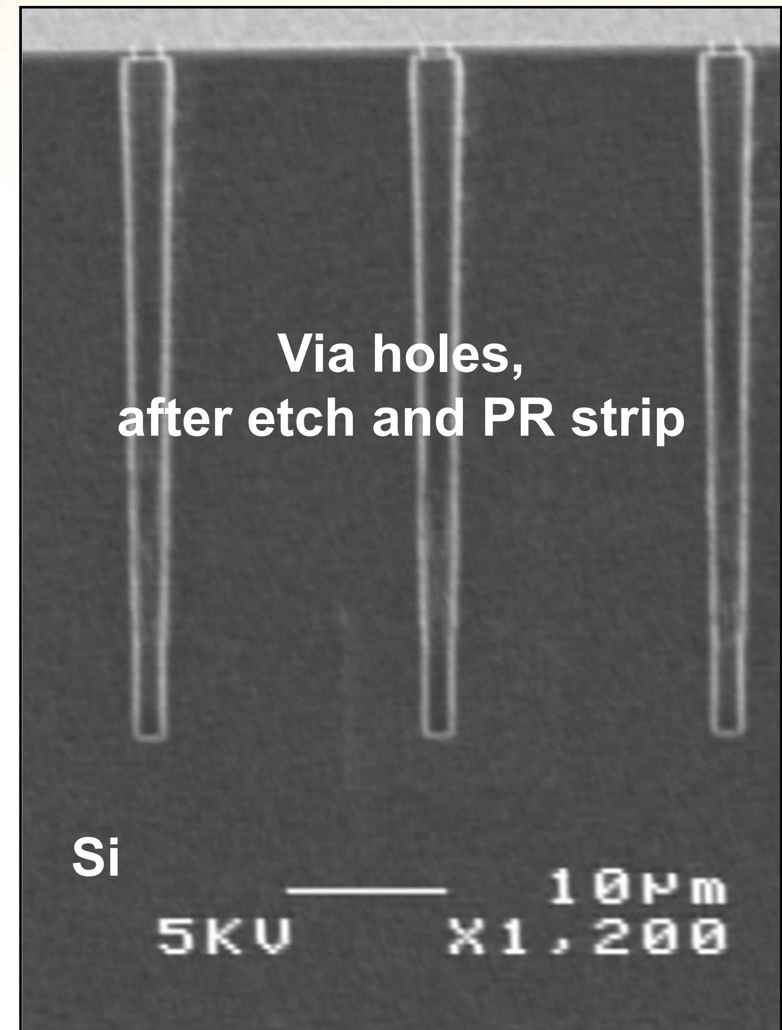
- Use 3 µm photoresist to pattern up to 2.5 µm diameter vias.
- Via diameter is limited by subsequent W-CVD thickness.
  - CVD W is a relatively high stress film.
  - W thickness greater than 1.2 µm is prone to peeling.



Via Etching and Resist Stripping

- Open SiO_2 mask using high selectivity, anisotropic plasma etch.
- Bosch etch the Si to the limits of the PR mask.
  - High etch selectivity to PR and positive taper; facilitates subsequent filling of via by CVD.
  - Creates deep, high aspect ratio holes in Si.
- Via depth ~50 µm with 2 µm diameter hole; aspect ratio ~25.
- Strip PR and Bosch polymer.

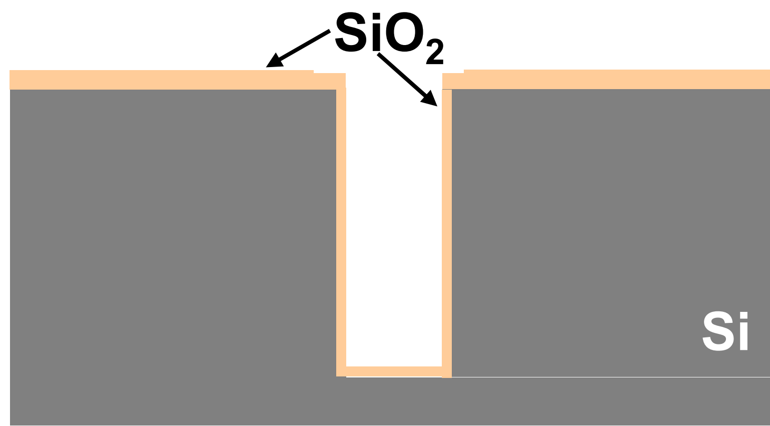


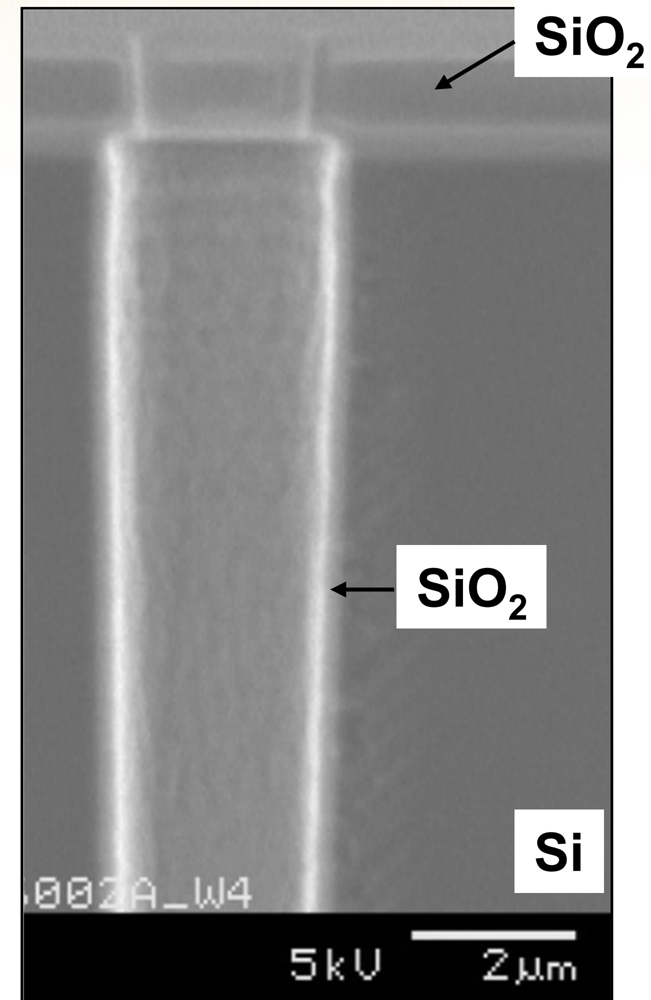


Sandia National Laboratories

Electrical Isolation of Vias by Thermal Oxidation

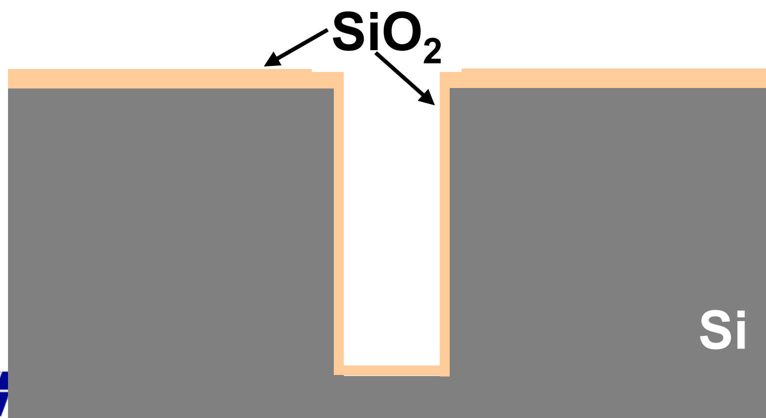
- Thermal oxidation of Si resulting in ~0.25 μm SiO_2 on via sidewall.
- Perfectly conformal.
- Excellent dielectric performance.
- Deposited oxide on device Si surface prevents oxidation.
- We also demonstrated dielectric isolation by PECVD and ALD.
- V_{BD}>10 MV/cm.

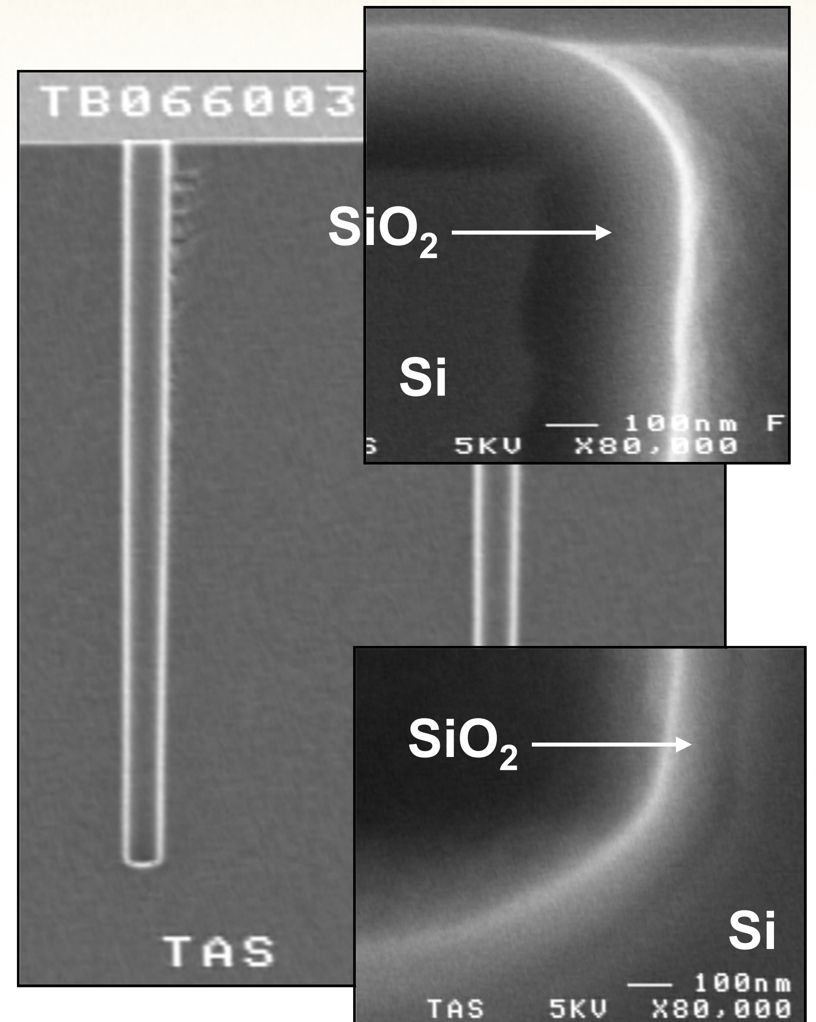




Low Temperature Dielectric Isolation by CVD

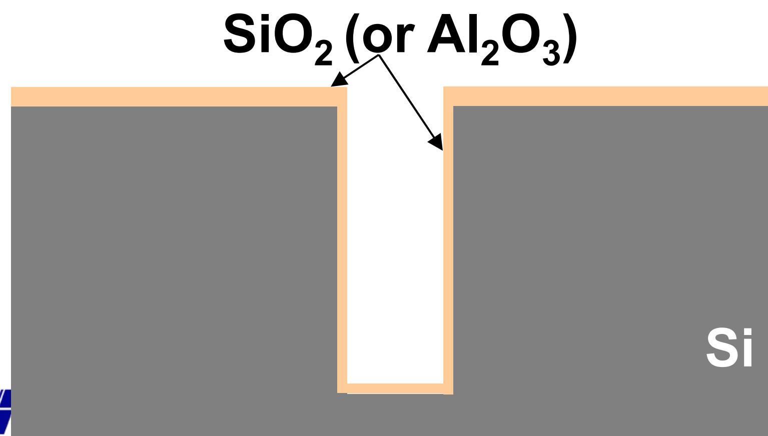
- Low temperature dielectric isolation achieved by CVD.
- USG film adsorbs moisture.
- USG film is sufficiently tensile that the film cracks.
  - Requires RTA to improve film robustness.
- Compromised conformality.
  - Note decrease in film thickness with depth into the via.

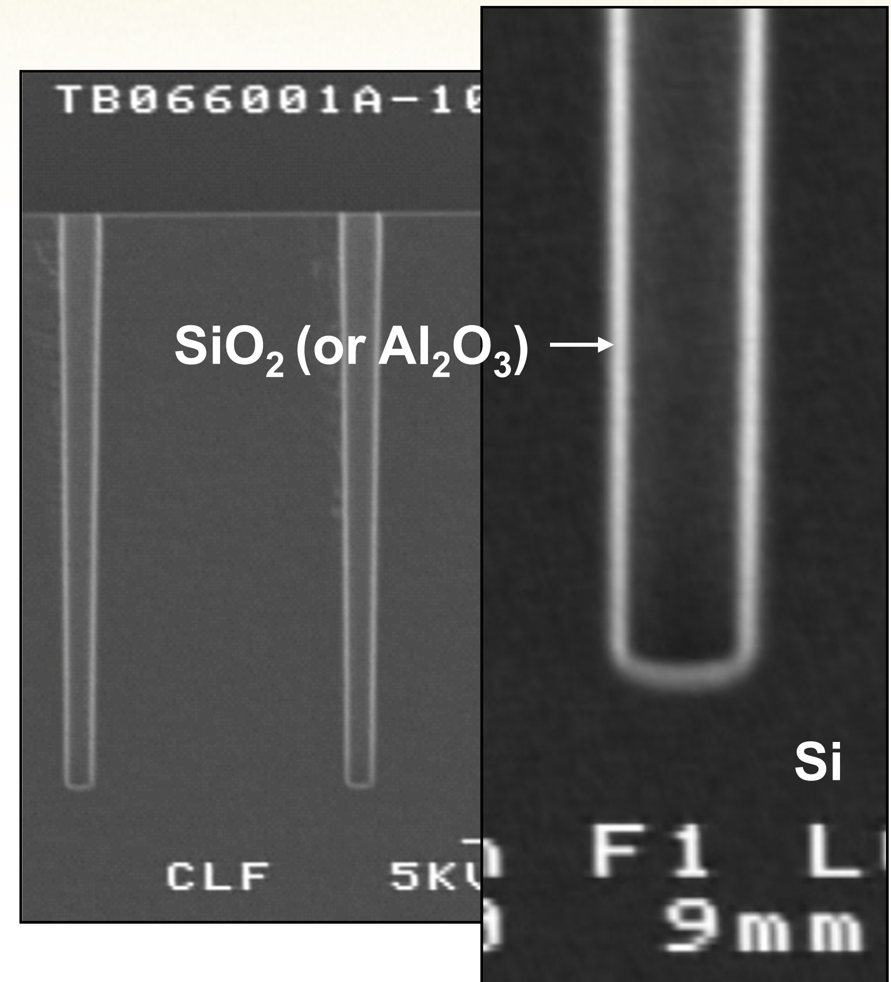




Low Temperature Dielectric Isolation by ALD

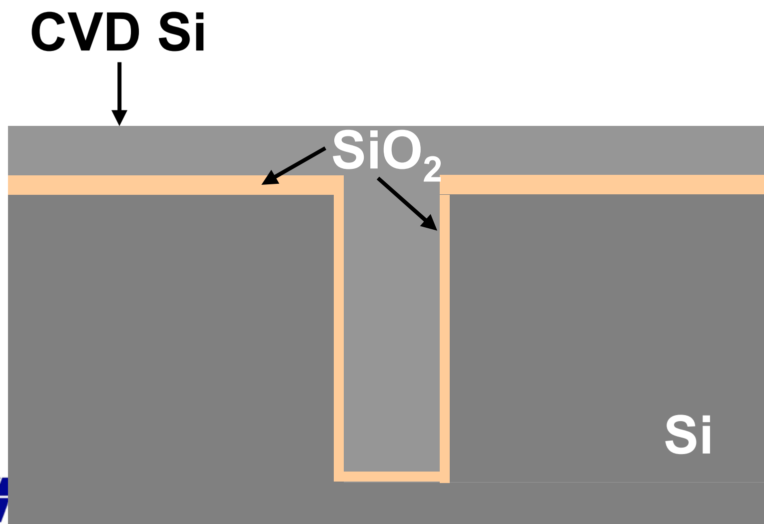
- **Atomic Layer Deposition (ALD) capable of achieving near room temperature SiO_2 deposition.**
- **But…ALD of SiO_2 is not production-worthy.**
- **Coated etched vias using ALD of Al_2O_3 to demonstrate viability of ALD for dielectric deposition.**
  - **Excellent conformality.**
  - **Low deposition rate.**

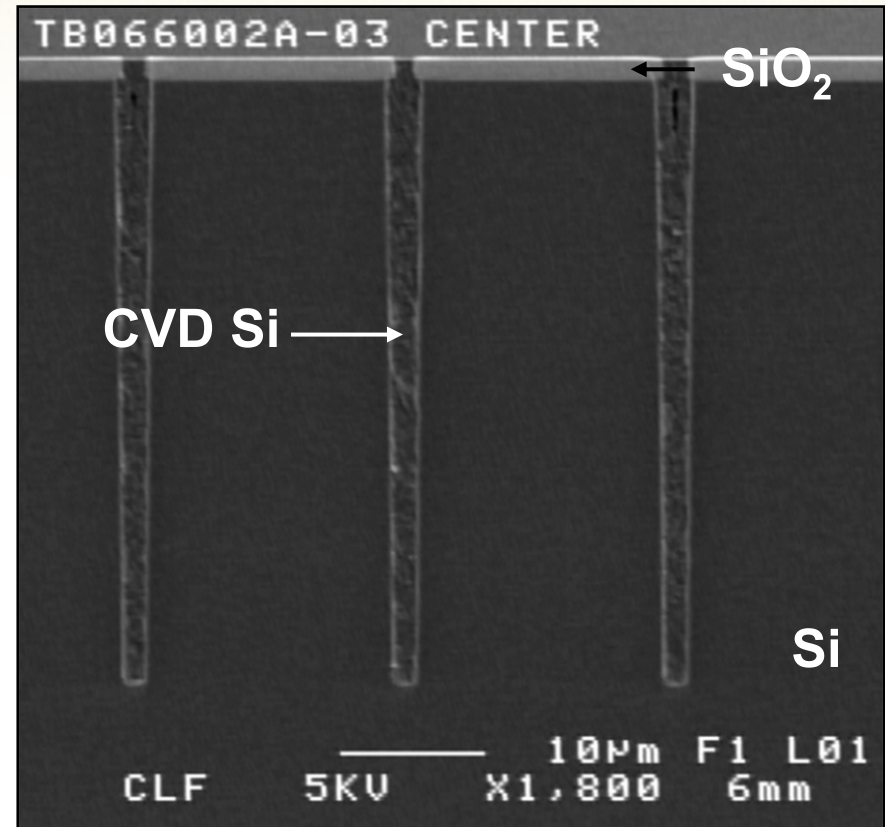




Via Filling with Sacrificial Silicon

- Thermally deposit amorphous Si at 700-800°C.
- Si deposition has excellent conformality.
- Si can be doped.
  - Demonstrated conductive Si vias with Si resistivity < 10^{-3} Ω-cm.



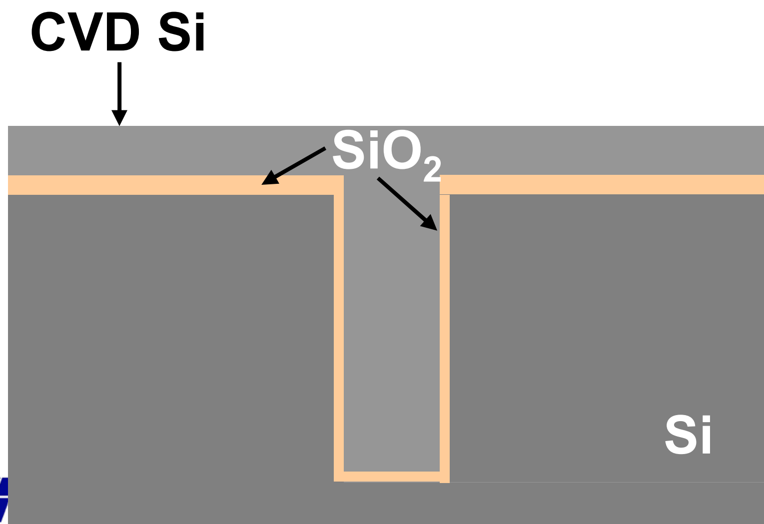


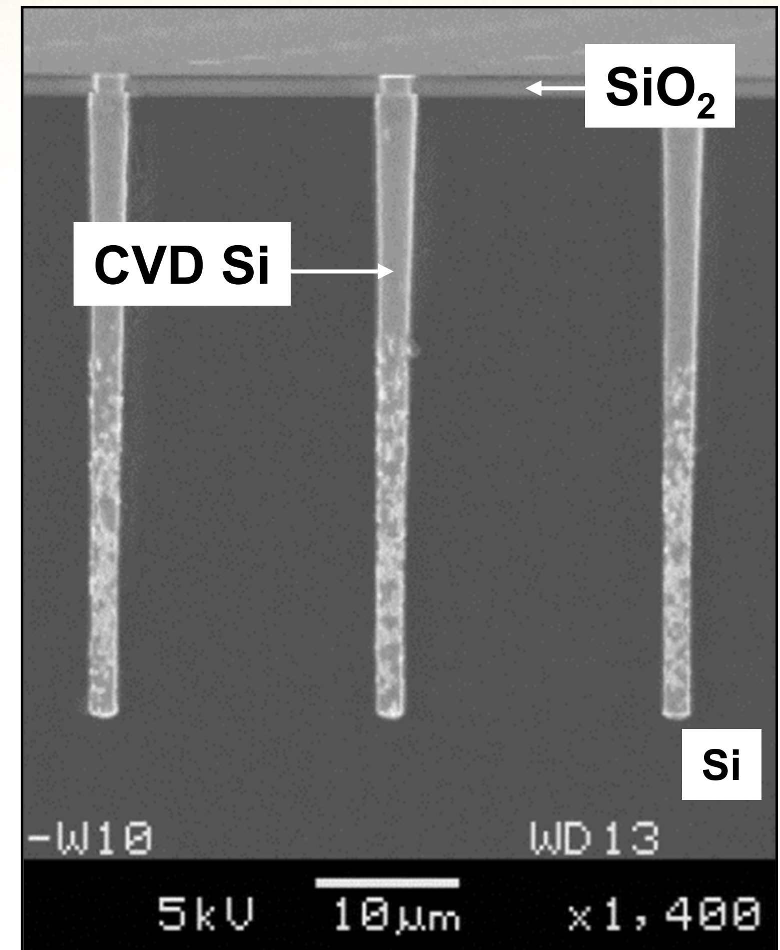
National Nuclear Security Administration

Sandia National Laboratories

Silicon Overburden Removal by CMP

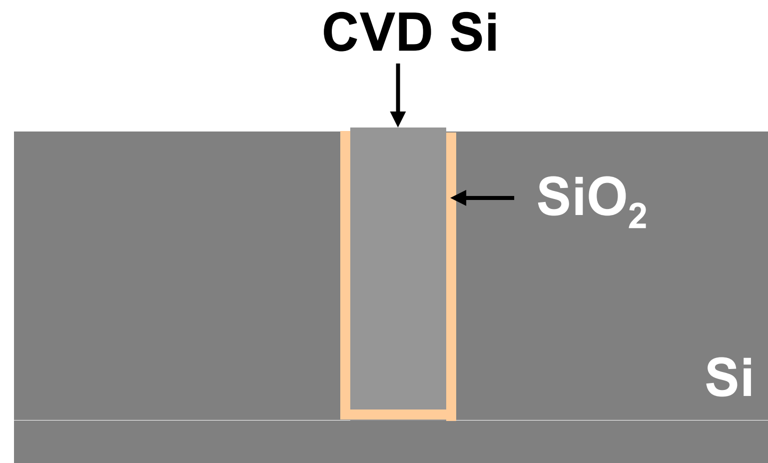
- Polish back the Si to the deposited oxide.
- Selectivity of the Si polish process to oxide approaches 100.
  - High selectivity allows a thin deposited oxide for the polish stop.





Oxide Hardmask Removal by Wet Etch

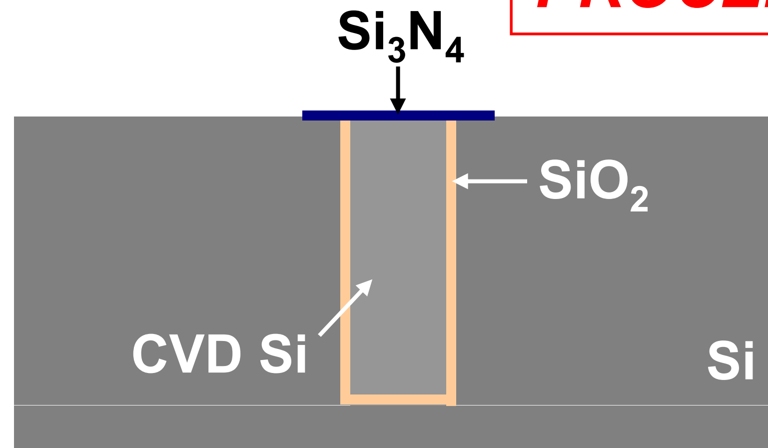
- Wet etch is preferable to plasma etch since FC-based plasma etch can implant carbon into Si.
- Minimize over etch!
  - Too much etch can lead to removal of dielectric isolation.
  - Deposited oxide can be chosen to maximize wet etch rate and thus etch selectivity to thermal oxide.



Silicon Nitride Barrier Formation

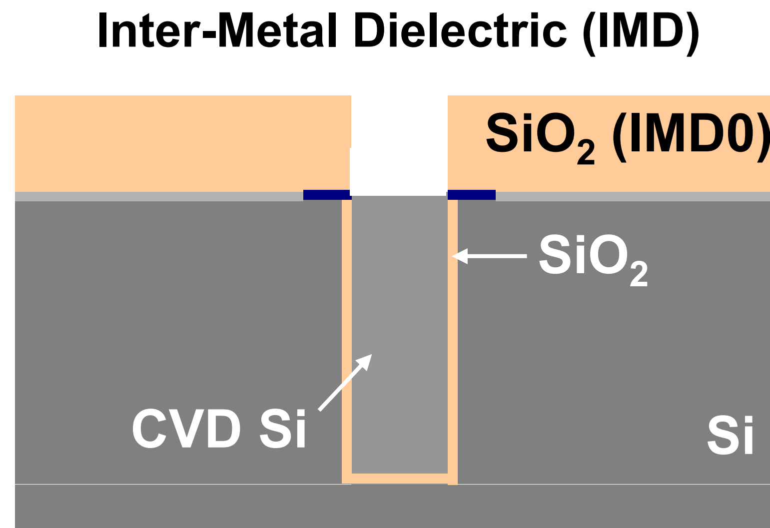
- Thin Si_3N_4 barrier protects Si in via from subsequent silicide formation.
  - Si_3N_4 is deposited on thin thermal oxide, which acts as stress buffer and as etch stop layer.
- Standard photopatterning and plasma etch processes define the Si_3N_4 feature.

FEOL PROCESSING PROCEEDS NORMALLY



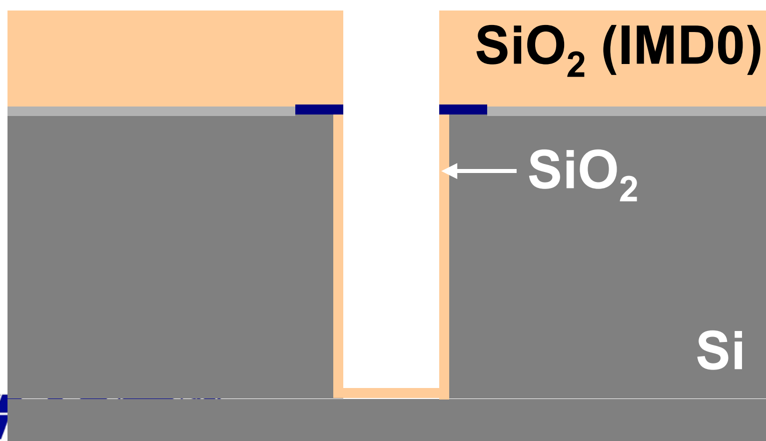
Contact Holes Formation to Expose Vias

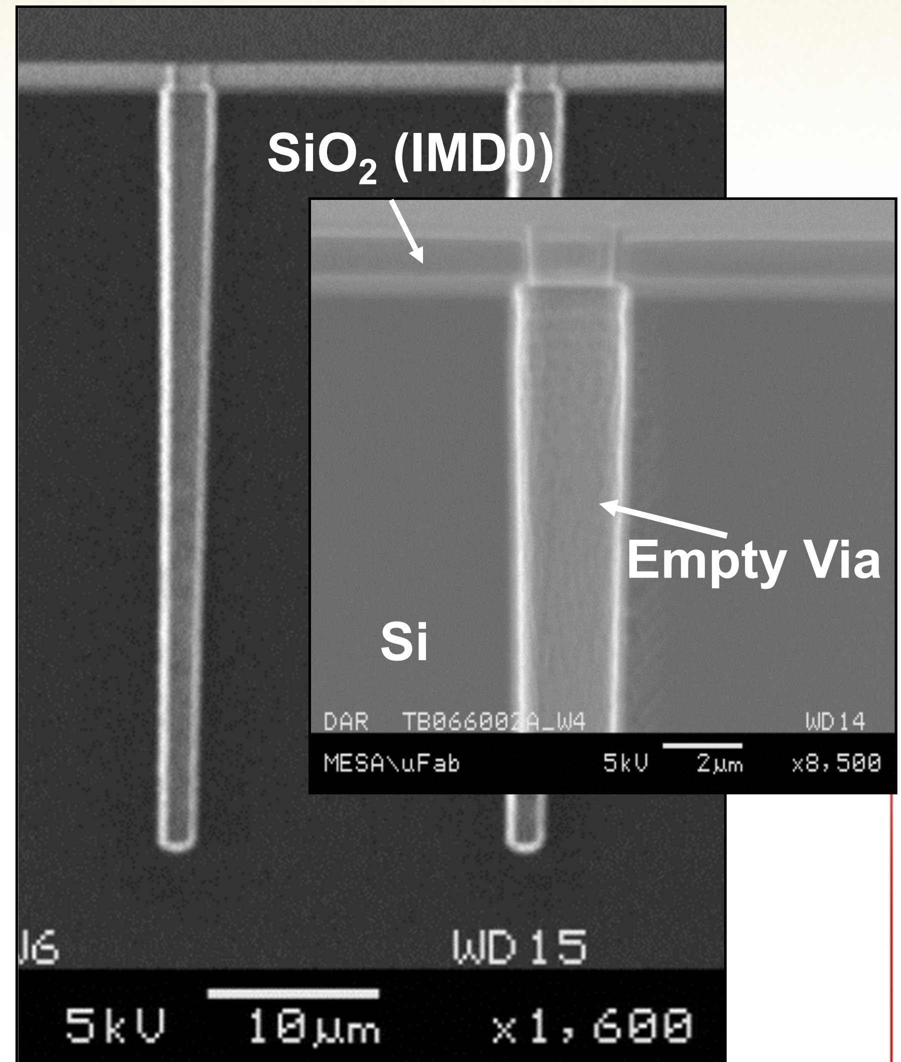
- After FEOL processing is complete, pattern and etch contacts through (Inter-Metal Dielectric) IMD0 film and Si_3N_4 barrier to expose Si in the via.
- These contacts can be formed during normal contact processing or as separate module from normal contact processing.



Removal of Sacrificial Silicon from Vias

- After the Si in the TSVs is exposed, it is removed.
- Demonstrated removal by chemical downstream etch (CDE) processes and by low bias high density plasma etch processes.
- Demonstration of Si removal by XeF_2 etching is planned.

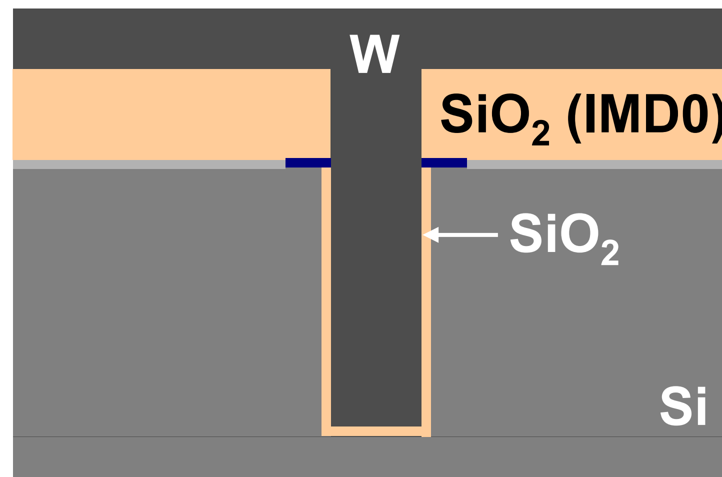




Sandia National Laboratories

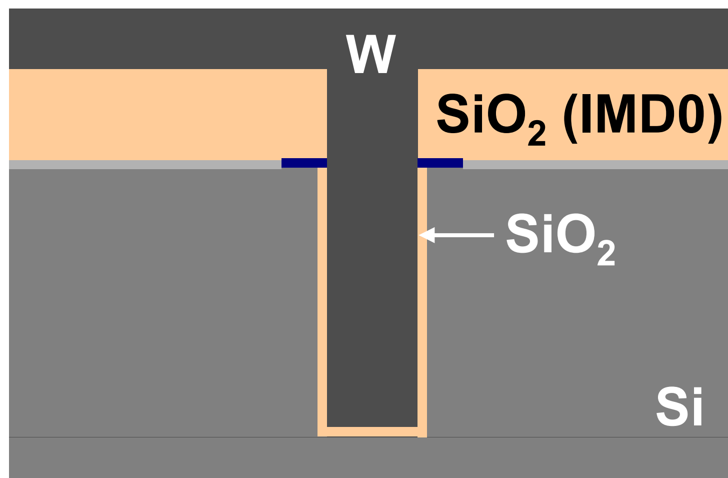
Via Filling with Tungsten

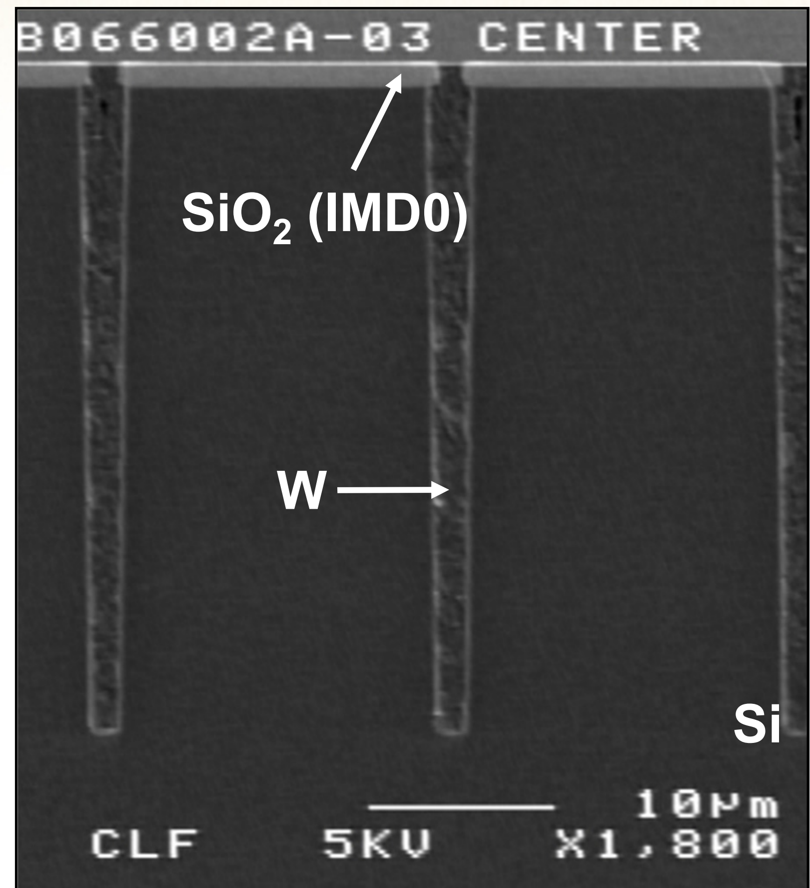
- W-CVD offers excellent conformality and is a well-known process for IC fabrication.
- Deposit PVD Ti/TiN liner (for adhesion) and 1.2 µm CVD W.
- Due to stress and process integration considerations, W-CVD is limited to a max thickness of ~ 1.2 µm, which limits the max hole diameter to ~ 2.4 µm.



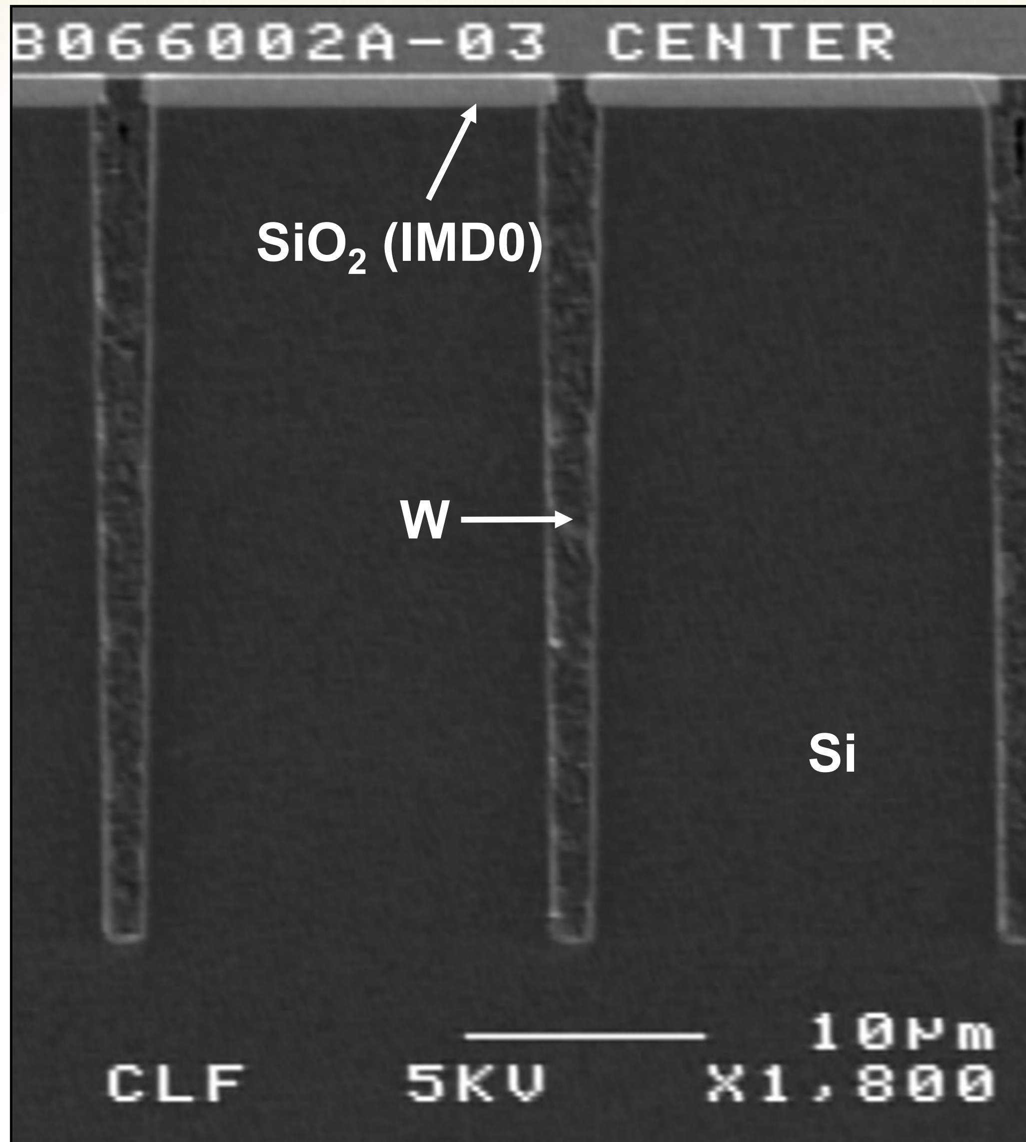
Tungsten Overburden Removal by W-CMP

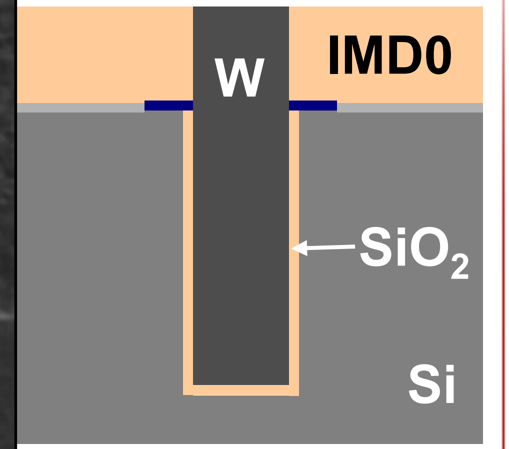
- W-CMP is common to BEOL IC processing.
- W-CMP selectivity to SiO_2 is ~40.
- Polish back the W to the deposited oxide.



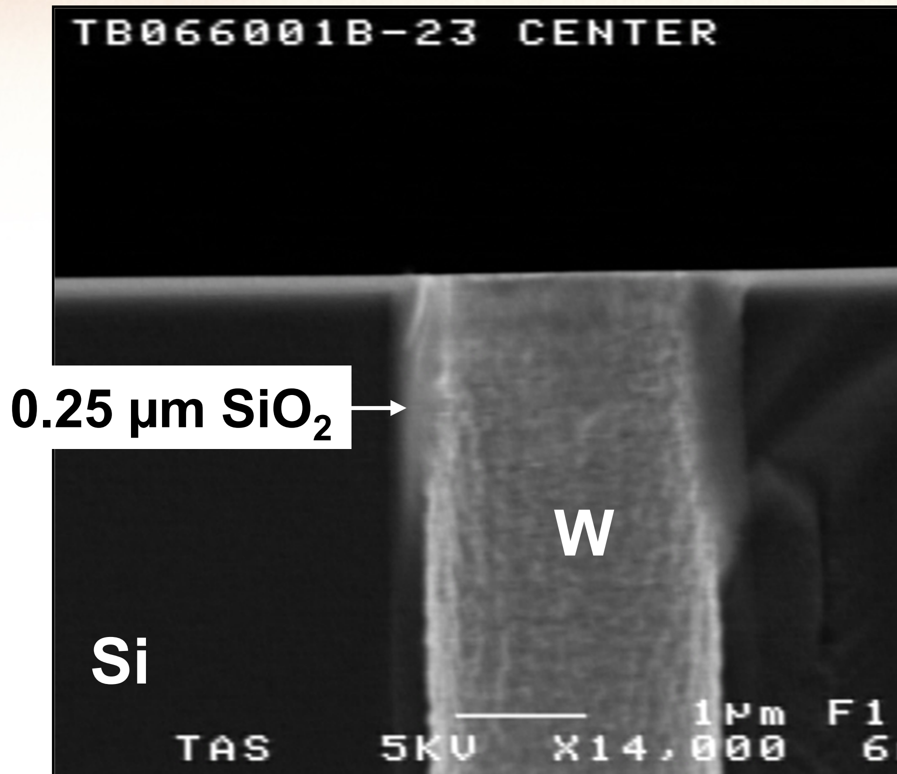


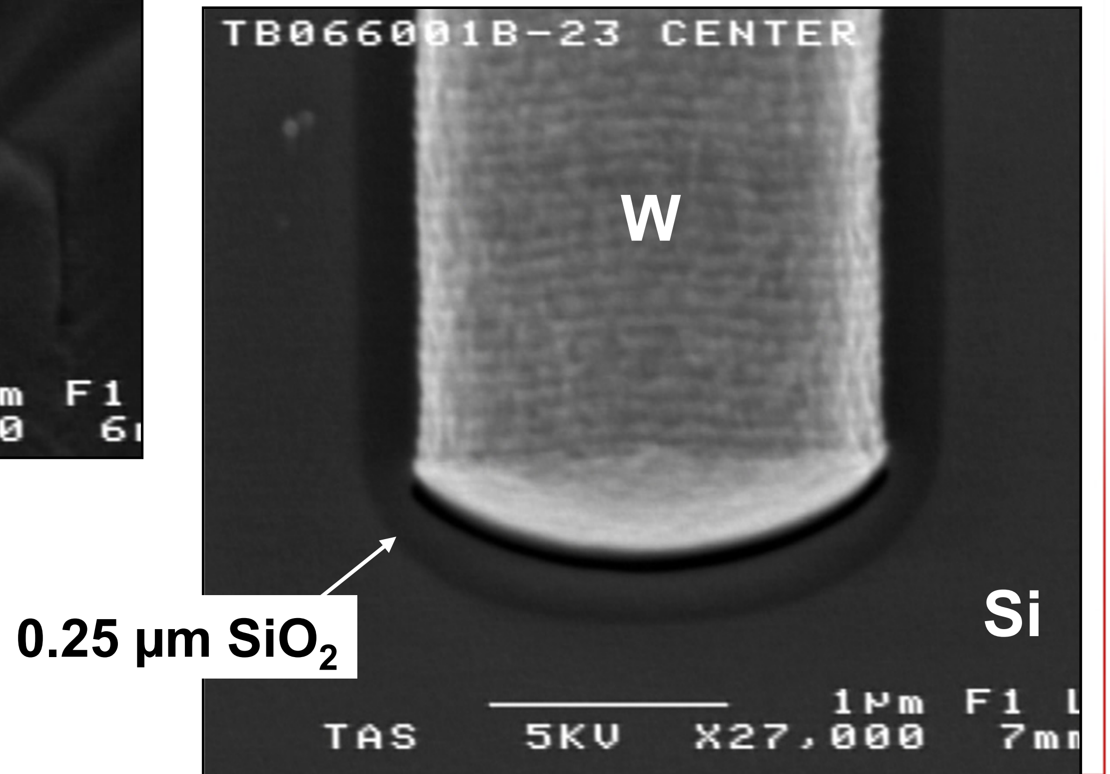
Fully Formed Tungsten Vias





Fully Formed Tungsten Vias

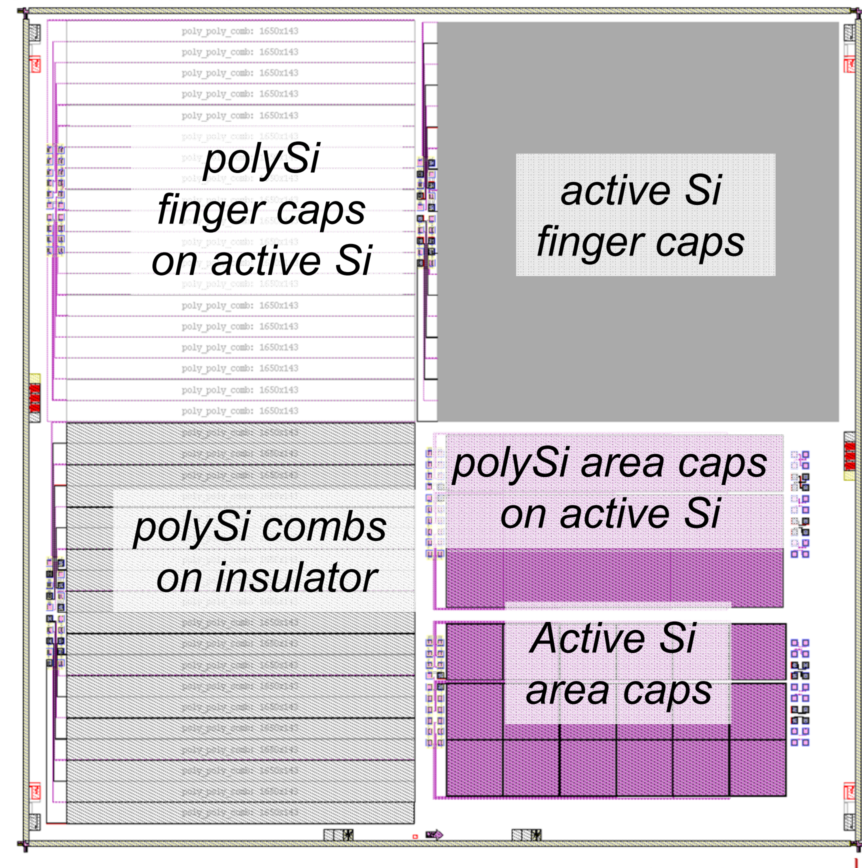




FEOL TSV Compatibility Assessment using GOI

Gate Oxide Integrity Monitor Test Vehicle

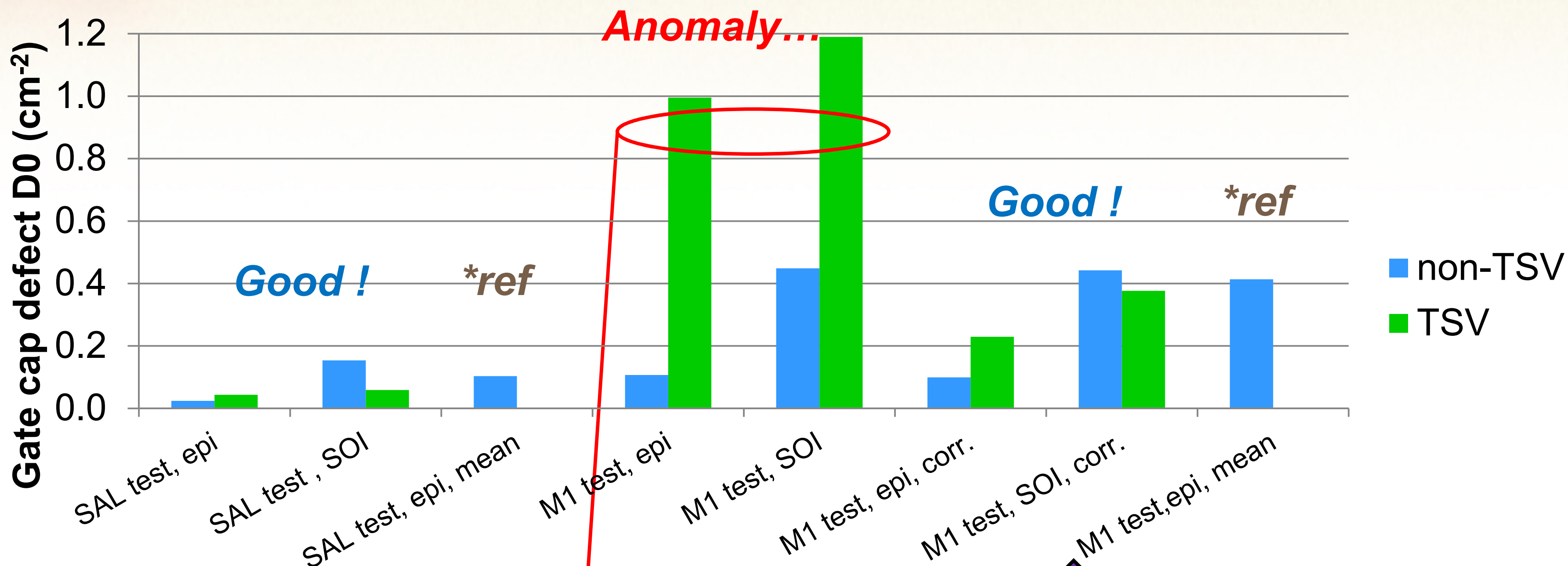
- **RS239 is the fab GOI monitor.**
  - Serps, combs, and caps.
- **Parametric performance is dependent on high quality gate oxide.**
  - Particles, damaged Si, charging, have negative impact on GOI.
  - Does TSV processing lead to particles, damaged Si, charging?
- **RS modified to allow full FEOL TSV processing with testing of standard RS239 structures, from front and back side of wafer.**
- **Parametric data from wafers w/ TSVs compared to years of weekly data from standard GOI wafers.**
- **Helps determine if TSV processing and/or wafer thinning impacts GOI.**



National Nuclear Security Administration

Sandia National Laboratories

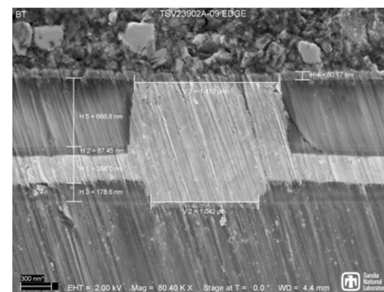
RS239 Good GOI with FEOL TSVs, epi or SOI



Known edge effects for left-most die results in shorts from cap pads to Si !

Working on process fix….

			3.00E+30 4,8	3.00E+30 5,8	3.00E+30 6,8			
		3.00E+30 3,7	3.00E+30 4,7	3.00E+30 5,7	3.00E+30 6,7	3.00E+30 7,7		
	3.00E+30 2,6	3.00E+30 3,6	3.00E+30 4,6	3.00E+30 5,6	3.00E+30 6,6	3.00E+30 7,6	3.00E+30 8,6	
2236 1,5	3.00E+30 [illegible],5	3.00E+30 3,5	3.00E+30 4,5	3.00E+30 5,5	3.00E+30 6,5	3.00E+30 7,5	3.00E+30 8,5	3.00E+30 9,5
2412 1,4	3.00E+30 2,4	3.00E+30 3,4	3.00E+30 4,4	3.00E+30 5,4	3.00E+30 6,4	3.00E+30 7,4	3.00E+30 8,4	3.00E+30 9,4
1237 1,3	3.00E+30 2,3	3.00E+30 3,3	3.00E+30 4,3	3.00E+30 5,3	3.00E+30 6,3	3.00E+30 7,3	3.00E+30 8,3	3.00E+30 9,3
	3.00E+30 2,2	3.00E+30 3,2	3.00E+30 4,2	3.00E+30 5,2	3.00E+30 6,2	3.00E+30 7,2	3.00E+30 8,2	
		3.00E+30 3,1	3.00E+30 4,1	3.00E+30 5,1	3.00E+30 6,1	3.00E+30 7,1		

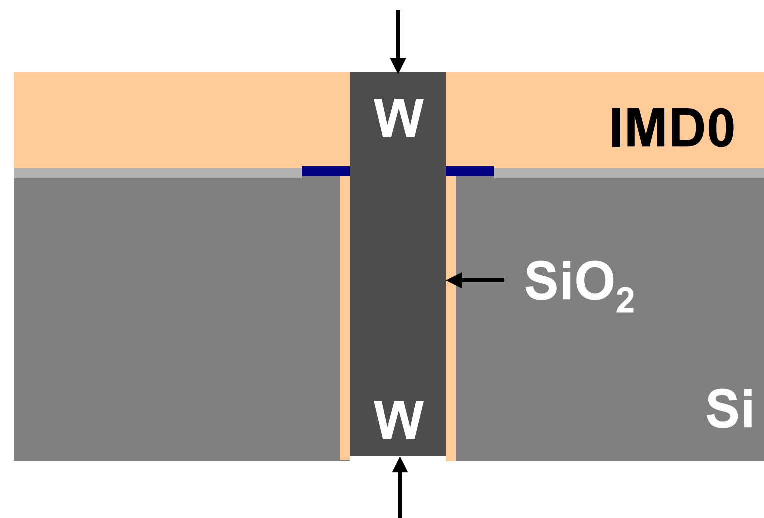


NNSA National Nuclear Security Administration

Sandia National Laboratories

Wafer Thinning to Expose Vias from Backside

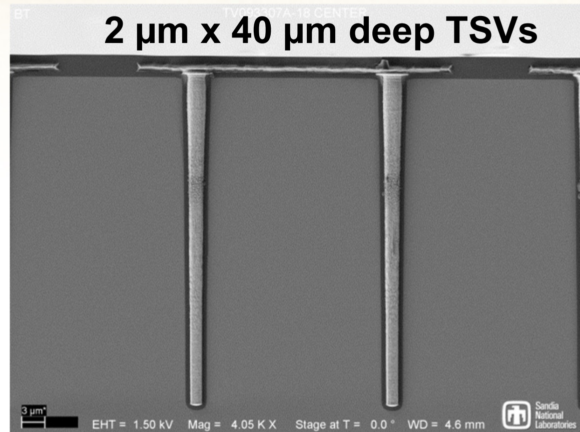
After processing is complete, thin wafer from backside to expose vias.



NNSA National Nuclear Security Administration

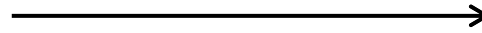
Sandia National Laboratories

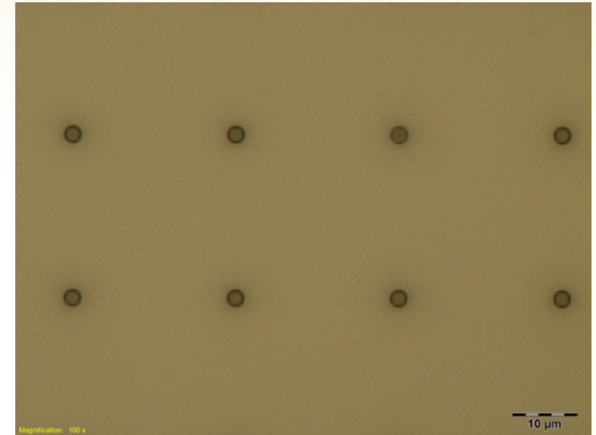
RS933 TSV/Thinning Sequence & Initial Data



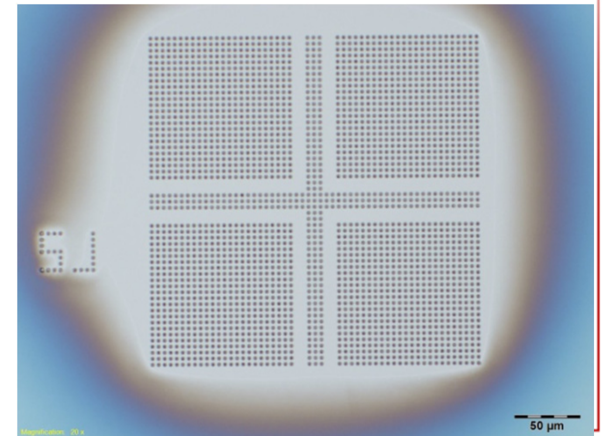
25 µm pitch

bond RS933 front to handle
backgrind
reveal TSVs

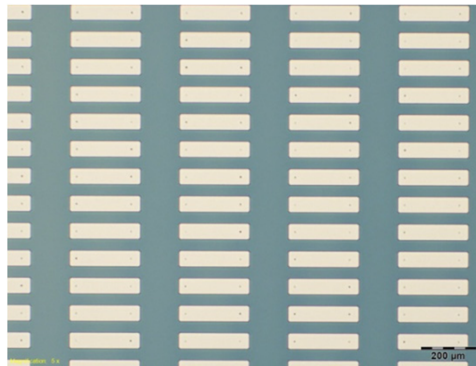


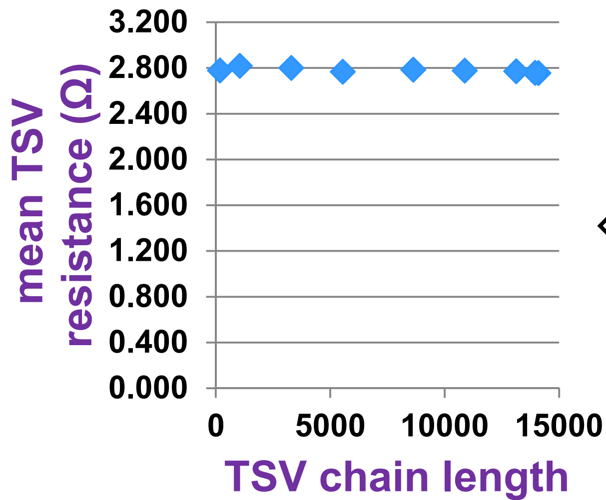


Si recess
PECVD oxide
CMP



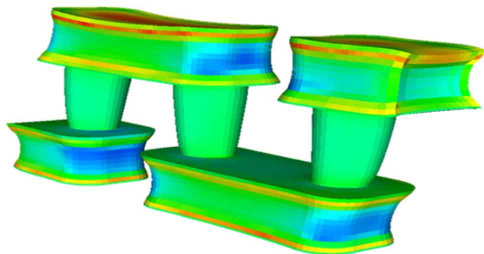
liftoff Al metal

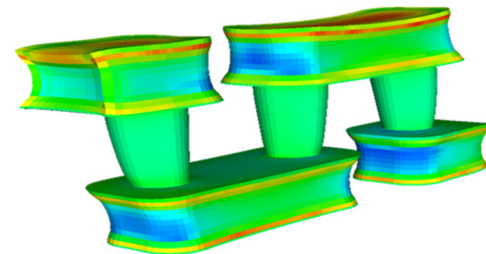




3D Integration Reliability

- Design complexity of 3D ICs introduces high level of sensitivity of reliability to structural interactions
  - Thermomechanical interactions among multi-level components;
  - Interconnects pass through materials with varying CTEs.
- Need understanding of internal stress and deformation (difficult to assess experimentally).

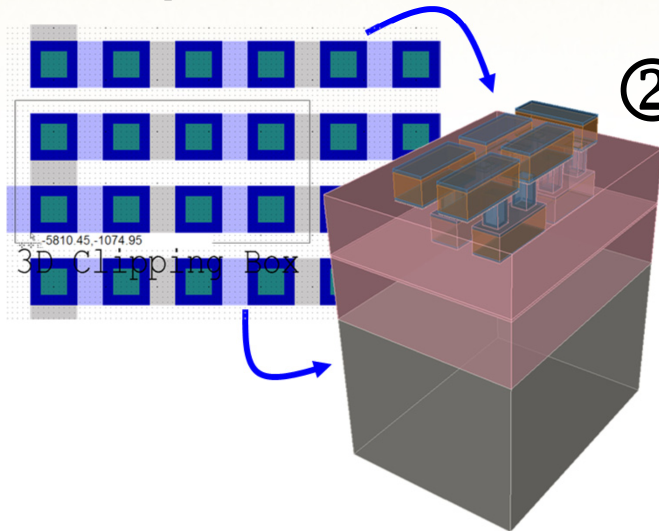




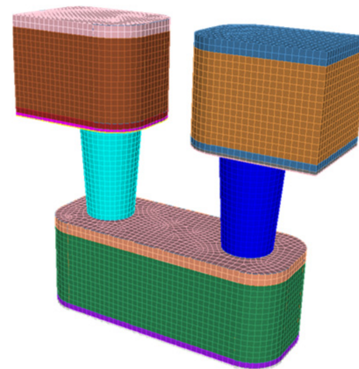
Modeling should be a critical task in the design phase to manage sensitivities and increase yield and reliability.

3D Thermomechanical Modeling Steps

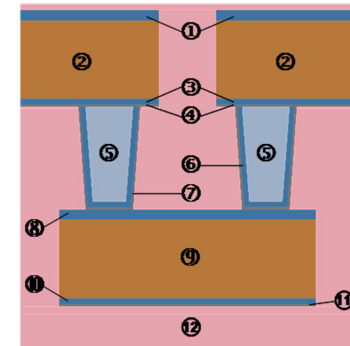
① **Build geometrical representation.**



② **Numerically discretize geometry (mesh).**



③ **Simulate physical behavior.**

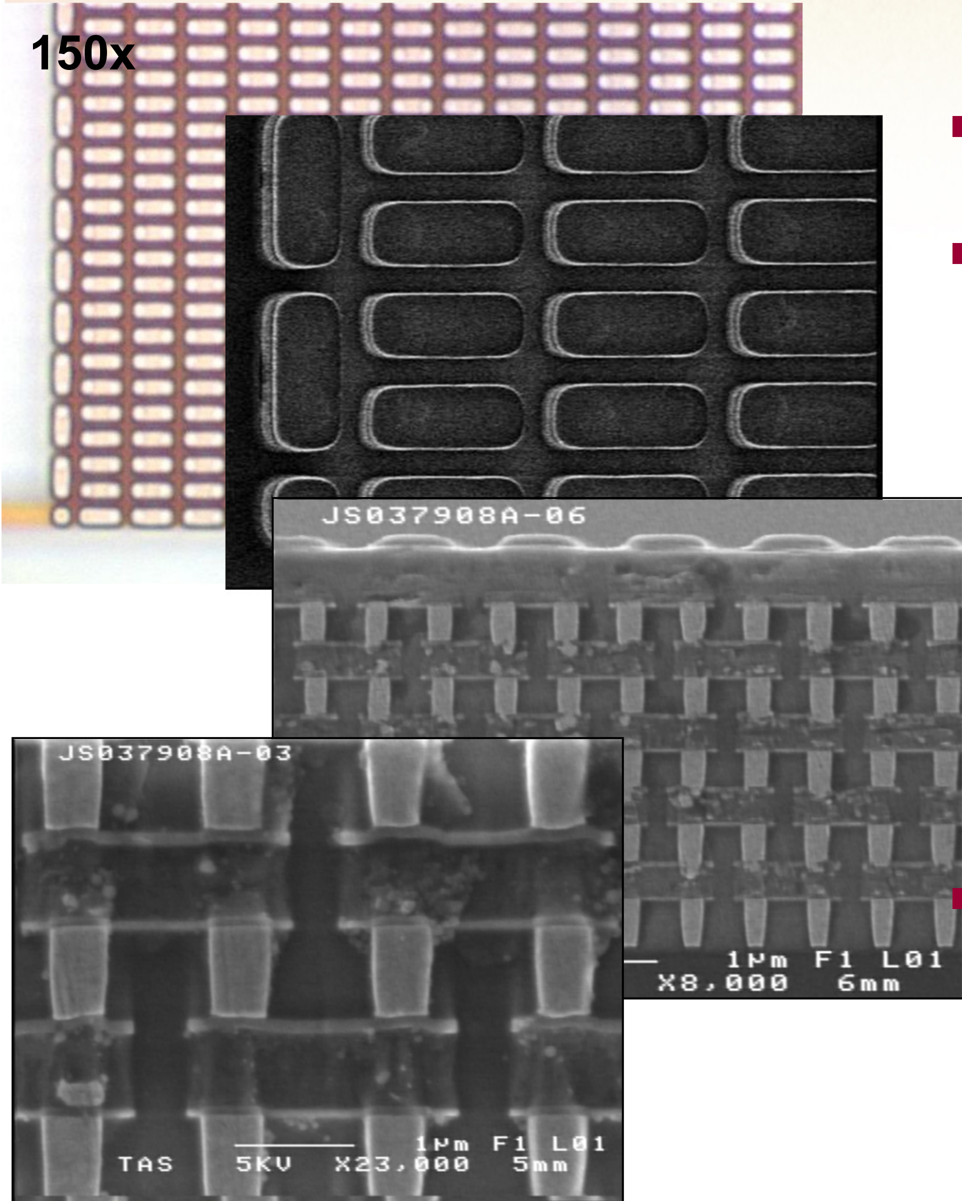


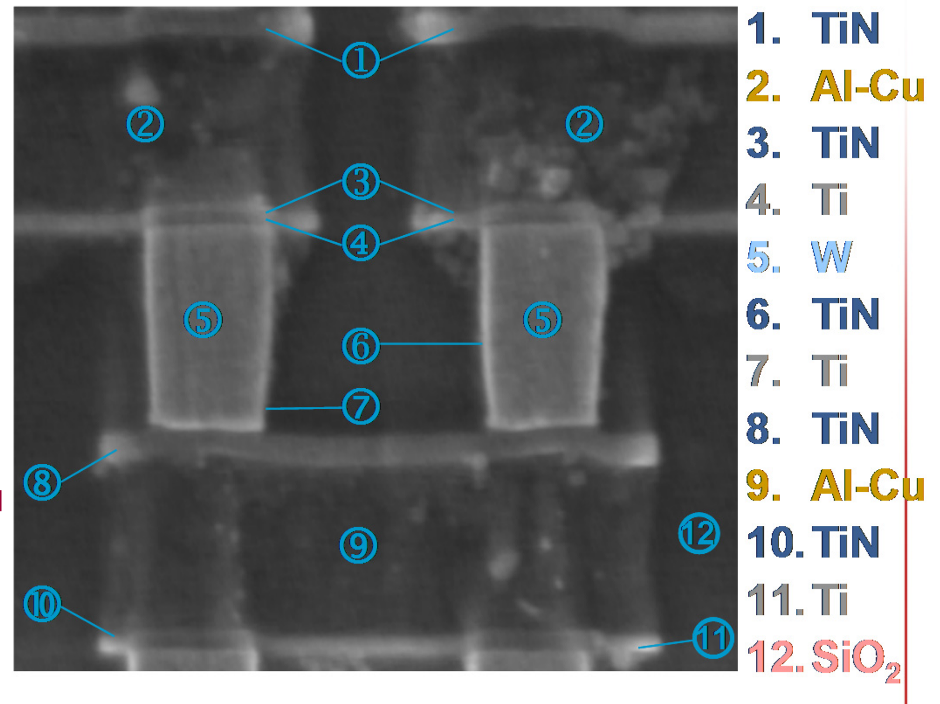
Input: material properties and boundary conditions.

- ***High fidelity is achieved via rigorous approach to each step.***
- **Iterate steps and refine model to achieve desired solution accuracy and robustness (design feedback).**

Example: A Back-end-of-the-line Via Chain

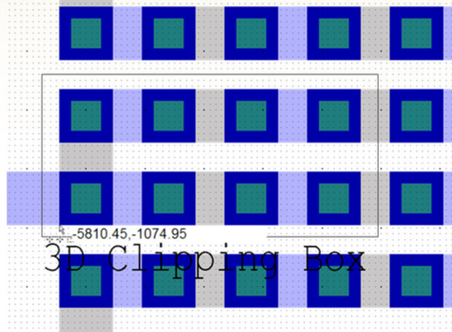
- We want to estimate fabrication-induced stresses of BEOL via chain.
- Vias 1 µm deep, 0.5 µm diameter; wires 0.7 µm deep.

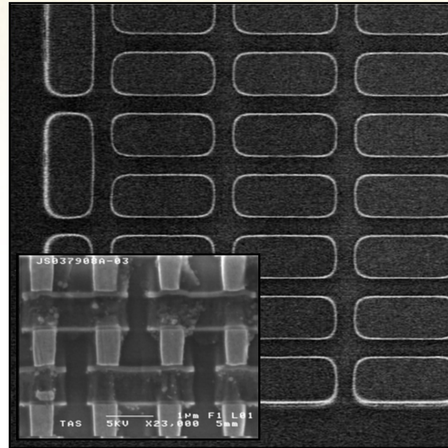


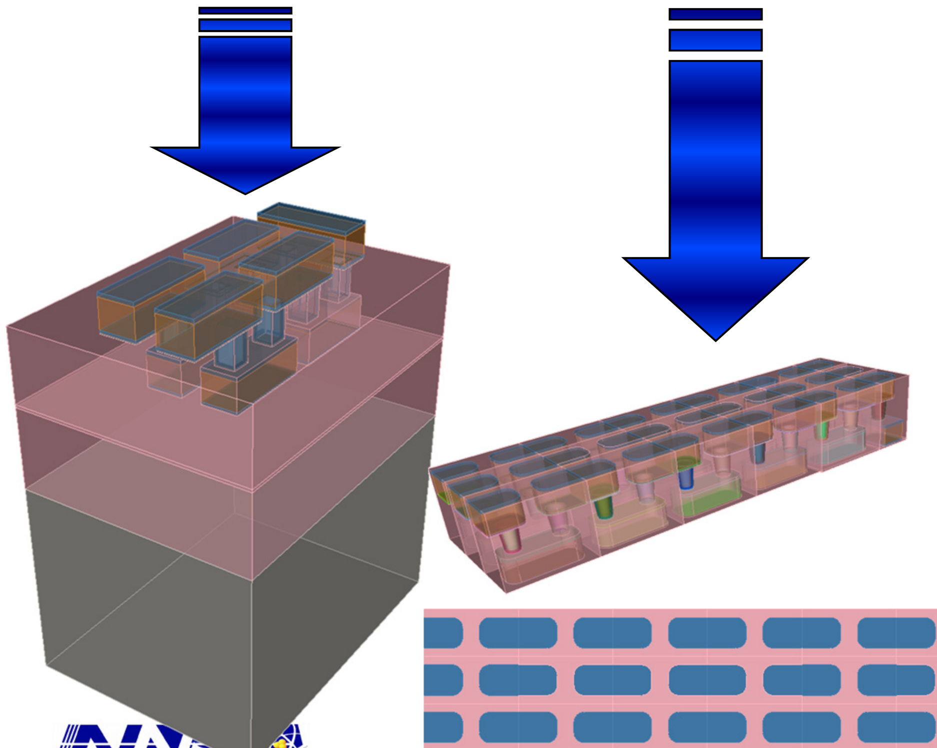


Step 1: Generate Accurate 3D Model

Sandia 3D Geometry Modeler

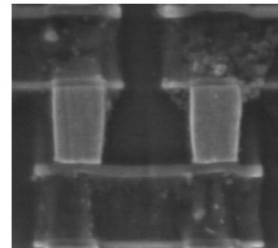


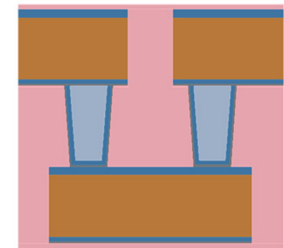


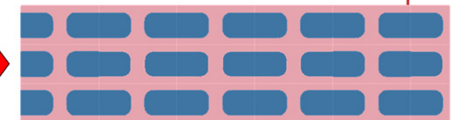


- Geometry built using fabrication process definitions.
- Modified to match *as-fabricated* geometry (SEM).
- Geometry parameterized to account for variations.

Actual **Simulated**

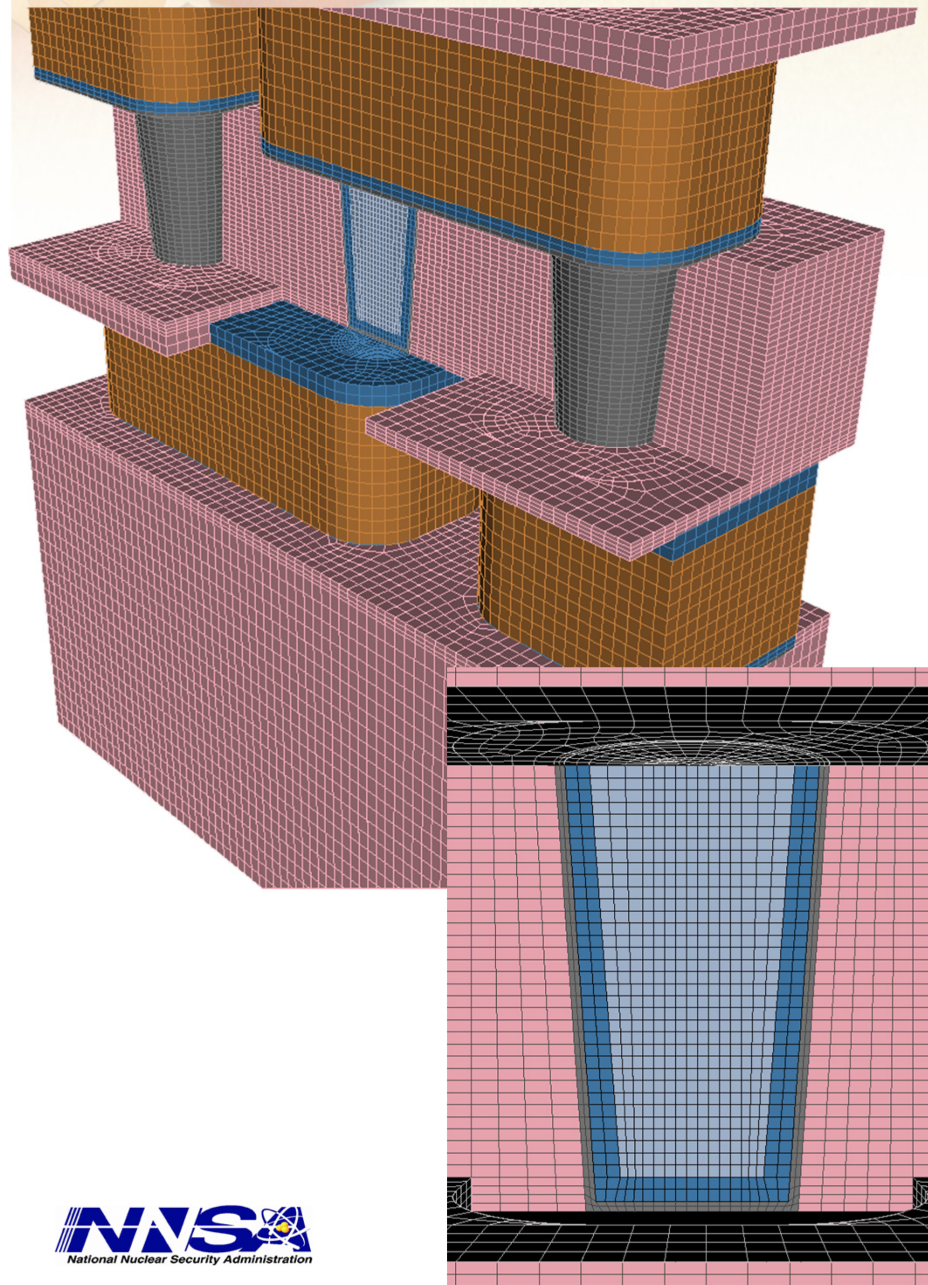






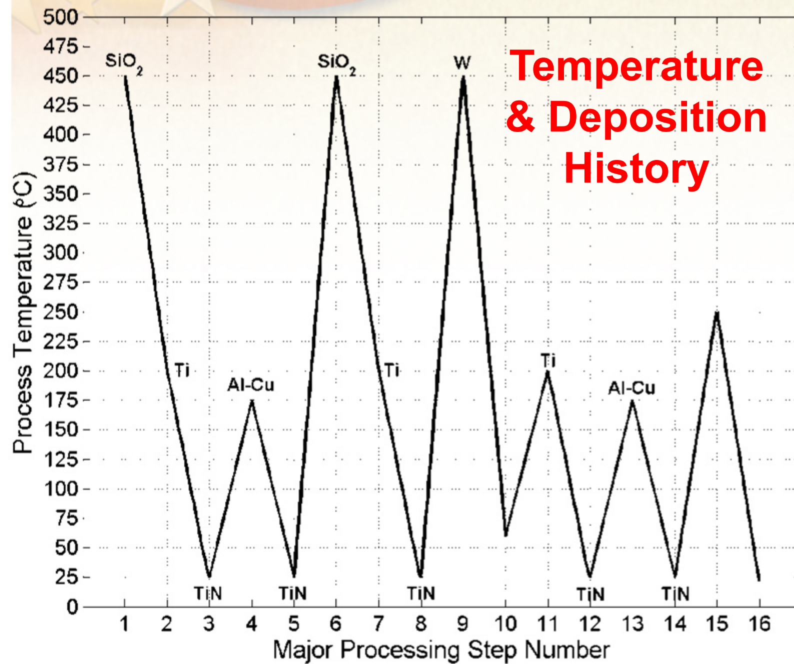
Features range from 20 nm to 10000 nm thick.

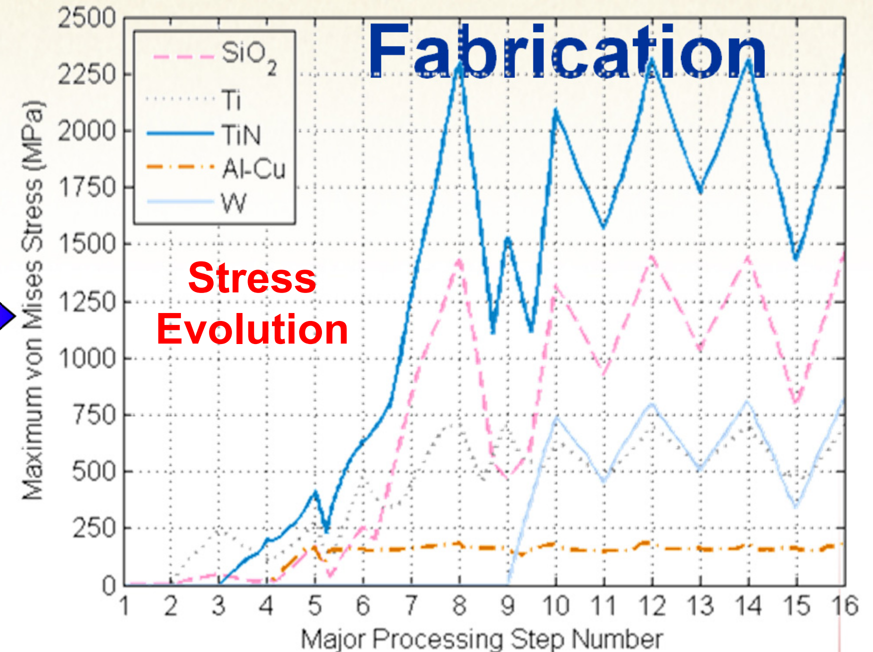
Step 2: Generate Detailed Mesh



- Use 8-node HEX elements: superior for stresses in layered structures.
- Requires geometry decomposition to enable contiguous meshing.
- Good element aspect ratio over all feature sizes.
- Created smallest elements in critical interconnect (via) regions
- Ultimately yields dense mesh (quarter-million elements).

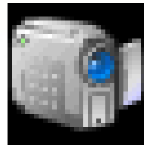
Model Results: Effects of Fabrication





- **Numerically instantiate finite elements at step when their associated layers are deposited.**
- **Evolution of peak von Mises stress, a measure of distortion energy, in each material.**
- **Zero stress plotted where material does not exist; plateaus indicate relaxation due to yield.**

Evolution of Stress During Fabrication



Fabrication Animation

Fabrication Stresses (Cross Section)

Summary

- FEOL metalized TSV processing provides very high density vertical interconnects for 3D integration.
- Established front-end fabrication processes can be used thus increasing yields, interconnect performance and their reliability.
- High density, high aspect ratio TSVs enable easier integration into 3D structures.
- Complementary modeling provides critical design support and will lead to devices with optimal performance and reliability.