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Silicon Nanowire Pirani Sensor Fabricated Using FIB Lithography

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As radio frequency microelectromechanical systems (RF-MEMS) mature as a manufacturable technology, packaging of the devices becomes increasingly important. Devices such as aluminum nitride (AlN) RF-filters require packaging which is either hermetic or under vacuum to protect the devices [1]. It then becomes critical to have a measurement of pressure inside the packaged chamber. Typically for this need, pirani gauges are fabricated using poly silicon or metal patterned on suspended membranes [2]. These type of devices increase die area, add complexity to fabrication flows, and difficulty when attempting to suspend the membranes. In this work we fabricate and characterize a suspended silicon nanowire for use as Pirani gauge by utilizing Ga lithography and plasma reactive ion etching for defining the nanowire geometry and simultaneously releasing the wire. This method benefits from the high surface to volume ratio inherent in the nano regime, decreased thermal conductivity of amorphous silicon (from implantation) and increased electrical conductivity of Ga doping to reduce device area and fabrication complexity of a Pirani gauge.

The nanowires are lithographically defined by implanting Ga, not milling, on SOI chips (500 nm 20 ohm-cm device layer on 3 um silicon dioxide) using a focused ion beam (FIB). The Ga is implanted, using a 30 KeV voltage, 25 nm deep into the silicon creating a 20 nm thick Ga-Si layer of 5 to 8 x 10^{16} cm^{-2} dosing. Since the Ga beam is focused down to a 15 nm beam waist, structures as small as 30 nm can be patterned in times comparable to electron beam lithography write times [3]. Following implantation, the chips are anisotropically plasma etched in an ICP-RIE (inductively coupled plasma reactive ion etcher) using a SF_6/C_4F_8 mixed mode etch chemistry. This etch defines the nanowire and contact pads; here we utilize a 100 nm by 2 um and 130 nm by 10 um nanowire between two contact pads of 50 um diameters. Following this etch the plasma is transitioned into a short SF_6 isotropic etch which undercuts and releases the nanowire up to implanted region. The resulting structure is a 50 um by ½ um tall pillars, separated by 10 um with a suspended nanowire of 10 um by 100 / 130 nm by 20 nm thick at ½ um above the oxide substrate, fig 1 and fig 2.

The wires were electrically characterized in a Lakeshore Cryostat/probe station. Resistivity as a function of temperature was measured using a Keithley 487 pico-ammeter / voltage source. When sourcing 100 nA, a 130 nm x 20 nm nanowire exhibited a 0.13 Ohm-cm resistivity at room temperature, fig 3. A 100 nm x 20 nm x 2 um and a 130 nm x 20 nm x 10 um nanowires were then measured as pressure was varied in the probe station with the stage temperature maintained at 293 K, fig 4 and 5. The pressure was measured using a pressure gauge attached to the main chamber and pressure was modulated by throttling air into the chamber and waiting an equalization period. At each pressure level, the 130 nm nanowire was measured at 1, 2 and 3 volts where the supplied power induced more heating, and hence higher resistivity change in the nanowire; this changed the sensitivity of the nanowire to pressure. Both nanowires demonstrated dependence on pressure in the 10^{-1} to the 10^{2} Torr ranges (3 orders of magnitude) and are modeled using a closed form solution to the heat equation [2,4]. With a 80 second FIB write time and 71 second plasma etch, Pirani gauge silicon nanowires are quickly created with usable pressure ranges from 100 mTorr to 100 Torr.

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[1] M. D. Henry, K. D. Greth, J. Nguyen, C. D. Nordquist et al., "Hermetic Wafer-Level Packaging for RF MEMs: Effects on Resonator Performance," IEEE 62ND Electronic Components and Technology Conference, 2012.
[2] C.H. Mastrangelo and R.S. Muller, "Microfabricated Thermal Absolute-Pressure Sensor with On-Chip Digital Front-End Processor," IEEE Journal of Solid State Circuits, Vol.25, No.12, 1991.
[3] M. D. Henry, M. J. Shearn, B. Chhim, and a Scherer, "Ga(+) beam lithography for nanoscale silicon reactive ion etching.," Nanotechnology, vol. 21, no. 24, p. 245303, 2010.
[4] T. Brun, D. Mercier, A. Koumel, C. Maroux, and L. Duraffourg, "Silicon nanowire based Pirani sensor for vacuum measurements," APL, 101, 183506, 2012.

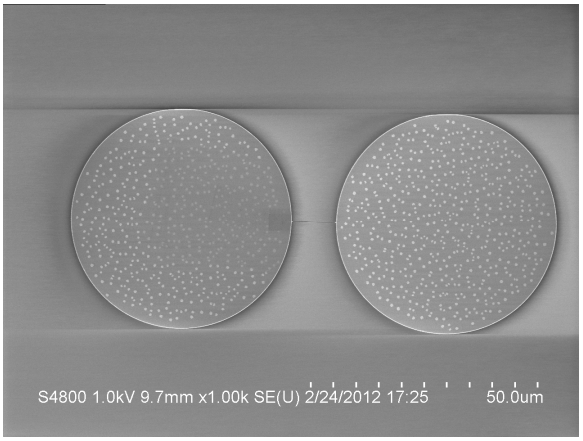

Figure 1. SEM of contact pads and suspended Ga masked silicon nanowire.

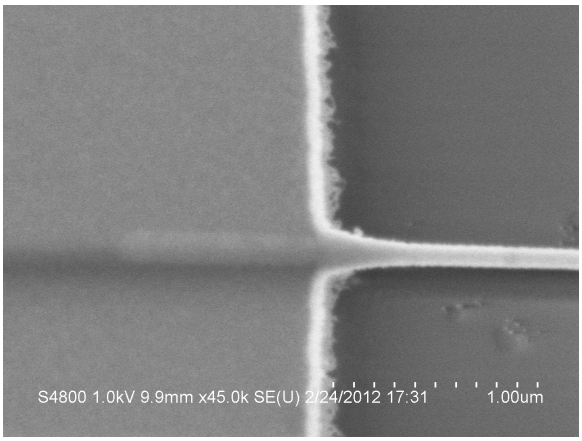

Figure 2. SEM of contact pad (left) and suspended nanowire (right).

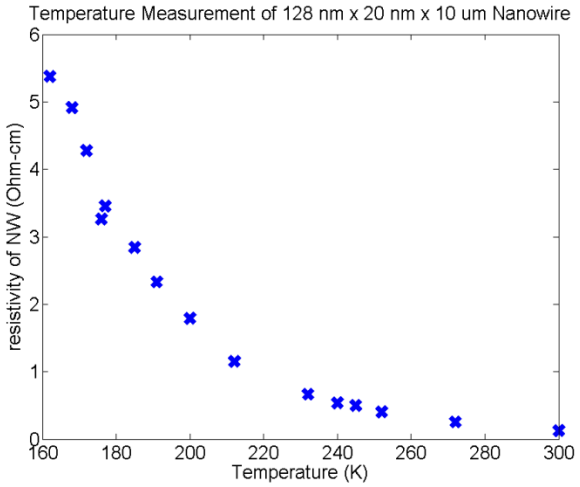

Figure 3. Resistivity dependence on temperature of a suspended 130 nm x 20 nm x 10 um silicon nanowire.

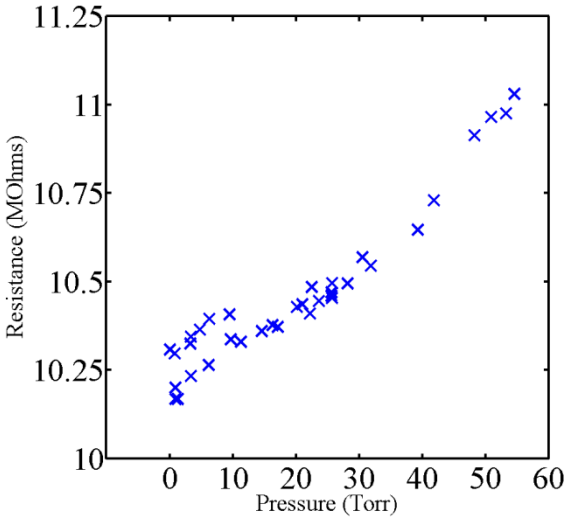

Figure 4. Graph of resistivity vs pressure for a suspended 10 nm x 20 nm x 2 um silicon nanowire measured at 1, 2 and 3 volts bias. Implanted dose was 8 x 10^{16} cm^{-2}.

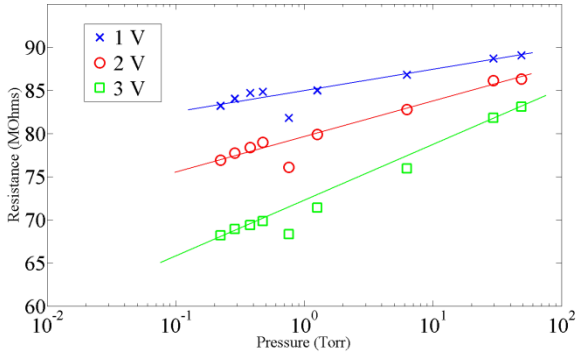

Figure 5. Graph of resistivity vs pressure for a suspended 130 nm x 20 nm x 10 um silicon nanowire measured at 1, 2 and 3 volts bias. Implanted dose was 5 x 10^{16} cm^{-2}.