



Development of Dual-Gated Bilayer Graphene Device Structures

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Sandia National Laboratories



Acknowledgements

■ Internal Graphene Team

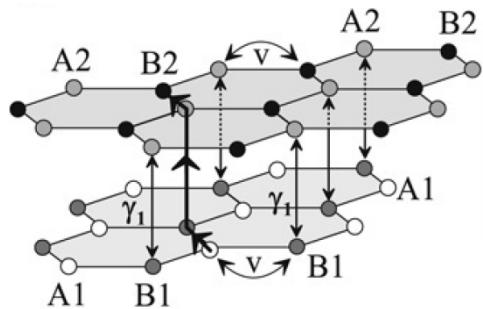
- Stephen W. Howell
- Thomas Beechem
- Allister Hamilton
- Khalid Hattar
- Taisuke Ohta

Roles

- PI, Device Design, Electrical Characterization
- Raman Spectroscopy
- Fabrication
- Ion Implantation
- Graphene Synthesis, LEEM-PEEM

Tunability via *Bilayer* Graphene (BLG)

BLG Structure (Bernal stacking)



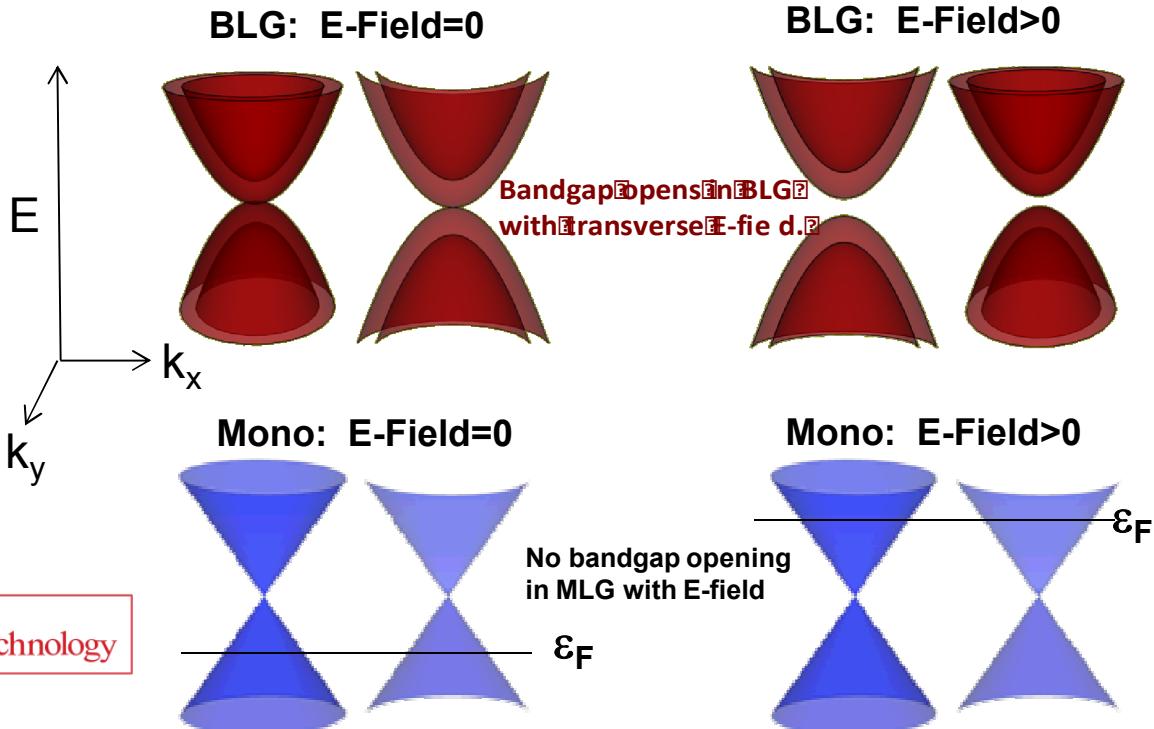
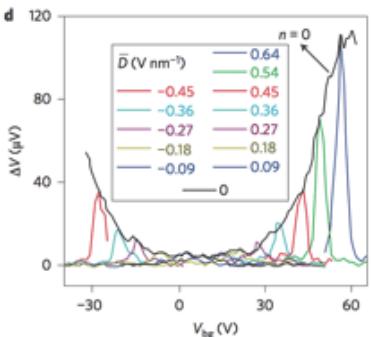
ARTICLES

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*nature
nanotechnology*

Dual-gated bilayer graphene hot-electron bolometer

Jun Yan^{1,2}, M-H. Kim^{1,2}, J. A. Elle^{2,3}, A. B. Sushkov^{1,2}, G. S. Jenkins^{1,2}, H. M. Milchberg^{2,3}, M. S. Fuhrer^{1,2*} and H. D. Drew^{1,2}



nature

Vol 459 | 11 June 2009 | doi:10.1038/nature08105

LETTERS

Direct observation of a widely tunable bandgap in bilayer graphene

Yuanbo Zhang^{1*}, Tsung-Ta Tang^{1,*†}, Caglar Girir¹, Zhao Hao^{2,4}, Michael C. Martin², Alex Zettl^{1,3}, Michael F. Crommie^{1,3}, Y. Ron Shen^{1,3} & Feng Wang^{1,3}

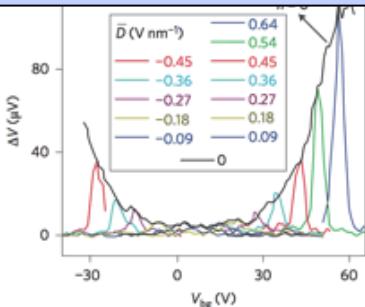
Tunability via *Bilayer* Graphene (BLG)

BLG Structure (Bernal stacking)

BLG: E-Field=0

BLG: E-Field>0

- BLG could enable real-time reconfigurable device concepts
- Potential disruptive applications:
 - Reconfigurable “tunable” optoelectronics
 - THz IR detector, IR filters and metamaterials
 - High-speed memory
 - Quantum devices (Qubits)
 - Graphene photonics

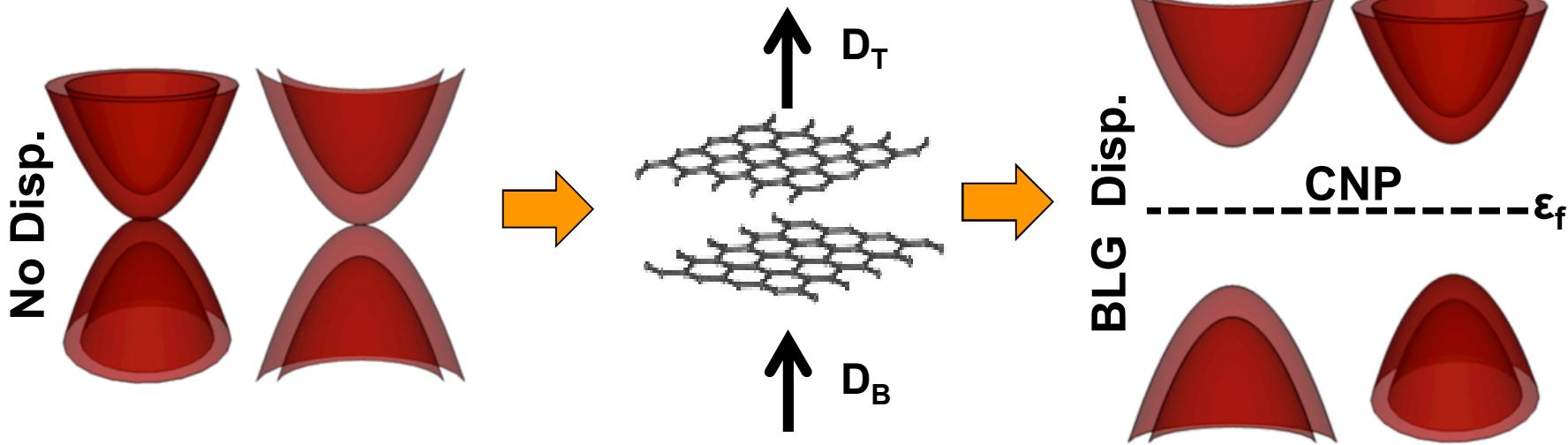


LETTERS

Direct observation of a widely tunable bandgap in bilayer graphene

Yuanbo Zhang^{1*}, Tsung-Ta Tang^{1*†}, Caglar Girir¹, Zhao Hao^{2,4}, Michael C. Martin², Alex Zettl^{1,3}, Michael F. Crommie^{1,3}, Y. Ron Shen^{1,3} & Feng Wang^{1,3}

Bandgap Creation in Bilayer Graphene



$$\delta D = D_B - D_T \rightarrow \text{Charge}$$

$$D_{\text{ave}} = (D_B + D_T)/2 \rightarrow \text{Breaks Symmetry}$$

$$D_B = \epsilon_B (V_B - V_B^\circ)$$

$$D_T = \epsilon_T (V_T - V_T^\circ)$$



Environmental Offsets (Doping)

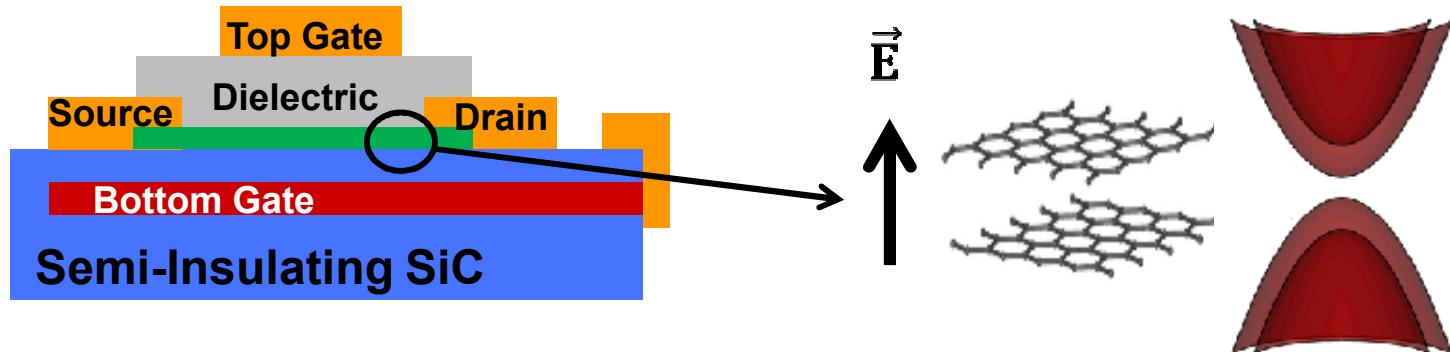
A combination of displacements (top & bottom gates) are needed to:

- Induce a bandgap
 - $D_{\text{ave}} \neq 0$
- Control Fermi Level (ϵ_f) to charge neutrality point (CNP)
 - $\delta D = 0$



Scalable Approach for Creating Dual-Gate BLG Device Structures

- **Problem:** To take full advantage of the possibilities that BLG offers, new techniques must be found to reproducibly fabricate arrays of BLG devices
 - **Current state-of-the-art:** BLG devices fabricated from exfoliated flakes of graphite
- **Sandia's Approach:** Use standard lithographic tools and processes to make arrays of BLG devices on the chip/wafer-scale
 - Develop chip-scale BLG synthesis on SiC
 - Create a back-gate in semi-insulating SiC using ion implantation
 - Creating a back-gate in semi-insulating SiC is very difficult

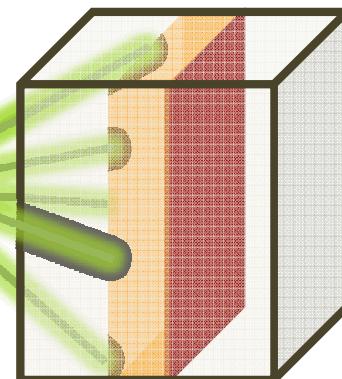


3 MeV Nitrogen Implants to Form a Back-Gate in SiC

3 MV NEC
Pelletron

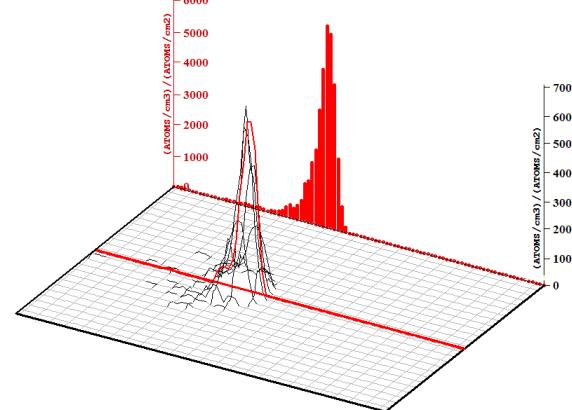


SiC
Sample

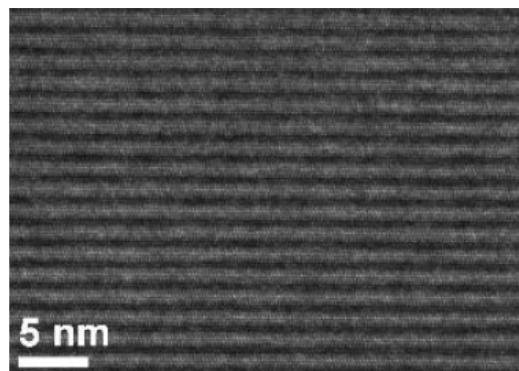


TRIM Simulation of Blanket
Implant Depth Distribution

Ion Range = 1.00 um Skewness = -2.803
Straggle = 871 Å Kurtosis = 18.530

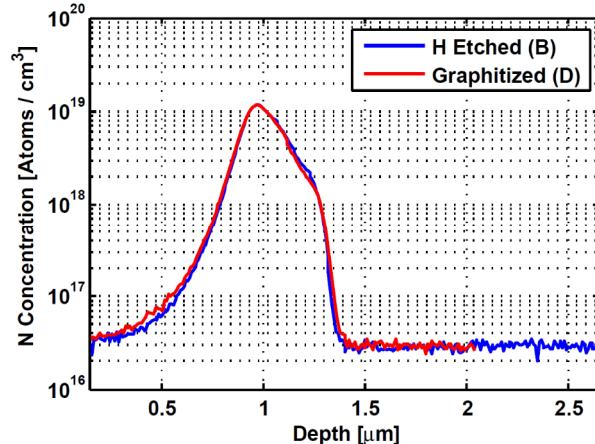


TEM Validation of
Microstructure



Tailored ion implantation provides both back gate and side contact structure

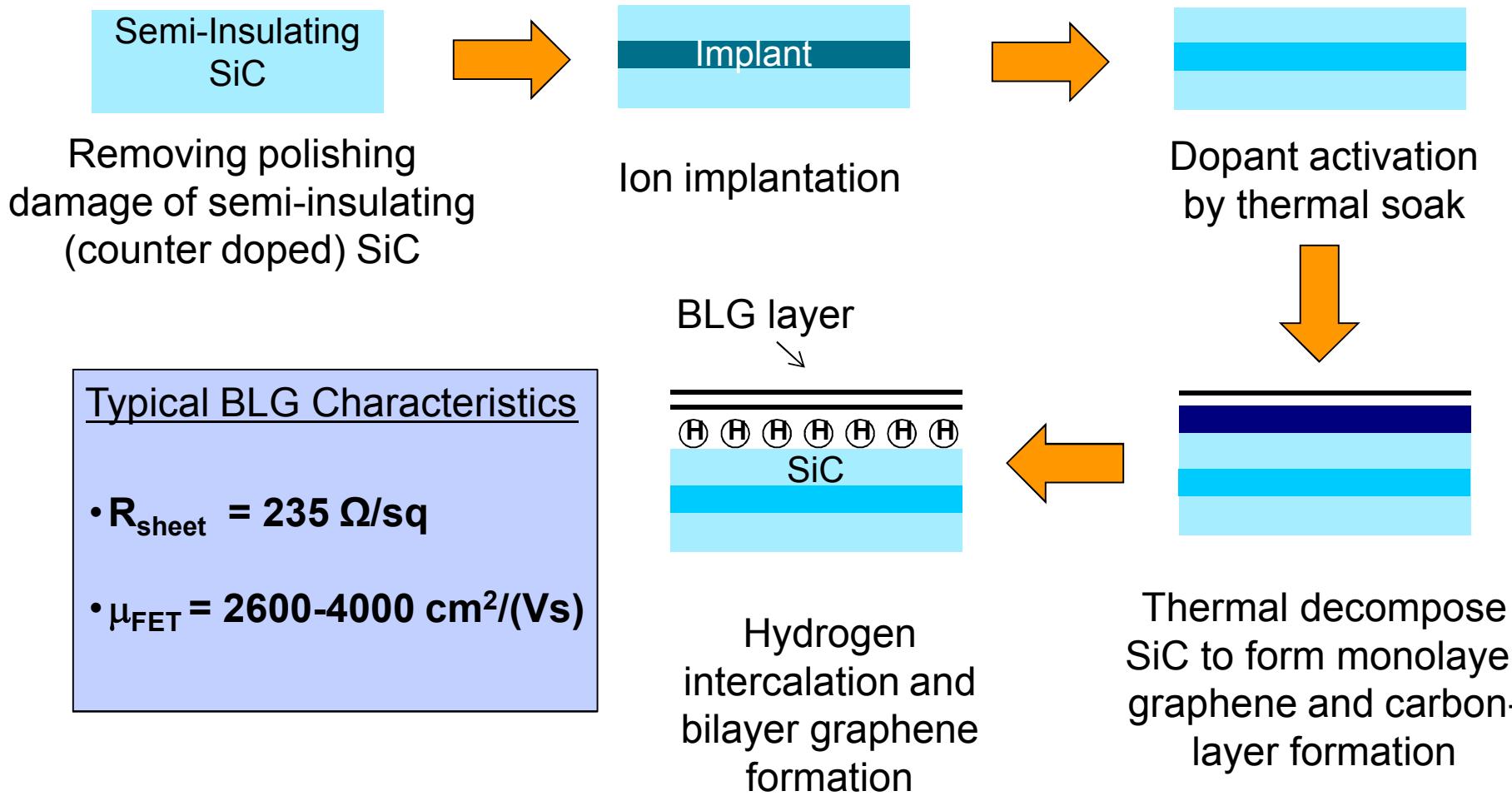
Validation of Implant Depth (SIMS)



Waldmann et al., Nature Materials, 10, 357 (2011)

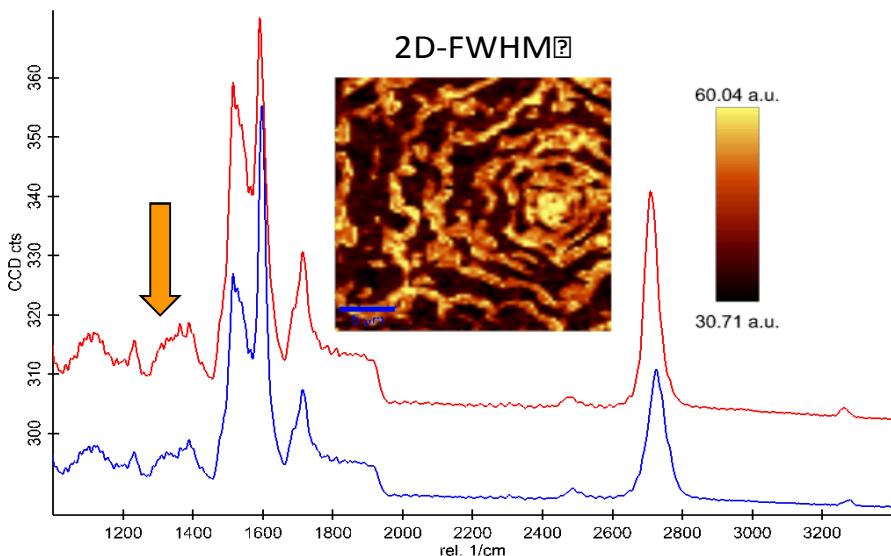
Chip-Scale Bilayer graphene synthesis on ion-implanted SiC

■ Process flow for chip-scale BLG synthesis on semi-insulating 6H-SiC (0001)

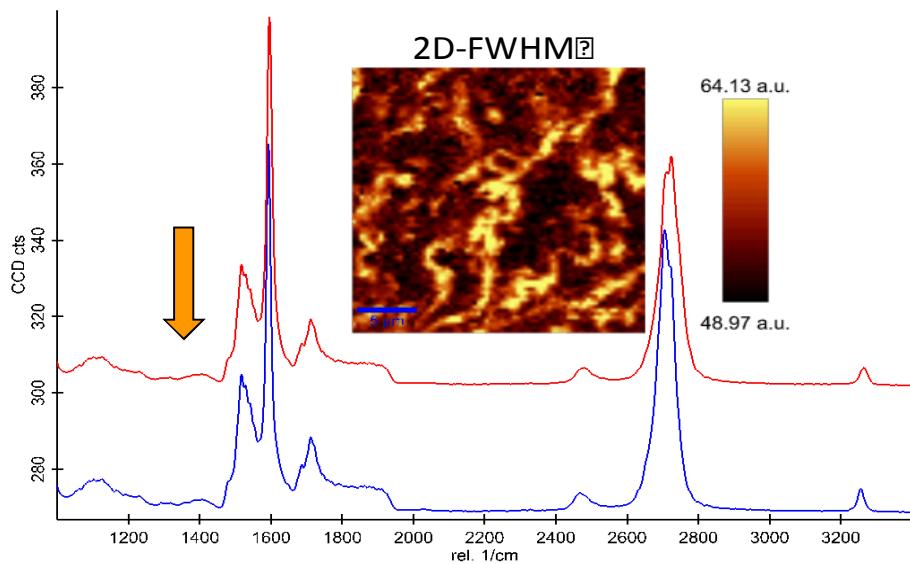


Raman Characterization During BLG Synthesis Process

Monolayer growth after implant



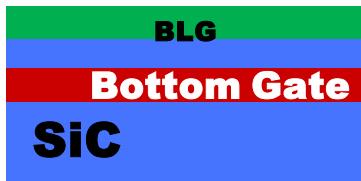
Bilayer growth after implant



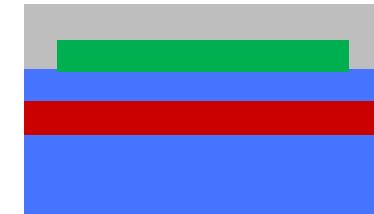
- Raman indicates:
 - Ion implantation does not prohibit high quality BLG growth on the SiC surface
 - minimal defects observed(minimal D peak at 1350 cm⁻¹)

Device Fabrication

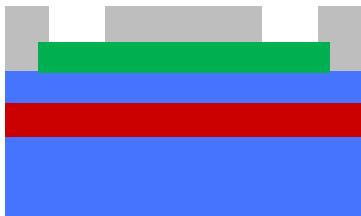
- Devices are fabricated using optical lithography



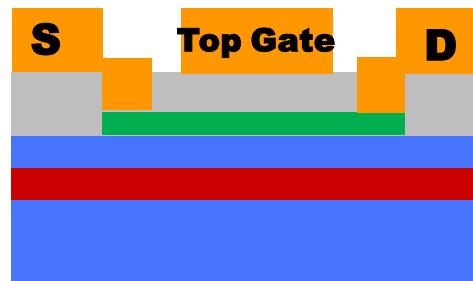
Isolate graphene



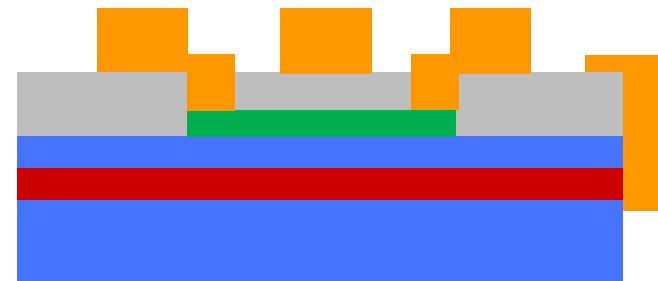
CVD SiO₂ deposition
(100 nm)



Etch vias to graphene



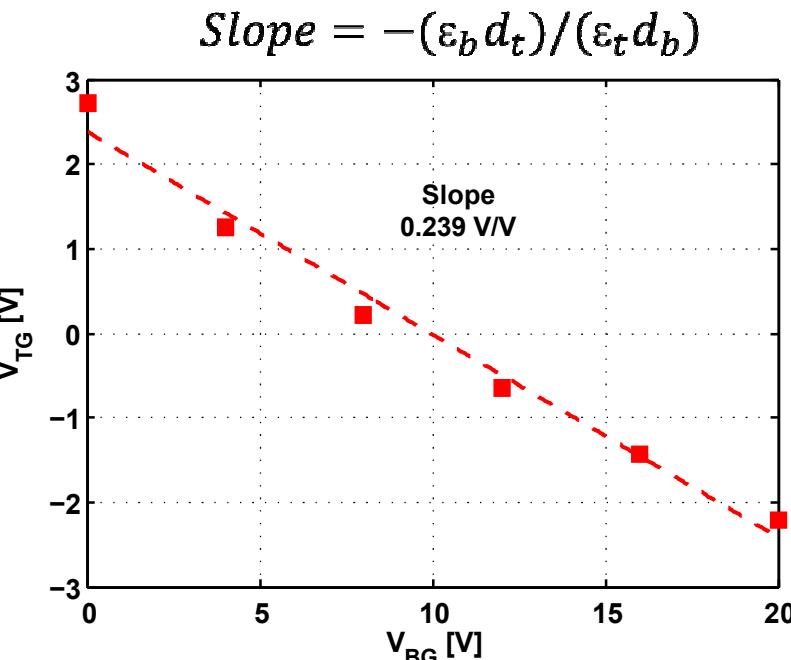
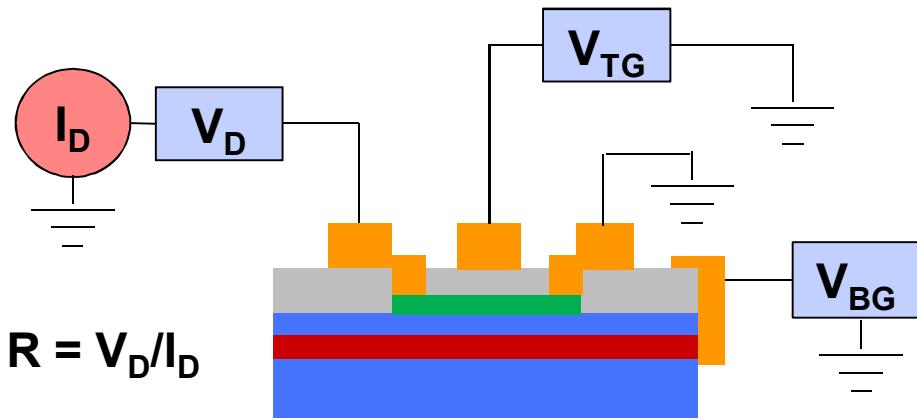
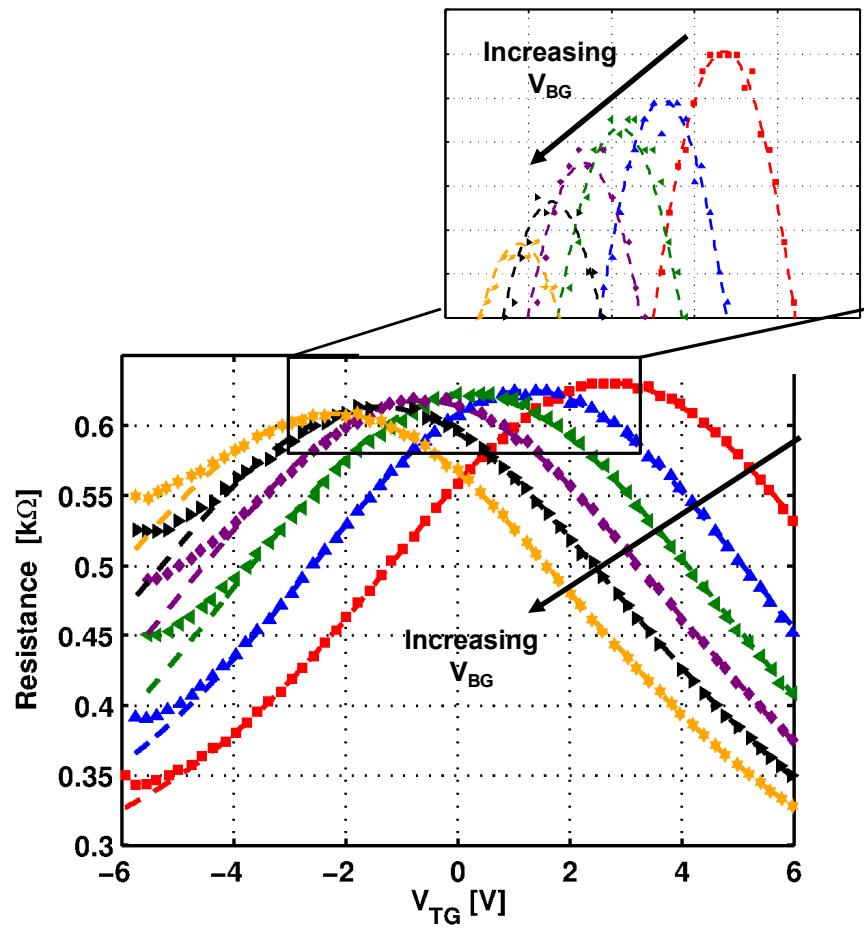
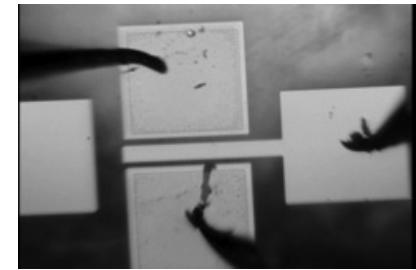
Deposited metal contacts



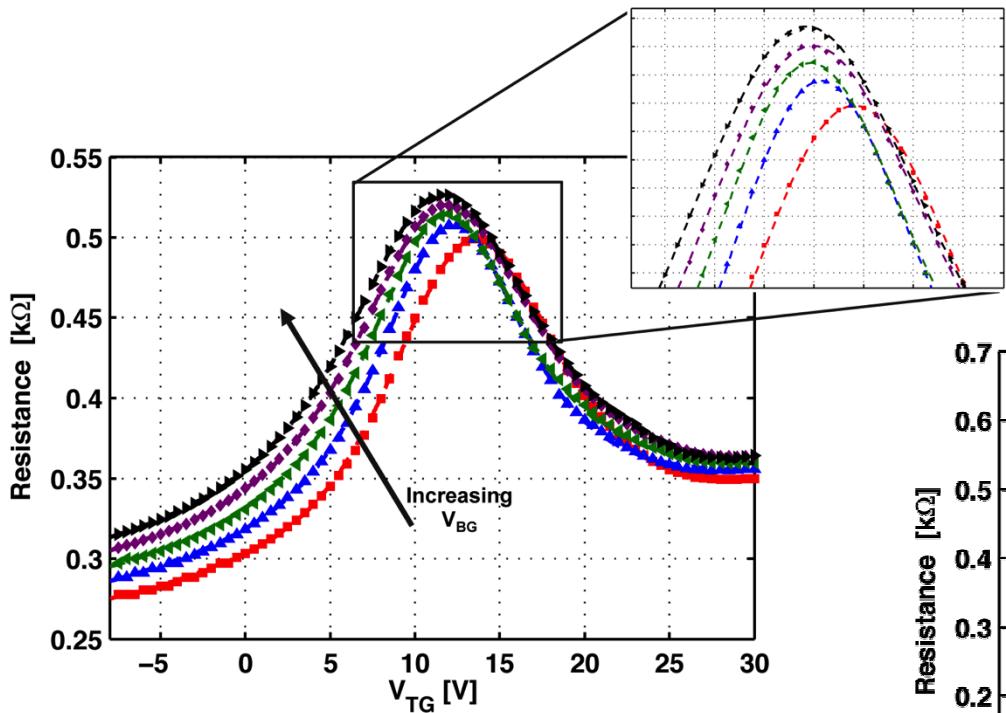
Deposited back-gate contacts

Bandgap Control via Dual Gating

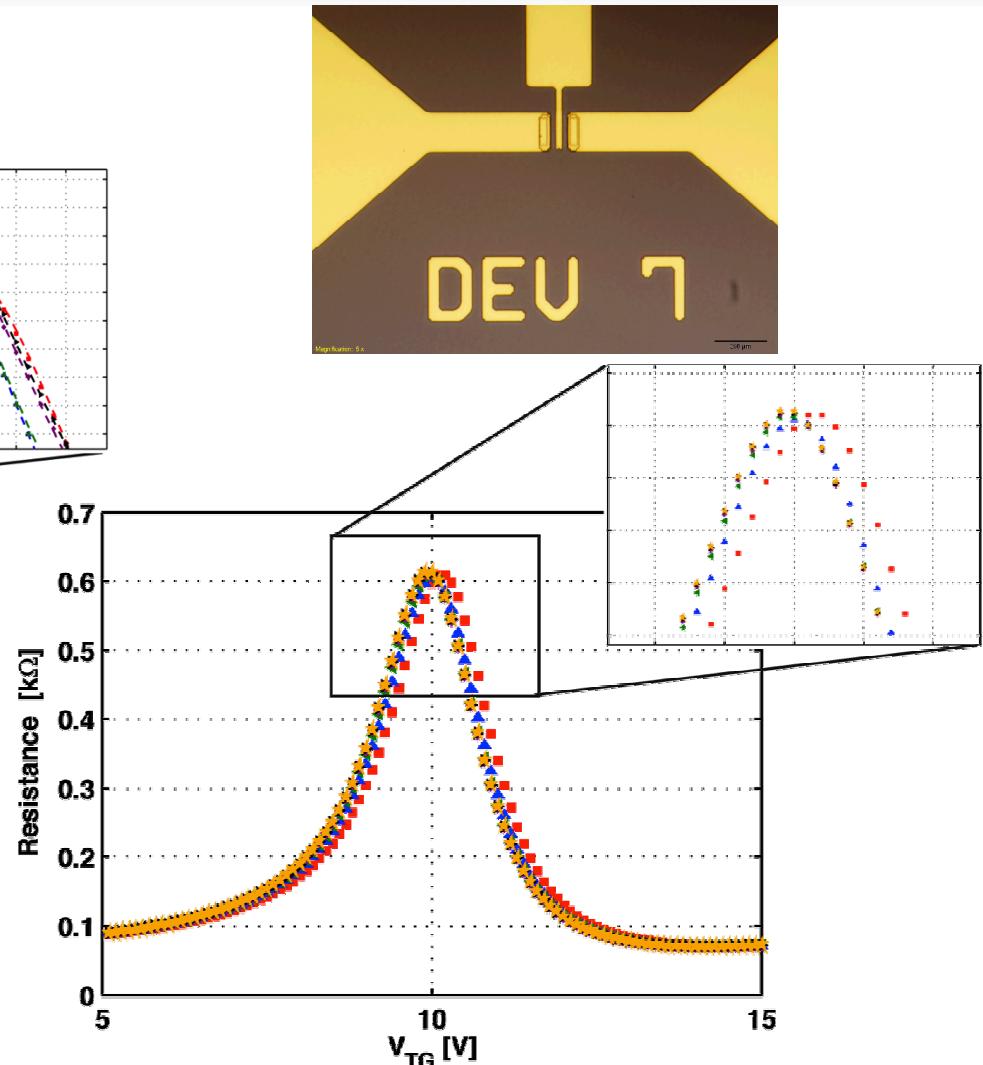
(1st Demonstration of scalable dual-gate BLG FETs)



Typical Dual-Gated BLG FET Electrical Response



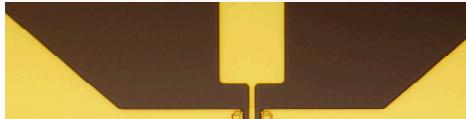
$V_{BG} = 0$ V to 20 V in 5 V Steps



$V_{BG} = 0$ V to 0 V in 0 V Steps

No change in resistance due to hysteresis!

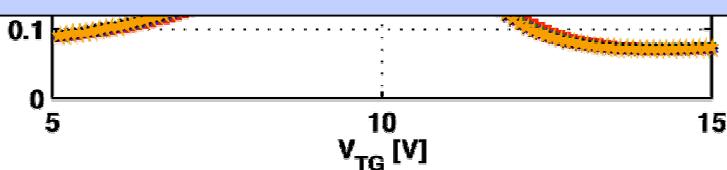
Typical Dual-Gated BLG FET Electrical Response



Resistance [$\text{k}\Omega$]

- Similar dual-gated response was observed for multiple devices fabricated on several different chips

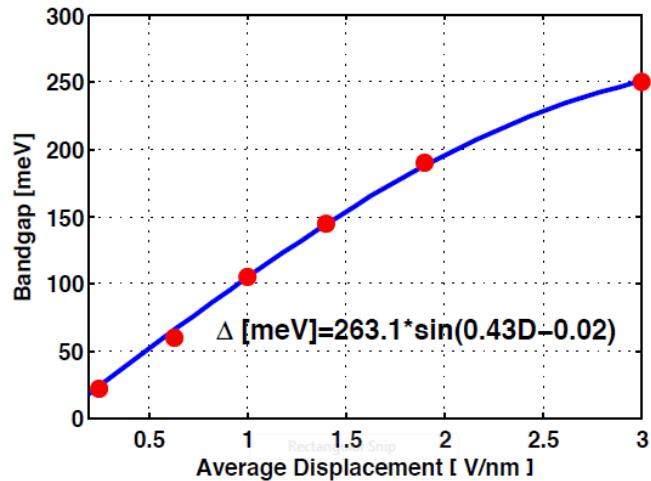
$V_{BG} = 0 \text{ V to } 20 \text{ V in } 5 \text{ V Steps}$



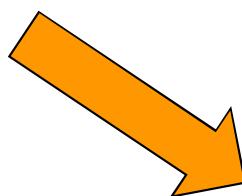
$V_{BG} = 0 \text{ V to } 0 \text{ V in } 0 \text{ V Steps}$
No change in resistance due to hysteresis!

Estimating Bandgap Modulation

Bandgap as a function of D_{ave}



V_T [V]	V_T° [V]	V_B [V]	V_B° [V]	ϵ_T	d_T [nm]	ϵ_B	d_B [nm]
-30-30	12	-175-200	12	3.9	100	9.6	1000

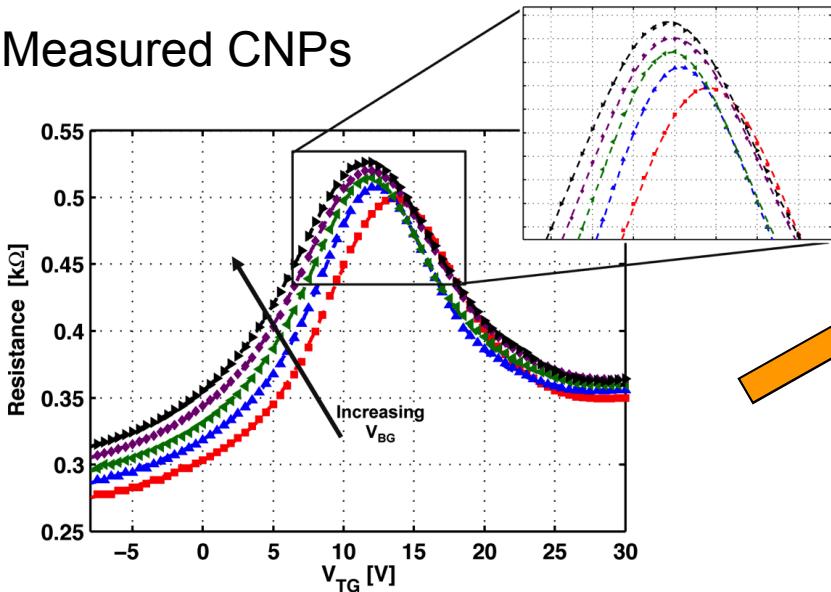


Estimates for BLG FETs

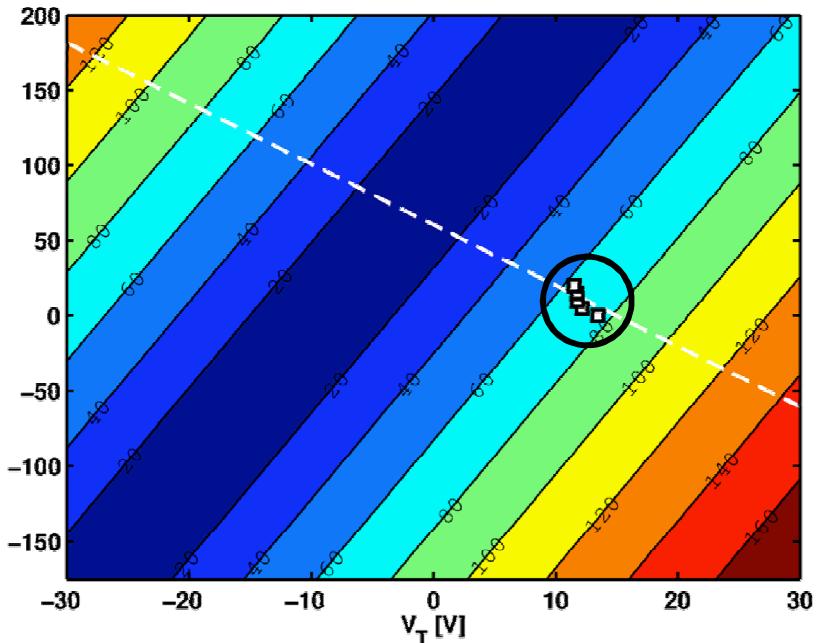


Bandgap Shift: ~ 20 meV

Measured CNPs

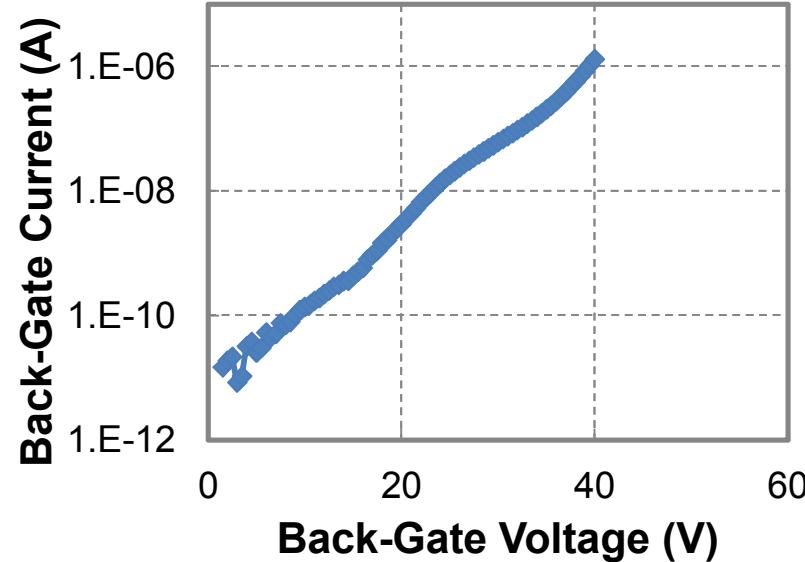
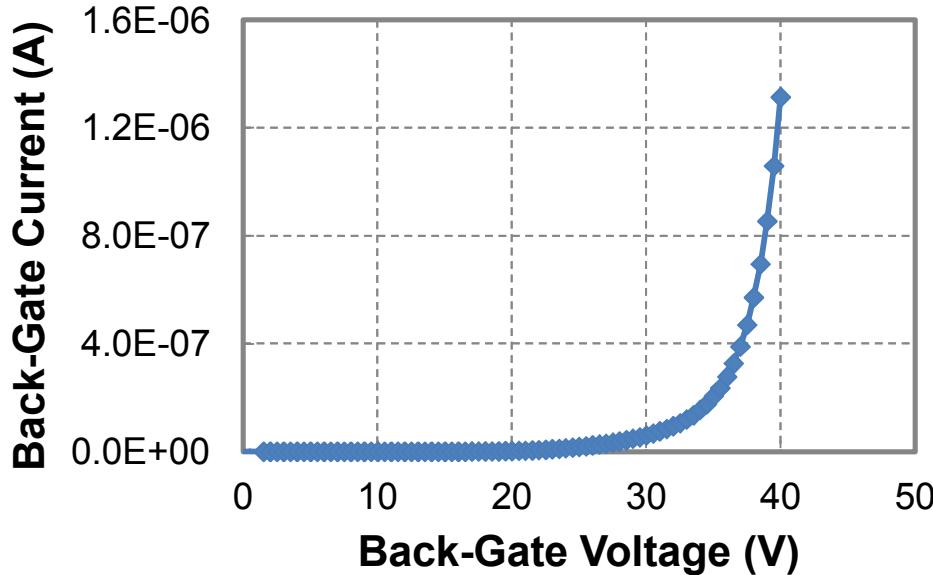


V_B [V]



*Adapted from Zhang et al.

Back-Gate Current Leakage



- The nitrogen (n-type dopant) implanted SiC forms a junction
 - The junction is reversed biased when $+V$ is placed on the back-gate implant
 - Large current flow when $-V$ is placed on back-gate implant
- Leakage from the back-gate limits the magnitude of the E field
- Work is ongoing to reduce this leakage



Conclusions

- The tunable electronic properties of bilayer graphene could enable new types of devices
 - Impacting applications from optoelectronic to quantum information
- To take full advantage of what BLG offers, new synthesis and fabrication techniques must be developed to create a large number of devices with high yield
- At Sandia, we have:
 - Developed chip-scale BLG synthesis on 6H-SiC
 - Used ion implantation to form a back-gate in SiC
 - Demonstrated high quality BLG growth post implantation
 - Realized a scalable dual-gated BLG device architecture
 - Demonstrated bandgap modulation (~ 30 meV) in arrays of BLG FETs



Posting of Postdoctoral Position (Nano-Enabled Microelectronics:643878)

The listed posting:

http://www.sandia.gov/careers/students_postdocs/postdocs.html

Desired:

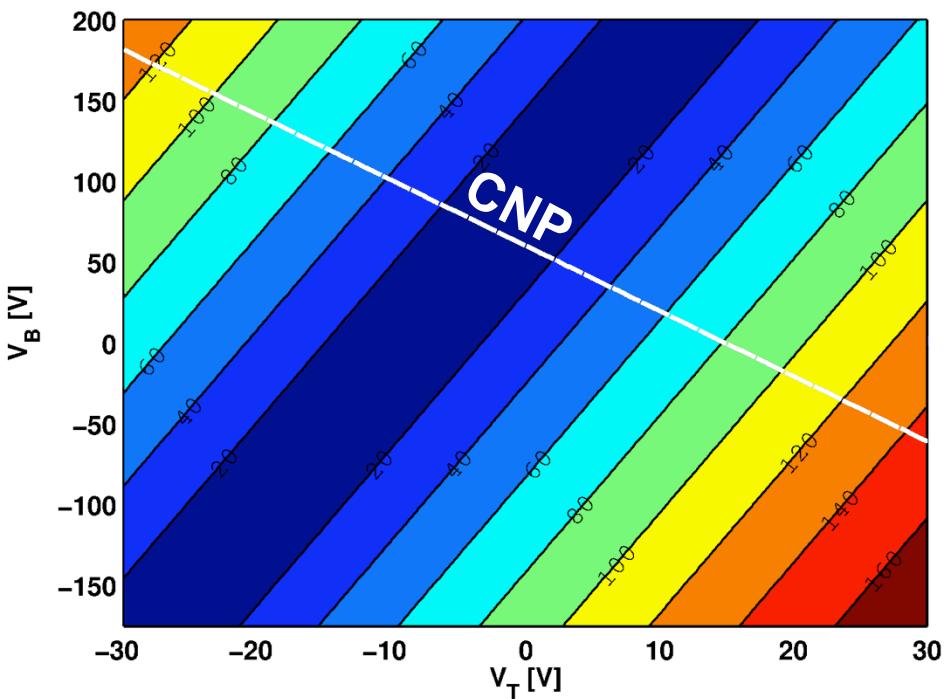
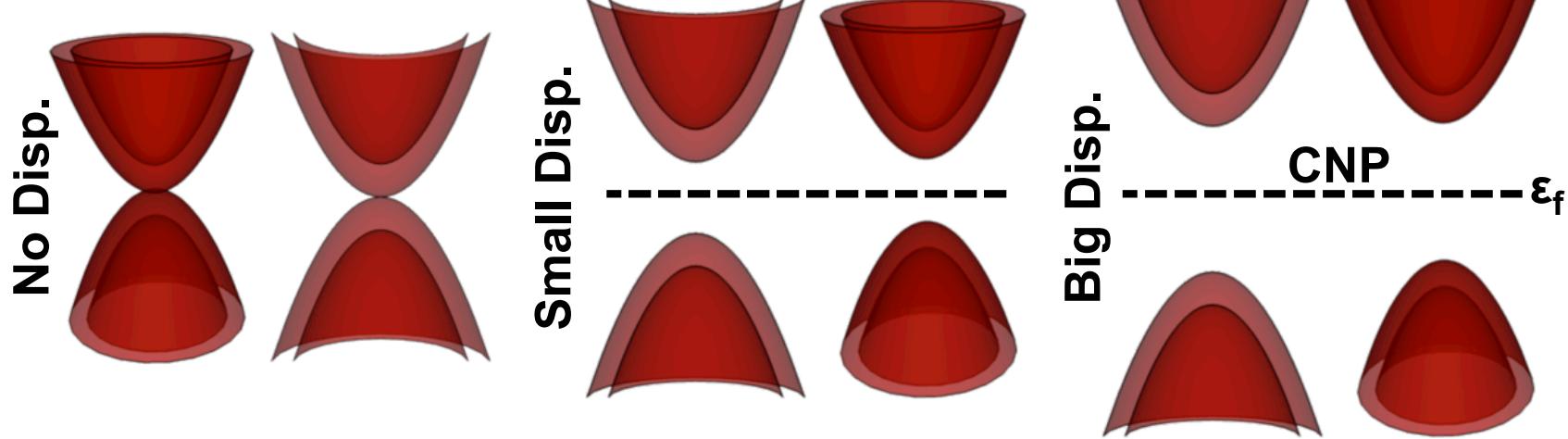
- An experimental background in scanning probe microscopy.
 - Tapping mode, scanning thermal microscopy, Conductive-AFM, near-field radiative heat transfer, Casimir force measurements, etc.
- An experimental background in Graphene and Carbon Nanotube research.
- Ability to work well in a dynamic, large, and multi-disciplinary research team environment.
- A willingness to learn new experimental techniques.
- Extensive experience in the design, fabrication, assembly, and/or characterization of micro/nano-scale systems.
- Experience in industrial, government, or other laboratory environments outside the academic community.



Additional Slides



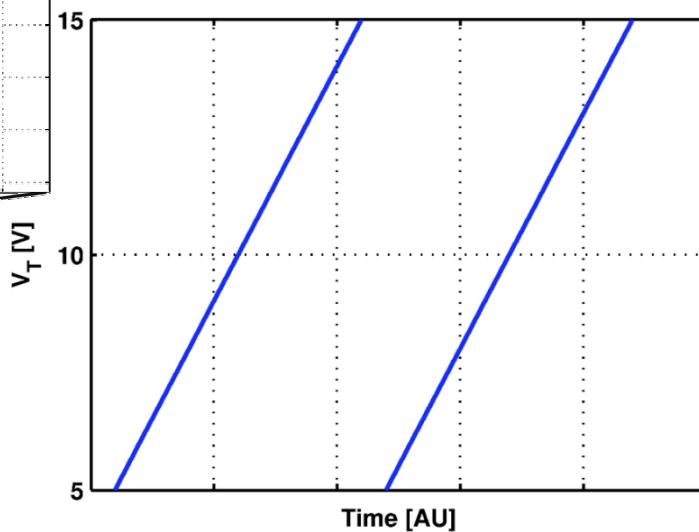
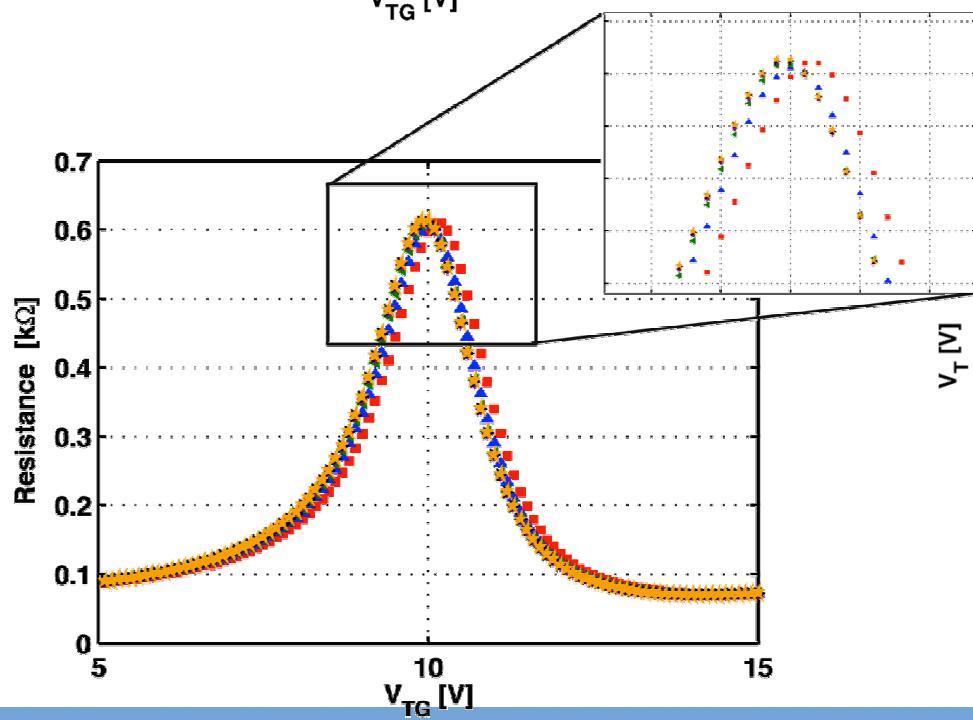
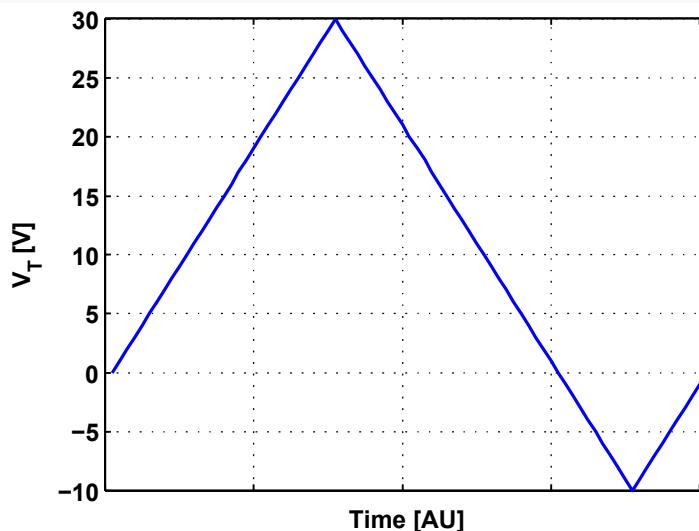
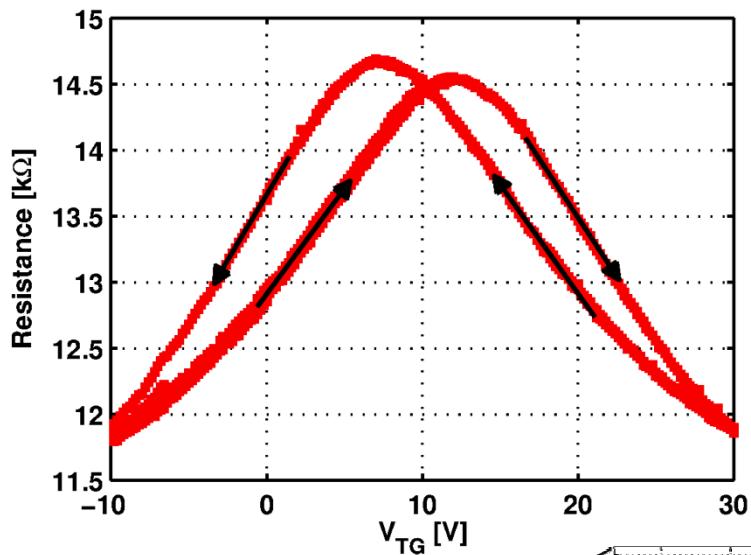
Bandgap Creation in Bilayer Graphene



A combination of electric displacements (top & bottom gates) are needed to:

- Induce bandgap
- Control Fermi Level (ϵ_f) to charge neutrality point (CNP)

Control Sweeps

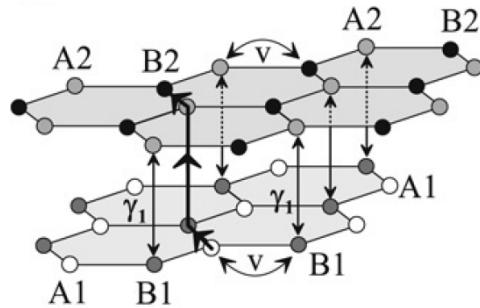




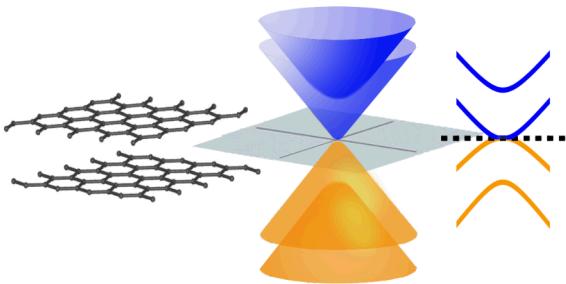
Bilayer Graphene (BLG): A Breakthrough for Tunable Bandgap Engineered Graphene Devices

BLG has a tunable bandgap in an electric field

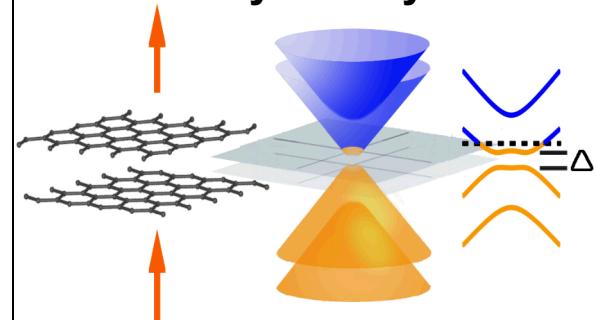
BLG Structure (Bernal stacking)



E Field = 0 Symmetric



E Field ≠ 0 Symmetry breaks



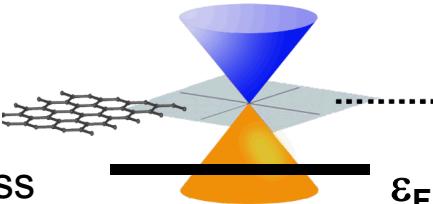
- BLG bandgap ranges from 0 – 250 meV (or higher?)

Large-area monolayer comparison

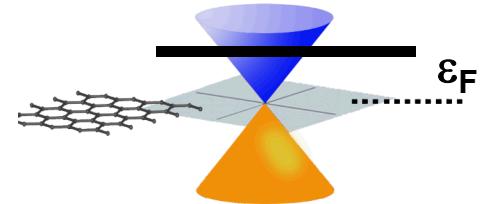
In presence of electric field:

- No bandgap opening
- Change in carrier concentration
- Change in carrier type (transition across Dirac point)

E Field = 0



E Field ≠ 0

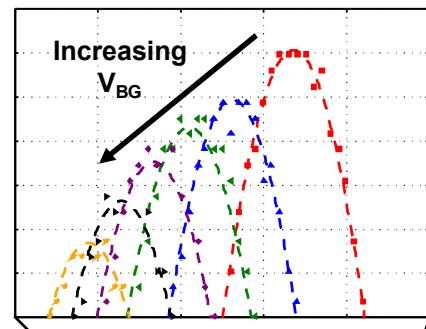
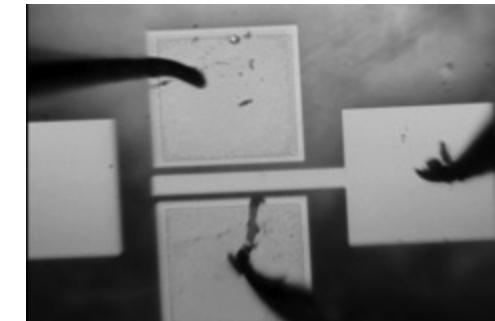
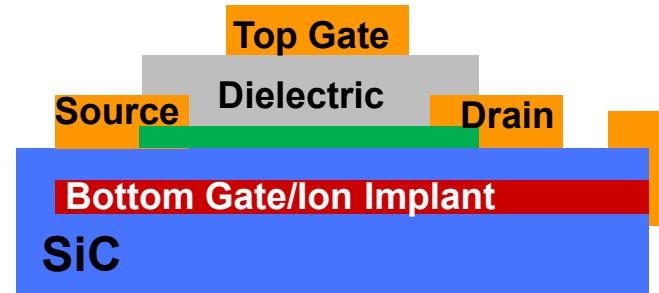
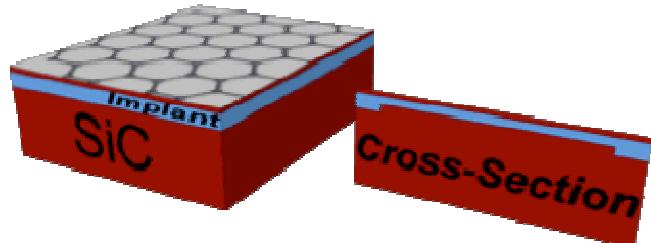


McCann *et al.* Solid State
Com. 143 110 (2007)

Optical measurement of the bandgap;
Zhang *et al.* Nature 459, 820 (2009)

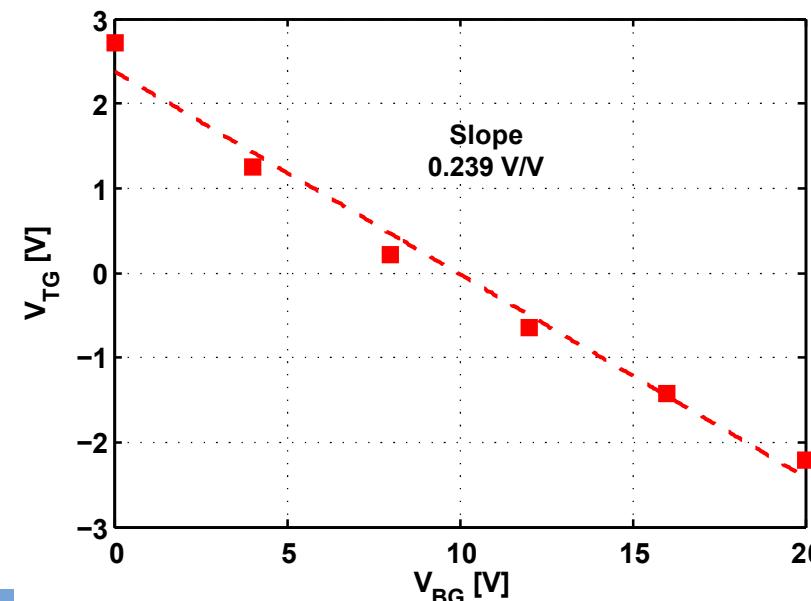
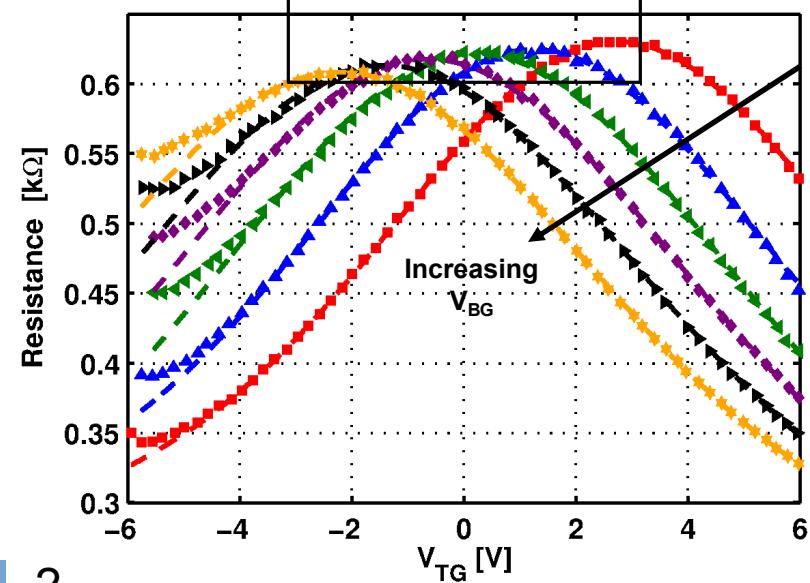
Bandgap Control via Dual Gating

(1st Demonstration of scalable dual-gating)



1st Demonstration of scalable dual-gating!

Invited Presentation SPIE NanoSci+Engineering:
Howell et al. *Development of dual-gated bilayer graphene device structures*. 2013





Acknowledgements

■ Internal Graphene Team

- Stephen W. Howell*
 - Allister Hamilton
- Carlos Gutierrez
- Taisuke Ohta*
- Kevin McCarty
- Thomas Beechem*
- Wei Pan
- François Leonard

Roles

- PI, Device Fab, Transfer
- PM
- SiC Synthesis, LEEM-PEEM
- CVD Synthesis, LEEM
- Raman Spectroscopy
- Low Temp Transport
- Optical Testing, Modeling

■ Internal Collaborators

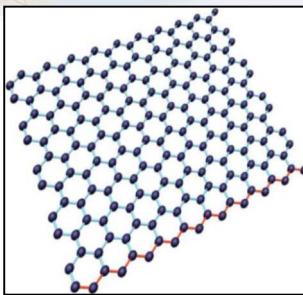
- Khalid Hattar, Eric Shaner, Igal Brenner, Paul Davids, Dave Peters*, Gary Kellogg, Young Jun, Greg Bogart, Larry Bacon, Gregg Wouters, Mike Siegal*, Matt Moorman, Luke Yates, Ralph Young and Norman Bartelt

■ External Collaborators

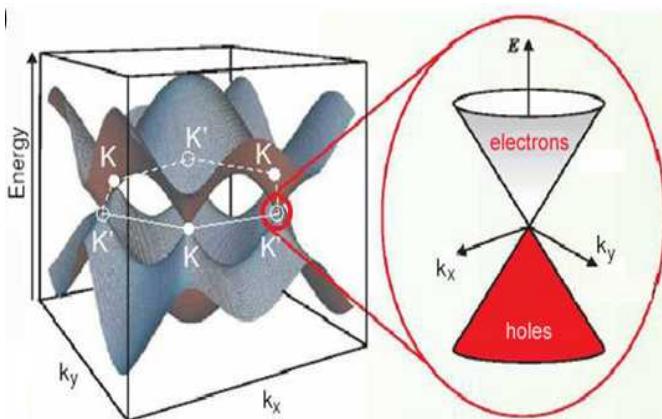
- Prof. Steven Pei, University of Huston
- Prof. Emanuel Tutuc, University of Texas Austin
- Jeremy Robinson, NRL

*PI of a graphene project

Graphene's Unique Blend of Properties Has Broad Disruptive Device Potential



- 2D hexagonal net of sp² bonded carbon atoms

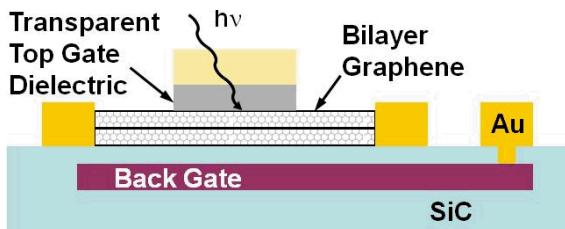


- Semi-Metal Band Structure (zero-bandgap)

Properties	Applications
High Mobility (250,000 cm ² /Vs)	RF Devices (GHz-THz) 300 GHz Demonstrated
Ambipolar conduction	Low Noise Freq Mixing
Spin Coherence Length (> 1 μm)	Quantum Information/ Spintronics
2D film (2DEG)	Quantum Interference Devices
Voltage control of carrier density and bandgap	FETs and Metamaterials MM transmission increase of 250% reported
High Mechanical Strength (Elastic modulus ~ 1 TPa)	MEMS and NEMS, Gas Permeability Applications
Transparency (98%)	Transparent Electrodes & Displays (replacement for ITO) Samsung: industrial-scale CVD synthesis process

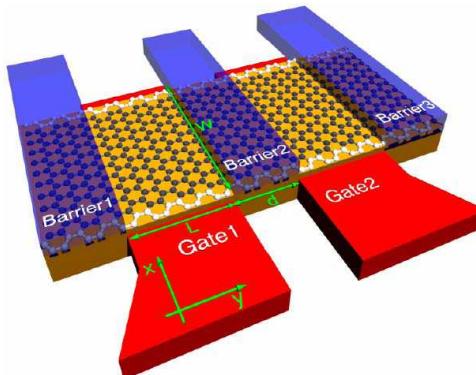
Increasing Interest towards Developing Disruptive Graphene Devices

Optoelectronics



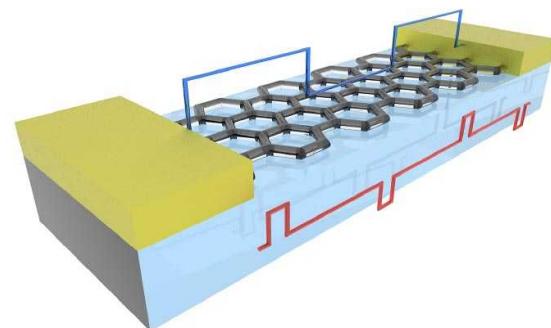
- Tunable IR Detector for improved spectral performance (Ryzhii/PRB '09)
- Plasmonic enabled THz electronics
- Photonics for improve communication

Quantum Computing



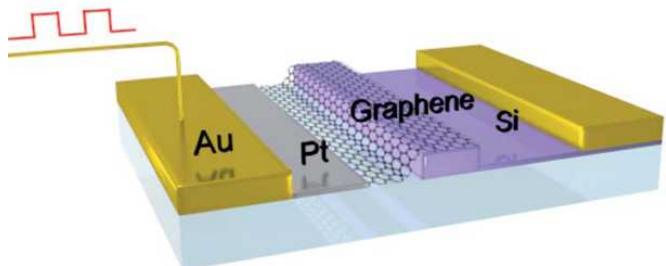
Double quantum dot structure proposed by the Trauzettel Group (Nature Physics 2007).

Flexible Electronics and Memory



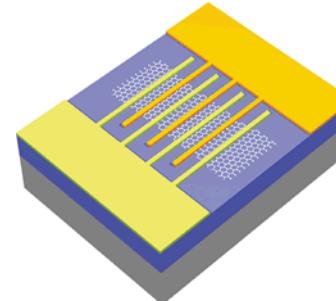
Graphene Nanoribbon Memory Concept: Sordan group: Small Volume 6 (2010)

Ultra High Volume Optical Data Transmission (Possible Petabit Transmission Speed)



Graphene-based waveguide-integrated optical modulator (Xiang Zhang group, UCB)

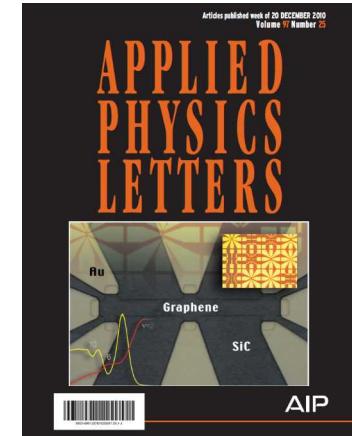
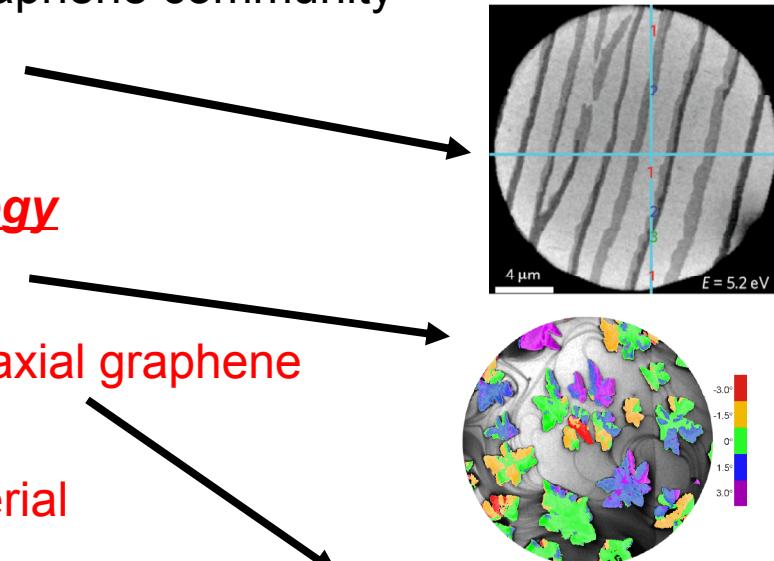
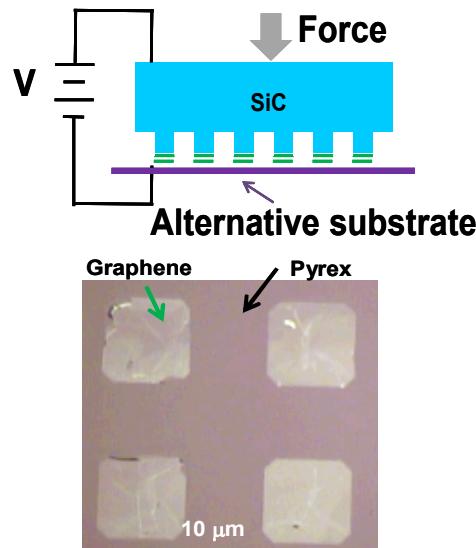
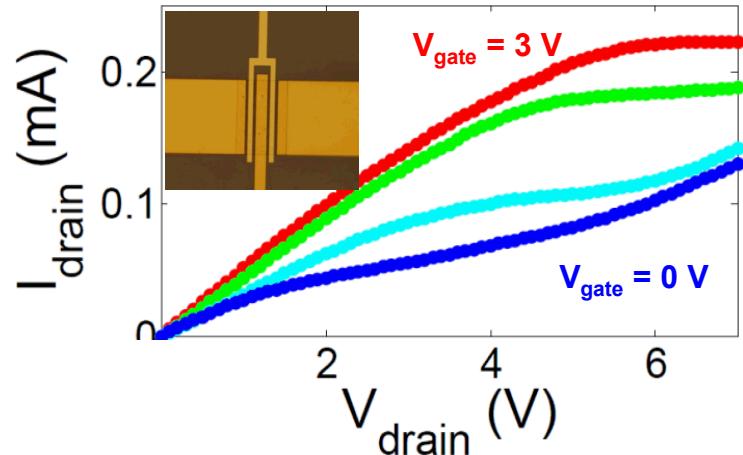
High Speed Photo Detectors (Possible Bandwidths > 500 GHz)



Metal-graphene-metal photodetector (Avouris group, IBM)

Summary of Major Results (Initial LDRD)

- Established Sandia as a technical leader in the graphene community
- Achieved large-area (chip-scale) synthesis on SiC
 - Developed Ar mediated thermal decomposition
- **Developed wafer-scale bilayer synthesis strategy**
- Characterized CVD graphene synthesis on metals
- Observed record mobility ($14,000 \text{ cm}^2/\text{Vs}$) for epitaxial graphene
- Observed IQHE in several devices
- Demonstrated controlled transfer of graphitic material
- Fabricated 1st generation GFETs

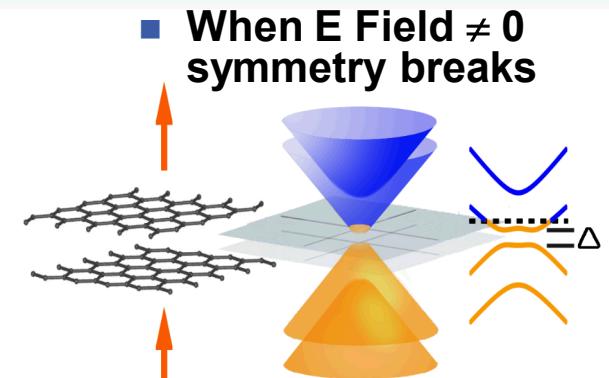


Pan, Howell, Ross, Ohta and Friedmann
Appl. Phys. Lett. 97, 252101 (2010)

New LDRD Effort: Bilayer Graphene (Possibility for Reconfigurable Graphene Devices)

Bilayer Graphene (BLG)

- Real-time control of bandgap by application of electric field
- Potential high impact applications:
 - Reconfigurable IR detectors and filters (electronic tuning)
 - Memory & Quantum devices



BLG Research Efforts

- Characterizing BLG optical/electronic properties
 - Developing dual-gated BLG Photo-FET devices
- Developed/Characterized twisted bilayer graphene (TBG)
 - Optical and electronic properties controlled by twist angle
 - Enables “designer” two-dimensional crystal systems with novel device properties

- When E Field $\neq 0$ symmetry breaks
- BLG bandgap ranges from 0 – 250 meV (or higher?)

Optical image of TBG
(Favorable mention in Science)

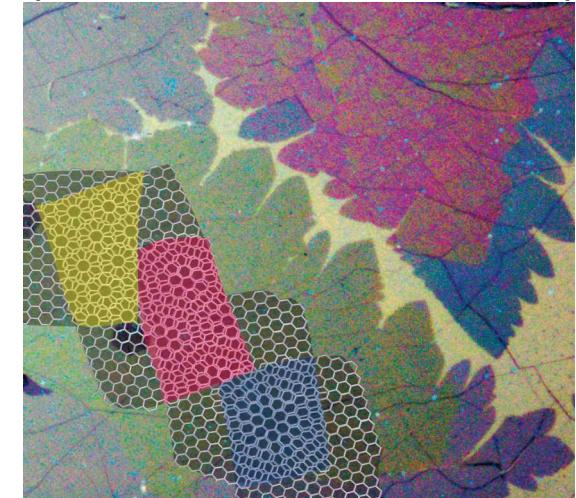
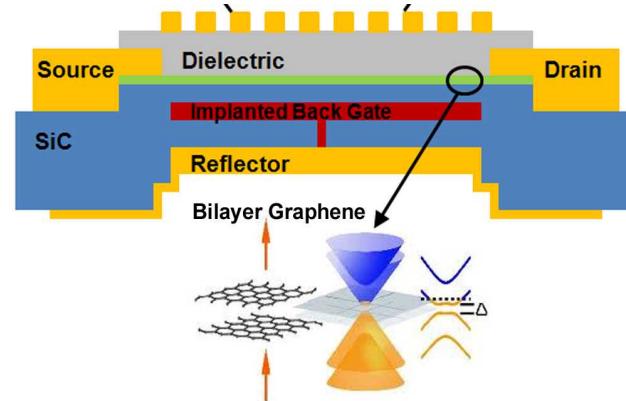
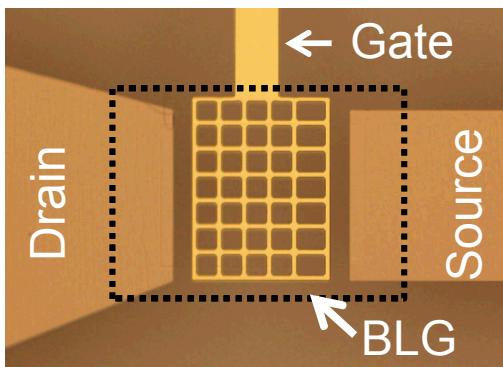


Photo-sensitive BLG-FET



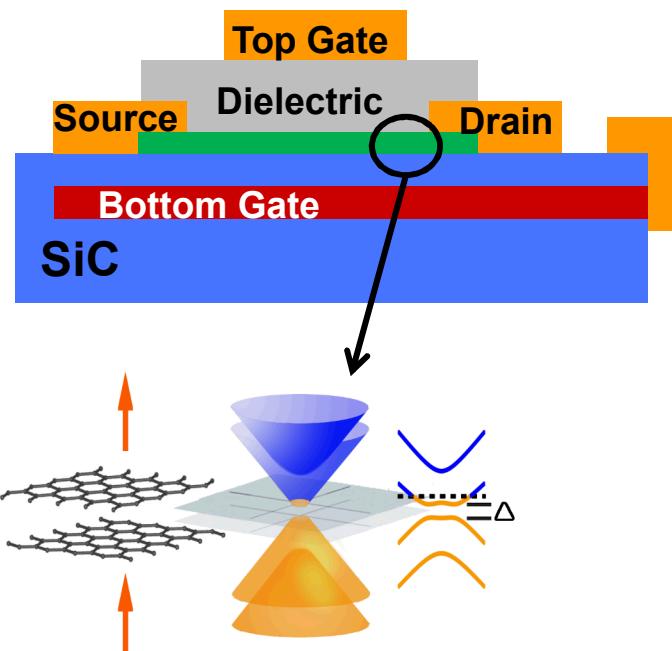
Robinson et al., ACS Nano



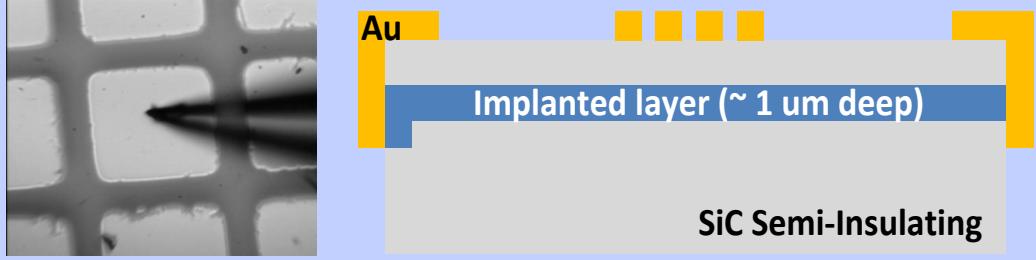
Dual-Gate Device Structures

(Collaboration with Sandia's Ion Beam Lab)

- A dual-gated device is required to both:
 - Create the electric field necessary to open and control the bandgap in BLG
 - Position Fermi level within the bandgap
- Creating the back-gate in semi-insulating SiC is very difficult
 - We are using ion implantation to dope the underlying SiC

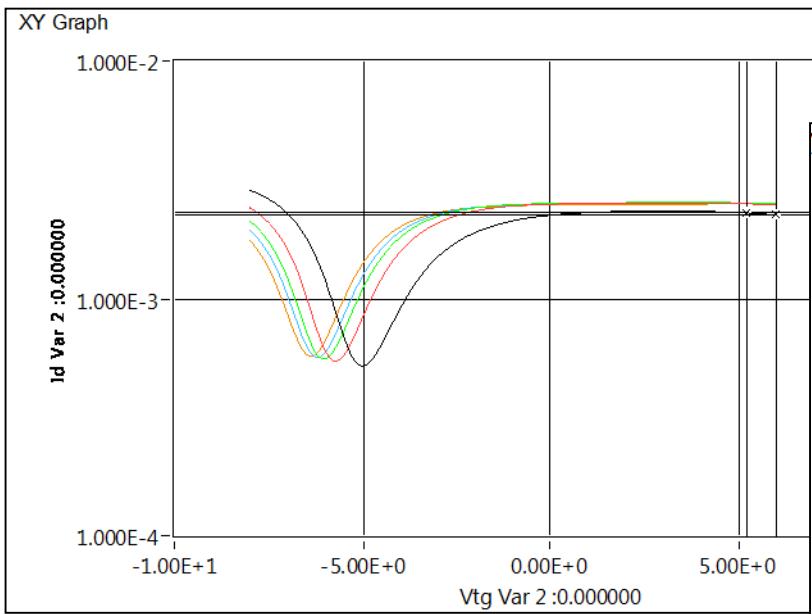


Results of Initial Ion Implantation



- Implanted N ions (target depth of 1 μ m)
- Capacitance measurements indicated an isolated conductive layer at a depth of \sim 600 nm in the SiC
- Demonstrated growth of quasi-free standing BLG on implanted SiC
- Demonstrated back-gate FET operation

First Demonstration of Dual-Gate Operation Using Epitaxial BLG



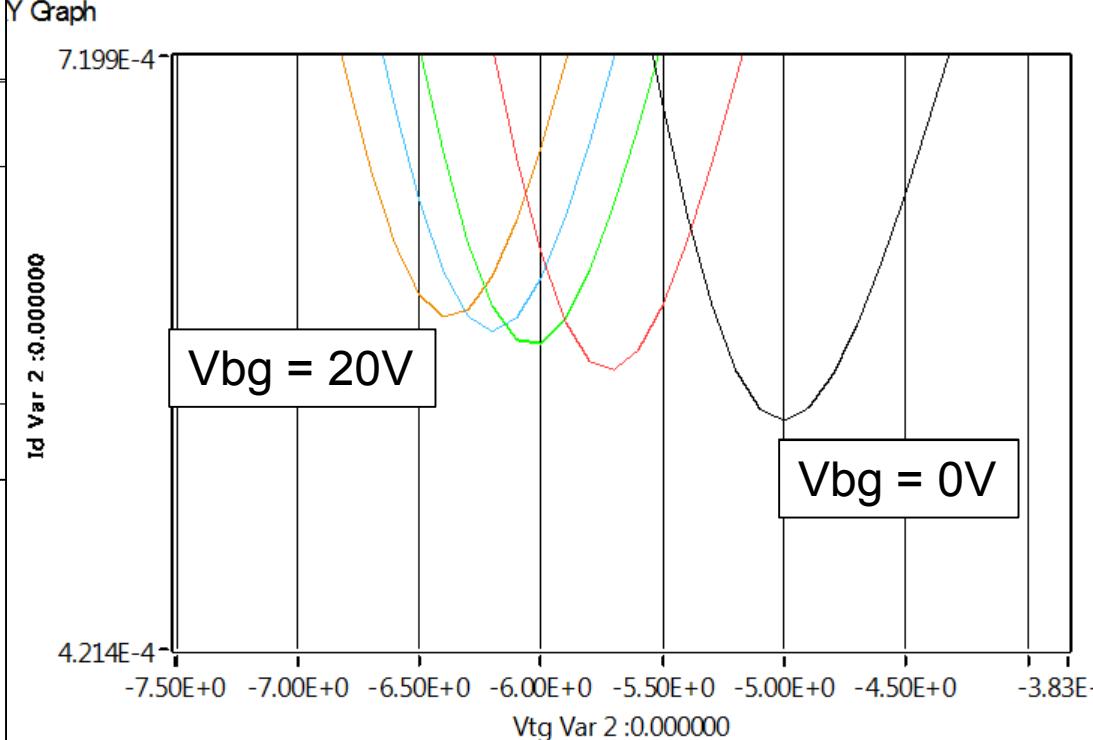
$V_{tg} = +6 \text{ V to } -8 \text{ V in } -100 \text{ mV Steps}$

$V_{bg} = 0 \text{ to } +20 \text{ V in } +5\text{V Steps}$

Hold Time: 30 sec

Delay Time: 0.1 Sec

Observed shift in minimum of $51 \mu\text{A}$



Vbg Step	Vtg @ min Id	Min Id
0 V	-5.0 V	5.18E-4 A
20 V	-6.4 V	5.69E-4 A



Large-Area Bilayer Graphene (BLG) Synthesis Developed at Sandia

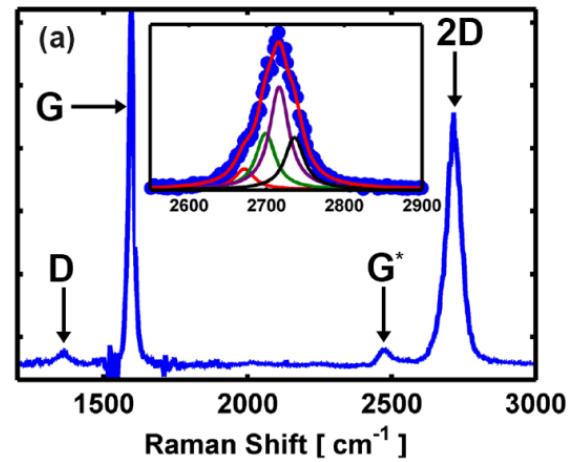
Sandia has differentiating capabilities in large-area bilayer growth

- Most BLG research uses exfoliated graphene
- Sandia is the only reported facility in the US capable of chip scale BLG synthesis

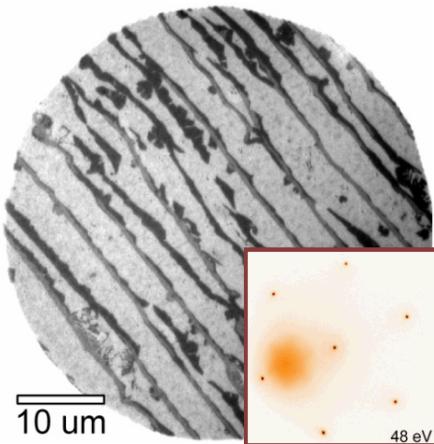
Synthesis methods:

- Thermal decomposition of SiC (current capability)
- CVD on metals (proposed new capability)

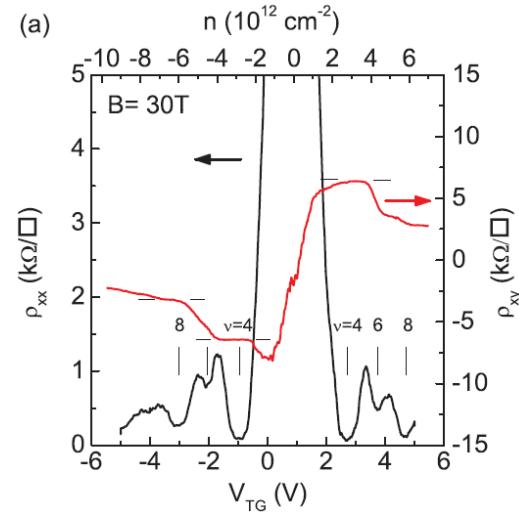
Low defects



Uniform film



Characteristic quantum
Hall states



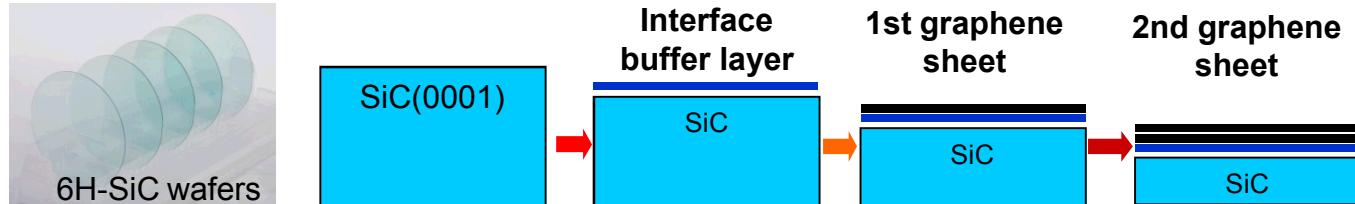
Collaboration with UT Austin

Lee, Kim, Points, Ohta, Beechem, Tutuc Nanoletters 11 3624. 2011

Understanding Graphene Growth on SiC(0001)

■ Graphitization of SiC:

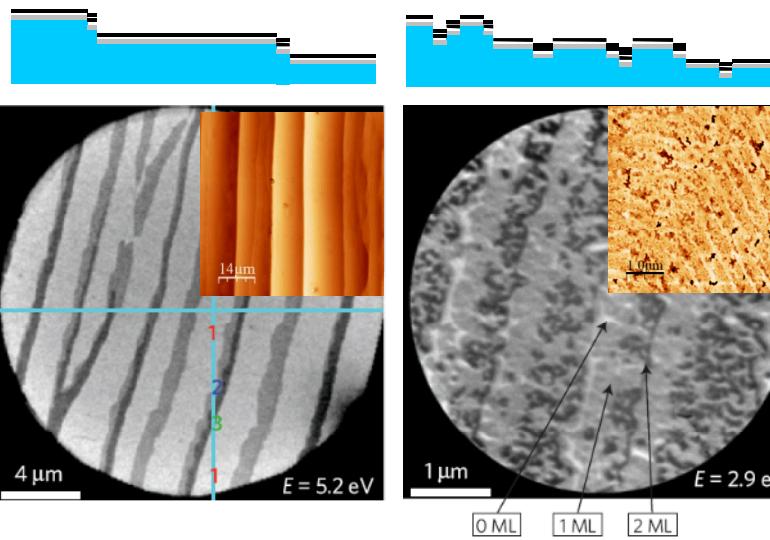
- Sublimation of Si at high temperature (>1200 °C) leaves graphene layer at SiC surface



■ Argon-assisted graphene synthesis

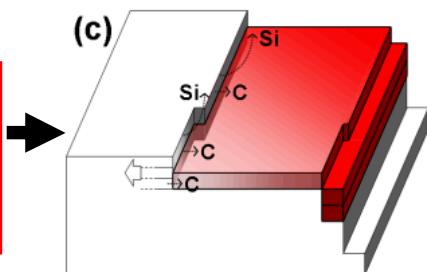
- Samples prepared using Ar at atmospheric pressure and high temp
- This method yields:
 - Domain sizes $> 100 \mu\text{m}^2$ and high uniformity
 - Exquisite control of mono/bilayers coverage

Atmospheric pressure Ar high temp. processing Ultrahigh vacuum mid temp. processing



■ Growth of Graphene on SiC

- Growth morphology strongly depends on the step structure



Step-flow growth

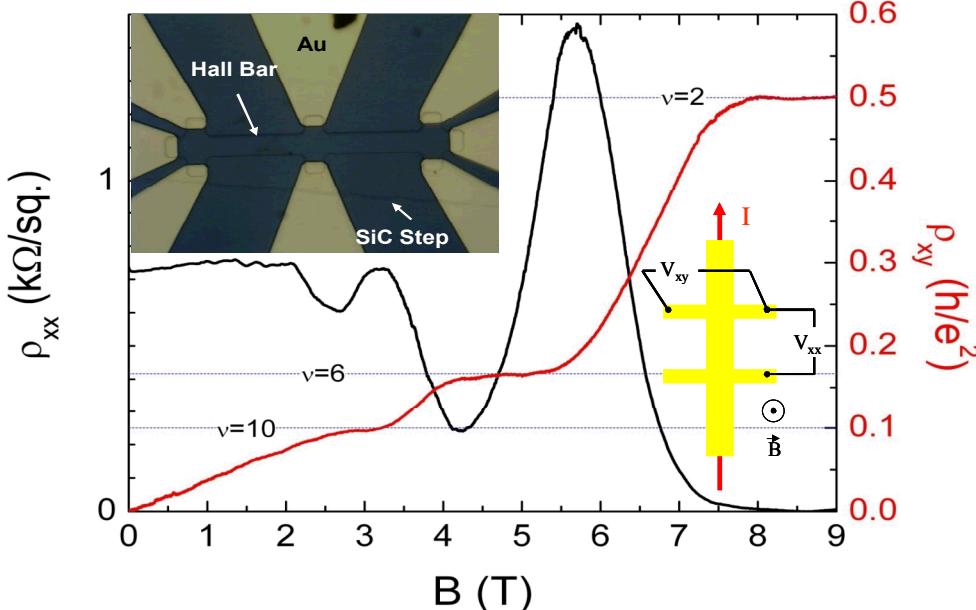
- Key for high large-area growth
- Real-time growth observations using LEEM

K. V. Emtsev et al., Nature Mater. 8, 203 (2009).
C. Virojanadara et al., Phys. Rev. B 78, 245403 (2008)

T. Ohta, N. C. Bartelt, S. Nie, K. Thürmer, G. L. Kellogg, PRB 81, 121411(R)(2010)

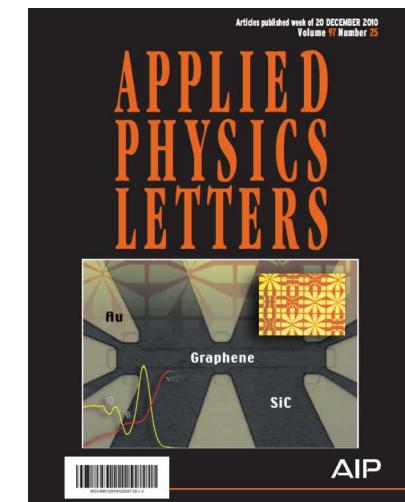
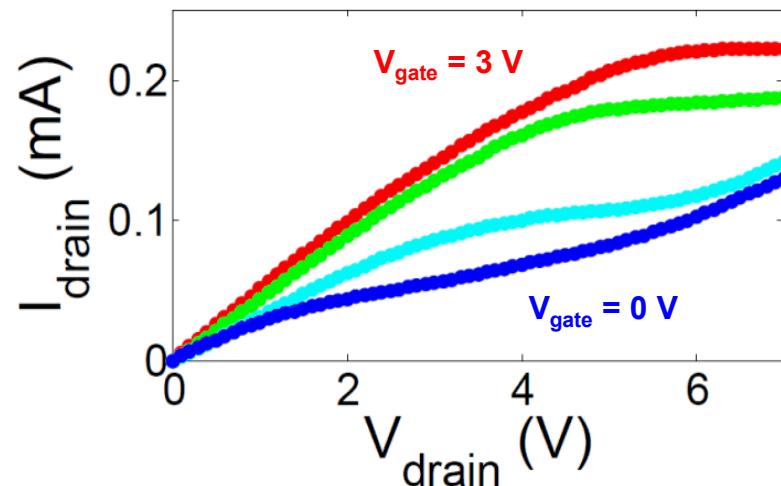
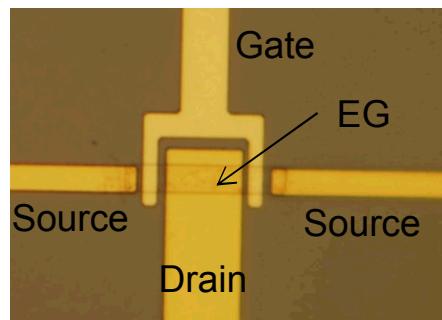
Electronic Characterization of Epitaxial Graphene (EG) Grown on SiC (0001)

Low Temp Transport Measurements (4 K)



- EG electron mobility: 14,000 cm 2 /Vs
 - Record mobility when reported
- Electron density: 6 \times 10 11 cm $^{-2}$
- EG sheet resistance:
 - ~1600 Ω /sq (average from 12 devices)
 - Indicates high uniformity
- Observed IQHE on 3 devices on the same chip

GFET Development

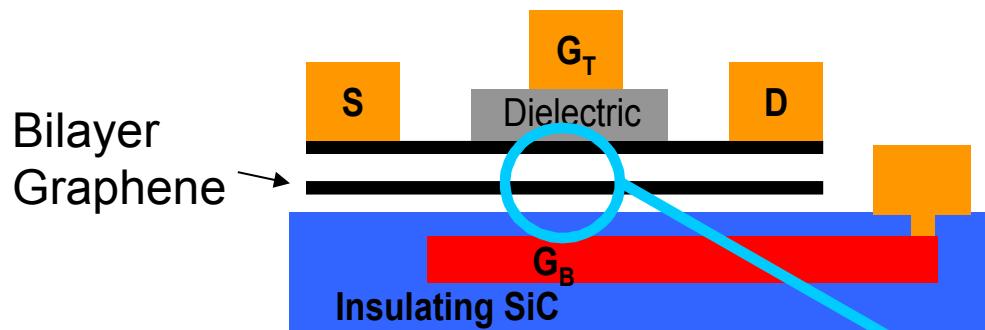


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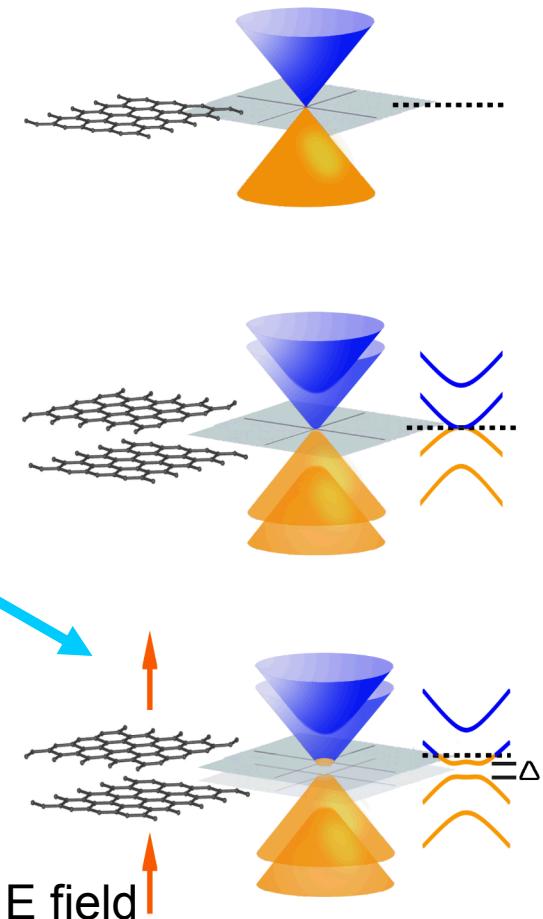


Breakthrough Concept: Reconfigurable Devices Enabled by Bilayer Graphene (BLG)

- Induction of bandgap by transverse electric field
- Real-time control of bandgap (tunability)
- BLG bandgap ranges from 0 – 250 meV (or higher?)



- **Unresolved technical questions:**
 - Graphene/material interaction physics
 - Optoelectronic properties of BLG
 - Limitations on bandgap magnitude
 - Manufacturability
- **Potential disruptive applications:**
 - Reconfigurable “tunable” optoelectronics
 - THz IR detector, IR filters and metamaterials
 - High-speed memory
 - Quantum devices (Qubits)
 - Graphene photonics



Bilayer bandgap images from: <http://infrared.als.lbl.gov/content/the-news/167-bilayer-graphene-gets-a-bandgap?format=pdf>