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Total Ionizing Dose and Displacement Damage Effects in Embedded Memory Technologies

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Abstract

The

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1 Introduction

1.1 Background

Today, embedded (on-chip) memory not computational circuitry is considered most essential feature of the computer architecture. The ability to rapidly store and retrieve large amounts of data has always been a principle driver in the design of computers, however today these demands are so great that many developers remark that in modern systems, computational circuitry is designed to support the embedded memory within integrated processers. Indeed in today's processor, memory occupies roughly half of the chip.

For developers of electronic systems designed for use in harsh radiation environment, the primacy of embedded memory in the digital integrated circuit (IC) underscores the importance of understanding the effects radiation on the devices and circuits that comprise the memory architecture.

The traditional memory hierarchy of the computer system is shown in Fig. 1. The hierarchy consists of on-chip cache composed of high density arrays of static random access memory (SRAM) and main memory built with dynamic RAM (DRAM). Both SRAM and DRAM are built for high performance, i.e., very low read and write times. However the stored information in these arrays is volatile, i.e., requires power, and in many cases must be constantly updated or refreshed. Non-volatile memory, which may be embedded or off-chip, is designed to store the most essential information for the computer. Due to its criticality to the system, stored information must be maintained reliably with power. Today, much of the embedded storage is built using floating gate MOSFETs and support circuitry that define flash memory elements. While the development of flash memory represented a significant advancement to the modern computer architecture, due to is ease of integration, non-volatility, and low cost, its latency and high write power requirements remain a significant drawback.

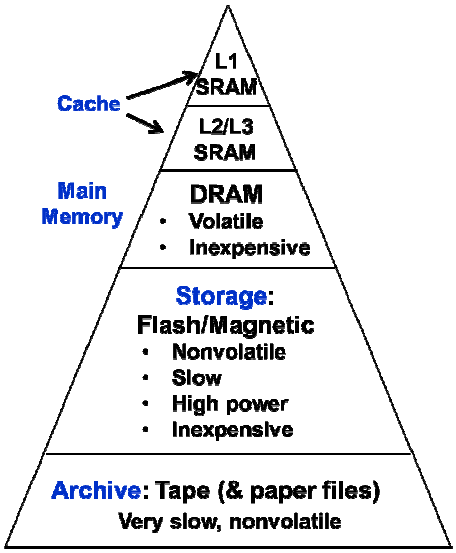

Fig. 1. Traditional memory hierarchy

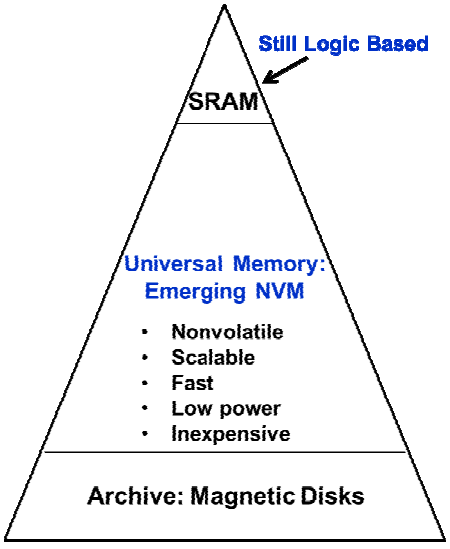

Fig. 2. Universal memory hierarchy

Digital systems designers are now looking at ways to replace the traditional hierarchy with a new paradigm based on storage class memory (SCM), shown in Fig. 2. In this new scheme drawbacks caused by the volatility DRAM, latency and high power requirements of flash are overcome by replacing these memory cells will high speed, non-volatile embedded elements that highly scalable and also low cost. The emergence of new memory and refinement of existing non-volatile device technologies now suggest that storage class memory will represent the future of memory in the integrated circuit. In addition to flash, the technologies that likely players in the new memory landscape include: Phase Change Memory (PCM); Spin Transfer Torque Magnetic RAM (STT-MRAM), and Redox or Resistive RAM (ReRAM).

While there are other candidates on the horizon such as ferroelectric RAM and Molecular memory, the advance memory technologies that will be discussed with be PCAM, STT-MRAM, and ReRAM.

Today basic mechanisms of cumulative radiation damage in solid state dielectrics (e.g., SiO_2) are well known. Since the radiation response of devices (MOSFETs and deep trench capacitors) used in SRAM and DRAM arrays is largely governed by damage to, or defect build-up in the dielectric, we understand much about how radiation affects traditional memory. Moreover this understanding has led to the development of numerous techniques that achieve radiation hardening by process and by design, RBBP and RHBD, respectively. Only recently have extensive investigations of radiation effect on non-volatile memory been undertaken. Most of the research on radiation effects in these technologies has focused on the most mature technology in the non-volatile class, .e., flash. However recent studies have been performed on PCM, MRAM, and ReRAM as well and the results looks very promising from the perspective of radiation hardness.

1.2 Objective

This course reviews the fundamental threats posed by cumulative radiation damage to solid state material and devices used in embedded memory. These radiation threats include: total ionizing dose (TID) and displacement damage (DD). For traditional memory such as SRAM DRAM, and flash, the course focuses on TID effects since the ionizing damage to a charge storage dielectric typically represents the primary mechanism for damage (and failure). For the new technologies, PCM, MRAM, ReRAM, we review what is known today regarding TID effects as well as provide some coverage of the effects of displacement damage, particularly in ReRAM.

1.3 Structure and scope

Section **Error! Reference source not found.**2 reviews the current state and potential future of embedded memory. Section 3 reviews the basic mechanisms of cumulative radiation effects in solid state material from the deposition of energy to the cumulative build-up of defects that affect a device response. Section 4 discusses the effect of ionizing radiation on charge-based memory technologies and section 5 focuses on new resistance change memory technologies and their response to total ionizing dose and displacement damage.

2 Embedded Memory Technologies

2.1 Concepts and Metrics

2.1.1 Fundamental Concepts and Definitions

Electronic memories can be broadly separated into two classes: those which lose their state when power is lost – known as *volatile* memories, and those which retain their state without power – known as *nonvolatile* memories (NMVs). The time a memory retains its state after a write operation is known as *retention*. A traditional NVM is expected to have a retention time greater than ten years, whereas the most common volatile memory, dynamic random access memory (DRAM) has a retention time of less than 1 second.

A second method of categorizing memories is based on the method of accessing data. Sequential access memories (SAM) must access data in series. A common memory which is a pure SAM is a magnetic tape storage system. The time required to read or write a bit on a tape drive (known as read/write latency) depends on the location of the data on the tape. Conversely, a random access memory (RAM) can read or write any bit of data with equal speed. Dynamic and static RAM (DRAM and SRAM) are the most common forms of RAM in use today. Some memories are not purely random or sequential access. For example, NAND flash has equal access to all blocks, but within a block it cannot erase a single bit.

It is useful to briefly outline a few common terms encountered in memory switching which can be a source of confusion. A write operation is often dented as a *set* or *reset*. The term *set* generally refers to the writing of a state of 1, and is synonymous with the *program*, and

on. Conversely, a reset operation writes a state of 0 to the memory, and is synonymous with the terms *erase*, or *off*. Memories which hold a state as the electrical resistance of a material (which includes most of the emerging technologies) generally refer to the low resistance state as *set* and the high resistance state as *reset*.

2.1.2 Performance and Reliability Metrics

Electronic memories have several key metrics by which their performance and reliability are gauges. The most important are defined in the following:

- Endurance:
- Write energy and current:
- Read/write speed (latency):
- Retention:

2.2 Modern Memory Technologies

2.2.1 Overview: The Modern Memory Hierarchy

The modern memory hierarchy, as depicted in Fig x, evolved out of necessity. The principle electronic memories available when this evolved (over three decades ago) were SRAM, DRAM, and magnetic storage. SRAM is capable of speeds as high as the processor itself (i.e. a few processor cycles, or less than 1 ns), but is expensive in terms of processor area. DRAM has a low cost in area (and dollars) than SRAM and capable of latencies less than 100 ns. However, it requires significantly more power and is usually located in modules physically separated from the processor die. Magnetic storage is very slow and requires the most power, but has the lowest cost per bit and is needed for archival storage. Flash memory has a cost and speed between that of DRAM and magnetic storage, and has recently started to replace magnetic hard disk drives in high end personal computers.

The characteristics of SRAM, DRAM, and magnetic memory shaped the modern memory hierarchy. When communicating directly with the logic processor, SRAM is needed because it has the same speed. However, the maximum SRAM available on a processor is typically less than 100 (MB), with the high performance level 1 (L1) cache (which is closest to the logic core) being limited to less than 1 MB. A comprehensive review of the of memory hierarchy of the Intel i7 (and memory hierarchy basics) is given in [http://www.edn.com/design/systems-design/4399725/Memory-Hierarchy-Design---Part-6--The-Intel-Core-i7]. A computer's main memory uses DRAM in physically separate modules, which in a modern system can range from a few to tens of gigabytes (GB).

2.2.2 Static Random Access Memory (SRAM)

SRAM is the fastest memory in the modern memory hierarchy, and is always used as the instruction and data cache for the logic processor. It is usually integrated on the logic die and may be partitioned into several levels, with Level 1 (L1) being the closest to the logic core. SRAM reliability is similar to the logic transistors – which can be switched one billion times per second for years before failure. Hence, SRAM is considered to have essentially unlimited endurance. However, SRAM retention is limited to the time power is available to the processor. When power is removed and restored, each cell will start in a random state.

An SRAM cell is a transistor based latch, which typically consists of six transistors arranged in a configuration shown in Fig. x. The heart of the latch is two CMOS inverters – pair T1-T3 and T2-T4 in Fig. x. Each inverter has a gate (T5 and T6) with the drain connected to the bit line and the gate connected to the word line. …(tbc)

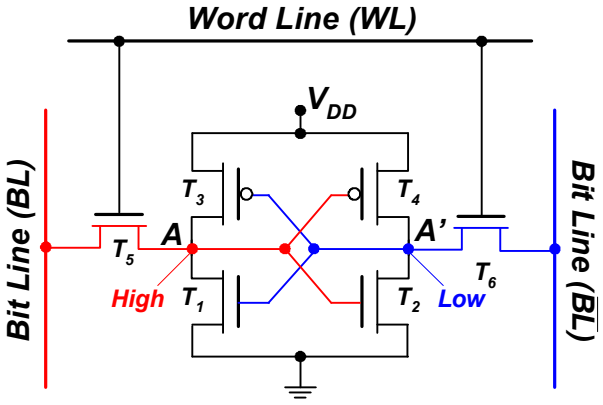

Fig. . Schematic of a standard 6-transistor SRAM cell. Courtesy D.K. Schroder (ASU).

2.2.3 Dynamic Random Access Memory (DRAM)

DRAM is a moderately fast semiconductor memory which is typically physically separated from the logic processor, and has a latency on the order of tens to hundreds of ns. The main memory of a computer is typically DRAM, which bridges the hard disk drive or solid state drive with the SRAM cache on the processor. DRAM typically requires several hundred pJ per read/write operation – largely due to the double data rate (DDR) interface. DRAM is a volatile memory and requires refreshing even with power available. Typical retention of a DRAM is less than one second and typically an entire DRAM module will be refreshed every 64 ms. The DRAM read process is destructive, and hence the read/write/refresh operations are similar. This operation consists of charging or discharging a capacitor and causes very little physical wear to the device. DRAM endurance is greater than 10^{15} although specific measurements of this are not often reported in the literature, and for practical purposes is considered unlimited.

A typical stacked DRAM cell is illustrated schematically in Fig. x (a). The cell consists of a metal-insulator-metal capacitor integrated with a select MOSFET. The charge in this capacitor represents the memory state of the cell: a 0 state is charged and a 1 has no charge on the capacitor (the reason for this stems from the original DRAM cell, which consisted of a floating gated diode without an additional capacitor). Note that the total capacitance consists of the sum of the MOSFET drain diode capacitance (C1) and the stacked capacitor (C2). The gate of the MOSFET is connected to the write-line row and the drain to the bit-line column of the cell. The write process is explained with reference to Fig. x(b). First, the information to write is placed on VA, and S3 and S4 are set to “write”, and S2 is closed. Then, the write line is pulled high, activating the select MOSFET channel. In order to write a one

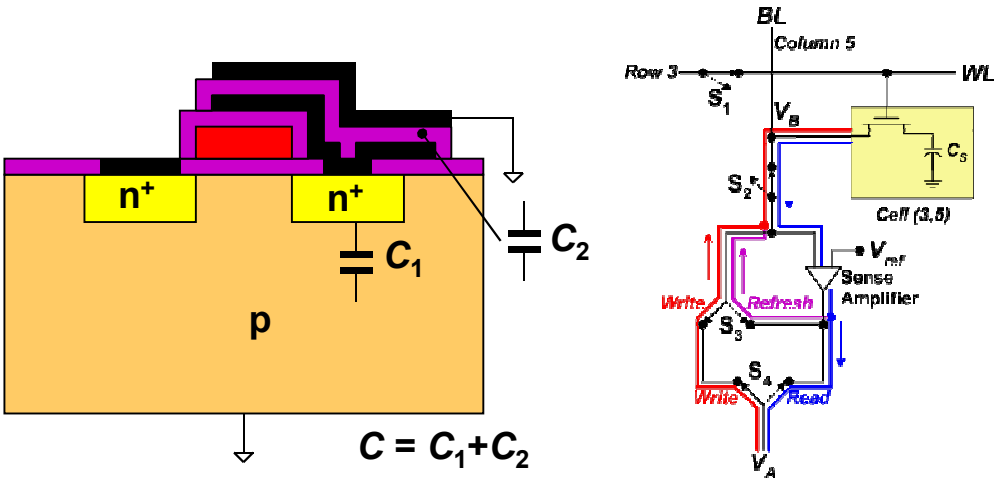

Fig. . (a) Schematic of a stacked DRAM device structure and (b) single DRAM cell in an array, illustrating the read and write operations. Courtesy D.K. Schroder (ASU).

2.2.4 Flash

Flash is a nonvolatile memory technology which has typical latencies between that of magnetic hard disk drives and DRAM (with read times on the order of 10 us and write times of 0.1 to 1 ms) which also has a cost and switching energy between that of HDDs and DRAM. Flash densities have improved dramatically in the past decade, and are nearing 20 nm critical feature sizes – although cell area scaling is likely nearing minimum dimensions. This has improved costs to the point that solid state disks are a common replacement or complement to magnetic hard disks. However, flash is not a strong UM/SCM candidate because of its long write latencies and high write voltages.

The basis of flash and its predecessor, the electrically erasable programmable read only memory (EEPROM – somewhat of a misnomer as it is not a ROM) is the floating gate cell. This structure, illustrated in Fig. x, resembles a MOSFET with a two gates. One gate is “floating”, as it is surrounded by an oxide insulator.

(tbc)

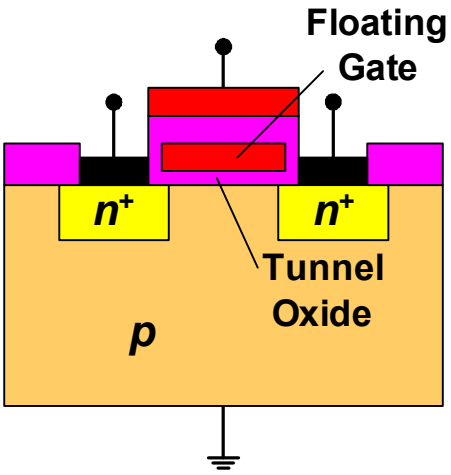

Fig. . Schematic of a floating gate memory structure. Courtesy D.K. Schroder (ASU).

2.3 Emerging Memory Technologies

2.3.1 The Future of Memory: Storage Class and Universal Memory

In 2008, IBM researchers Freitas and Wilcke identified a significant problem with the modern memory hierarchy: a latency gap of four orders of magnitude exists between the DRAM and magnetic disks [Freitas2008]. Even when using a flash-based solid state drive (SSD), a latency discontinuity of two orders of magnitude exists. Hence, this creates a the potential near term market for an emerging memory technology to act as a buffer between the main memory (DRAM) or L2/L3 cache and the magnetic or flash based disk. This concept was named storage class memory (SCM). (tbc)

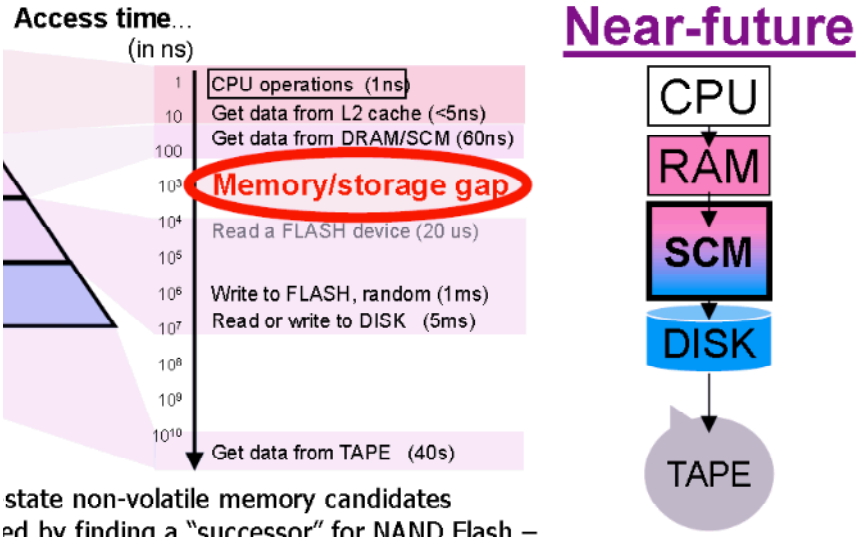

Fig. . (a)

While SCM creates a relatively near-term opportunity for emerging memory technologies to improve performance and fill a gap in the memory hierarchy, it is also possible that one of these technologies could replace DRAM, flash, and magnetic storage. This Universal Memory would drastically simplify the modern memory hierarchy as illustrated in Fig. x. However, a Universal Memory (UM) will require a very versatile device: it must have $>10^{15}$ endurance, >10 year retention, read/write latencies of <10 ns. (tbc)

The three most promising technologies to achieve SCM/UM requirements are phase change random access memory (PCRAM), magnetic RAM (MRAM), and redox RAM. All three of these technologies are nonvolatile resistive memories – hence the state is read by determining the resistance of the two terminal element. Each of these memories are back end of line (BEOL) technologies (although they typically require select/drive transistors). In the following, the key concepts, advantages, and disadvantages of each SCM/UM candidate are reviewed.

2.3.2 Phase Change RAM

The concept of phase change memory (PCM) was invented by Ovshinksy roughly a half century ago and remains the basis of a number of common modern nonvolatile memory technologies: compact discs (CDs), digital video disks (DVDs), and blue-ray discs. Phase change memory is based on the concept that the optical reflectivity of certain chalcogenides is differs significantly between the amorphous and crystalline phases. Furthermore, these phase change materials, GeSeTe (GST), being the most common, can be switched between the amorphous and crystalline phases by a melting and controlled the cool-down process.

Phase change random access memory (PCRAM) is a strong SCM/UM candidate which uses a phase change material (often GST) integrated with a transistor. When the phase is switched between the amorphous and crystalline states, in addition to a change in optical reflectivity, a significant change in resistivity can be detected. A PCRAM cell (depicted in Fig. x(a)) reads the resistivity of the GST to determine the state. The crystalline state is lower resistance than the amorphous state, defining the 1 (set) and 0 (reset) states, respectively. The PCRAM cell is written using a large resistive electrode which acts as a heater. The temperature versus time of the heater operation determines the final state of the GST, as illustrated in Fig. x(b). The low resistance (SET) crystalline phase is achieved by a long, lower temperature/current pulse and the high resistance amorphous (RESET) state is achieved with a fast, high current pulse.

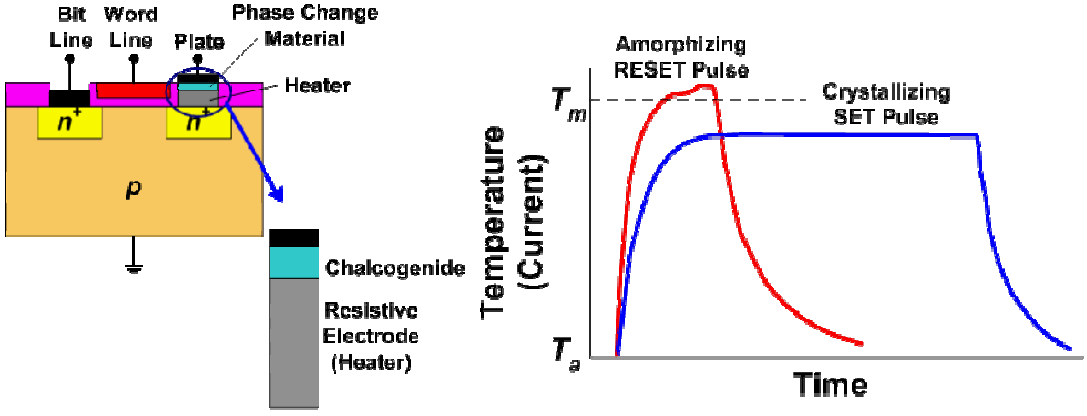

Fig. . (a) Schematic illustration of a typical phase change memory cell and (b) plot of temperature (proportional to current) versus time during the set and reset process. Courtesy D.K. Schroder (ASU).

Commercial PCRAM cells are produced by several companies including Micron and Samsugn at the xx nm node []. In addition, BAE produces a radiation hardened PCRAM product []. PCRAM has relatively high endurance, with reports as high as 10^{12} write cycles, although typical arrays are commercial products are rated at 10^{6} cycles (as they are generally designed to compete with flash memory). Write speeds of less than 10 ns are possible, and scaling has been demonstrated down to less than 10 nm (at the single device level) [wong paper]. However, PCRAM has two significant issues: high temperature retention and a high RESET current (and energy).

(tbc)

2.3.3 Spin Transfer Torque RAM

Field switched magnetic random access memory has existed for nearly two decades, and the more recently developed spin transfer torque RAM (STT-RAM) is a leading UM/SCM candidate technology.

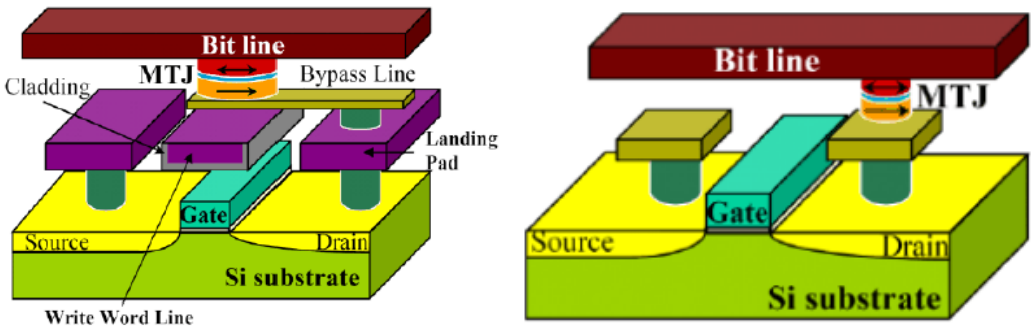

Fig. . Schematic depiction of the (a) the traditional field switched MRAM cell and (b) STT-MRAM cell. Courtesy D.K. Schroder (ASU).

2.3.4 Redox RAM

Redox RAM (ReRAM) is one of the most promising SCM/UM candidates due to its high speed [ref], low current/energy [], high endurance [], and excellent scalability. However, it is the least mature, with limited capacity commercial parts only beginning to appear in the past year [adesto]. ReRAM can be categorized by the switching mechanism in three major classes: valence change memory (VCM), electrochemical memory (ECM), and

thermochemical memory (TCM) [Waser2009]. The VCM and ECM are considered the most promising as a SCM/UM candidate, and hence are the two considered in the following.

A typical VCM cell (depicted in Fig. x(a)) consists of a transition metal oxide (TMO) switching layer sandwiched between two electrodes. One electrode is typically a reactive, ohmic metal, and the other is inert. Typical switching oxides include TaOx, HfOx, and TiO2, although this type of behavior has been demonstrated in numerous other oxides. In the Pt/Ta/TaOx/Pt example depicted in Fig. x(a), the ohmic electrode is Ta and inert electrode is Pt. VCM ReRAM exhibit a bipolar switching behavior which can be characterized by a hysteresis curve (Fig. x(b)). When a positive voltage past a certain threshold is reached, the device switches to the low resistance (SET) state; whereas when a negative voltage of an opposing threshold is reached the device switxches to the high resistance (RESET) state. The switching mechanism in VCM ReRAM is not fully understood, but is generally thought to be due to modulation of the conductivity in a switching channel that is roughly 50-200 nm in diameter []. In particular, it is thought that oxygen anions are able to enter and exit this channel due to the forces of electric field, as well as thermal effects related to channel current.

VCM ReRAM has impressive metrics: scaling to less 10 nm [imec iedm], endurance greater than 10^{12} cycles, switching energy <1 pJ and currents of less than 10 uA [HP stuff], as well as switching speeds less than 1 ns. If these cell-level parameters are achieved in a large array, this would nearly meet the needs of a DRAM replacement universal memory.

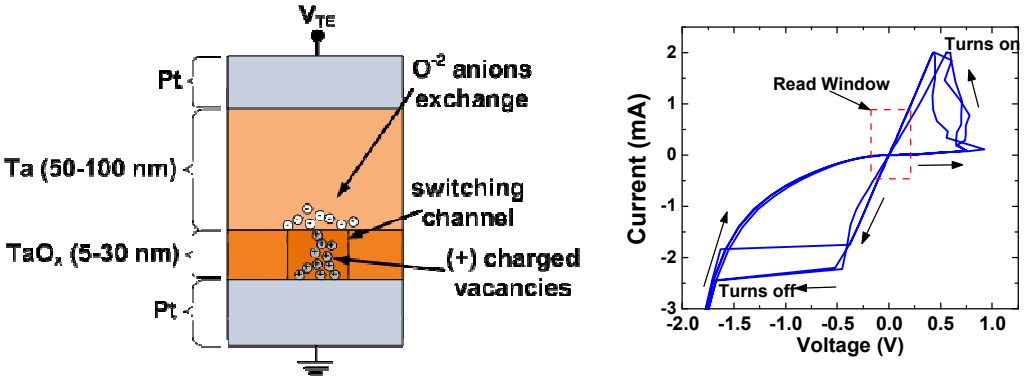

Fig. . (a) Schematic illustration of the operation of a TaOx memristor illustrating O-2 anions dissociating from the TaOx when subject to a positive bias on the top electrode (b) Typical I-V hysteresis curves of a TaOx ReRAM cell.

ECM ReRAM, also known as conducting bridge RAM (CB-RAM) and programmable metallization cell (PMC) has many similarities to VCM. Switching is bipolar and occurs at similar (and sometimes lower) voltages as VCM. Endurance and retention are also similar. However, the memory is more mature and the switching mechanism is better understood. A typical ECM cell is made of a solid electrolyte – numerous oxides and chalcogenides have been used. However, in an ECM cell, switching is due to the formation and dissolution of an Ag or Cu filament, which can be observed in situ [].

3 Cumulative Radiation Effects: Basic Mechanisms

3.1 Total Ionizing Dose

3.1.1 Overview of Total Ionizing Dose and Damage Processes in SiO_2

Ionization of a target material is caused by the interaction of high-energy photons or charged particles (mainly protons and electrons) with the atoms of that material [1]. Photon interactions are not a primary concern in the natural space environment. However, exposure to photons can occur in nuclear reactor and other research facilities, during sterilization processes, and is of increasing concern in medicine, where the increased use of radiation in

cancer therapy can threaten the operation of implantable electronics, e.g., pacemakers. High energy photons are also used for TID evaluations since most laboratory sources used to characterize total-dose effects emit x-rays or gamma rays.

Photons interact with material through three different processes, namely the photoelectric effect, the Compton effect, and pair production [2] as illustrated in Fig. 3. For each of these processes, the primary result of the interaction is the creation of energetic secondary electrons. Protons and other charged particles also generate ehps that lead to ionization damage.

Based on these interactions (i.e., photon or charge particles), the electron-hole pair (ehp) density generated is proportional to the energy transferred to the target material [3]. Stopping power or linear energy transfer (LET) is the particle energy loss per unit length (dE/dx). It is a function of the particle mass and energy as well as the target material density [4]. The units of LET are commonly expressed as MeV.cm^2/mg.

Fig 3 shows a plot of LET vs. particle energy for electrons and protons [4]. The LET for protons is higher than electrons at lower energies, but decreases rapidly with increasing energy. Electrons show a non-monotonic response, decreasing as a function of particle energy before increasing for energies above 1 MeV. The total amount of energy deposited by a particle that results in ehp production is commonly referred to as total ionizing dose. The SI unit for TID is Gy (1 Gy = 1 J/kg); however, rad (radiation-absorbed dose) is the conventional unit used in the space industry (1 rad = 100 erg/g = 6.24×10^{13} eV/g = 10^{-2} Gy). One rad (material) is equivalent to 100 ergs absorbed by one gram of the target material.

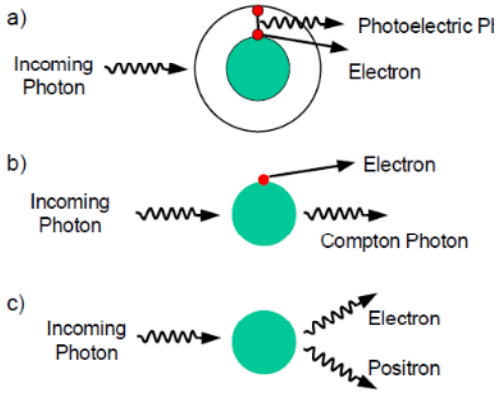

Fig. 3. Schematic drawing of three processes through which photons interact with material: a) photoelectric effect, b) Compton effect, and c) pair production [1]

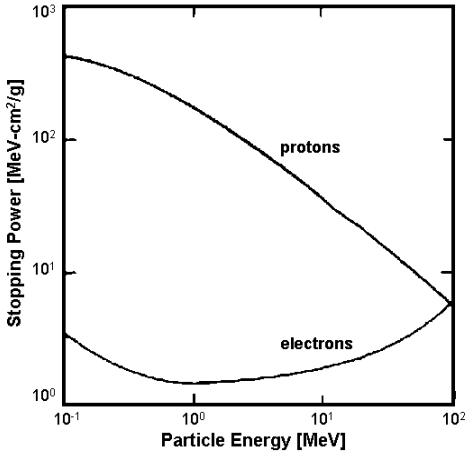

Fig. 4. Stopping power for electrons and protons as a function of particle energy [4].

The physical processes that lead from the initial deposition of energy by ionizing radiation to the creation of ionization defects are: 1) the generation of ehps, 2) the prompt recombination of a fraction of the generated ehps, 3) the transport of free carriers remaining in the oxide, and either 4a) the formation of trapped charge via hole trapping in defect precursor sites or 4b) the formation of interface traps via reactions involving hydrogen [5]. These processes are summarized graphically in Fig 5 [2].

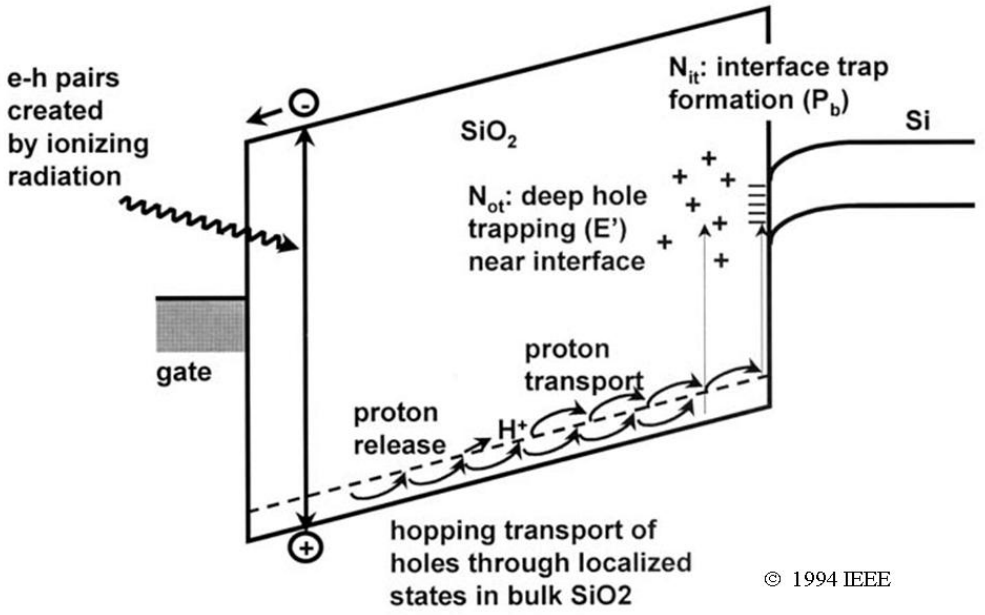

Fig. 5. Illustration of the main processes in TID damage [2].

In ehp generation (process 1), a fraction of the kinetic energy of the incident particle is lost to ehp creation. The mean energy, E_p, needed to ionize a material is dependent on the bandgap of the target material. The number of ehps generated for a given dose is thus strongly dependent on E_p as well as the material density. The relationships between ionization energy, material density, and generated carriers are listed in Table I for three materials: GaAs, Si, and SiO_2 [1]. The ehp density per rad, denoted as κ_g (column 3 in Table I), is obtained using the following conversion formula:

$$\kappa_g\left[\frac{\#\text{ehp}}{\text{cm}^3\text{rad}}\right] = 100\left[\frac{\text{erg}}{\text{g}}\right]\left[\frac{1}{\text{rad}}\right]\bullet\frac{1}{1.6x10^{-12}}\left[\frac{\text{eV}}{\text{erg}}\right]\bullet\frac{1}{E_P}\left[\frac{\#\text{ehp}}{\text{eV}}\right]\bullet\rho\left[\frac{\text{g}}{\text{cm}^3}\right]. \qquad (1)$$

Table I.

Relationship between, ionization energy,
material density, and generated carriers [1].

Material	Mean E_p (eV)	Density (g/cm^3)	Pair density, generated per rad, κ_g ($pairs/cm^3$)
GaAs	~4.8	5.32	$\sim 7x10^{13}$
Silicon	3.6	2.328	$4x10^{13}$
Silicon Dioxide	17	2.2	$8.1x10^{12}$

Once generated, a fraction of the ehps are annihilated through either columnar or geminate recombination (process 2) [2, 6]. The ehps that escape this initial recombination process divided by total number of ehps generated is the fractional charge yield, denoted by f_y. Fig 6 plots f_y as a function of the radiation type [2, 6]. The figure also indicates that electron-hole pair recombination is a function of the electric field within the material [7].

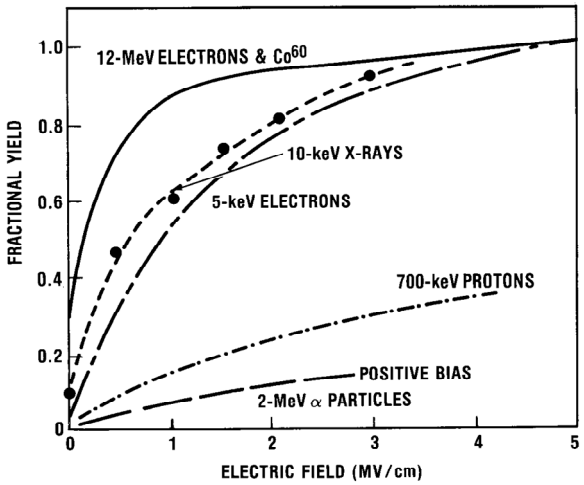

Fig. 6 Fractional yield of holes generated in SiO_2 as a function of electric field in the material [2, 6].

The fractional yield of ehps increases monotonically as the local electric field increases. It is generally believed that electrons, having a much higher mobility than holes in oxides, are rapidly swept out of the dielectric [8]. The surviving holes will undergo polaron hopping transport via shallow traps in the SiO_2 (process 3) [8]. A fraction of these transporting holes may fall into deep traps in the oxide bulk or near the Si/SiO_2 interface, thereby forming trapped positive charge (process 4a) [8]. The hole trapping efficiency (f_{ot}) is also a function of the electric field in the oxide [1]. The trapped hole defect may, depending on its proximity to the interface, exchange charge with the underlying Si via electron tunneling [9, 10]. Reactions between holes and hydrogen-containing defects or dopant complexes can also lead to the formation of a second type of ionization defect: the interface trap (process 4b) [11, 12].

3.1.2 Total Dose Induced Oxide-Trapped Charge and Interface Trap Formation in SiO2

Oxide-Trapped Charge (N_{ot})

Oxide trapped charge is typically net positive due to the capture of a hole in neutral oxygen vacancies and the subsequent formation of oxygen vacancy defects, or E' centers [13-18]. There are primarily two types of E' defects: E_δ', and E_γ'. The E_δ' center is a "dimer" vacancy, which forms a relatively shallow trap for holes in the oxide. Most of the E_δ' centers have energies located in the SiO_2 bandgap within 1.0 eV of the oxide valence band [16]. The shallow trap level of the E_δ' makes it a good candidate for the defect type responsible for hole transport through SiO_2 (process 3) [16]. The E_γ' center is a significantly deeper trap then the E_δ' defect, residing at energy levels greater than 3 eV above the oxide valence band [14, 16]. While E_γ' centers may be located throughout the oxide, most are found near the Si/SiO_2 interface [17-19].

Both types of E' centers can exchange charge with an adjacent Si layer [14]. The ability of the E' defect to "communicate" with the Si is a strong function of its proximity to the interface [9]. E' centers that readily capture carriers from or emit carriers to the adjacent Si are often called border traps or switching states. They are generally located within 3 nm of the Si/SiO_2 interface and can exchange charge via electron tunneling on time scales of microseconds to seconds [9, 10]. E_γ' centers located at distances greater than 3 nm from the interface (i.e., in the oxide bulk) may capture and emit carriers, but the probability of this process occurring is low. Thus, E_γ' defects in the oxide bulk are generally treated as fixed (i.e., bias independent) positive oxide charge (Not). Removal or compensation of N_{ot} may require elevated temperature and/or biased anneals over relatively long periods of time. A schematic illustration of the location of border traps (switching states) and oxide trapped charge (fixed states) in the MOS system is illustrated in Fig 7. The buildup of N_{ot} in an oxide can be expressed as [19, 20]

$$\Delta N_{ot} = D\kappa_g f_y f_{ot} t_{ox}, \quad (2)$$

where D is the total ionizing dose deposited. As Eq. 2 shows, ΔNot is proportional to the thickness of the oxide.

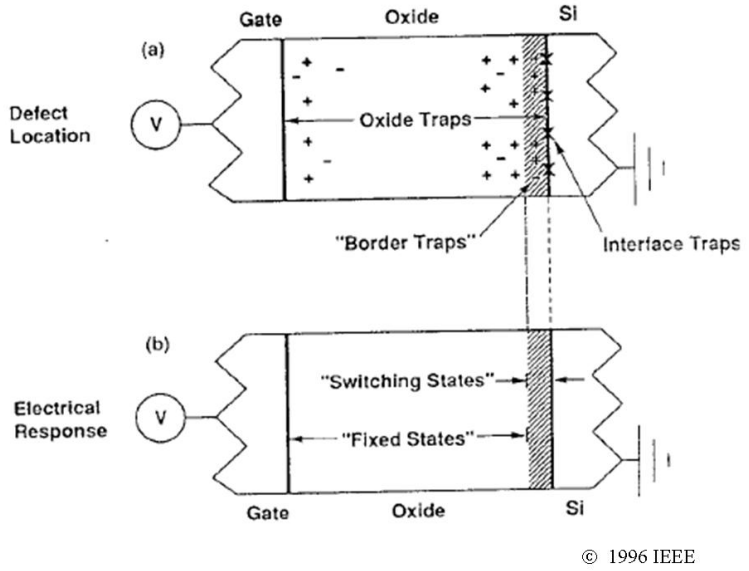

Fig. 7. Location and stability of trapped charge in SiO_2 [10].

Interface Traps (N_{it})

Like border traps, a second type of ionization defect, the interface trap will also exchange charge with an adjacent Si layer. However, unlike border traps, interface traps (N_{it}) are located exactly at the interface. Thus, there is essentially no barrier to trapping and de-trapping of carriers in the near-surface Si. Interface traps can therefore have a significant effect on carrier mobility and recombination rates of carriers at the semiconductor surface.

Interface traps are primarily dangling bond defects called P_b centers [21]. The most important and abundant of these centers is called the P_{b0} center. A secondary contribution is provided by a closely related defect called P_{b1}. Schematic illustrations of P_{b0} and P_{b1} defects on (111), (110), and (100) silicon are shown in Fig 8 [22].

The three initial processes that lead to N_{it} formation are similar to processes that lead to the formation of oxide trapped charge (i.e., ehp generation, recombination, and transport). However, the final formation of dangling bonds relies on several other reactions. The first reaction is between transporting holes and hydrogen containing oxide defects (D'H), which releases protons (H^+) [11]. Although it has been contended that direct reactions with holes can create interface traps, it has been shown experimentally that (near and above room temperature) most interface traps are created by protons [23]. Moreover, density-functional theory calculations confirm that the formation of interface traps by direct hole interaction is not energetically favorable under most conditions [24]. Thus, the creation of a Pb center primarily relies on the presence of H^+ near the interface. Other potential sources of protons that have recently been identified are dopant-H complexes in the Si bulk [12]. In their 2005 paper, Tsetseris et al. reported that hole interactions with these hydrogen complexes can lead to the creation of protons that move toward the interface under negative gate biases [12]. These effects seem to share a common origin with a significant reliability threat in advanced CMOS technologies, i.e., negative bias temperature instability (NBTI) [12].

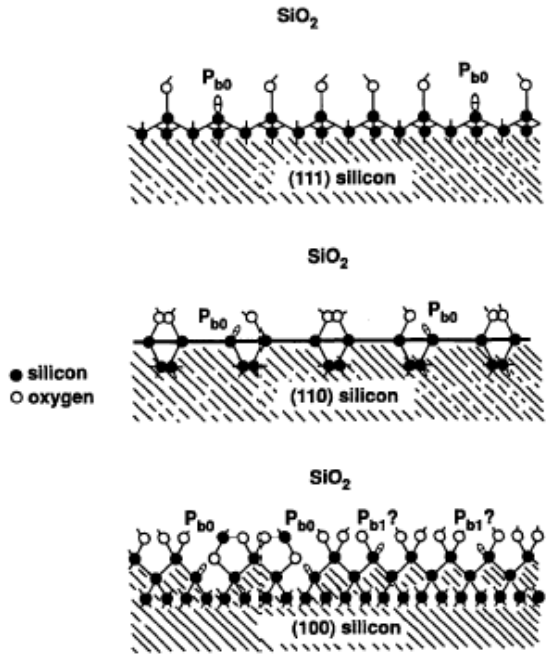

Fig. 8. Schematic illustration of Pb0 and Pb1 interface trap defects on (111), (110), and (100) silicon [22].

Protons diffusing or driven by the electric field to the SiO2 interface can remove hydrogen atoms from H-passivated dangling bonds (D) via the simple reaction [11, 24]

$$SiH + H^{+} \Rightarrow D^{+} + H_2 . \tag{3}$$

The resulting defect (D+) is the interface trap.

Unlike oxide trapped charge, interface traps are characterized by a distribution of energies within a Silicon (Si) bandgap, i.e., between the valence and conduction bands, E_v and E_c, respectively. The trap distribution in energy is denoted as $D_{it}(E)$, with units of $cm^{-2}eV^{-1}$, where

$$N_{it} = \int_{E_v}^{E_c} D_{it}(E)dE . \tag{4}$$

Interface traps located below the intrinsic Fermi level (E_i) of Si are typically assumed to be donor-like (neutral if filled by an electron and positively charged if empty). Interface traps above Ei are acceptor-like (neutral if empty and negatively charged if filled).

Fig. 9 shows measured energy distributions of P_{b0} and P_{b1} traps in Si, reported by Lenahan et al. in 2002 [21].

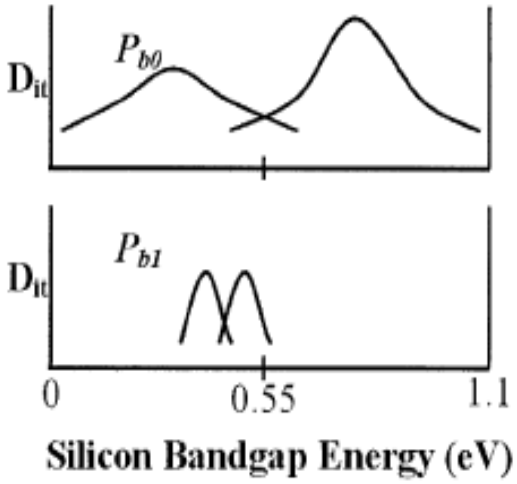

Fig. 9. Energy distributions of P_{b0} and P_{b1} trap in Si [21]

While most models assume uniform Dit energy profile, some recent works have applied model that capture the impact of non-uniform disttibutions on device response [25].

3.1.3 Annealing of Oxide Traps and Interface Traps

The annealing (i.e., compensation) of radiation-induced trapped holes in SiO_2 is a long-term process that is strongly dependent on temperature and applied electric field. The basic mechanisms for electron compensation are tunnelling of an electron from the Si substrate and compensation by thermal excitation of an electron from the valence band [26]. Both tunnelling and thermal emission have been combined into a single model by McWhorter et al. that describes a tunneling front and a thermal emission front, where the position of both varies logarithmically with time [27]. In other words, the distance into the oxide bulk from where trapped holes can be removed, measured from either the Si-SiO_2 interface for the case of tunneling or from the valence band edge for thermal emission, varies as ln(t). Fig 9 illustrates hole trapping along with the annealing/compensation processes. The trapped positive charge can be neutralized by adding an electron to the relaxed E'_γ center. The added electrons eliminate the unpaired spin and therefore compensate for the positive charge by creating a dipole structure by the transition from (b) → (c). The electron compensation process is reversible as illustrated by the transition from (c) → (b), where the electron has tunnelled back into the substrate. True annealing can occur when the electrostatic force between the two ends of the dipole structure (c) is sufficient to reform the Si-Si bond. This situation is indicated by the transition from (c) → (a) [26].

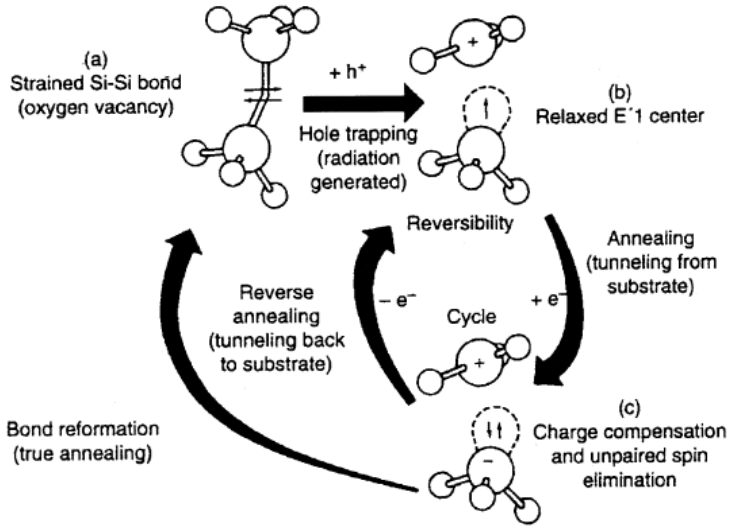

Fig. 8. Model for hole trapping and de-trapping (annealing) and for intermediate electron compensation and reverse annealing phenomenon [26].

The spatial and energy distributions of N_{ot} will strongly affect the rate at which charge neutralization occurs. For tunneling, the spatial distribution of N_{ot} must be close to the Si/SiO_2 interface. For thermal emission, the energy distribution needs to be close to the valence band energy. Unlike oxide-trapped charges, N_{it} buildup occurs on timeframes much slower than oxide-trapped charge build-up and can take thousands of seconds to saturate after a pulse of ionizing radiation. Interface-trapped charges do not typically anneal at room temperature, only at higher temperature [1]. These properties make N_{it} charge effects important for LDR applications and total dose evaluations. Annealing behaviors have critical implication with total dose assessment of electronic devices.

3.2 Displacement Damage

Highly energized particles (protons, electrons, neutrons and heavy ions) can damage semiconductor materials by displacing atoms as the particle moves through the material [5]. In silicon, Frenkel defects (interstitial silicon and vacancy pairs) are formed when incident particles collide with silicon nuclei or when primary recoil atoms collide with other atoms in the lattice [5]. The vacancies and interstitials created by these collisions introduce allowable energy states in the band gap of a semiconductor material. The presence of these states can change the electrical performance of electronic devices, leading to various radiation responses. For minority carrier devices such as bipolar transistors, the primary impact of the radiation-induced energy levels is the creation of bulk traps (N_t) in the material. Bulk traps increase carrier recombination in a forward biased junction (e.g. the base-emitter junction in active operation), which increases base current and may reduce collector current. Both alterations to current lead to a reduction in current gain. A linear relationship between incident particle fluence and bipolar current gain was postulated by Messenger and Spratt [28]:

$$\frac{1}{\beta(\Phi)} = \frac{1}{\beta_{pre}} + K\Phi \quad . \tag{4}$$

where β_{pre} is the current gain prior to radiation exposure, $\beta(\Phi)$ is the current gain after irradiation, Φ is the particle fluence, and K is a composite displacement damage factor. The units of K are cm^2. Experimental studies, past and present, use the damage factor as an analytical tool for characterizing displacement damage effect. For example, there is a linear relationship between reciprocal gain and particle fluence in the experimental data shown in Fig. 9. These data, originally presented by Summers et al. in 1987, illustrate the dependence of the damage factor, K (the slope of the curves), on the type and energy of the incident particle [29]. As the figure indicates, the damage factor is larger for 16.8 MeV He ions than either 40.0 MeV He ions or 4.3 MeV deuterons.

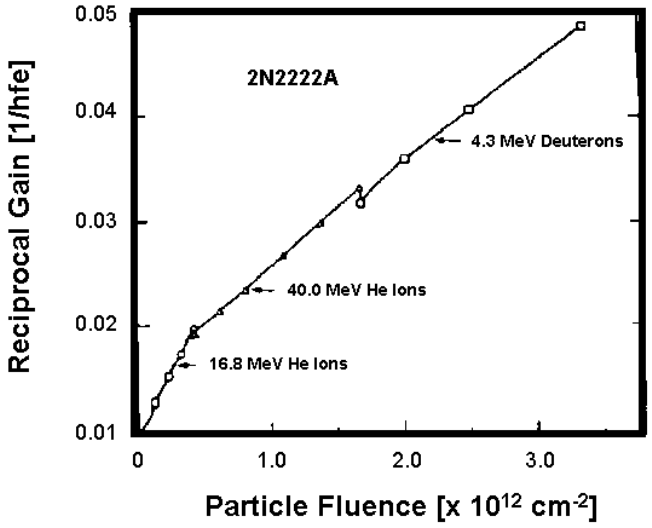

Fig. 9 Reciprocal gain vs. particle fluence for sequential irradiations on the 2N2222A NPN BJT with 16.8 and 40.0 helium ions and 4.3 MeV deuterons [29].

Further experiments, conducted by Summers, also revealed damage factor in discrete bipolars to be dependent on the polarity of the device (i.e., NPN or PNP for BJTs) and the bias conditions applied during electrical characterization. Fig. 10 shows these dependencies by plotting the damage factor vs. collector current for various particles (65 MeV helium ions, 3.7 MeV protons, and fission electrons) incident on two types of discrete silicon switching transistors (2N2222A NPN and 2N2907A PNP transistors). The PNP device shows a larger damage factor than the NPN device for identical bias conditions. This difference is a function of several variables, including the doping and geometry of the base regions of the respective transistors. Fig. 10 also indicates that, although K decreases with increased collector current, at a fixed collector current, the ratio of the damage factor for neutrons (Kn) to the damage factor for any other particle is the same, regardless of the bias conditions or device type [29]. According to Summers, the damage factor ratio between neutrons and any other incident particle is a “unique” function of particle type and energy only [29]. This claim is supported by the experimental data shown in Fig. 11. These data are the damage factor ratios (K/Kn) for five types of transistors (four NPN transistors and one PNP transistor) plotted vs. energy for three particles (protons, deuterons, and helium ions).

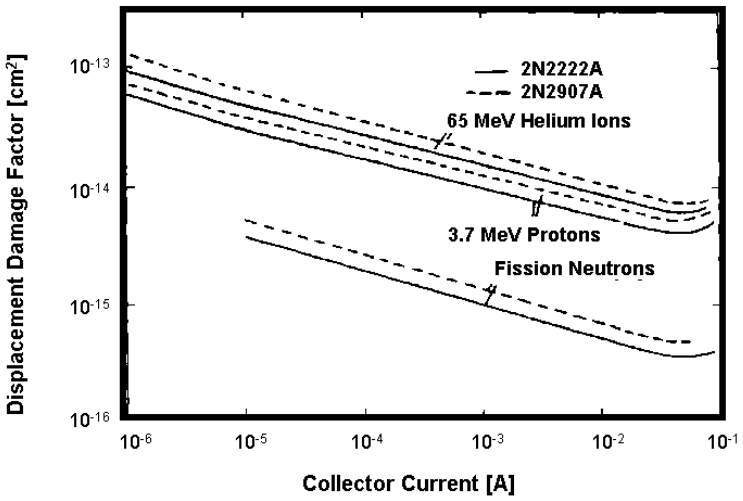

Fig. 10 Displacement damage factors vs. collector current for 2N2222A NPN and 2N2907A PNP BJTs for fission neutrons, 3.7 MeV protons, and 65.0 MeV helium ions [29].

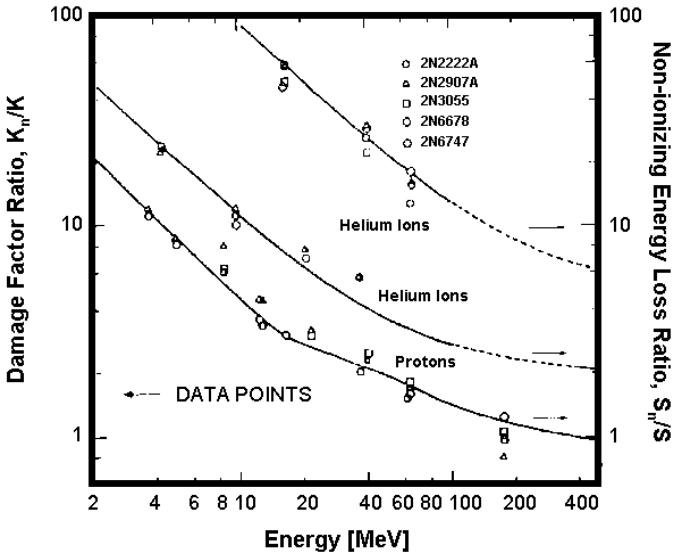

Fig. 11 Damage factor ratios for bipolar transistors for proton, deuterons, and helium ions to 1 MeV equivalent neutrons as a function of energy. The solid lines are obtained from analytical calculations of the NIEL ratio [29]

The displacement damage caused by different particles can be correlated analytically on the basis of non-ionizing energy loss (NIEL). NIEL, commonly represented as the variable S, is calculated as the energy loss per unit mass to lattice displacement as a particle moves through the target material [5]. NIEL has the same units as LET (i.e., MeVcm^2/g) and, as with LET, is a nonlinear function of the type and energy of the incident particle type. In Fig. 12 the non-ionizing energy loss is plotted vs. energy for three types of incident particles: electrons, protons and neutrons [30]. The curves were calculated using the analytical model developed by Burke [31]. The calculation of NIEL requires approximations for the differential cross-section for atomic displacements ($d\sigma/d\Omega$) and the average energies of recoil atoms (T), corrected for Lindhard energy partitioning [32].

NIEL is calculated by evaluating the integral

$$S = \frac{N}{A}\int_{\theta_{\min}}^{\pi} \frac{d\sigma(\theta)}{d\Omega} T(\theta)\, d\Omega \quad , \qquad (5)$$

where N is Avogadro's number, A is the atomic mass, θ is the scattering angle, d□ is the differential solid angle centered about θ, and $\theta_{min\ min}$ is the scattering angle for which the recoil energy equals the threshold for atomic displacement [29, 32-34]

The model calculations of non-ionizing energy loss in silicon give values of Sp =1.94x10^{-3} MeVcm^2/g for 200 MeV protons and Sn = 2.04x10^{-3} MeVcm^2/g for 1 MeV neutrons [29, 32]. Given these values, the NIEL ratio of 200 MeV protons to 1 MeV neutrons (Sp/Sn) is 0.95. The secondary electrons generated by 10 keV x-rays have energies below 0.01 MeV. As Fig. 12 shows, the x-ray-induced NIEL in silicon is many orders of magnitude smaller than that of either protons or neutrons. It is for this reason that the displacement damage caused by 10 keV x-rays is considered negligible in solid state materials, even materials used in advanced non-volatile memory.

In their 1987 paper, Summers et al. showed that the damage factor ratio of protons measured at several energies (as well as deuterons and Helium ions) to 1MeV neutrons (K/Kn) was within approximately 10% of the calculated ratio of the NIEL of both particles in silicon (S/Sn) [29]. Fig. 11 demonstrates the similarities between K/Kn and S/Sn. The experimental data, showing the damage factor ratios as a function of particle type and

energy, are shown as symbols. The solid lines, through the experimental data, are the results of the analytical NIEL calculations (Eq. 17).

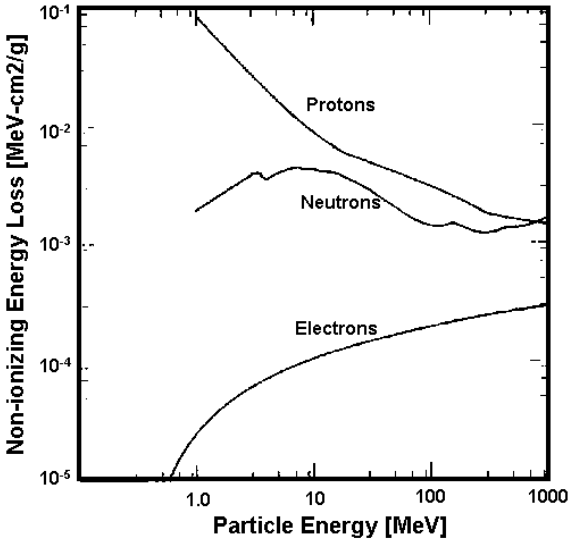

Fig. 12 Calculation of non-ionizing energy deposition in silicon by electrons, protons, and neutrons [30].

At the present time, it is unclear whether the lack of exact correlation between the measured damaged factors and the analytically derived NIEL curve is due to experimental uncertainty or a real effect. For example, the NIEL calculations used in this work do not take into account several second-order effects associated with high-energy particle interactions (e.g., nuclear inelastic and relativistic effects). Moreover, the spread in the measured damage factors may also be a function of variations in the part types (e.g., transistor geometry or polarity). This variability must be taken into account when trying to correlate the amount of NIEL caused by a high-energy charged particle such as proton with neutrons.

4 Radiation Effects in Charge-based Memory

4.1 Static RAM

4.1.1 Bulk CMOS

Impact of TID Defects on MOS Structures

Fixed oxide trapped charge can have a significant impact on the D.C. parameters of CMOS devices and integrated circuits. One of the most important and well-studied effects is the negative shift in the D.C. drain current vs. gate-to-source voltage (Vgs) for both n- and p-channel MOSFETS. This effect is illustrated in Fig. 13. The figure shows that for a fixed Id, the radiation-induced buildup of Not shifts the Vgs bias point more negative (i.e., by ΔVot). In n-channel MOSFETs, this shift leads to a reduction in threshold voltage and an increase in off-state and drive currents. In p-channel MOSFETs, Vt increases negatively, while off-state and drive currents are reduced.

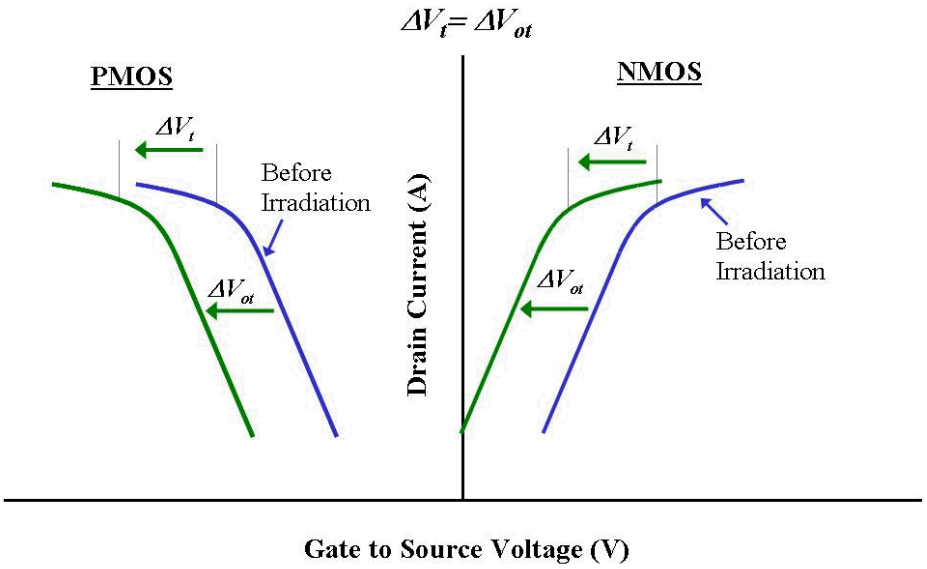

Fig. 13. Illustration of the effect of fixed oxide trapped charge on n- and p-MOS devices.

Radiation-induced D.C. voltage shifts can be calculated using the following equation:

$$\Delta V_{ot} = -\frac{t_{ox}}{k_{ox}\varepsilon_0} q\Delta N_{ot} \quad , \tag{6}$$

where k_{ox} is the dielectric constant of SiO_2 and ε_0 is the permittivity of free space [35]. Given Eqs. 2 and 6, the theory predicts that negative threshold voltage shifts caused by fixed oxide trapped charge buildup are proportional to the square of oxide thickness, i.e.,

$$-\Delta V_t\left(N_{ot}\right) = -\Delta V_{ot} \propto t_{ox}^{\,2} \quad . \tag{7}$$

This theoretical relationship has been verified through numerous experiments [20]. The relationship in Eq. 7 indicates that as the gate oxides of advanced CMOS technologies are scaled to thinner dimensions, the threat of shifts in D.C. parameters due to N_{ot} buildup in the gate oxide is reduced [36, 37]. Instead, hole trapping in the thicker shallow trench isolation dielectrics is now a greater radiation threat in modern CMOS technologies. Typical STI trenches are much thicker than gate oxides. For advanced CMOS technologies the thicknesses range from 300 nm to 450 nm [38]. The impact of fixed positive oxide trapped charge buildup in STI structures will be discussed in detail below.

As noted above, depending on their proximity to the Si/SiO_2 interface, E' centers can "communicate" with an adjacent Si layer [9, 10, 14]. Most of these switching defects are located within 3 nm of the interface and can exchange charge on time scales between 0.01s to 1s [10]. The mechanism of charge exchange is dependent on the nature of the oxide trap. For example, the Eδ' defect can simply capture and re-emit trapped holes [14]. This process has been shown to be more likely in pMOS transistors [14]. In pMOS transistors, the Eδ' defect has a high hole capture cross section and a relatively low barrier for re-emission relative to nMOS devices [14]. For Eγ' defects, the mechanisms are somewhat more complex. Most theories contend that the acting carriers for charge transfer in and out of the Eγ' defect are tunneling electrons. It is now widely held that the positively charged Eγ' centers can trap an electron, forming a highly stable dipole structure [8-10, 14, 39] . While it is possible for these trapped electrons to be re-emitted, the dipole will also act as a shallow electron trap that is relatively easy to fill or empty depending on the surface potential of the underlying Si [8, 39].

The impact of switching oxide (border) traps on CMOS D.C. parameters is different than the impact of fixed oxide charge discussed in the previous section. Unlike Not, the charge state

of the switching trap can vary with bias. As such, the signature effect of border traps on MOSFET D.C. parameters cam be more similar to the effect of interface traps.

One of the principle effects of interface trap buildup is an increase in the subthreshold swing of a CMOS device. This effect is illustrated in Fig 14, which shows a characteristic stretch out (ΔVit) in the Id vs. Vgs response for both n- and p-channel devices. The mechanism for this effect is the bias-dependent trapping or de-trapping of charge at the interface as the device surface is swept from accumulation to inversion by the gate voltage. Fig. 14 shows that the threshold voltage is also impacted by Nit buildup. It should also be noted that depending on the pre-irradiation characteristics of the MOSFET, interface trap buildup may also increase off-state drain current.

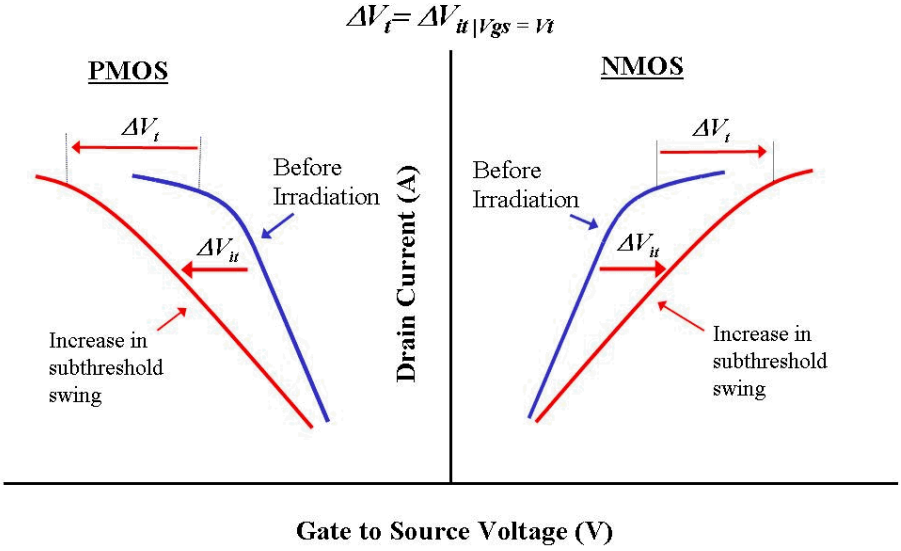

Fig. 14. Illustration of the effect of interface traps on n- and p-MOS devices.

In D.C. measurements, it is difficult to distinguish the effects of interface traps (Pb centers) and switching oxide traps (near interface E' centers). The key difference between the two defect types is that the charge exchange frequency at switching E' centers is low (< 100 Hz) compared to Pb centers (> 1 kHz) [40, 41]. Therefore, independently measuring the effects and/or densities of either defect type requires A.C. or noise measurement techniques (e.g., A.C. conductance, charge pumping, or 1/f noise).

The combined effects of oxide and interfacial defects on surface potential can be modeled analytically with the surface potential equation

$$\left(V_{gb} - \phi_{MS} + \phi_{nt} - \psi_s\right)^2 = \gamma^2 \cdot \phi_t \, H(u). \qquad (8)$$

Eq. 24 is a modified form of the implicit equation for surface potential [42-44]. In this equation, ψ_s denotes surface potential, V_{gb} is the applied gate-to-body bias, ϕ_{MS} is the gate-to-body workfunction difference, γ is the body factor, ϕ_t is the thermal voltage, and $u = \psi_s/\phi_t$. The parameter ϕ_{nt} represents a defect potential which is added to model the effects of Not and Nit. The function H(u) in (8) captures the charge contributions of both fixed charge and free carriers in the Si and is expressed as

$$H(u, \phi_n) = e^{-u} + u - 1 + e^{-\beta(2\phi_b + \phi_n)}(e^u - u - 1) \qquad (9)$$

where ϕ_n is the "channel voltage" otherwise known as imref splitting, $\beta = 1/\phi_t$, and ϕ_b is the bulk potential [42, 43].

In MOS devices, the primary distinction between Not and Nit is that, to first order, the charge contributed by oxide trapped charge is fixed while the charge contributed by interface traps will vary with surface potential [45, 46]. If the energy distribution of interface traps, Dit, is assumed uniform, then the defect potential can be expressed analytically as,

$$\phi_{nt} = \frac{q}{C_{ox}}[N_{ot} - D_{it} \cdot (\psi_s - \phi_b)], \quad (10)$$

where q is the absolute value of the electron charge and C_{ox} is the oxide capacitance per unit channel area [45, 46].

Eq. 8, through its inclusion of the defect potential, enables surface potential across a MOSFET channel to be calculated analytically not only as a function of terminal voltages and device parameters (e.g., oxide capacitance, workfunction difference, and doping), but also as a function of oxide and interfacial defects. This is critical when modeling radiation effects in CMOS devices [47].

Defect Extraction from MOS Structures

In order to quantify TID defect build-up in advanced CMOS isolation structures, post irradiation measurements can be performed on conventional MOSFETs, field oxide MOS capacitors (FOXCAPs) or field oxide transistors (FOXFETs) fabricated in the process being evaluated. Fig. 15 plots the pre and post irradiation response characteristic of FOXCAPs designed in a 130 nm CMOS process. The FOXCAP was built with an array of single capacitor cells placed in parallel. Each cell integrates an n-type poly-Si top gate over the STI, which is deposited into the p-well (body). C-V measurements were taken prior to radiation exposure, after irradiations up to 1 Mrad (SiO2), and after an elevated temperature post-irradiation anneal (1 week at 100°C). As shown in Fig. 15, the p-type FOXCAP exhibits the characteristic negative shift in the C-V response after irradiation This response indicates a build-up in radiation-induced defects. The positive shift in the C-V curve after the one week anneal indicates a moderate amount of defect removal or compensation occurs in these oxides as a result of time and/or temperature dependent processes. The build-up of oxide trapped charge in the STI oxide can be computed as

$$\Delta N_{ot} = -\frac{k_{ox}\varepsilon_0}{qt_{ox}}\Delta V_{mg} = -\frac{k_{ox}\varepsilon_0}{qt_{ox}}\Delta V_{ot}, \quad (11)$$

where ΔVmg is the change in the midgap gate voltage. The build-up of interface traps above midgap can be approximated as

$$\Delta N_{it} = -\frac{k_{ox}\varepsilon_0}{qt_{ox}}\left(\Delta V_{inv} - \Delta V_{mg}\right), \quad (12)$$

where ΔVinv is the change in the gate voltage at inversion. Using Eqs. 11 and 12, the build-up of Not and Nit in the oxide can be computed at each dose level. The values for Vinv and Vmg, pre- and post-irradiation can be obtained from closed form equations for capacitance across the MOSCAP system [48].

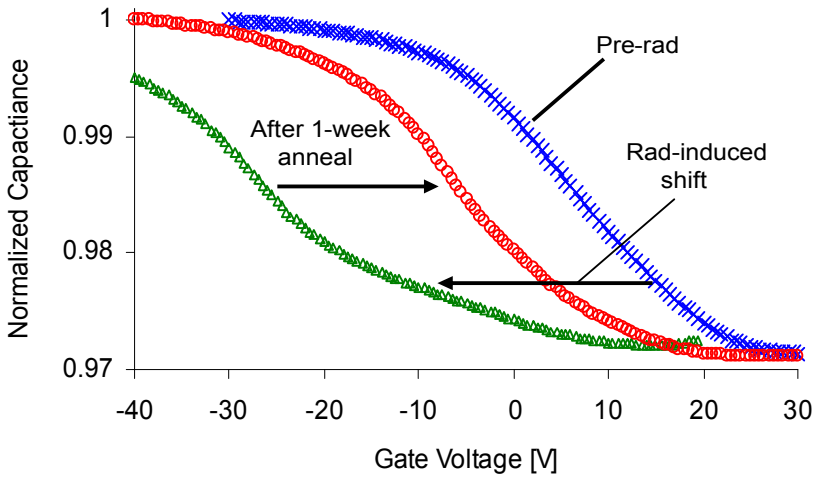

Fig. 15.. C-V response of the FOXCAP

While MOS capacitors are excellent TID evaluation structures, they are not always available on test coupons. However, measurements on conventional MOSFETs and FOXFETs can also be used to extract TID defects as a function of radiation exposure level. One excellent technique, is the charge separation method originally proposed by McWhorter and Winokur [49]. For this method, the MOS subthreshold equation

$$I_d = \mu \frac{W}{L} \sqrt{\frac{\varepsilon_{Si} q N_A}{2\psi_S}} \left(\frac{kT}{q}\right)^2 \left(\frac{n_i^2}{N_A}\right) \exp\left(\frac{q\psi_S}{kT}\right) \left[1 - \exp\left(\frac{-V_{ds}}{kT}\right)\right], \quad (10)$$

is used. Device parameters such as body dopy, N_A, mobility, μ, gate width and length (W and L) can be obtain from the manufacturer or extracted empirically as lumped constant. Changes in the midgap voltage (ΔVmg), which allow for the extraction of N_{ot} with dose (Eq. 1 above), are the shifts in gate-source voltage (V_{GS}) measured at the fixed midgap current, Idm.g., as shown in Fig. 5. Idm.g. is the value of Id in Eq. 3 when the surface potential ψ_S is set to the bulk potential, ϕ_b. Changes in the N_{it} concentration are calculated from Eq. 2 above, where the ΔVinv is the shift in V_{GS} at the inversion current, Iinv. Iinv. is the value of Id in Eq. 3 when the surface potential ψ_S is set to $2\phi_b$.

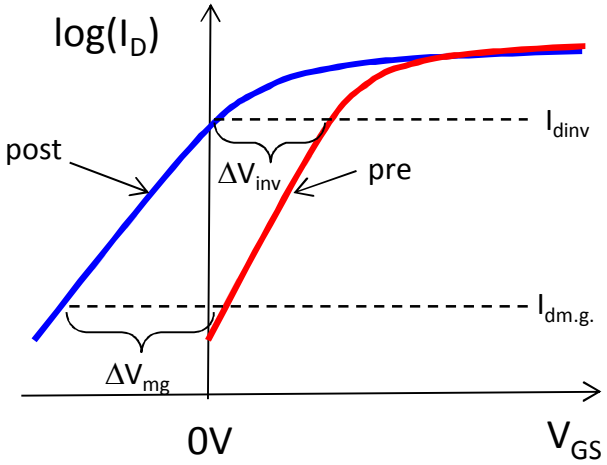

Fig. 16. Illustration of charge separation method used to extract Not and Nit buildup in MOSFETS

Effects on Isolation Oxides

In the 1980s Saks and Ancona predicted that technology scaling would reduce a MOSFET's susceptibility to radiation-induced damage in gate oxides [50]. This is due primarily to the fact that, to first order, defect buildup in gate oxides scales with tox (Eq. 2). Radiation tolerance in thin gate oxides is further enhanced by the increased likelihood of positive charge annihilation or compensation by tunneling elections from the adjacent materials [51]. Inherent gate oxide hardness was demonstrated at the 0.25 μm technology node [52]. At this node, the oxide thickness is typically less than 6 nm, which is less than twice the approximate distance for high probability electron tunneling (i.e. ~ 3 nm) [9, 51]. Gate oxide hardness trends have continued to be observed in subsequent smaller technologies, e.g., 0.18 μm (tox = 3.2 nm) and 0.13 μm (tox ~ 2 nm) [53]. Defect buildup in thicker isolation oxides is typically the dominant cause of radiation-induced degradation in the D.C. parameters of modern CMOS devices and integrated circuits. A representative cross-section of a modern bulk n-channel MOSFET is shown in Fig. 17. As the figure illustrates, the shallow trench isolation (STI) structures enclosing the active device are much thicker (by more than two orders of magnitude) than the gate oxide. In bulk CMOS technologies the isolation oxide, whether it is local-oxidation-of-silicon (LOCOS) or STI, thickness is typically greater than 300 nm.

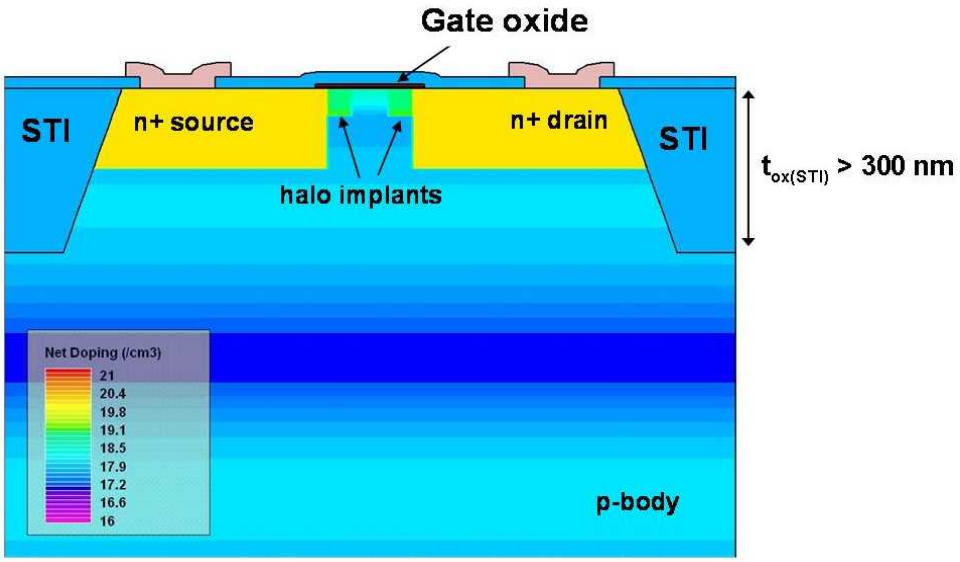

Fig. 17. Representative cross-section of a bulk n-channel MOSFET in a modern CMOS technology.

Fig. 18 shows the cross-sectional diagrams of n-channel MOSFETs with (a) LOCOS isolation and (b) STI. In Fig. 18, the radiation-induced charge buildup is indicated with the "**+**" symbol. For the case of LOCOS isolation, charge buildup occurs at the bird's beak region and along the base of the field oxide (extending from drain to source where the gate overlaps the thick field oxide). In STI oxides, radiation-induced charge will build up near the trench corner and along the base of the field oxide. In most deep-submicron technologies, LOCOS isolation has been replaced with STI and therefore radiation damage to STI oxides will be the primary focus in this dissertation.

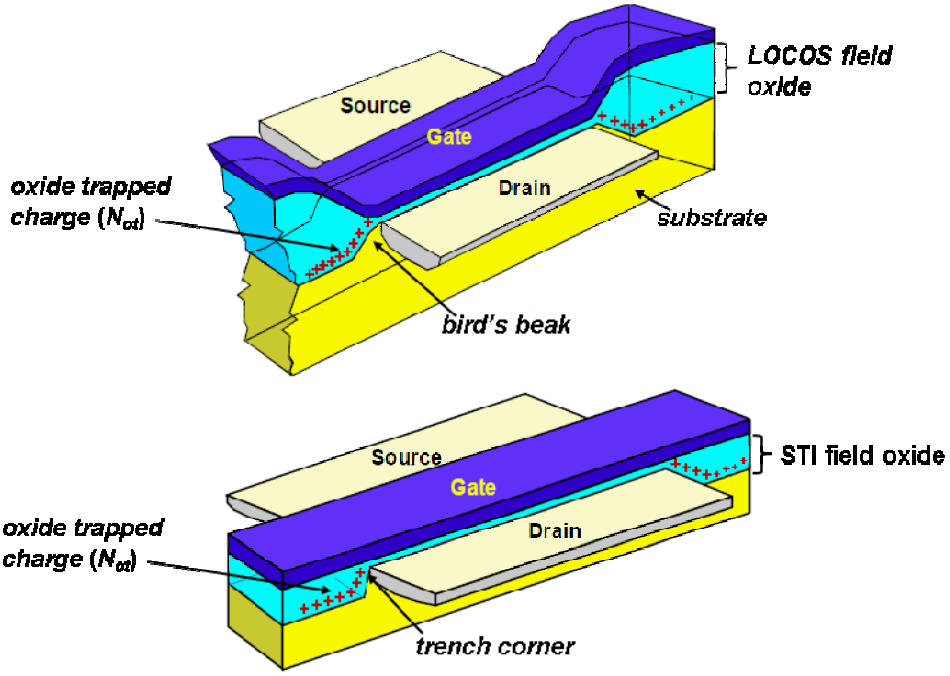

Fig. **Error! No text of specified style in document.**18 Cross-sectional diagrams of n-channel MOSFETs with (a) LOCOS isolation and (b) STI [54, 55].

The primary effect of field oxide charging is the creation of leakage paths that result in the degradation of device performance and IC functionality. The possible leakage paths that are typically associated with defect buildup along the base and sidewalls of field oxides are indicated on the layout of two inverters in parallel shown in Fig. 19. These are indicated as: (1) leakage between drain and source of an n-channel transistor, (2) leakage between the

n^+ drain/source regions of different n-channel devices, (3) leakage between an n-well of a p-channel device and the n^+ drain/source region of a nearby n-channel device, and (4) leakage between the n-well regions of two isolated p-channel devices.

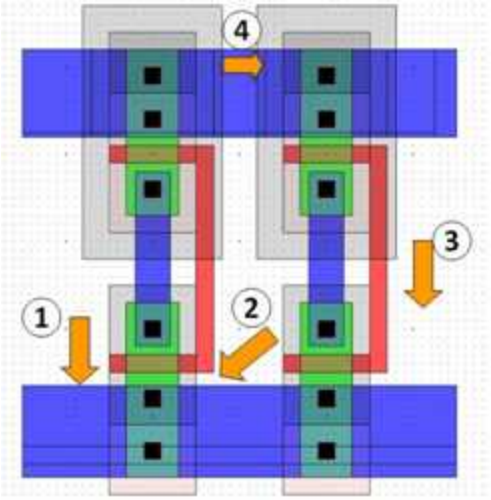

Fig. **Error! No text of specified style in document.**19. Layout of two inverters in parallel showing possible leakage paths associated with defect buildup along the base and sidewalls of field oxides [26].

Drain-to-source leakage is also referred to as edge leakage or intra-device leakage and is typically associated with the buildup of radiation-induced defects along the sidewall of the field oxides. This kind of leakage can typically be characterized by measuring the radiation-induced degradation of the I-V characteristics for a specific n-channel transistor.

The impact of STI radiation damage on the n-FET current-voltage characteristics of one deep sub-micron technology is shown in the experimental data in Fig. 20 [53]. These data were obtained from total ionizing dose (TID) measurements on 0.18 μm n-channel MOSFETs fabricated by the Taiwan Semiconductor Manufacturing Company (TSMC) [53]. The data show that off-state leakage current, $I_{d,off,}$ shows a significant monotonic increase above 200 krad(SiO2), reaching a level above 100 nA at 500 krad(SiO_2) of total dose [53].

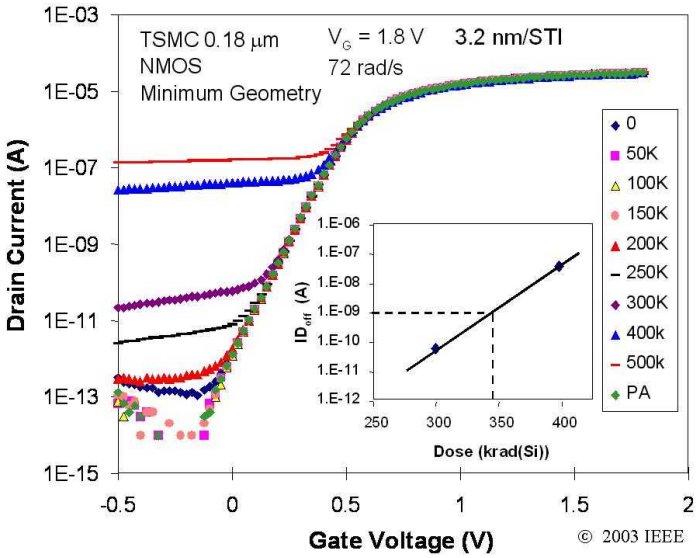

Fig. 20. Impact of STI radiation damage on the current-voltage characteristics of nFET fabricated in TSMC 0.18 □m CMOS [53].

The primary cause of increased $I_{d,off}$, is the reduction in threshold voltage and increase in drive current in the parasitic n-FET formed along the two edges of the "as drawn" device (Fig. 21a). Prior to radiation exposure, the threshold voltage is high and drive current is low for the parasitic device relative to the "as drawn" structure. Upon exposure to ionizing radiation, the threshold voltage of the parasitic device is reduced significantly relative to the "as drawn" transistor (Fig. 21b). This is because the "gate" oxide of the parasitic structure is formed from the STI, which is much thicker than the "as drawn" gate dielectric. In addition to negative voltage shifts, the drive current of the parasitic n-FET also increases significantly (Fig. 22b). This is due to the fact that the effective width of the parasitic transistor (Weff.), to which drive current is proportional, increases as surface along the STI sidewall inverts in response to Not buildup [56]. The degree to which ΔNot can invert this surface is also inversely proportional to the doping concentration along the sidewall [56]. Thus, a higher doping concentration in the p-type body will typically mitigate the effects of fixed oxide trapped charge in the STI or LOCOS isolation for older technologies.

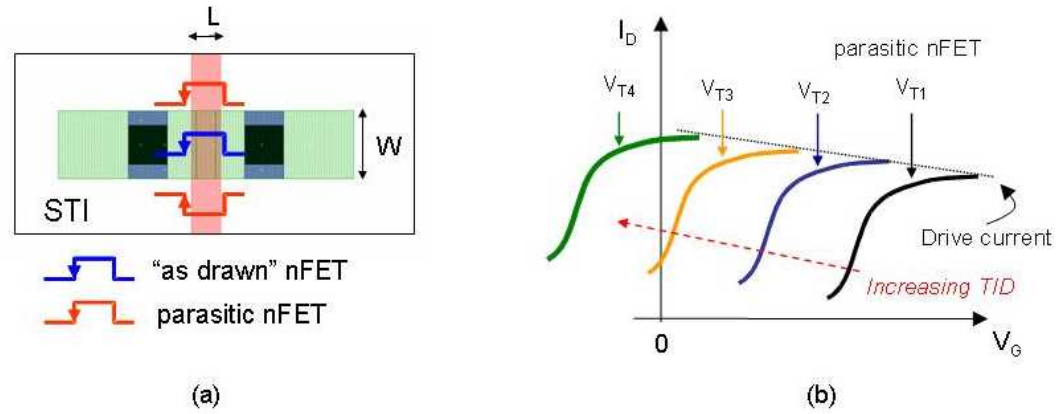

Fig. 21. a) Illustration of the circuit-level models associated with the n-channel MOSFET with parasitic nFETs, and b) the effects of increasing Total Ionizing Dose (TID) radiation exposure on the threshold voltage and drive current of the parasitic nFET [56].

In order to examine the scaling trends of drain-to-source leakage, the pre- and post irradiation Id vs. Vgs characteristics of a commercial 130 nm CMOS technology are shown in Fig. 22 [57]. These data indicate that negative voltage shifts in the parasitic edge devices are significantly smaller than the 180 nm TSMC technology (Fig. 20). The increased radiation tolerance of the 130 nm technology may be due to the aggressive use of halo implants. In advanced CMOS technologies, highly-doped halo implants are used to suppress short channel effects (SCEs). Like the thinning of gate oxides, this deep-sub-micron processing technique seems to be fortuitously increasing the radiation tolerance of modern CMOS devices. At the 130 nm node, where the physical gate length is below 100 nm, the halo doping may extend across the entire channel for minimum gate length devices. This significantly increases the p-type doping concentration along the entire STI sidewall, between the drain and source of the n-channel MOSFETs. The increased doping will inhibit the impact fixed oxide charge, thereby increasing the inherent radiation hardness of ultra-small bulk CMOS devices.

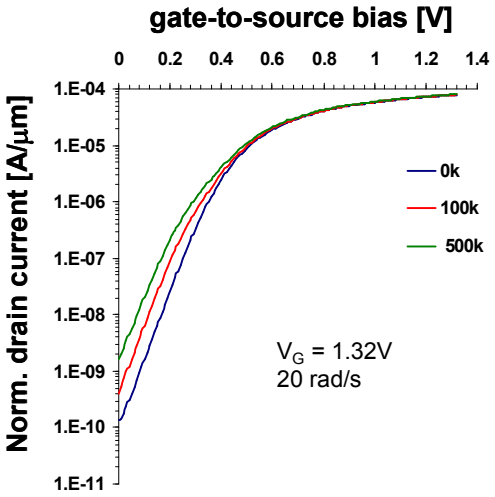

Fig. 22. Impact of STI radiation damage on the current-voltage characteristics of nFET fabricated in 0.13 □m CMOS [57].

Leakage that occurs between two separate devices (i.e. leakage paths 2, 3 and 4 in Fig. 19) is also known as under leakage or inter-device leakage and is typically associated with the buildup of radiation-induced defects along the base of the field oxides. Characterizing inter-device leakage requires specially designed test structures such as the FOXFETs or field-oxide capacitors (FOXCAPs). Shown in Fig. 23 is a cross-sectional diagram indicating drain-to-source and leakage (l) and leakage between the n+ source/drain region of an n-channel device and the n-well region of an adjacent p-channel device (2).

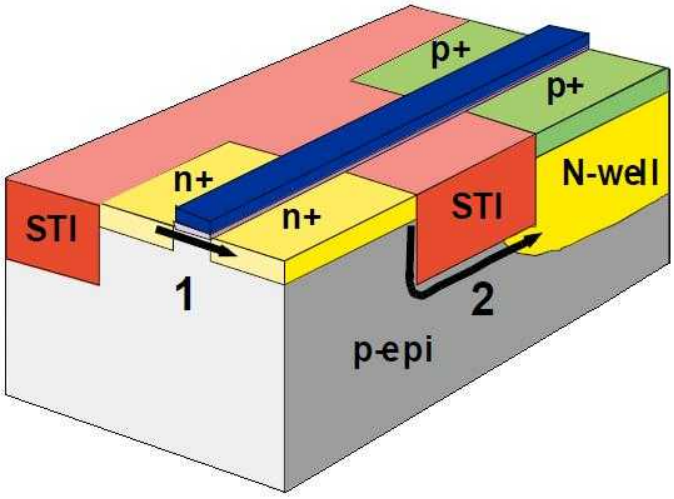

Fig. 23 Cross-sectional diagram indicating: (1) drain-to-source leakage and (2) leakage between the n+ source/drain region of an n-channel device and the n-well region of an adjacent p-channel device [54, 55].

The impact of inter-device leakage on the supply current can be observed in the following inverter chain example, shown in Fig. 24 below. Path (a) represents the leakage path caused by n-FET device-to-device leakage. The bold line corresponds to the radiation-induced parasitic path between two n-FET drains. The current path from VDD to ground is completed via the second stage p-FET and first stage n-FET, both biased in their linear region in this example. Path (b) represents the leakage path caused by n-FET drain/source-to-n-well leakage. The bold line corresponds to the radiation-induced parasitic path between the first stage n-FET drain and the n-well of the first stage p-FET. Here the current path from VDD to ground is completed via the first stage n-FET biased in its linear region in this example.

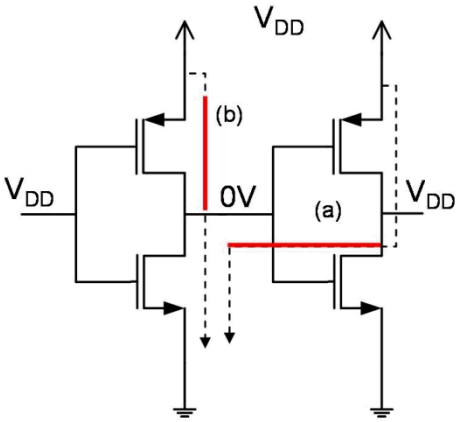

Fig. 24. Example of how inter-device leakage can increase the supply current of inverter chain. Path (a) represents the leakage path caused by n-FET device-to-device leakage. Path (b) represents the leakage path caused by n-FET drain/source to p-FET n-well leakage.

4.1.2 Silicon On Insulator

4.1.3 Radiation Effects on SRAM

** Terence Stuff

Since high operating temperature caused by increased current is the likely cause of failure, the circuit having the highest power consumption or current density is most likely the failing circuit. Since, presumably, leakage paths are created everywhere in the die (under all field oxides), it is possible that the magnitude of the leakage current is flow uniform across the die. Thus, the temperature is constant everywhere on the surface of the die at any given time. However, it is also possible that some circuits, by design, generate a higher leakage current density when radiation-induced leakage paths are created. In that case, the largest leakage currents are localized at specific regions of the chip which would lead to temperature variability across the die surface. That is, one area is hotter than another area of the die. To determine which scenario is occurring on the part (uniform or non-uniform leakage current density), photoemission testing is performed. Photoemission microscopy (PEM) is a popular and practical technique for locating defects or areas of high current density on a silicon device. It takes advantage on the transparency of common semiconductor materials to infrared (IR) light to allow the imaging of structures beneath the surface of the IC. The basic theory of operation is as follows. At a forward-biased p-n junction, the barrier to the diffusion of majority carriers is reduced. The reduced barrier, in turn, permits a net transfer of holes from the p-side to the n-side and of electrons from the n-side to the p-side. Some of these hole-electron pairs recombine as they travel through the space-charge region. When an electron-hole pair recombination takes place, a photon is emitted. This process is known as radiant recombination. The wavelength of the photon is about 1100 nm, which is in the IR region (400-1500 nm). The function of the photoemission microscope is to detect these IR-region photons. Any photon activity that is detected is marked by a red spot (called hot-spot) on the resultant picture. The more intense the recombination (e.g. high forward-bias current), the brighter the red spot becomes. Therefore, non-ideal response, such as CMOS latch up, saturated transistors, and electrostatic discharge damage can be imaged since all these events involve forward-biased junctions [22], [23]. Recent publications [23], [24] suggest that PEM can also detect areas of high ohmic currents in silicon (e.g. radiation-induced leakage currents, MOS devices operating in linear region) if the carrier density is locally high enough. It is important to note that emission spots do not necessarily mean defects or failures, just high current density. PEM failure localization requires a control part for comparison. This requires decapsulating a pre-rad and post-rad (but before failure) part and observing them under a photoemissions microscope while both parts are under bias.

If leakage currents are uniformly distributed over the device, the picture would be covered by a sea of faint red spots. If leakage currents are not uniformly distributed, only the areas of high current density would be overlaid by bright red spots in the picture. The picture of the radiated part shows the latter. In fact, there are many brighter, isolated spots in the RAM cells (picture of pre-rad part shows no emission spots in the RAM cells). Thus, the RAM cells have the highest current and power density. Also, the RAM cells have a higher operating temperature than the rest of the modules.

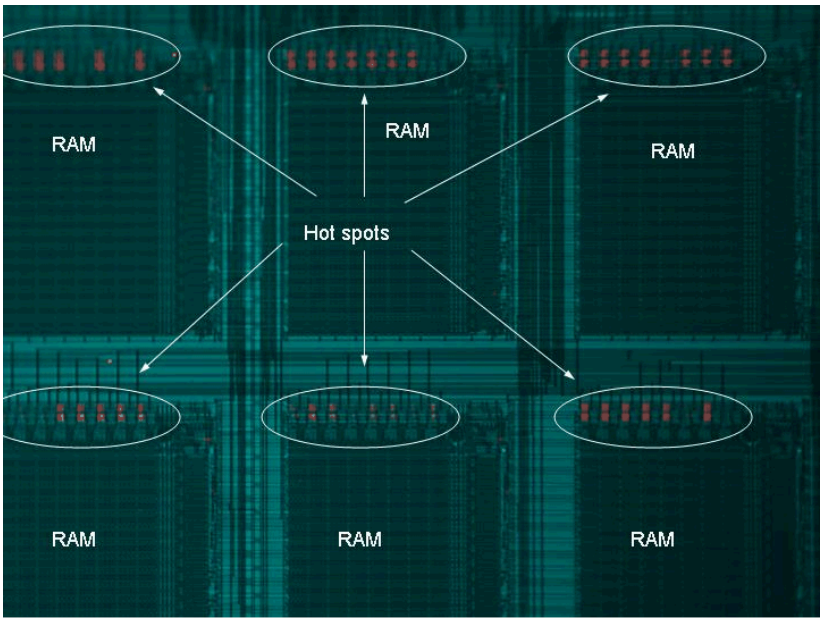

Fig 5.9: Photoemission of post-rad SRAM cells

In the TI-MSC1211, there are a total of 10 RAM cells, 6 of which are shown in figure 5.9. Each RAM cell has 128 byte-addressable locations. The 128 bytes are partitioned into 4 columns of 32-bit word lines. There are 8 identical planes, with each plane representing one bit of the byte-addressable data. The diagram below shows a detailed block diagram of the RAM cell.

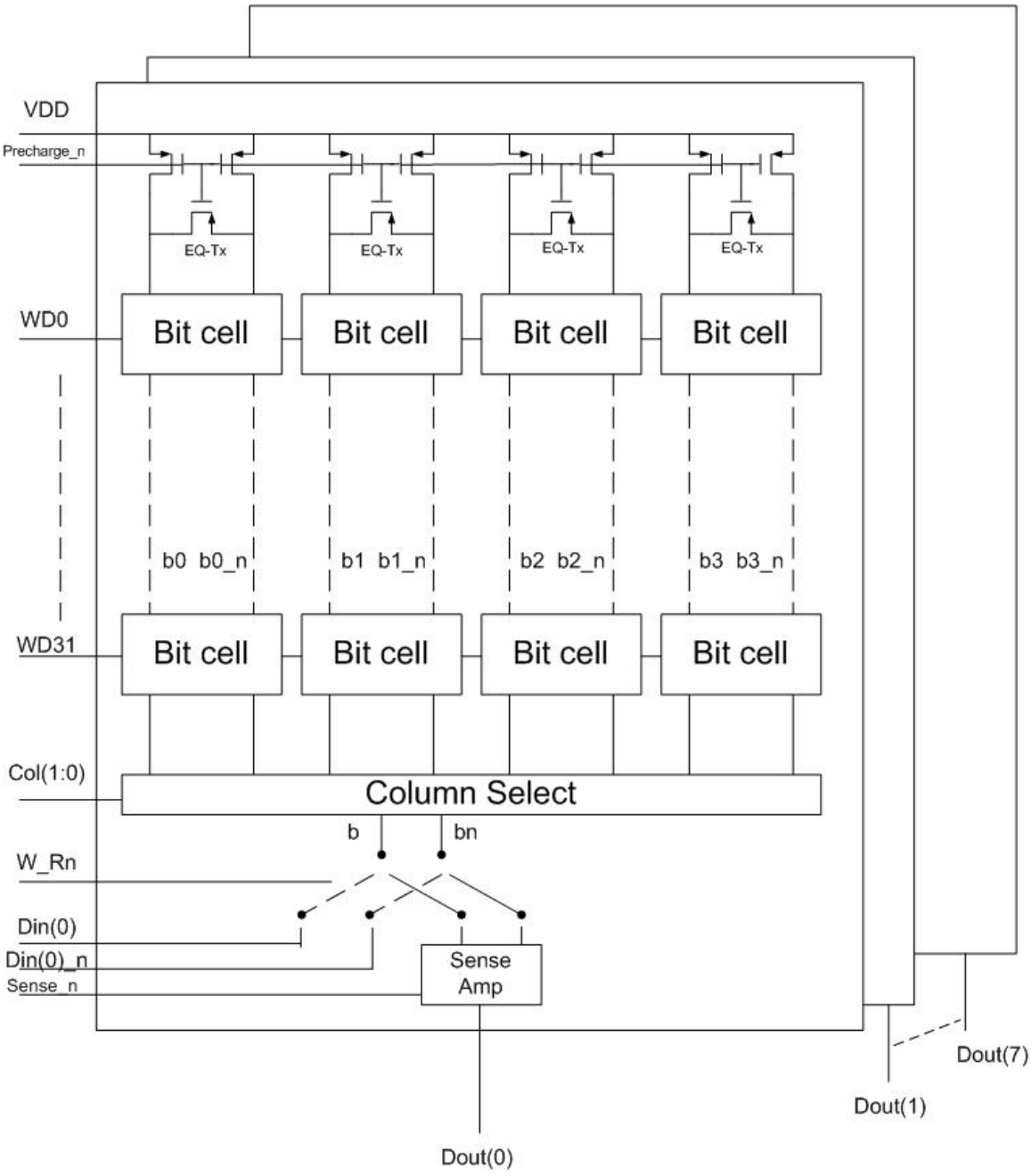

Fig 5.10 Schematic of SRAM cell

Signals driving the word lines WD0 to WD31 and column select (col(1:0)) lines are generated in the address decoding circuit (not shown). WD0 to WD31 select the desired row of bit cells (at most, only one line is active at any given time). Of those bit cells, column select lines col(1:0) are used to select the appropriate cell. Thus, one bit-cell is selected at most at any given time per plane. By default, all word lines are deactivated (logic value 0), that is, no bit cell is selected.

The write enable line W_Rn is used to determine the direction of the b and bn lines. If it is set to logic 1, the data input lines DIN(7:0) and DIN(7:0)_n drive b and bn lines. In other words, a write operation is performed. Otherwise, b and bn lines drive the inputs to the sense amplifier. In other words, a read operation is performed. By default, the line is at logic 0 i.e. in read mode.

The differential sense amplifier amplifies the voltage difference between the b and bn lines. This reduces read access time. The driving capability of a single bit-cell is poor. If b and bn

lines were connected directly to an external bus, the additional capacitance would cause their transition times (high-to-low time or low-to-high time) to become extremely slow. The amplifier compensates for the restricted fan-out driving capability [25]. The bit lines b and bn are connected to the positive and negative input terminals of the amplifier. There are three steps to the read operation. First, all the bit lines (b0, b0_n, b1,…, b3_n) are precharged to VDD by forcing the line precharge_n low. Simultaneously, the equalization p-channel devices (labeled EQ-Tx in figure 5.10) are turned on, ensuring that the voltages on both bit lines are equal so that no difference voltage exists across the inputs of the sense amplifier. Next, the precharge and equalization devices are disabled and the correct bit is selected by enabling one of the word lines and one of the column lines. For each of the 8 sense amplifiers (there is one for each memory plane), one input line is pulled low by the selected bit-cell. The third step involves enabling the sense amplifier. Once a fixed amount of time has elapsed, the sense amplifier is enabled by forcing the sense_n line low. The elapsed time must be long enough so that the appropriate input line has sufficient time to discharge. A sufficient differential voltage (approximately 0.5-1 V) must be present at the differential inputs before the sense amplifier is activated. By default, the sense_n line is set to logic 1 i.e. the sense amplifier is disabled.

When the TI-MSC1211 is initially powered on, the RAM is, by default, in precharge mode, that is, precharge_n is logic 0. Under this condition, all word lines are deactivated, W_Rn line is at logic 0, and sense_n line is at logic 1. Inspection of the photoemission results suggests the hot spots are located in the p-channel transistors used for precharging. However, a leakage path is not formed in p-channel transistors as a result of irradiation. To explain why these transistors have such high current densities after irradiation, the interaction between leakage paths in the single bit cells and the precharging circuitry must be studied. The following diagram shows the connections between a standard bit cell and the precharge p-channel devices.

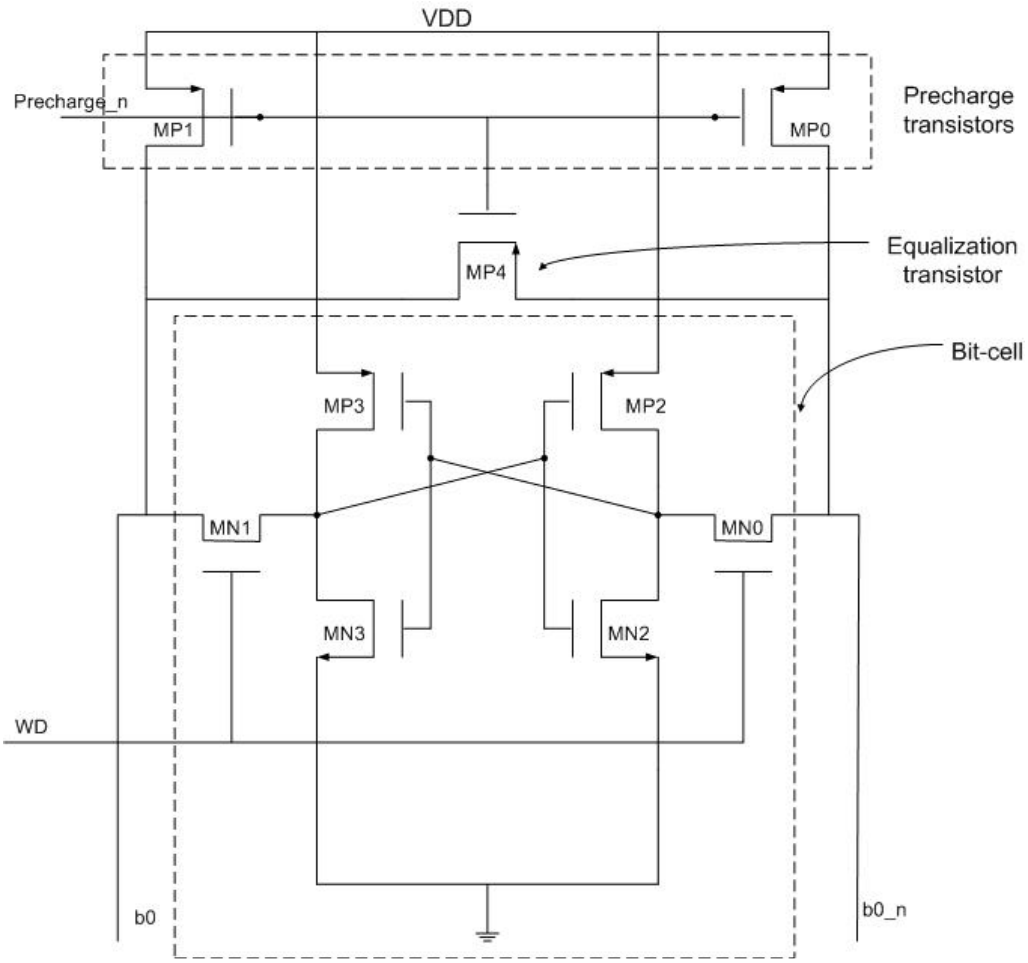

Fig 5.11: RAM bit-cell pre-radiation .

The p-channel devices MP0, MP1, and MP4 are on because the precharge_n signal is at logic 0. Since default value of WD is at logic 0 and the sense amplifier is disabled (default value of sense_n is logic 1), there is no path for current to flow between VDD and GND. The result is that both b0 and b0_n are connected to VDD via transistors MP1 and MP0, respectively. That is, b0 and b0_n are pulled to logic 1. For a post-radiated device, the situation can be illustrated in the following diagram.

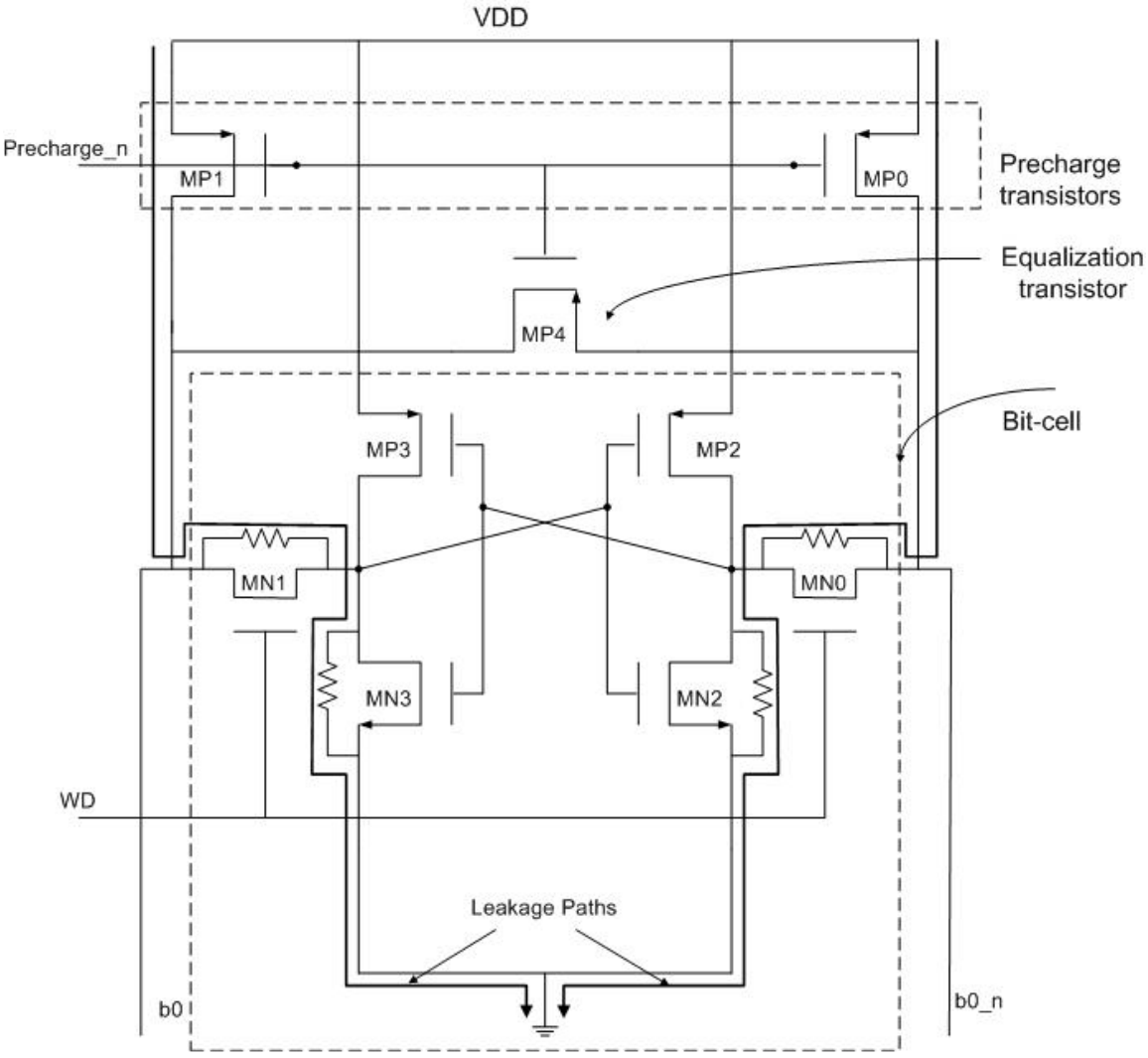

Fig 5.12: bit-cell post-radiation.

Trapped charge in the field oxide around devices MN0, MN1, MN2, and MN3 has created an inversion layer under the field oxide. This allows current to flow between the source and drain even though the gate voltage is below the threshold voltage, thereby dissipating power. For illustration purposes, these drain-source leakage paths are represented by placing a resistor between the drain and source terminals in figure 5.11. There are two leakage paths from power to ground for each cell. Since there are 32 bit cells connected in parallel to the bit lines b0 and 0_n, the precharge devices MP0 and MP1 have to supply current for all 32 parallel paths to ground. Thus, the current flowing through the precharge transistors should be 32 times higher than the leakage current for a single n-channel device. Thus, transistors MP0 and MP1 in figure 5.11 are continuously dissipating relatively large amounts of static power during precharge. There are 4 sets of precharge transistors per plane and 8 planes in one RAM cell. The photoemission picture (figure 5.9) shows the brightest red sports are located in the RAM cells. Thus, the current densities of the RAM

cells are higher than other modules and are operating at a higher temperature than other modules.

The circuit responsible for the catastrophic failure is likely the same circuit that has the highest operating temperature. The evidence and analysis presented in this section strongly suggests that the RAM cells are responsible for the failure. However, it is also possible that the RAM cells are heating up neighboring circuits causing them to operate under excessive temperatures. Determining which scenario is correct could be an area for future study.

4.1.4 Hardening by Design

4.2 Dynamic RAM

4.3 NAND and Flash NVM

5 Radiation Effects in Resistance Change Memory Technologies

5.1 Phase Change

5.2 Magnetoresisitive RAM

5.3 Resistive Switching Memory

6 Summary

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