SAND2013-4762C

Use of the TurboSiP© Software to Predict the Long-Term Reliability of Solder Joints on Photovoltaic Systems

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***Abstract* — The TurboSiP© software predicts the thermal mechanical fatigue (TMF) of commonly used solder joints. The input parameters are package materials, interconnection design, solder alloy (Sn-Pb or Pb-free), and the environment. This computational tool was used to predict the TMF lifetimes of (a) collector circuit solder joints used in photovoltaic solar panel systems as well as (b) 1206 chip capacitor and (c) 14 I/O SOIC package solder joints on the printed circuit boards of the inverter module. All interconnections were analyzed as having the eutectic Sn-Pb solder. A service temperature cycle was defined from data logger parameters. Accelerated aging test conditions were also evaluated in the software. The TurboSiP© predicted lifetimes for the collector circuit as well as convention component solder joints that were more-than-adequate to meet the customer's requirements.**

***Index Terms* — photovoltaic systems, accelerated life testing, rainflow counting, thermomechanical solder fatigue**

I. INTRODUCTION

Thermal mechanical fatigue (TMF) is a commonly-observed failure mode of solder interconnections that are subjected to severe temperature environments. An example of the TMF fracture of a surface mount component solder joint is shown in Figure 1, in this case, a small resonator device. Thermal mechanical fatigue, which is a variant of the low-cycle fatigue category, occurs when two conditions are present: First, there is a mismatch in coefficients of thermal expansion (CTEs) between the two substrate materials that are joined together (referred to as the global CTE mismatch) and/or between the solder alloy and the substrate materials (local CTE mismatch). The second condition is the presence of a temperature cycle. Under the temperature cycle, dissimilar expansions and contractions take place in the materials due their different respective CTE values. The result is the creating cyclic mechanical strains in the materials that lead to fatigue deformation in the solder and subsequently, cracking that caused failure of the interconnection (Figure 1).

Computational materials model can provide a timely, cost-effective means to predict the TMF of solder interconnections. Modeling provides a tool for investigating the effects of different materials, geometries, and environmental conditions on the reliability of solder joints without the need for extensive experimental programs. The rapid growth in the capabilities of computer hardware has allowed for the development of more complex software applications, including those with the ability to predict materials deformation behavior. Such a software package has been developed by Sandia National Laboratories that, in this case, predicts solder joint TMF. The software is referred to as TurboSiP© (a registered trademark of Sandia Corporation) and can be used for analyzing the TMF behavior of common solder joint configurations found on printed circuit boards and structural applications. The engineer inputs into the software (a) the solder joint geometry, (b) the material properties (e.g., CTE, elastic modulus, etc.) and (c) the temperature environment. The software predicts the deformation contours expected from the stress field as well as crack initiation and propagation, all as a function of the number of temperature cycles.

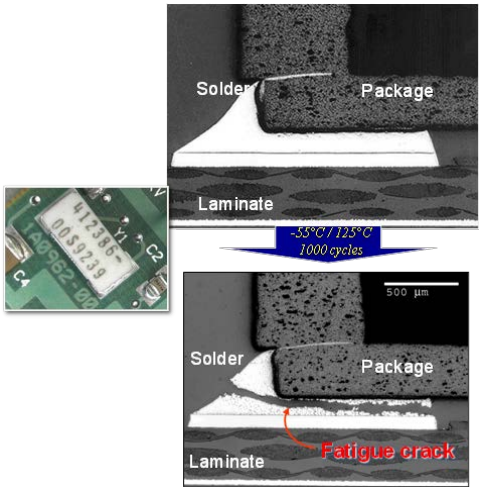
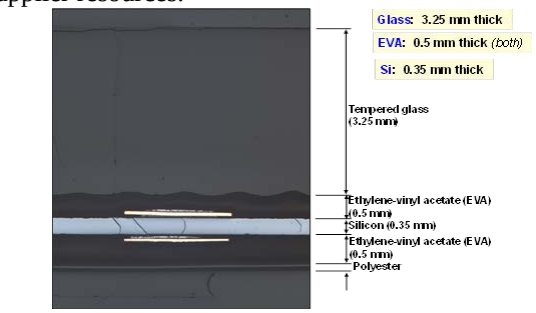


Figure 1. Cross section micrographs show the TMF crack in the solder joint of a surface mount component (-55°C/125°C; 1000 cycles).

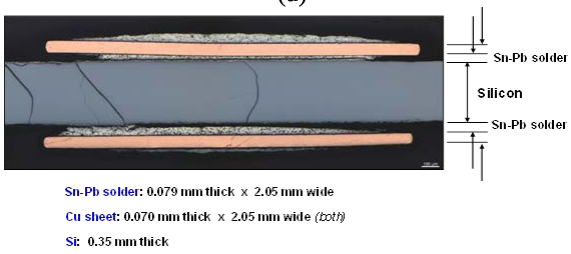
II. ANALYSIS

The TurboSiP© software was used to investigate the TMF of 63Sn-37Pb (wt.%, abbreviated Sn-Pb) solder joints found on (a) the collection circuitry on the front face of the photovoltaic panel and (b) the printed wiring assembly electronics on the backside of the panel product. In the case of the collection circuitry that is connects together the silicon (Si) modules on the front, it was necessary to subject a unit to destructive analysis in order to obtain the details of the solder joint

structure. A panel was cut into segments of gradually smaller size. The smallest portion was then further dissected using metallographic cross section techniques to determine the construction details. The optical micrographs in Figure 2 illustrate the construction of the solder joint on the module side of the panel. Figure 2a shows the overall "stack-up" of materials while Figure 2b shows the details of the solder interconnection. The mechanical properties were documented for those parts using either existing data libraries or referring to supplier resources.



(a)



(b)

Figure 2. (a) Low magnification optical micrograph shows the stack-up of materials on the module side of the panel. (b) High magnification micrograph shows the construction details of the solder joint.

As noted, the TurboSiP© software was also used to predict the TMF of solder joints on two commonly used the printed wiring assembly components. Those components were the 1206 size, leadless ceramic chip capacitor and a 14 I/O small-outline integrated circuit (SOIC) package. The latter used gull-wing leads to form the interconnections to the printed circuit board. The packages and the configurations of the respective solder joints are shown in Figure 3. The geometries of these two package types, as well as layout of the associated printed circuit board pads, have all been standardized by the electronics industry and are a part of the TurboSiP© software library.

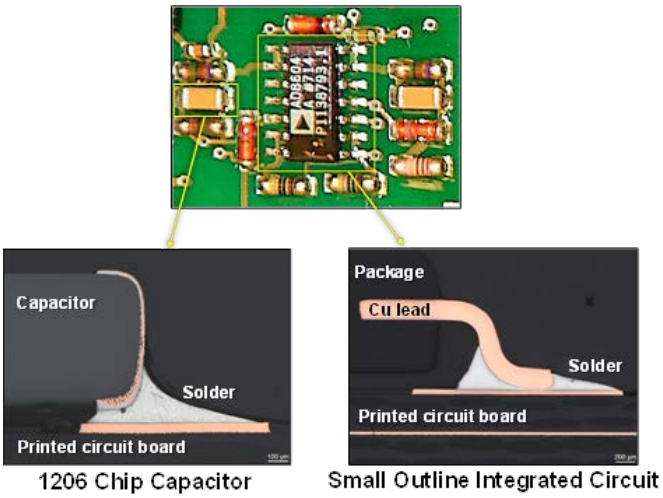


Figure 3. Stereo photograph and optical micrograph show the packages and solder joints of the 1206 chip capacitor and SOIC component that were modeled using the TurboSiP© software.

The more challenging effort of this analysis was the identification of an appropriate temperature cycle. Although data logging can provide a very detailed account of temperature variations down to several minutes, the TurboSiP© software has a limitation on the complexity of the cycles that can be addressed by it. A one-day service cycle was derived from such a collection of information. The minimum and maximum temperatures were 20°C and 60°C.

III. EXPERIMENTAL RESULTS

The finite element mesh of the collection circuit solder joint is shown in Figure 4. The detailed view identifies the Si module substrate, Sn-Pb solder, and Cu sheet substrate that together comprise the interconnection. The extent of TMF cracking is illustrated in Figure 3 for the service cycle of 20°C/60°C. Crack initiation occurred at 30,000 thermal cycles (82 years). The cracks initiated at the outer edges of the solder joint and at the latter's interface with the Si plate where there is a significant stress concentration caused by the dissimilar materials. Also, the asymmetry of the materials stack caused the cracks to develop preferentially in the lower solder joint. The cracks propagate towards the center of the joint as indicated by the white arrows. Cracking continued to completion (≈100%) after 165,000 cycles (165,000 cycles ÷ 365 cycles/year = 452 years !). Because the predictive fidelity of the model is greatest in the several hundreds to approximately 10,000 cycles, values of 30,000 and 165,000 signify an "unlimited" lifetime to the solder.

Crack propagation has also initiated in the top solder joint. The black arrows show the length of the top joint cracks after 165,000 cycles.

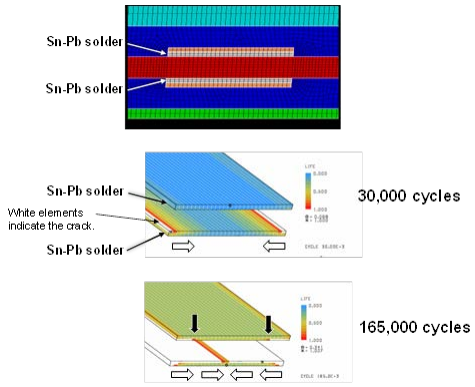


Figure 4. Finite element mesh of the module collection circuit solder joint with software predictions of TMF cracking under the service environment (20°C/60°C)

The fact that the solder joints appear to have unlimited service lifetime necessitates that an assessment be made of the next likely failure event, which is the low-cycle fatigue of the Cu sheet conductors. That analysis cannot be performed by the TurboSiP© software. Instead, a more intricate computational materials model will be used to perform that assessment.

The 1206 chip capacitor solder joints were examined with the TurboSiP© software (Figure 5). A quarter-symmetry was used in the TurboSiP© computations, which is constructed by "slicing" the component along two symmetry planes. One symmetry plane, which is label in the image, slices the capacitor in-half along its long dimension, including the solder joint. The second plane cuts the capacitor in half between the solder joints. The three images below the finite element mesh show the TMF damage contours and crack propagation (20°C/60°C service cycle) after 2,000 cycles (5.5 years), 14,000 cycles (38 years), and 36,000 cycles (99 years). The latter case represents the instance of complete failure. The crack path that actually causes the final failure of the interconnection is located up the face of the capacitor termination.

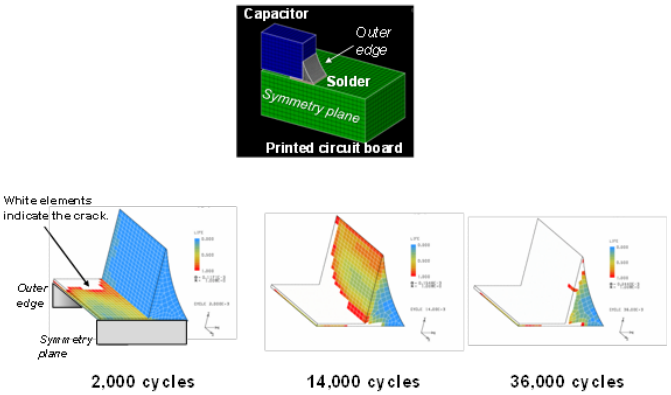


Figure 5. Finite element mesh is shown of the 1206 capacitor using the quarter symmetry. The model predictions are depicted for TMF deformation and cracking (white elements) of the solder joints (20°C/60°C) using a downwards view of the joints. The images depict the degradation after 2,000 cycles, 14,000 cycles, and 36,000 cycles (final failure).

The TurboSiP© computations also addressed the TMF of 14 I/O SOIC solder joints. The finite element mesh is shown in Figure 6 that represents the quarter symmetry of this package. Since there is an odd number of gull-wing leads per side (seven and seven), the symmetry plane extends down the middle of the center lead (labeled "4" in the picture) as well as its associated solder joint. The model computations of TMF are shown in the contour plots at the bottom of the figure. Note that the view provided by the finite element mesh at the top of the figure is downwards while the view is upwards of the solder joints in order to clearly show the crack development. Very limited cracking is observed after 45,000 cycles (123 years!). A complete failure was observed after 330,000 years (904 years!). The crack path at final failure is along the solder/Cu pad interface, the latter belonging to the printed circuit board. Clearly, like the 1206 chip capacitor, the SOIC solder joint have, for all intents-and-purposes, exhibited an unlimited lifetime under the 20°C/60°C temperature cycle.

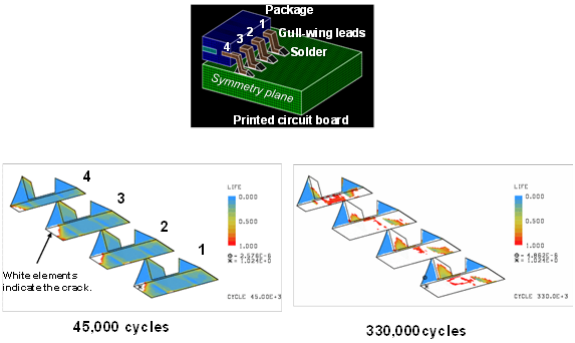


Figure 6. Finite element mesh of the 14 I/O SOIC package using the quarter symmetry. The model predictions are depicted of TMF deformation and cracking (white elements) of the solder joints (20°C/60°C).

The TurboSiP© software also provides a tool for estimating TMF failures under accelerated aging conditions. Besides the fact that the software expressly calculates the cycles to failure, acceleration factors can also be determined to correlate the accelerated aging test results to the service life reliability. Accelerated aging profiles differentiated by the minimum and maximum temperatures: 0°C/100°C and the more severe case of -55°C/125°C. The hold times (15 min) and uniform ramp rates (6°C/min) are the same for either cycle. The number of cycles required to start a crack are listed in Table 1 for each the three solder joint types and three environments. An acceleration factor (AF) was also calculated for each of the accelerated aging conditions, based on the service cycle (20°C/60°C) being the baseline (AF=1). The AF is the ratio of cycles to crack initiation or failure at service over the cycles to crack initiation or failure in the accelerated aging test. For example, if there was available empirical temperature cycle data (e.g., -55°C/125°C) for the collection circuit solder joints that confirmed failure at 6,000 cycles, the AF would predict those solder joints to fail after 165,000 service life cycles.

Table 1. The TurboSiP© predictions of cycles for TMF crack initiation and propagation to failure for the three solder joint geometries and three environments..

Component	Temperature Cycle (°C)	Cycles to Start the Crack	AF – Start the Crack	Cycles to Finish the Crack	AF – Finish the Crack
Collection Circuit	20°C/60°C *(service)*	43,000	1	165,000	1
	0°C/100°C	2,400	17.9	20,000	8.25
	-55°C/125°C	425	101	6,000	27.5
1206 Chip Capacitor	20°C/60°C *(service)*	19,600	1	240,000	1
	0°C/100°C	1,500	13.1	36,000	6.67
	-55°C/125°C	300	65.3	11,000	21.8
14 I/O SOIC	20°C/60°C *(service)*	552,600	1	4,000,000	1
	0°C/100°C	35,000	15.8	330,000	12.1
	-55°C/125°C	5,300	104	62,500	64.0

IV SUMMARY

1. TurboSiP© is a software tool for predicting the TMF of commonly used solder joints. The input parameters include package materials, interconnection design, solder alloy (Sn-Pb or Pb-free), and the environment.
2. This software was used to predict the TMF lifetimes of crystalline silicon module collector circuit solder joints. The specific cases were the TMF reliability of 1206 chip capacitor and 14 I/O SOIC components soldered to a printed circuit board. A service temperature cycle was defined based on measured thermal profiles. Accelerated aging test conditions were also exercised in the software.
3. Simulations showed that both the module circuit, the 1206 capacitor and SOIC component solder possessed sufficient service lifetime to meet the customer's operational expectations.

ACKNOWLEDGEMENT

Sandia National Laboratories is a multi-program laboratory managed and Security Administration under contract DE-AC04-94AL85000. This work was funded by the US Department of Energy Solar Energy Technologies Program.

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