A GATE DRIVE CIRCUIT FOR GATE-TURN-OFF (GTO) DEVICES IN SERIES STACK*

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Abstract

A gate-turn-off (GTO) switch is under development at the Advanced Photon Source as a replacement for a thyratron switch in high power pulsed application [1]. The high voltage in the application requires multiple GTOs connected in series. One component that is critical to the success of GTO operation is the gate drive circuit. The gate drive circuit has to provide fast high-current pulses to the GTO gate for fast turn-on and turn-off. It also has to be able to operate while floating at high voltage. This paper describes a gate drive circuit that meets these requirements.

1 INTRODUCTION

The relatively low voltage ratings of GTO devices compared to thyratrons require the series connection of these devices when used as replacement in certain thyratron applications. For this series configuration, a basic requirement is a gate driver circuit that can be operated at a high floating potential.

The gate current requirement of the GTO used in the study, Westcode WG10040R36, is listed in Table 1. The turn-on gate current has two components, a fast initial pulse and a constant component. The leading edge portion of the current pulse is two to three times the value required to sustain the on state of the device. The high initial current is needed to supply charge quickly into the nonlinear gate capacity of the GTO in order to reduce its turn-on time. The recommended amplitude by Westcode is between 70 and 100 amperes. After the GTO device is turned on, a substantial amount of gate current is still needed to maintain a low on-state resistance and, hence, a low voltage drop across the GTO's anode and cathode.

Table 1: GTO gate current requirement

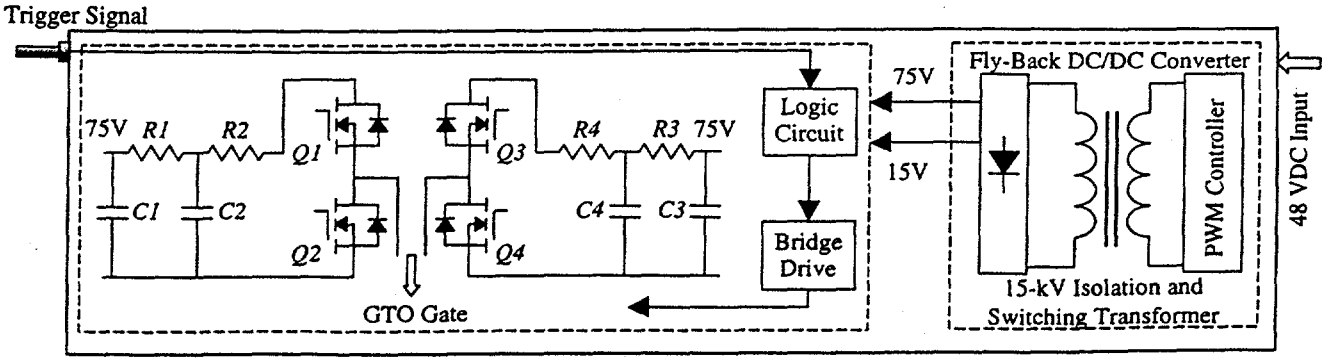
	Initial Current	Sustained Current
Turn On	70 ~ 100A	20 ~ 50A
Turn Off	> 100A	-

During the turn-off process, a large current is required in the reverse direction to remove charges from the junction and restore the forward-voltage-blocking capability. The amplitude of the turn-off gate current can be much greater than that required for turn-on, depending on the current at which the GTO is trying to turn off. The greater the turn-off current, the greater the amplitude has to be. The speed of the GTO's recovery depends on how fast the charge is removed.

A low-leakage-inductance pulse transformer, which also provides the high voltage isolation, can be used to supply the leading edge portion of the current pulse. The current level needed to keep the on-state resistance low for the duration of the on state, however, will most likely be provided by some other means if this duration is in many microseconds.

2 DIRECT GATE DRIVE CIRCUIT

A direct gate drive circuit has been developed for the GTOs. As shown in Figure 1, the output of the drive circuit is connected directly to the GTO gate without a pulse transformer. The drive circuit is divided into two sections, a low voltage section and a high voltage section. The low voltage section contains a fly-back type DC/DC converter that provides the required power for the high voltage section. The high voltage section has the control



$R1 = 1.2\Omega$, $R2 = 0.5\Omega$, $C1 = 220\mu F$, $C2 = 4.4\mu F$, $R3 = 30\Omega$, $R4 = 0.25\Omega$, $C3 = 220\mu F$, $C4 = 6.6\mu F$

Figure 1: Block diagram of the GTO gate drive circuit

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logic and GTO gate drive circuitry. A high-frequency switching transformer couples the two sections providing the energy transfer and the necessary high voltage isolation.

2.1 DC/DC Converter

The fly-back type DC/DC converter uses a current mode pulse-width modulation (PWM) controller chip, UC2844, with a power MOSFET, IRF640, driving a custom-wound high-frequency and high-voltage isolation (15 kV) transformer. The PWM controller operates at a nominal frequency of 90 kHz. The converter is designed for a 1-A maximum switching current at 50% duty cycle, resulting in a power transfer from the low-voltage section to the high-voltage section of approximately 13 watts maximum. A set of voltage and current switching waveforms is shown in Figure 2.

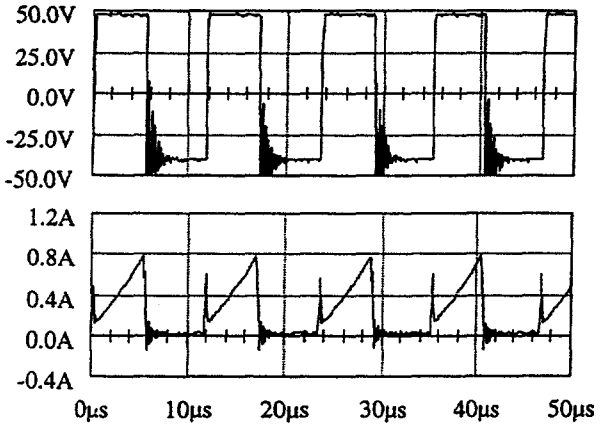

Figure 2: Converter switching voltage and current

Input power to the converter is 48 VDC. The switching transformer has one input winding of ten turns and three output windings of seventeen turns, four turns, and two turns, respectively, all made from #22, 15-kVDC wire. The input winding conducts a ramping current of up to one ampere when the MOSFET turns on. The stored energy in the primary winding is then transferred to the output windings when the MOSFET turns off.

The two-turn output provides a feedback signal to the PWM controller for voltage regulation. A resistor divider reduces the feedback signal before sending it to the voltage feedback input pin of the PWM controller. A variable resistor in the divider is used to adjust the level of the feedback voltage and, in turn, to set the output voltage. The four-turn output is rectified and regulated to supply 15-V power to the logic circuit and the MOSFET drive in the high-voltage section. The seventeen-turn output feeds two rectifiers to charge two dual *RC* circuits to 75 volts.

Taking advantage of the insulation property of ferrite, the switching transformer uses a ferrite toroid, P44914-TC from Magnetics, as the core. The criteria for choosing the type of ferrite core are the need for a large window to accommodate the windings, which are relatively large due to the high-voltage insulation, and low core losses.

2.2 Gate Circuit

The drive circuit is based on power MOSFETs connected in an H-bridge configuration. Figure 1 shows the basic bridge circuits with the *RC* networks that shape and deliver current to the GTO gate. *R1*, *R2*, *C1*, and *C2* are for turn on, while *R3*, *R4*, *C3* and *C4* are for turn off.

During turn on, for a given supply voltage, *R2*, *C2*, the MOSFET bridge on-state resistance, GTO gate resistance, and the stray inductance (which cannot be ignored in this case because of the speed of the pulse) determine the amplitude and duration of the fast component of the current pulse to the GTO gate. The level of the bridge output current after the leading edge portion is mainly determined by resistors *R1* and *R2*. The bridge on-state resistance and the GTO gate resistance are very small compared to the sum of *R1* and *R2* and, therefore, have little effect on the current level after the initial pulse. The relatively large time constant of *R1C1* compared to *R2C2* guarantees that the bridge output current remains essentially constant for the duration of the pulse after the initial high current component dies out.

The requirement for initial GTO device turn-off is similar to the one for turn-on. A large negative short-duration current pulse is produced by the turn-off network, *R3*, *C3*, *R4*, and *C4*, to quickly remove the stored charge in the gate structure of the device. The amplitude of this pulse can be much higher than that required for turn-on, depending on how much current the GTO is forced to turn off. While a substantial amount of current is required to maintain the low on-state resistance of the device, a negative gate voltage of only a few volts is needed to keep it off after the stored gate charge is removed by the initial current pulse. In this case *R3* is much greater than *R1*. The turn-off process continues after the initial pulse terminates. Although the device recovers its reverse blocking capability shortly after this negative current pulse, its forward blocking capability returns much more slowly. This recovery lasts many microseconds after the initial negative pulse.

Both the rise time and the amplitude of the gate current are affected by the stray inductance in the circuit. To achieve a fast gate current pulse, the stray inductance has to be minimized. For this reason, low inductance components are used, short and wide traces are employed on the PC board, and the connection between the gate drive board and the GTO is kept at the minimum length.

Two MOSFETs are connected in parallel to form each switch section of the H-bridge because of the high speed and current demand of the GTO gate. Since the resistance in the *RC* circuit for the initial fast pulse is only a fraction of an ohm, the MOSFETs need to have a low on-state resistance in order not to affect the amplitude of the gate

current. Power MOSFET IRF540N from International Rectifier was chosen for its very low on-state resistance, 0.052Ω, and large drain current rating, 27A.

2.3 Operation

In the normal off state of the H-bridge, *Q1*, *Q3* and *Q4* are off while *Q2* is on. *Q2* provides a return path for a bias circuit (not shown in Figure 1) to provide a negative bias of about -3V to the GTO gate. At the leading edge of the input trigger signal, *Q2* shuts off while *Q1* and *Q4* are driven on and held on for the duration of the trigger signal.

The width of the on pulse is controlled by the trigger signal. Since several GTOs are connected in series and GTOs have different turn-on and turn-off speeds, the leading edge and the trailing edge of each trigger signal are independently controlled in order to turn on or turn off all the GTOs at the same time.

At the termination of the trigger pulse, the GTO turn-off process is started. *Q1* and *Q4* are turned off while *Q2* and *Q3* are turned on. The energy in the turn-off network is discharged into the GTO gate. Ideally *Q3* is turned on only for a duration sufficient to remove the stored gate charge in the GTO. This occurrence is evidenced by the gate voltage going negative and staying negative. Any extra drive is clamped by the zener action of the gate-cathode diode of the GTO device. An *RC* circuit in the logic controls the on duration of *Q3*. It provides easy adjustment for the length of the turn-off pulse. As mentioned earlier, the recovery time for the GTO forward voltage blocking capability is attained many microseconds after the gate voltage goes negative. Therefore *Q2* is held on to maintain a negative gate bias until the next trigger signal arrives. Figure 3 shows a gate current pulse generated by the drive.

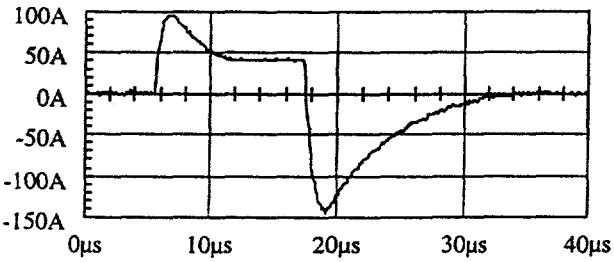

Figure 3: GTO gate current pulse

The trigger signal is transmitted to the card by fiber optics. It provides needed isolation between the high-voltage section and the low-voltage section. An HP HFBR2521 fiber receiver, rated for 5 Mbits/s at 19 meters, is used. Its internal logic operates at 5 volts while its open-collector output is rated for 18 volts. This enables CMOS integrated circuits (ICs) to be used in the logic circuit, thus providing more tolerance for noise produced by switching actions of the power MOSFETs and the GTOs.

Two high voltage half-bridge driver ICs, HIP2500 by Harris, are used to drive the power MOSFET H-bridge. The HIP2500 has current outputs suitable for driving the gates of power MOSFET devices. Its high-voltage section output is also capable of floating up to 500 volts above its ground; thus, it meets the requirements for driving the top switches of an H-bridge configuration.

2.4 Advantages and Disadvantages

A direct gate drive has several advantages compared with conventional single primary and multiple secondary pulsed-transformer-based gate drives. It has very low inductance and, therefore, can supply very fast gate pulses to the GTO gate. It can produce long constant gate current if the GTOs are required to stay on for a long period of time. It also permits adjustment of the turn-on and turn-off timing of each GTO independently to compensate for variations in a GTO's switching speed. The high-frequency switching and high-voltage isolation transformer has a very simple structure and can be constructed easily. Since each GTO/gate drive pair is completely independent, any number of the GTOs can be used in series to accommodate the requirement of the high voltage.

The disadvantage of the direct gate drive is that if one of the drives fails to send the turn-on gate pulse to its GTO, the GTO will be damaged by an over voltage when other GTOs are turned on. A domino effect may follow in which all the GTOs are destroyed. Similarly, if one drive fails to send the turn-off gate pulse, other GTOs may be damaged by excessive voltage in the reverse direction. To improve the reliability of the GTO switch operation, certain voltage redundancy needs to be considered when deciding the number of GTOs to be used in series. Some interlock mechanism may need to be devised to link all of the gate drives together. If a malfunction is detected in one drive, the trigger signals must be stopped for all the drives.

3 CONCLUSION

Seven direct gate drive cards have been built to drive a GTO switch of seven GTOs connected in series. With these cards, the GTO switch has successfully switched a half-sine current pulse of 6000 amperes with a base width of 12 microseconds. Further study will be done on improving the reliability of the drive and finding a suitable interlock mechanism.

4 REFERENCES

[1] O. Despe and J. Wang, "Design of a Gate-Turn-Off (GTO) Switch for Pulsed Power Application," EPAC98, pp. 2281-2283, Stockholm, 1998.