PHILIPS

Low-Cost Illumination-Grade LEDs

Final Report

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Executive Summary

Solid State Lighting is a cost-effective, energy-conserving technology serving a rapidly expanding multi-billion dollar market. This program was designed to accelerate this lighting revolution by reducing the manufacturing cost of Illumination-Grade LEDs. The technical strategy was to investigate growth substrate alternatives to standard planar sapphire, select the most effective and compatible option, and demonstrate a significant increase in Lumen/$ with a marketable LED. The most obvious alternate substrate, silicon, was extensively studied in the first two years of the program. The superior thermal and mechanical properties of Si were expected to improve wavelength uniformity and hence color yield in the manufacture of high-power illumination-grade LEDs. However, improvements in efficiency and epitaxy uniformity on standard c-plane sapphire diminished the advantages of switching to Si. Furthermore, the cost of sapphire decreased significantly and the cost of processing Si devices using our thin film process was higher than expected. We concluded that GaN on Si was a viable technology but not a practical option for Philips Lumileds. Therefore in 2012 and 2013, we sought and received amendments which broadened the scope to include other substrates and extended the time of execution.

Proprietary engineered substrates, off-axis (non-c-plane) sapphire, and c-plane patterned sapphire substrates (PSS) were all investigated in the final 18 months of this program. Excellent epitaxy quality was achieved on all three candidates; however we eliminated engineered substrates and non-c-plane sapphire because of their higher combined cost of substrate, device fabrication and packaging. Ultimately, by fabricating a flip-chip (FC) LED based upon c-plane PSS we attained a 42% reduction in LED manufacturing cost relative to our LUXEON Rebel product (Q1-2012). Combined with a flux gain from 85 to 102 Lm, the LUXEON Q delivered a 210% increase in Lm/$ over this time period. The technology was commercialized in our LUXEON Q product in Sept., 2013. Also, the retention of the sapphire increased the robustness of the device, enabling sales of low-cost submount-free chips to lighting manufacturers. Thus, blue LED die sales were initiated in the form of a PSS-FC in February, 2013.

Progress Towards Milestones

Title: 150mm Substrate Specifications
Planned Date: Jan 31, 2012
Description & Verification Method: Define substrate specifications that enable 150mm GaN template quality and PL wavelength uniformity.
Progress: The patterned sapphire substrate (PSS) specification includes pattern layout, etch depth and final surface quality. The specifications sufficient to meet the goals of the project were completed in Sept. 2012.

Title: 150mm LED Epi Structure
Planned Date: Sept 30, 2012
Description & Verification Method: Develop epitaxy process to demonstrate 452nm LED with performance comparable to commercial LUXEON Rebel LEDs available at end of Phase II. Projected performance goal is <3.0V Vf and >475mW flux at 350mA/mm^2.
Progress: Epitaxy development on the optimized PSS wafers was sufficiently developed by Dec. 2012 to consistently deliver the required device performance. Device performance described below met the <3.0V, >475mW flux. The commercialized product PSS-FC was spec'd at 500mW minimum power in the 440 to 460nm range with a typical Vf of 2.9.

Title: 150mm Wafer Fabrication
Planned Date: July 31, 2012
Description & Verification Method: Develop wafer fabrication processes to address extraction efficiency of 150mm InGaN on alternate substrate for a LUXEON Rebel demonstration.
Progress: Wafer Fab issues included PSS thinning, inspection through the patterned sapphire and calibration of full wafer testing. Minor modifications and calibration addressed all problems and a high yield commercially viable process was obtained by Dec. 2012.

Title: 150mm Run-to-Run PL Wavelength Uniformity
Planned Date: Dec 31, 2012
Description & Verification Method: Quantify run-to-run PL wavelength uniformity achieved with 150mm alternate substrates that employs process control via optical pyrometry. Goal is to demonstrate uniformity superior to that achieved with 3-inch sapphire during Phase I.
Progress: Wavelength uniformity of InGaN LED structures grown on PSS matched our standard InGaN on sapphire by Dec, 2012. Results on alternate substrates match but do not exceed our standard growth on sapphire.

Title: 150mm Lamp Build
Planned Date: October 31, 2012
Description & Verification Method: Develop and demonstrate lamp build processes for LUXEON Rebel warm-white lamps. Parts must be available for analysis and reliability testing.
Progress: Commercially viable lamp build process was obtained by Dec. 2012 and lamps were tested for reliability.

Title: 150mm Lamp Reliability
Planned Date: January 30, 2013
Description & Verification Method: Report 500 hour reliability test data of LUXEON Rebel LEDs from epitaxy on 150mm alternate substrate.
Progress: Excellent reliability demonstrated by Jan. 2013. After 1000hrs at 85C with a 700mA drive current ($1mm^2$ chip) and a humidity of 85%, 0 failures out of 2605 devices were recorded.

Title: 150mm Warm-White LED Lamp
Planned Date: January 31, 2013
Description & Verification Method: Demonstrate LUXEON Rebel warm white lamp from epitaxy on 150mm Si. Performance goal is to match commercially-available LUXEON Rebel performance at end of Phase II, (estimated specifications >110 Lm/W, 3000K CCT, 80 CRI at 350mA/mm2).
Progress: In Q2 of 2013, we achieved typical 3000K, 80 CRI performance of 104Lm/W. Hero results exceeded 110Lm/W.

Title: Epitaxy Cost Modeling
Planned Date: February 28, 2012
Description & Verification Method: Develop a model to project the device cost reduction, lumen per dollar increase achieved with the various 150mm substrates utilized in the program.
Progress: Completed Nov. of 2013. 42% reduction in LED manufacturing cost relative to our standard LUXEON Rebel product (Q1-2012 basis). A flux gain from 85 to 102 Lm was realized over the same time period resulting in a 210% increase in Lm/$. PSS was the only alternate substrate for which warm white LEDs were successfully processed.

Year 1 (June 2010-May 2011) Project Activities

Technical Highlights of Year 1

- IQE within 16% of GaN on Sapphire achieved
- Demonstration of 420mW from a 1mm LUXEON Rebel operated at 350mA, λ=450nm
- Established GaN on Si process flow from epitaxy to lamp build
- Excellent electrical performance demonstrated, Vf=2.85V at 350mA, Vr<-20V
- Wafer Processing and Initial Testing of device epitaxy grown on 6" substrates
- Completed Team Training of new employees hired under the program

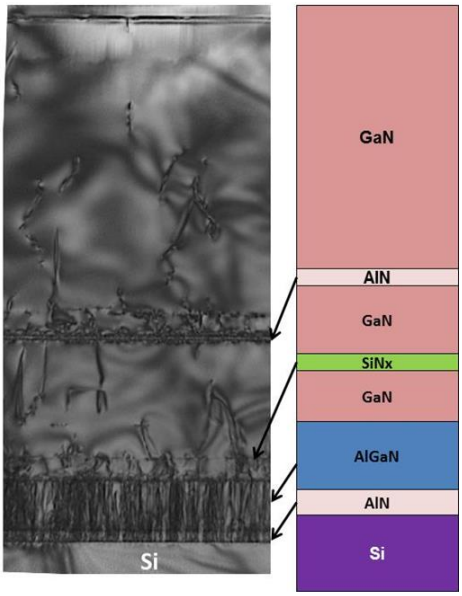


Fig. 1 TEM of GaN on Si Epitaxy

The initial effort focused on epitaxy development of an optimized template (epitaxial layers grown before the active region) on 3-inch Si wafers. Epitaxy starts with a thin AlN buffer layer to prevent attack of the Si by Ga precursors and to set the lattice constant and control the compressive strain of the following layers. Growth of ~1µm of highly dislocated GaN follows the AlN. Typically a series of thin (<30nm) AlN or SiNx interlayers followed by micron thick GaN were grown. In Fig. 1, a TEM cross section of a template structures reveals the layer structure and the dislocation behavior. After each interlayer, the dislocation density is high but dislocation bending and annihilation reduces dislocation density in the GaN layers. After a few cycles of interlayer/GaN the dislocation density is controlled to below $8x10^8$ cm^{-2}. An additional value of the multiple cycles is the greater mechanical strength of the epitaxy. For LED fabrication, the Si growth substrate must be removed and a thicker epitaxy is more robust. For device work, Si doping of the uppermost GaN layer is required for lateral current spreading. However, Si doping affects strain and dislocations, setting up complex interactions that require many experiments to properly balance. Using template structures as shown in Fig. 1 we simultaneously achieved acceptable stress, defect level, and electrical conductivity without excessive cracking.

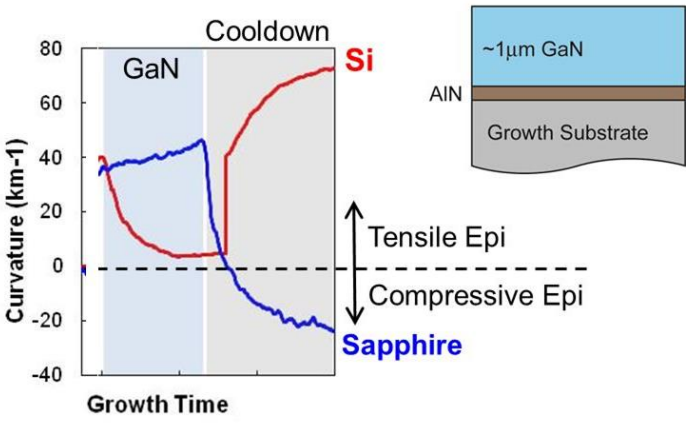


Fig. 2 Wafer Curvature of Si and Sapphire during Growth and Cooldown

Wafer curvature is a principal metric for template development requiring in situ tools. Sample data taken during growth and cool-down of GaN on Si and GaN on sapphire are shown in Fig. 2. Because the coefficient of thermal expansion (CTE) of sapphire is greater than GaN while the CTE of Si is *less* than GaN, the stress behavior is roughly opposite on the two substrates. During cool-down the epitaxy on Si becomes more tensile

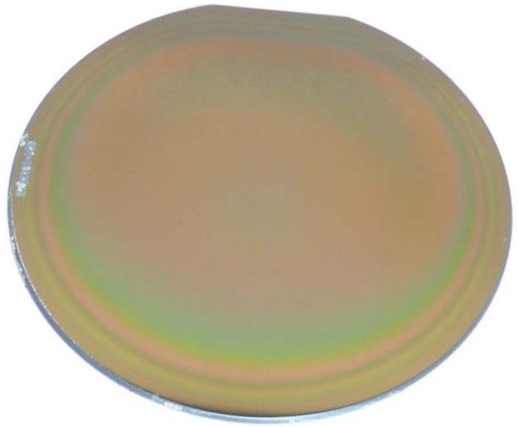


Fig. 3 Crack-free LED structure on Si

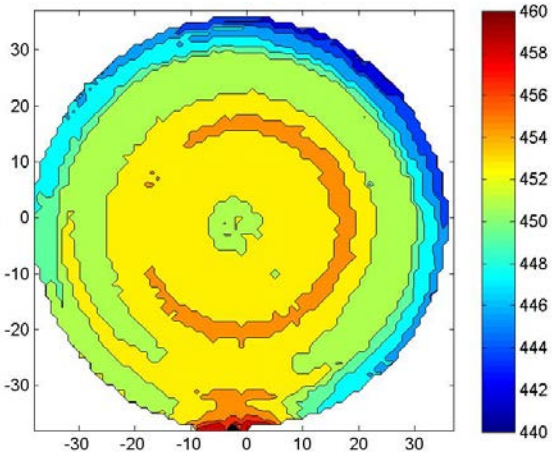


Fig. 4 PL Map of LED structure on Si

strained and is prone to cracking. (The epitaxy on sapphire becomes compressive which is more crack resistance and robust.) The epitaxy on Si must be grown in a compressive state to avoid cracks and bowing forming upon cool-down.

In Fig. 3 we show a typical 3" GaN on Si device wafer. The wafer is crack-free. Note that the ID mark and the extreme edge of the wafer show signs of deposition. Wherever the AlN did not coat the Si substrate, uncontrolled growth of amorphous Si+GaN structures were observed. These structures affect device fabrication as discussed below. Once the template was established, simple device structures were produced to determine the wafer to wafer and within wafer PL uniformity. Si has a higher thermal conductivity than sapphire and emits light in the wavelength band used for standard pyrometry. Thus the substrate growth temperature is directly measured whereas with standard pyrometry the sapphire temperature is indirectly determined. Emission wavelength is strongly influenced by growth temperature, so an improvement in temperature control translates into higher color yield and thus lower cost per yielded die. This advantage was confirmed by conducting a 9-wafer series of a GaN on Si LED structure and measuring the run-to-run wavelength standard deviation with photoluminescence (PL) mapping. Compared to 3" GaN on sapphire controls, the GaN on Si wavelength deviation was 30% lower. Similarly, within a wafer, improved uniformity was observed. The PL map of a 3" GaN on Si wafer is shown in Fig. 4; the standard deviation was measured to be 2.9nm. However, the development of epitaxy on 150mm sapphire included improvements in temperature control of active region growth. During Year 2, the progress on 150mm sapphire continued to reduce the prospective advantages of Si. By the end of Year 2, uniformity was not considered a strong driver for Si.

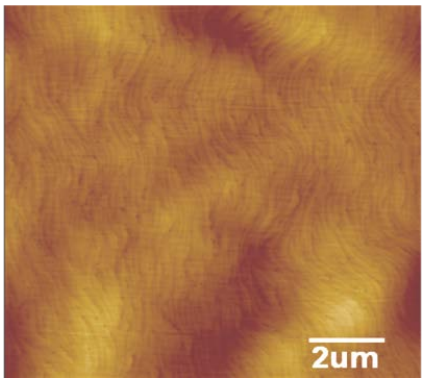


Fig. 5 AFM image of GaN on Si

Other key material characteristics included surface morphology, sheet resistance, and bow. The surface morphology was measured with AFM and an orderly arrangement of atomic step terraces was obtained as seen in Fig. 5. When an integrated doping level of $8x10^{12}$ cm^{-2} Si atoms was obtained the corresponding sheet resistance was < 40 Ω/□. This value is low enough for high performance LED fabrication and we focused on active region

and device development for the rest of the project. We consistently achieved a bow of <30 µm which was better than GaN on sapphire.

We proceeded with development of a 3-inch LED structure. To accelerate development a "fast-feedback" electroluminescent (EL) device effort was initiated and maintained throughout the program. Current-voltage, and emission wavelength, could be accurately measured and internal quantum efficiency (IQE) of the epitaxy structure could be roughly estimated from EL device data. In addition to the EL characterization, variable temperature PL measurements were used to estimate IQE. The results for a series of "same reactor/same active region" wafers grown on sapphire and Si are shown in Fig. 6. The rough equality between Si and sapphire with a small advantage to sapphire was a typical result. Another figure of merit was the Hot-Cold (H/C) factor: IQE at 85ºC divided by IQE at 25°C. The best epitaxy achieved a H/C factor of >0.90, compared to the 0.95 to 0.96 of GaN LED on sapphire. The epitaxy development effort required several hundred growth runs to optimize for internal quantum efficiency (IQE) and electrical performance.

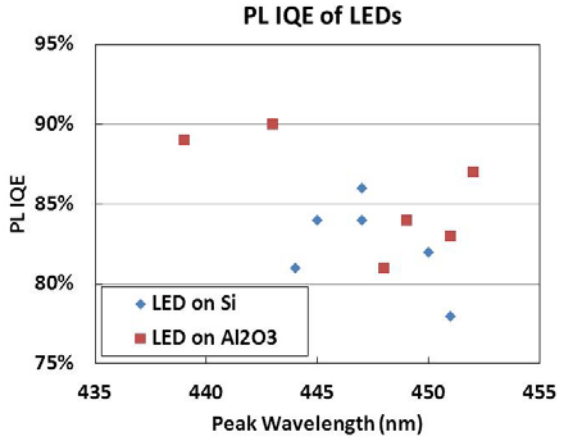


Fig. 6 Comparison of IQE of GaN on sapphire to GaN on Si

The LUXEON Rebel platform was selected over a vertical thin film (VTF) for our device demonstrations from 3" wafers. The deciding factors were the ease of direct comparison with our commercial product and the minimal development required for wafer fab processing. The wafer fab, full wafer test, and die fab proceeded well as little innovation was required. Our turn-time for wafer and die fab processing was approximately three weeks total. One problem we encountered was the 5-10µm tall Si+GaN structures on the edges of the wafers (mentioned above) that complicated contact lithography. We switched from a contact aligner to a stepper to avoid the problem. However, it was required to thin the GaN on Si wafers prior to wafer processing because of a limit on the stepper tool. Either the material used to protect the p-GaN surface during the thinning or the chemical used to remove the material affected the p-GaN surface and increased the p-contact resistance. The forward voltage, Vf, was raised by 6-10%, and the root cause was not resolved in time to correct it during the remainder of the GaN on Si effort. In the first year, 16 wafer fab lots were successfully completed and provided valuable feedback for epitaxial growth.

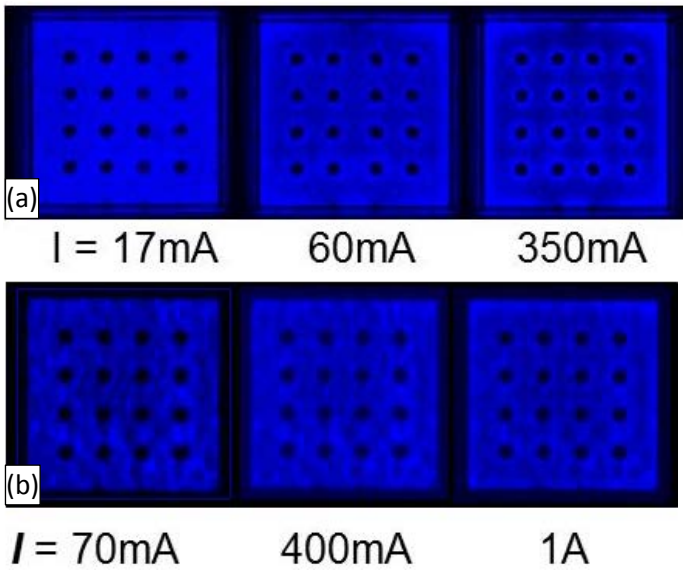


Fig. 7 Surface image of (a) Early and (b) Later GaN on Si LEDs

The back-end steps were: 1.Die Fab, 2. Die attach using gold-gold interconnects, 3. Underfill with either epoxy or silicone loaded with silica which protected the metals, 4. Si wet etch which left tall underfill wings at the die perimeter, 5. Roughening of the top surface AlGaN and GaN layers, and 6. Dome encapsulation. The back-end processing proved more difficult than expected because the protective silicone underfill was not sufficiently resistant to the acids used to remove the Si substrate and the dry etch AlGaN roughening processes. Therefore we used an epoxy underfill for higher yield lamp builds but at a penalty in light extraction. The 100μm tall epoxy wings blocked light and reduced power output by several per cent. The silicone underfill absorbed less light but the yield was much lower. At the die edge, visual evidence of chemical attack on >90% of the devices was observed with a correlated electrical shunt current. The trade-off was either high yield with epoxy or highest light output with silicone.

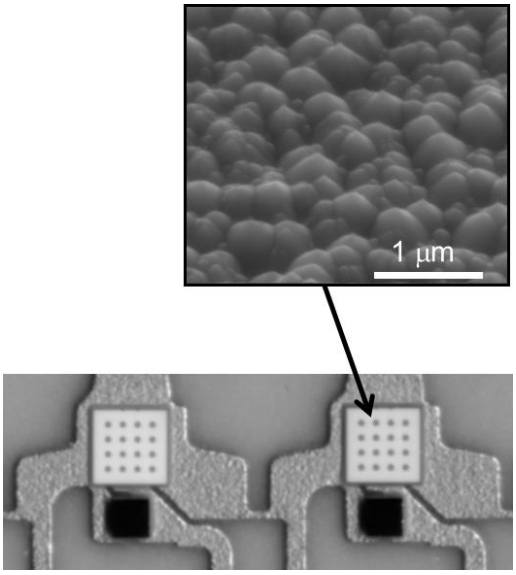


Fig. 8 Roughened dice on submount and SEM of surface morphology

Using the mounted LEDs we imaged the emitting surface to evaluate the lateral current spreading. In Fig. 7, we show the images at several currents for two devices (a) an early device with a sheet resistance of 60Ω/□ and (b) a device with an improved template having a <40Ω/□ sheet resistance. Device (a) clearly shows current crowding at 350mA (41A/cm^2). The light emission is brightest around the n-contact dots and frame. The efficiency is negatively impacted because the light generation occurs in regions of highest optical loss. Also, the well-known droop effect reduces the average IQE for highly non-uniform current densities. In (b), we show emission images from a later device measured up to 1A (123 A/cm^2). The intensity pattern at I=1A varies randomly across the die because of morphology correlated epi effects but shows little crowding around the n-contacts even up to 1A. At I=1A, we measure a worst case of +/-22% variation across the die indicating that the n-GaN sheet resistance of <40 Ω/□ is sufficiently low to provide adequate current spreading at I= 350mA.

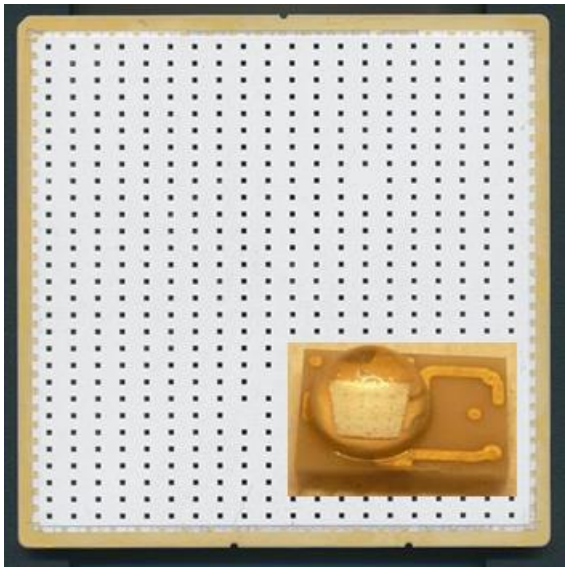


Fig. 9 Submount populated by GaN on Si LEDs and a finished lamp

Dry-etch roughening of the aluminum-containing layers was deemed necessary as our standard photo-electrochemical (PEC) etch was incompatible with the non-conductive AlN interlayers. Etch experiments varying power, time and chemistry in an ICP etcher were initiated. A setup to quantitatively measure diffuse reflectivity of roughened devices was established and data correlated to etch conditions. Unfortunately, each revision in template design necessitated a revision in roughening recipe. As the template design stabilized, an effective and reproducible device

roughening recipe was achieved and improvements in roughening continued into Year 2.

In Fig. 8, the darkfield image of TFFC devices on the submount tile after roughening shows a bright white surface indicative of good light scattering and high reflectivity. The inset shows an SEM image of the surface. The roughness is finer than is typical for PEC etching but the scattering power in the 400 to 460nm wavelength range equaled our PEC standard in Year 2.

After roughening, the devices were overmolded at the submount level and sawn into LUXEON Rebel lamps. In Fig. 9 we show an image of an alumina submount populated by GaN on Si devices and in the inset, a singulated lamp. The best device performance from Year 1 is shown in Table 1 along with the program target and what competitors had reported at that time (1Q-2011). The light output (LOP) of 437mW at 448nm was below spec for reaching the goal of the program. The deficit is related to combination of IQE, the not-yet-optimized roughening and the residual underfill wings. The Vf of 3.06V, elevated by about 6% relative to GaN on sapphire controls, was a result of the interaction between the p-GaN and the resist protection during thinning. The 448nm wavelength was shorter than the target of 450-452nm.

350 mA/mm^2, 25°C	Current	Program Target	*Industry Reports*
LOP (mW)	437	>520	*450*
V_f (V)	3.06	2.9	*3.3*
λ (nm)	448	452	*450*
WPE (%)	40.7	50	*39*
Wafer Size	3-inch	150mm	*2-inch (?)*

Table 1. Performance of Best Year 1 LED

Year 2 June 2011 to May 2012 Project Activities

Technical Highlights of Year 2

- IQE within 10% of GaN on Sapphire achieved
- Initial reliability data with no gradual degradation

Improvement in epitaxial quality continued in Year 2. Cracking was eliminated and final bow consistently held to below 20µm, significantly better than GaN-on-sapphire. Sheet resistance, defect density (TDD), internal quantum efficiency (IQE), and H/C factor all approached but never completely matched our GaN on sapphire standards. During the year, the IQE of GaN on sapphire was benefiting from subtle improvements in active region design which could not be adapted and transferred to growth on Si, given the available resources. To compare Si and sapphire IQE fairly we had to use the same basic active region structure on both substrates in the same reactor. Meanwhile, IQE of wafers grown on 150mm sapphire continued to improve. Also, development of epitaxy uniformity on 150mm sapphire improved until achieving a significant gain in color yield on Si became impractical.

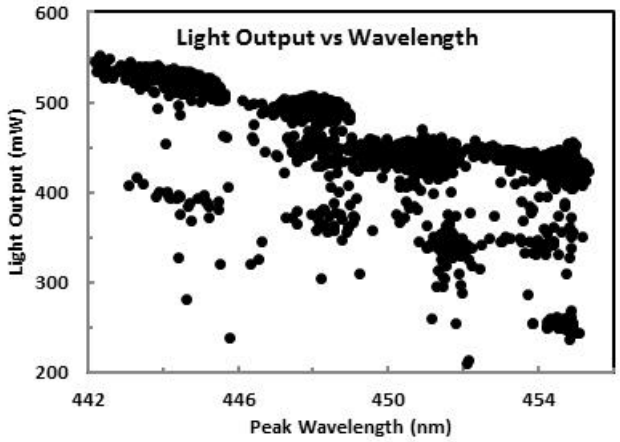


Fig. 10 LOP data vs. λ for several wafers

Wafer and back-end process development continued during Year 2 and significant improvements in roughness and robustness were achieved. However the fundamental problem of underfill attack was not resolved. Chips from many epitaxy runs were processed and tested on submounts. The 350mA data from multiple tiles are show in Fig. 10. These results are not calibrated to an absolute standard but accurately show the relative performance as a function of wavelength. The upper envelop of the distribution is indicative of the decrease in power output with increasing wavelength. The 1.7% decrease per nm of wavelength shift is significantly higher than what we observe for GaN on sapphire but no physical cause of the discrepancy was discovered. The *calibrated* power output values from both GaN on Si and control lamps from GaN on sapphire grown in the same reactor are given in Fig. 11. There are fewer data points because these lamps were processed with silicone underfill to boost light output, at a cost in yield. Hero lamp performance at several wavelengths is given in Table 2. As a comparison our commercially available products with a typical wavelength of 448nm delivered at room temperature a power output of 480 and 520mW depending upon flux bin. The GaN on Si hero result of 440mW was approximately 12% below this performance level.

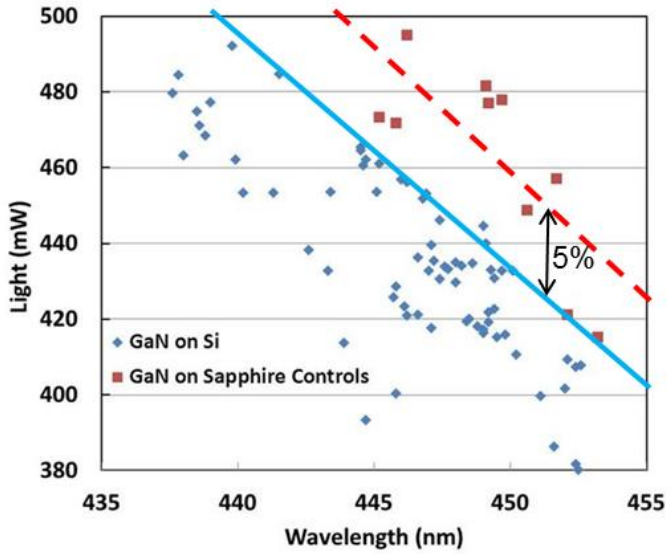


Fig. 11 LOP vs. λ for best Year 2 devices compared with GaN on Sapphire controls

Initial reliability measurements at 350mA, 85C and 700mA, 85C (low humidity) were conducted. The 50 lamps were not screened before testing and there were 3 quick failures but the remainder showed no gradual degradation and no failures between 20 until 168 hours.

In the original proposal, we anticipated that the superior material properties of Si combined with the maturity of the Si substrate production would translate into higher epitaxy yields with tighter wavelength distributions. The tighter wavelength bins would translate into higher wafer fab yields. In practice, during growth there is considerable convex bow associated with GaN on Si epitaxy and achieving a tight peak wavelength distribution presents a similar challenge as for sapphire. Essentially, our epitaxy development on 150mm sapphire delivered the uniformity gains promised for Si, without the disruption of switching technologies. We were convinced that with moderate effort, the electrical characteristics for GaN on Si and GaN on sapphire would be equivalent. Matching IQE seemed feasible but only given a full deployment of engineering staff

Emission Wavelength (nm)	440	442	445	447	450	453
Power Output (mW)	492	485	466	453	433	408
Forward Voltage (V)	3.27	3.40	3.40	3.44	3.25	3.26
External Quantum Efficiency (%)	50	49	48	47	45	43
Wall Plug Efficiency (%)	43	39	39	38	38	36

Table 2. Performance of best GaN on Si LEDs from Year 2

and slowing down development on sapphire. Many of the back end process issues could be resolved by switching to a VTF architecture, requiring additional process and package development. However, introducing a Si-based VTF would require a major overhaul of epitaxy, wafer fab, and packaging. The risk and cost of such a conversion was not warranted by the performance nor by the potential cost saving of Si over sapphire. By the end of the second year (May, 2012), we did not regard Si as the optimum alternate substrate.

Two other options briefly evaluated were engineered substrates and non-c-plane sapphire. The details are proprietary but there were potential advantages in growth uniformity or cost. For example, engineered substrates may be designed such they remain flat throughout the epitaxy process. Based upon PL data, uniform epitaxy of excellent quality was grown on these candidates but we did not succeed in fabricating high extraction LEDs because of the difficulty of removing the substrate. Non-c-plane sapphire also offered no barrier to high quality epitaxy. However, the new templates on the alternate substrates produce higher final bow and approximately 30% higher residual strain as measured by Raman scattering measurements. The unbalanced stresses associated with the lower symmetry complicated the thinning of the wafers and high die fab yields were too difficult to attain. So in both cases, the epitaxy development looked promising and LED structures were grown with low defect densities, but there were stubborn device fabrication issues in either thinning or removing the substrate. We looked for a technology which offered a compelling advantage but could be introduced into the company product portfolio without a major disruption. The optimum technology appeared to be patterned sapphire substrate (PSS) where micron-scale scattering features could be introduced into the sapphire substrate and the FC architecture could be largely unchanged. We focused our efforts on PSS-based technology for the remainder of the program.

Year 3 through Aug 31, 2013

Technical Highlights of Year 3

- Warm White Efficacy Data on PSS devices
- Excellent Reliability Demonstrated
- Commercial Level Performance achieved with a 42% cost reduction (basis Q1-2012 LUXEON Rebel)
- Product Announcement of a PSS LUXEON Flip Chip for die sales
- Product Announcement of LUXEON Q having an overall 210% Lm/$ advantage over a Q1-2012 LUXEON Rebel

The program goal was a significant cost reduction of an illumination-grade lamp product. At the beginning of Year 3, we selected the patterned sapphire substrates (PSS) as the optimum alternate substrate. We developed our own 150mm PSS fabrication process compatible with high volume manufacturing. The process steps are: 1. Hard mask deposition, 2. Photoresist patterning, 3. Mask etch, 4. Resist strip, 5. Sapphire wet etch, and 6. Hard mask strip. In Fig. 12, we show an image of the PSS surface with 3-5 micron features. The PSS process attains high yields at a reasonable cost per wafer which is included in the cost model below. A PSS epitaxy growth recipe was developed using standard coalescence strategies. The morphology of the completed epitaxy growth was essentially identical to our epitaxy on planar substrates. Similarly only minor adjustments were required to achieve parity on other important epitaxy characteristics including uniformity, yield, internal quantum efficiency (IQE), and forward voltage (Vf).

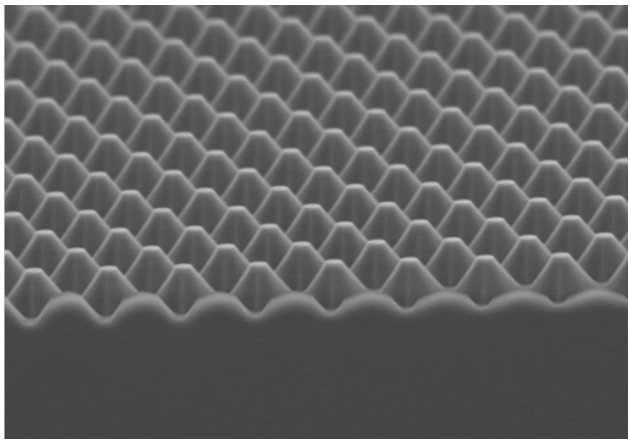


Fig. 12 SEM image of the PSS surface

Chip Fabrication

Lateral Die are the PSS-based chips commonly found in low cost illumination products. In this architecture, the die is mounted epitaxy-up with the sapphire below the active region. Heat flow from the active region must pass through the sapphire substrate. Transparent conductive oxides (TCO) are applied to the p-type epitaxy to form an electrical contact and spread the current. Metal fingers are patterned on the TCO to help spread current and metal pads are created for wirebond attach. In contrast, our form of PSS device is a flip-chip similar to our TFFC products. As seen in the schematic of Fig. 13, the sapphire is above the active region (dotted line in the Figure) and heat flow passes through the metallization and dielectric stack applied during wafer processing to reach the submount. The lower thermal resistance of these layers relative to the thick sapphire substrate is a fundamental

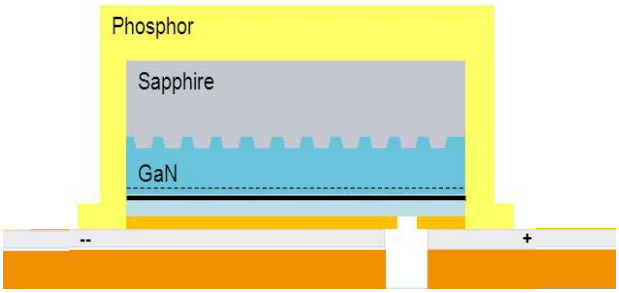


Fig. 13 Schematic of a PSS-FC with conformal phosphor

advantage of the PSS-FC. We designed a two part wafer process flow compatible with automated high-throughput equipment in our San Jose facility. The first part of the flow was based upon wafer processing of our TFFC product line. More than 15,000 1x1mm devices per wafer were fabricated into functioning but incomplete devices. After the first stage electrical contacts were completed and the wafer was ready for full wafer test of electrical characteristics and emission wavelength. Electrical characterization was extensive including several negative and positive bias voltage test points. In the second stage, additional wafer processing added an electrical isolation layer and a plated metal layer to redistribute the contacts and provide two solderable pads. The high wafer fab yield was similar to our results with TFFC devices on standard substrates. As part of the development, plated metal thickness and redistribution layout were varied to improve solderability and reduce stress. Also, singulation strategies and sapphire thickness were optimized. After die fabrication, the full wafer test data is used to bin the devices according to electrical characteristics and wavelength. We show the underside of a solderable CSP device in Fig. 14. The two solder pads are seen on the underside of the chip. In Fig. 15, we show a sideview of the chip. The sapphire with the scoring from the laser scribing is visible and the plated metal and solder pads are also seen. The epi and non-gold metals are fully protected by sapphire, dielectric and gold-based metallization.

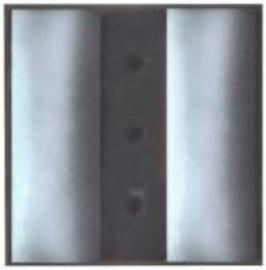


Fig. 14 PSS-FC backside of die

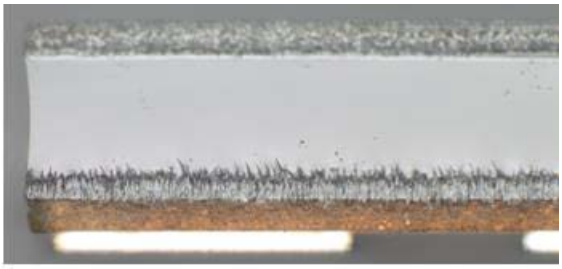


Fig. 15 Side view of PSS-FC

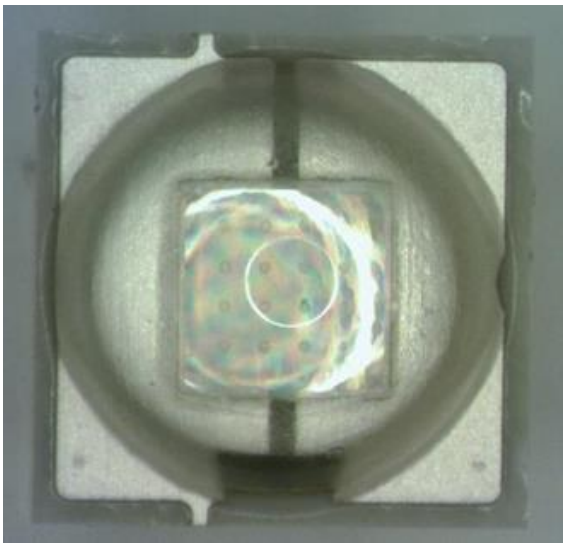


Fig. 16 Mounted and encapsulated PSS-FC

Packaging/Testing a Pump Emitter

In Fig. 16 the blue emitter is shown packaged on a reflective submount with a molded silicone dome. The diffractive pattern creates the false colors visible in the chip. The 3.5x3.5mm footprint of the submount is 10% less area than our LUXEON Rebel benchmark (3.0x 4.5mm). Further reductions in footprint represent an opportunity to reduce packaging costs.

In Fig. 17 the performance as a function of wavelength for two wafers from one common epitaxy run is shown. One wafer is a PSS wafer processed into PSS-FCs; the other wafer is standard sapphire processed into TFFC devices. The devices are all 1x1mm die, mounted on the same submount type and encapsulated. The performance deficit is 1-4% in this case.

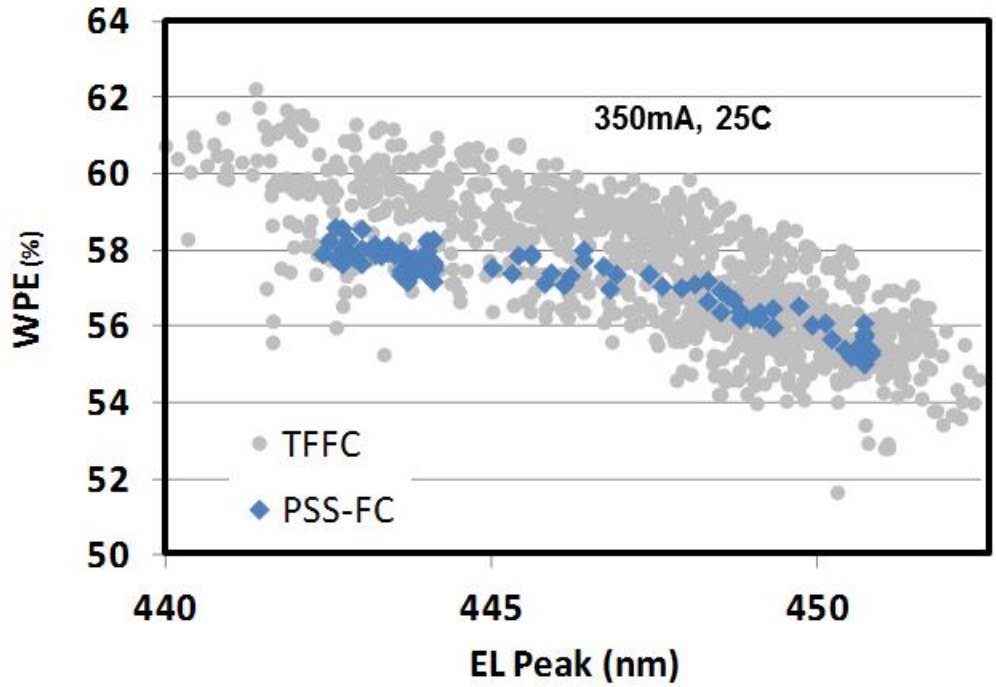


Fig. 17 Comparison of standard TFFC and PSS-FC

In Fig. 18 we show the hot/cold performance of a group of 1mm PSS-FC LEDs. The power output of 1250mW at 1A, 85 °C is at an emission peak at 450nm. The wall plug efficiency (WPE) at 350mA is 54% at 85 °C. These specifications are sufficient to meet our performance goal of a commercial grade white emitter with >100 Lm/W at 350mA (CRI=80, CCT=3000K).

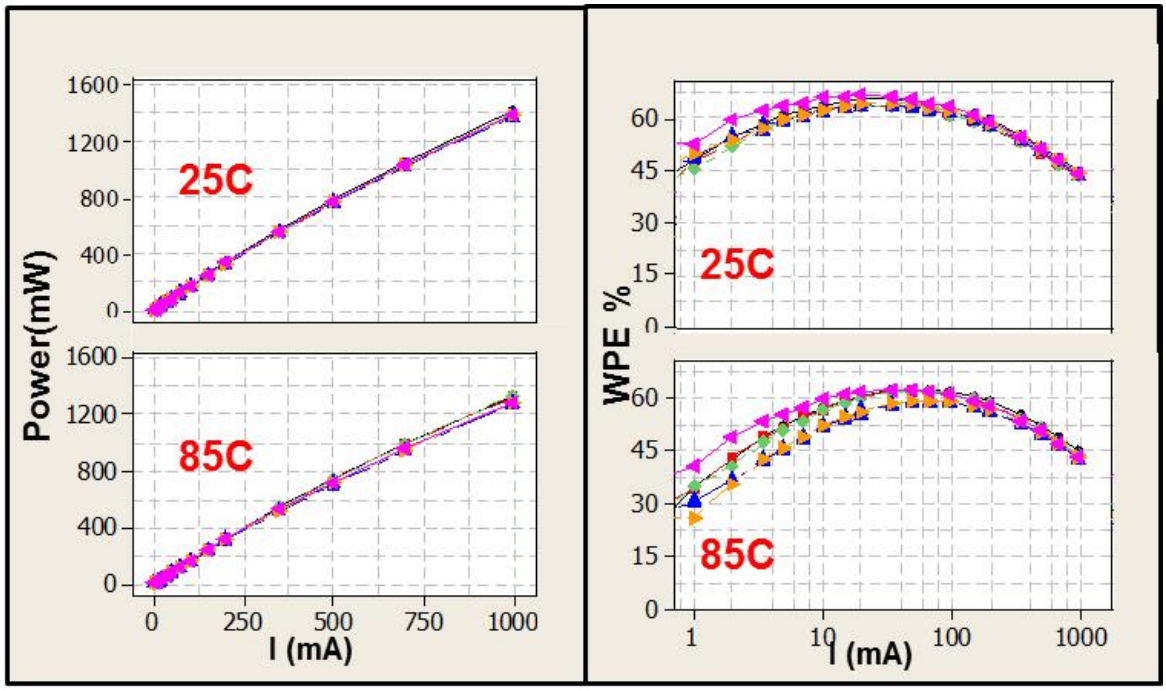


Fig. 18 Power Output and Efficiency of PSS-FC LED at 25 and 85C, λ=450nm

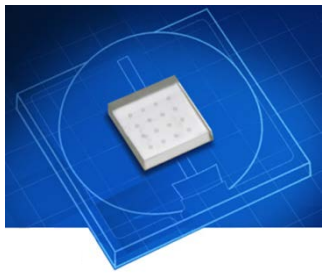
Test	Failures / Sample Size
HTOL – 85C @700mA (1000hr)	0 / 2979
WHTOL 85C / 85% RH @ 700mA (1000hr)	0 / 2605

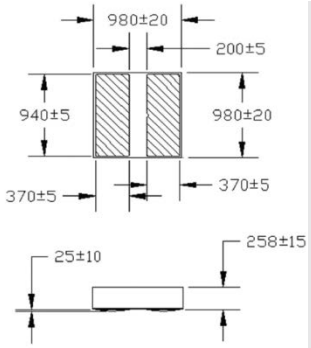
Table 3. Reliability results for PSS-FC

Reliability is a major requirement for an Illumination-grade LED. The PSS architecture has consistently shown excellent reliability and yields at least comparable to TFFC devices. In Table 3, we show two sets of reliability results after 1000 hrs (6 weeks) of testing of a few thousand devices at 700mA. The chips have been AuSn-attached to a ceramic tile and over-molded with a silicone dome. The HTOL test is performed at 85°C ambient with low humidity and the WHTOL ambient is 85°C with a relative humidity of 85%. Zero failures indicate the robustness of the PSS-FC.

The PSS-FC LEDs on bin tapes are ready to sell as low cost "die level" blue emitters and a die-on-tape LUXEON Flip Chip LED product was released on Feb. 12, 2013. An excerpt from the data sheet is shown in Fig. 19. This chip scale package (CSP) greatly reduces manufacturing cost for those customers needing a solderable blue pump LED. For white performance the die may be further packaged by attachment to submounts, application of phosphor and encapsulation. The performance depends upon the reflectivity of the submount but can be very close to a more expensive TFFC.

Product	Peak Wavelength Range [1] (nm)	Forward Voltage V_f [2,3] @ nominal drive current (V)			DC Forward Current I_f (mA)		Radiometric Power [4] (mW)	
		Min	Typ	Max	Nominal	Max	Min	Typ
LHDF-RB10000000000	440 - 460	2.7	2.9	3.1	350	1050	500	550





Benefits

- High current density for high lumen and lm/$ at high lm/W
- High-packaging density
- 5-sided emitter for dispense and remote phosphor applications
- Surface mount capable
- No wire bonds

Fig. 19 PSS-FC product details and performance specifications

Fig. 20 LUXEON MP 3535

Phosphor Development

New combinations of phosphors and host materials are being introduced at a rapid rate. The selection of the phosphor to attain the lowest cost while delivering illumination-grade performance is a complex challenge. One aspect of the challenge is the different geometry of a 5-sided PSS chip compared with a 2-D emitting surface of a TFFC. Commercially available Lateral Die PSS-based lamps feature a phosphor slurry dispensed into a reflective cup. For example, see our LUXEON MP 3535 in Fig. 20. For the PSS-FC, we over-molded phosphors in a silicone

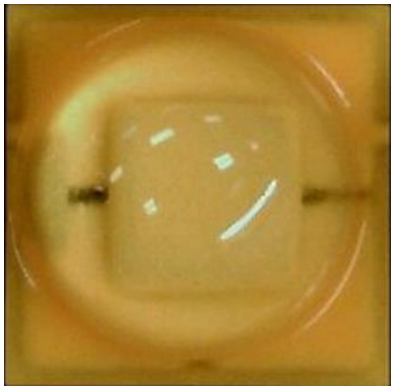


Fig. 21 LUXEON Q

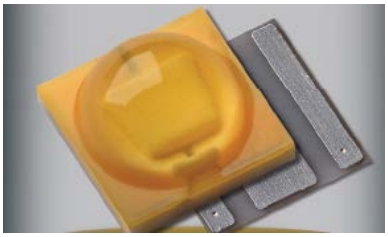


Fig. 22 LUXEON Q Product

matrix to conformally coat the PSS chips. In Fig. 21 we show a 1mm PSS-FC with a warm-white phosphor, mounted on a silver-coated submount. The silicone encapsulation dome is applied in a separate molding. An opportunity to further reduce phosphor utilization and thus cost would be to tailor the phosphor deposition to the immediate vicinity of the chip. We were not able to explore this possibility in this program but future development is anticipated.

The LUXEON Q is our commercial warm-white PSS-FC product launched Sept. 24, 2013. A device image and performance data from the product data sheet are shown in Fig. 22 and Table 4. The backside metals were modified to include a thermal pad between the two electrical contacts. Warm white performance at 350mA drive current and 85 °C are shown in Table 4. Note that median efficacy is >100 Lm/W with CRI =80 at a CCT of 3000K. Hero devices exceeded 110 Lm/W meeting the primary performance goal of the program to match or exceed the typical Lm output of our commercial devices but at substantially reduced cost.

Part Number	Nominal CCT (K)	CRI	Typical Luminous Flux (lm)			Typical Forward Voltage (Vf)			Typical Efficacy (lm/W)		
		700 mA	350 mA	700 mA	1000 mA	350 mA	700 mA	1000 mA	350 mA	700 mA	1000 mA
L1Q0-2780	2700K	80	100	177	231	2.81	2.93	2.99	102	86	77
L1Q0-3080	3000K	80	102	183	240	2.81	2.93	2.99	104	89	80
L1Q0-3580	3500K	80	106	189	251	2.81	2.93	2.99	108	92	84

Table 4 Specifications for the LUXEON Q Product family

Cost Analysis

The original cost reduction goal of the program had as a comparison, the LUXEON Rebel device fabricated from 3" standard sapphire at the beginning of the program (June 1, 2010). Over time the methodology to calculate manufacturing costs has improved and calculating a consistent "cost" from 2010 would be complicated. Therefore, we selected the LUXEON Rebel from Q1-2012 as a basis. The details of manufacturing costs are proprietary so we represent the improvement as a % cost down in Fig. 23. The Q3-2013 LUXEON Rebel is included and provides a measure of cost down resulting from many small improvements. The additional reduction in cost with the LUXEON Q is a result of the elimination of several back-end processes, a reduction unique to a PSS-based product. The total 42% reduction in manufacturing cost may be accounted for in two parts, a 23% reduction of incremental improvements and a further 25% PSS cost advantage over TFFC (the reductions to be applied sequentially). A flux gain from 85 to 102 Lm was realized over the same time period resulting in a 210% increase in Lm/$. These cost reductions combined with the improved performance, robustness and high current capability of LUXEON Q will support further market penetration of LED-based lighting.

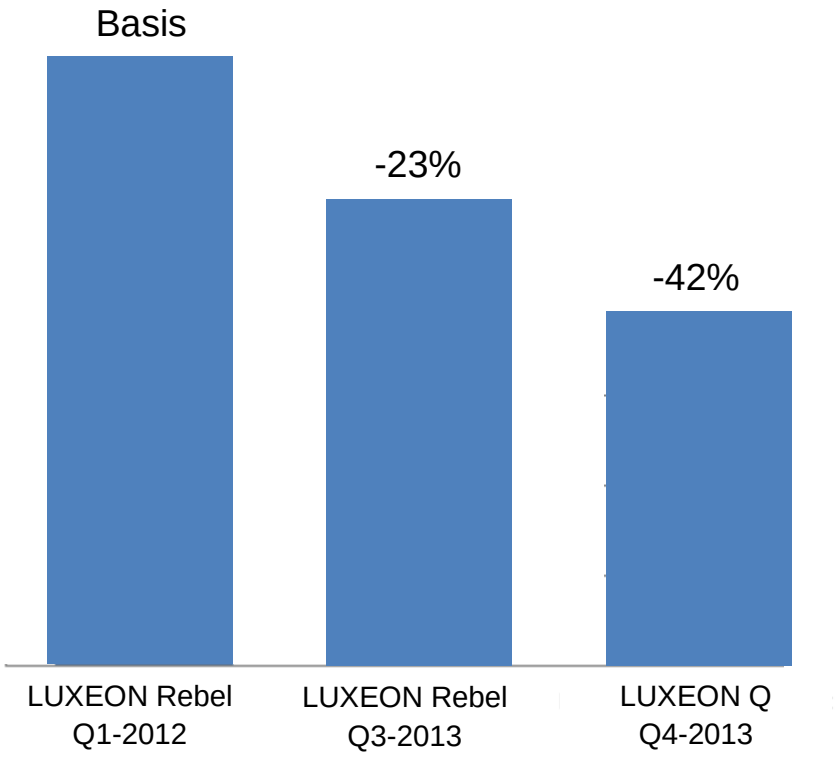


Fig. 23 Relative Cost of LUXEON Rebel and LUXEON Q

Products Developed

No Patents or inventions were generated by work performed on the Low Cost Illumination project.

Publications

1. John Epler, Linda Romano, Byung-Kwon Han, and Mike Craven, “Low Cost Illumination-Grade LEDs Enabled by Nitride Epitaxy on 150mm Low Cost Substrates”, presentation and poster presented at DOE SSL R&D Manufacturing Workshop, San Jose, CA, April 21, 2010.
2. Mike Craven, “Low Cost Illumination-Grade LEDs Enabled by Nitride Epitaxy on Silicon Substrates”, presented at DOE SSL Manufacturing Workshop, Boston, MA, April 12, 2011.
3. John Epler, Raj Singh, and Mike Craven, “Low Cost Illumination-Grade LEDs Enabled by Nitride Epitaxy on Silicon Substrates”, poster at DOE SSL Manufacturing Workshop, Boston, MA, April 12, 2011.
4. Byung-Kwon Han, Robert Armitage, Rajwinder Singh, and John Epler,” Low Cost Illumination-Grade LEDs Enabled by Nitride Epitaxy on 150mm Si (and other low cost) Substrates”, poster at DOE SSL Manufacturing Workshop, San Jose, CA, Jun 14, 2012.
5. Brendan Moran, John Epler, Rob Armitage, Byung-Kwon Han, Ted Mihopolous, Isaac Wildeson, Hee Jin Kim, Parijat Deb, Rao Peddada, Sal Akram, Joe Flemish, Shu Li, “Low Cost Illumination-Grade LEDs Enabled by Nitride Epitaxy on 150mm Alternate Substrates,” poster and presentation at DOE SSL Manufacturing Workshop, Boston, MA, June 5, 2013.

Commercial Products

1. Product release announcement, Patterned Sapphire Substrate Flip Chip (PSS-FC), Feb. 12, 2013.
2. Product release announcement, LUXEON Q (white emitting PSS-FC), Sept. 24, 2013.