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Characterization of SOI MEMS Sidewall Roughness

Leslie M. Phinney[1], Bonnie B. McKenzie[2], James A. Ohlhausen[2], Thomas E. Buchheit[2], and Randy J. Shul[3]

[1]Engineering Sciences Center
[2]Materials Sciences and Engineering Center
[3]Microsystems Center
Sandia National Laboratories
Albuquerque, New Mexico

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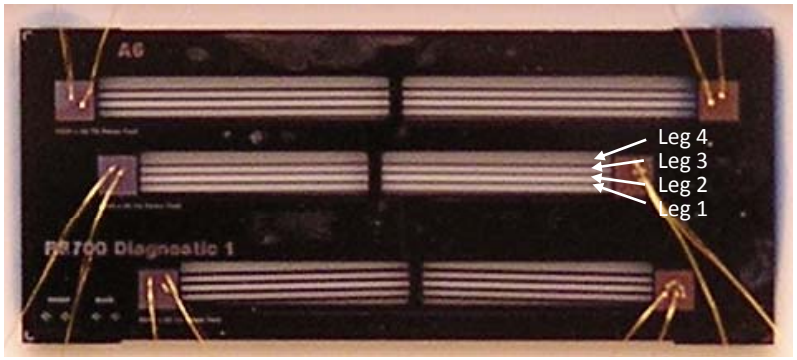
Motivation

- Deep reactive ion etching (DRIE) of silicon on insulator (SOI) enables high aspect ratio MEMS devices like microactuators, optical switches, accelerometers, and nanopositioners.
- Sidewall roughness occurs due to the repeated cycles of polymer deposition, ion sputtering, and chemical etching during DRIE.
- Sidewall roughness impacts mechanical characteristics like fracture strength and adhesion and friction behavior.
- Study on the effect of aspect ratio on SOI sidewall roughness was initiated.



SOI Thermal Microactuators
125 μm thick
5500 μm long actuator legs
50 μm wide actuator legs

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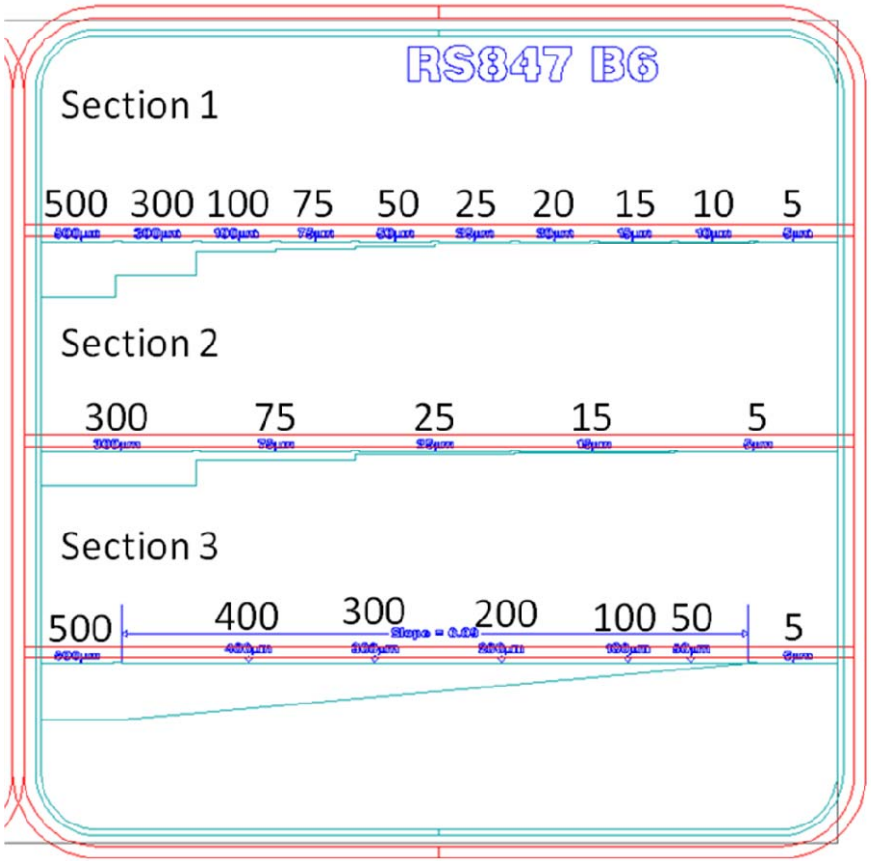
Characterization Die Schematic and Aspect Ratios



Schematic of SOI die design containing the sidewall characterization surfaces

Section 1		Section 2	
Trench Width	Aspect Ratio	Trench Width	Aspect Ratio
5 μm	25	5 μm	25
10 μm	12.5	15 μm	8.33
15 μm	8.33	25 μm	5
20 μm	6.25	75 μm	1.67
25 μm	5	300 μm	0.42
50 μm	2.5		
75 μm	1.67		
100 μm	1.25		
300 μm	0.42		
500 μm	0.25		

Trench widths and aspect ratios for sidewall characterization die fabricated with a 125 mm thick SOI device layer

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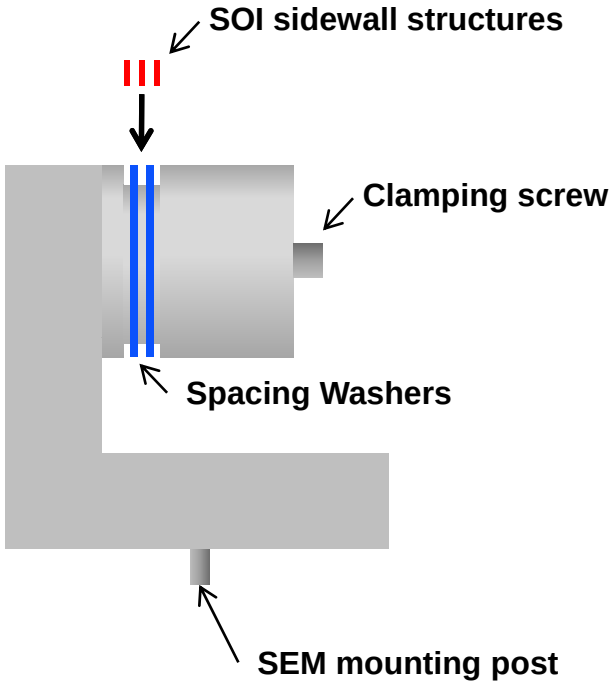
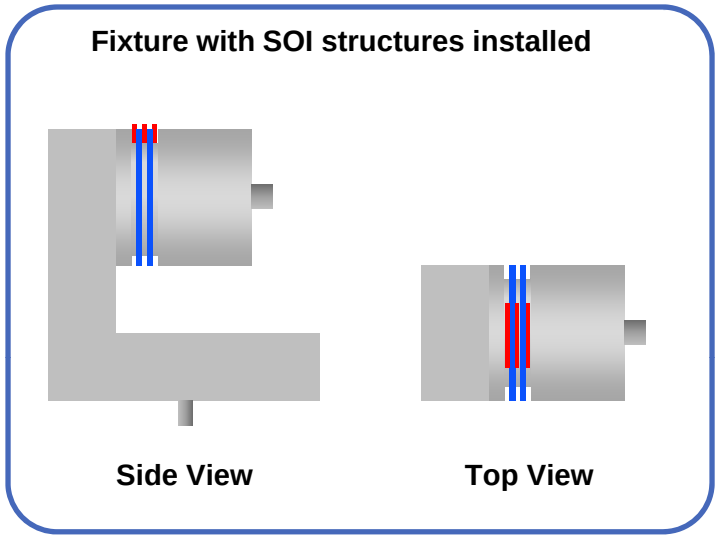
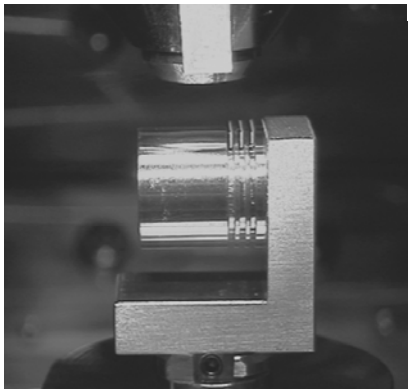
SOI Sample Fixture



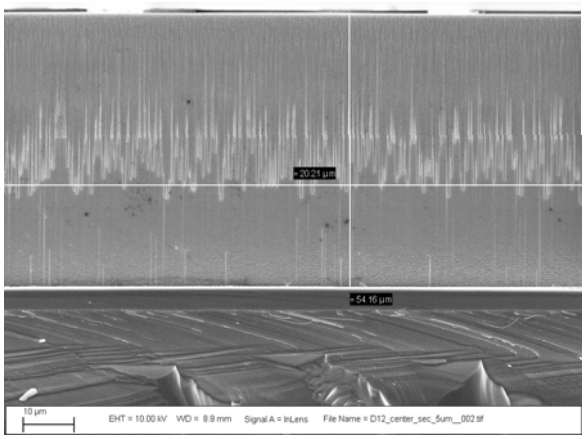




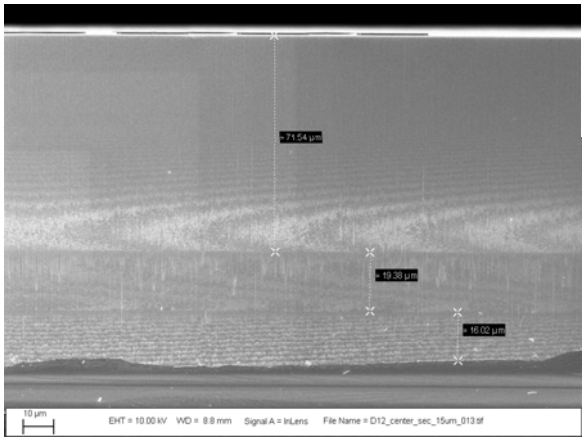
SOI sample fixture in the Zeiss Supra 55VP SEM

SOI sample fixture in the Veeco Dimension Icon AFM during analysis

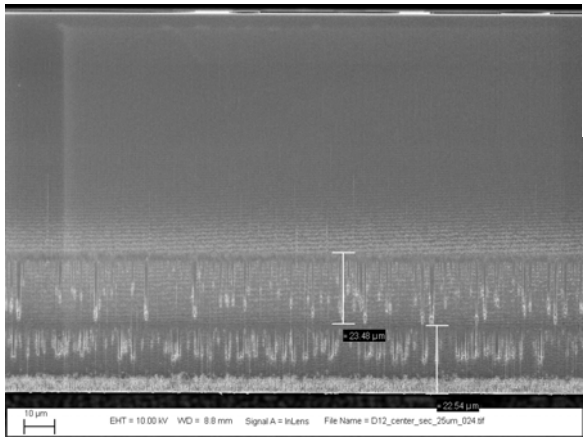
SEM Images
RS847 Die D12, Section 2 (Edge Die)



5 μm



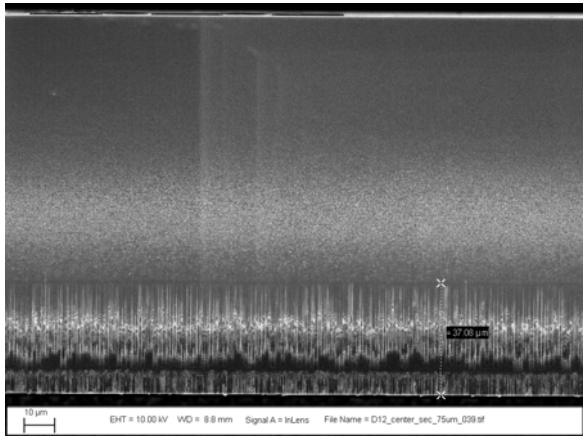
15 μm



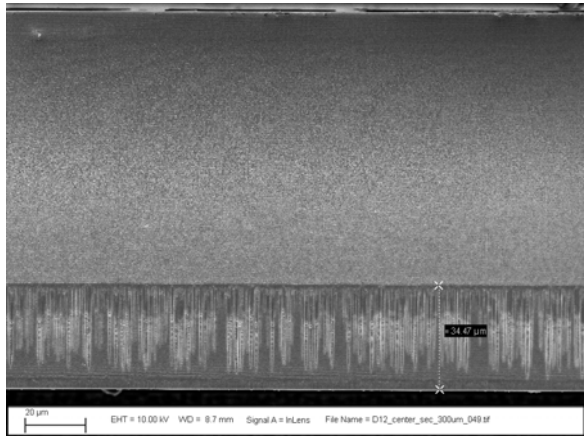
25 μm

Scalloping

Curtaining



75 μm



300 μm

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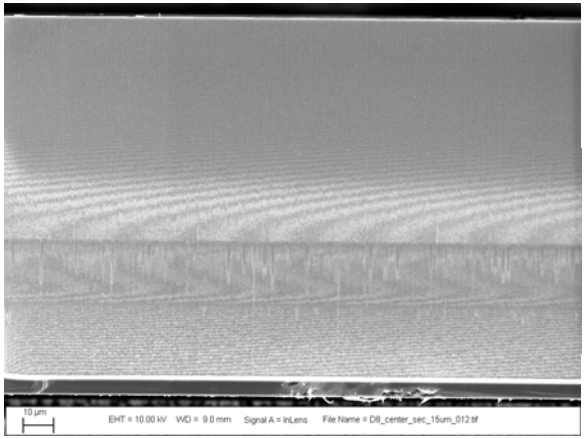
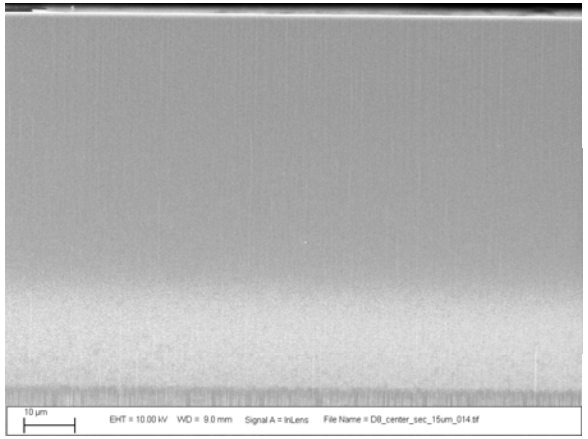
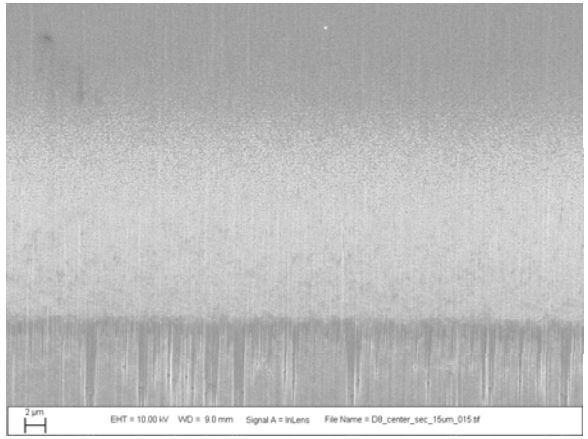
SEM Images
RS847 Die D8, Section 2, 15 μm trench



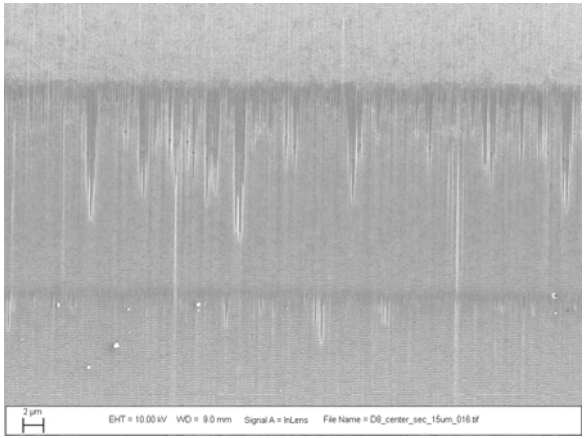
Full Height – 10 μm



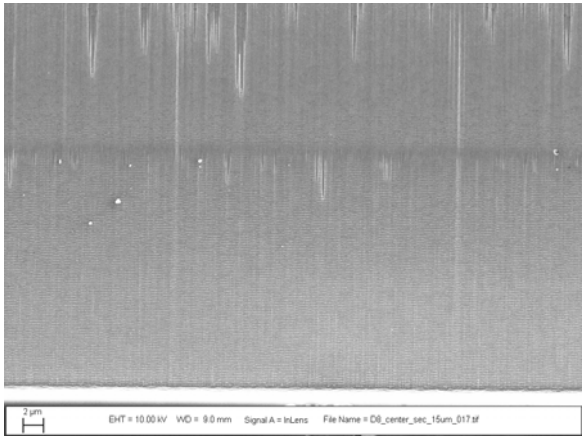
Top Section – 10 μm



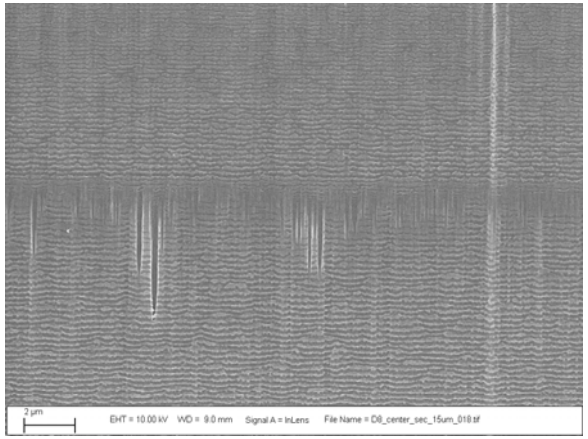
Border – 2 μm



Lower Section – 2 μm



Lower Section – 2 μm



Lower Section – 2 μm

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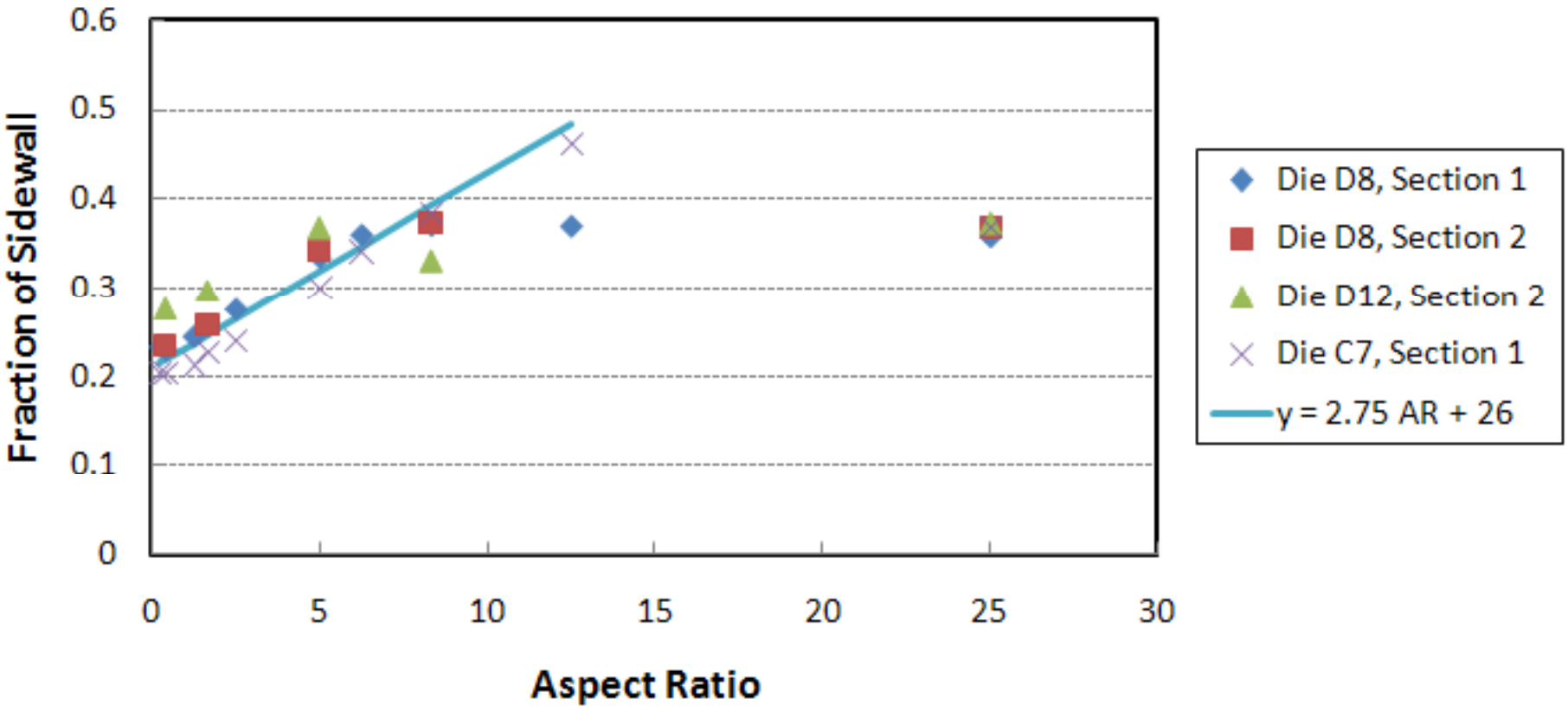
Height of Rougher Curtaining Section



Height of the rougher curtaining region at the bottom of the sidewall divided by the total etched height as a function of the trench aspect ratio. All of the samples cleared the trench for aspect ratios of 6.25 and below. Die C7, Section 1 is the only one that cleared the trench for aspect ratios of 8.3 and 12.5, and its data continuing to follow the trend line for those aspect ratios.

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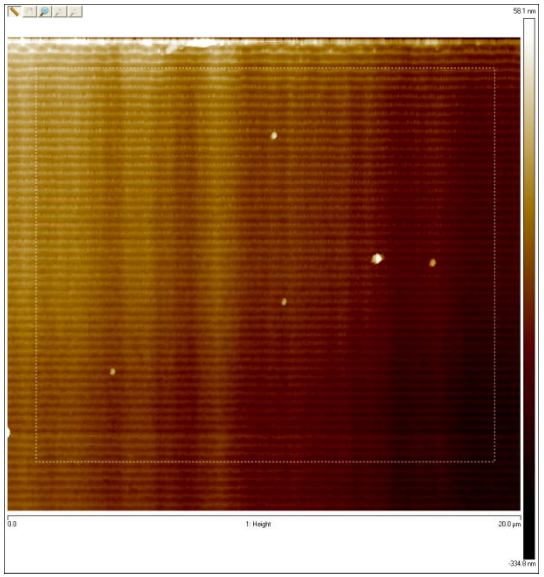
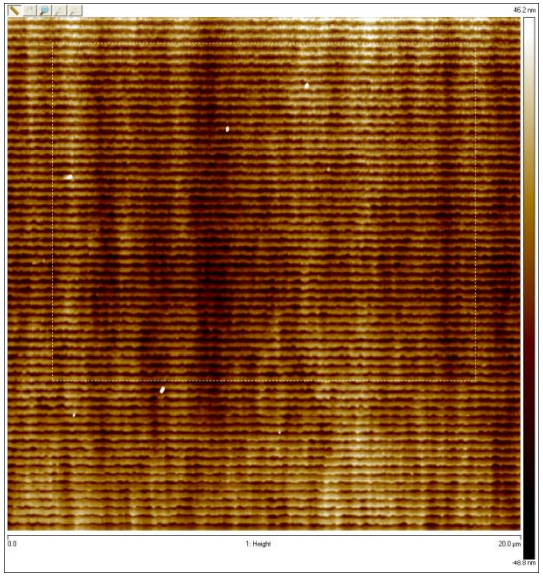
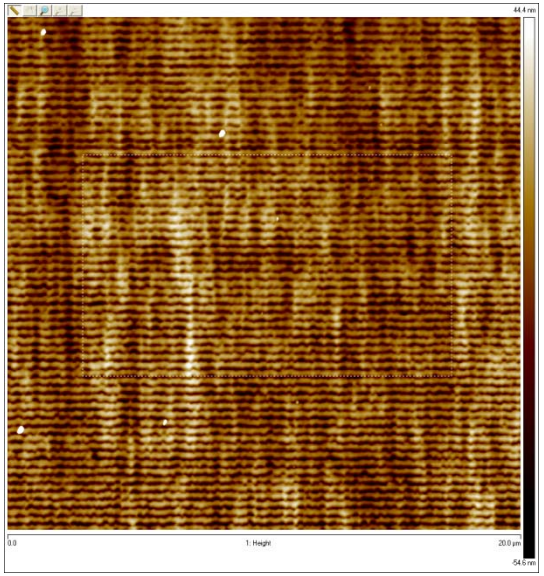
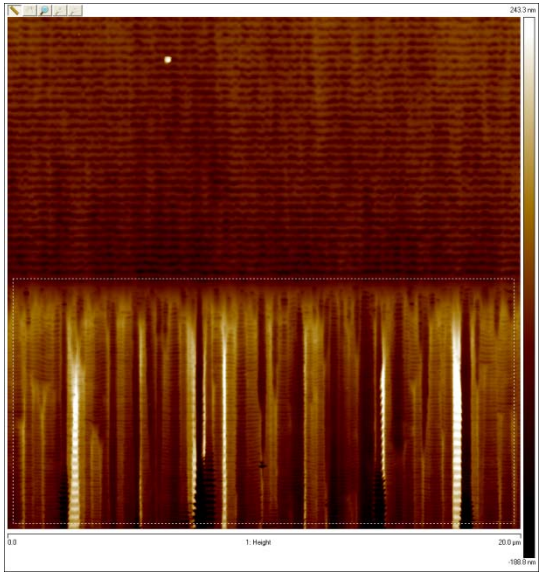
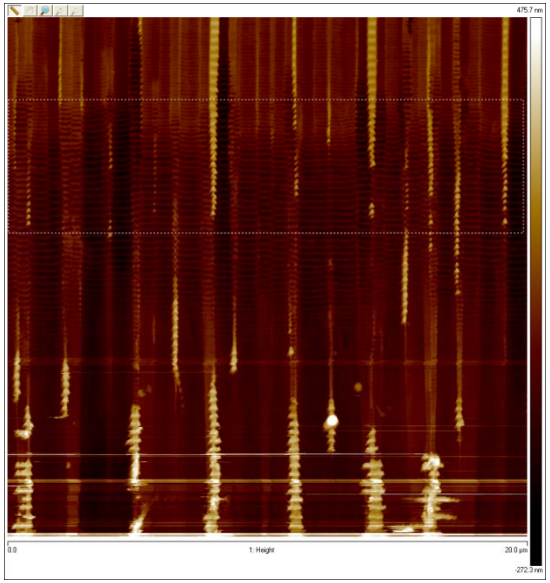
AFM Images
RS847, W100, 100μm trench Top to Bottom

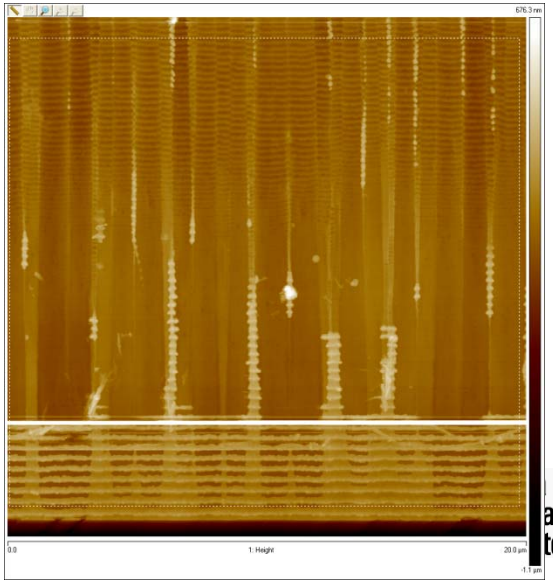




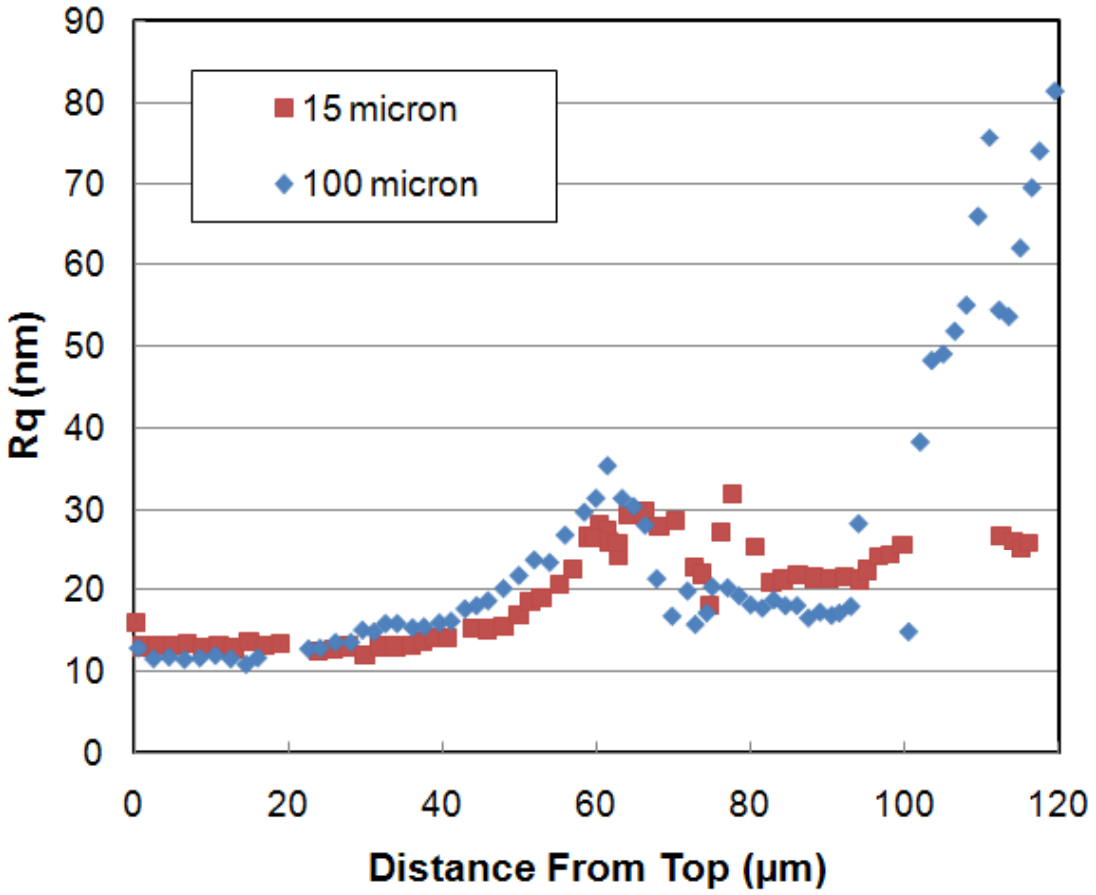








Roughness Along the Sidewall



RMS Roughness as a function of distance from the top surface for two trench widths: 15 μm and 100 μm corresponding to aspect ratios of 8.3 and 1.25, respectively.

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Summary and Conclusions

- DRIE SOI sidewall roughness investigated for aspect ratios from 25 to 0.25.
- Upper regions exhibited sidewall roughness with a scalloping morphology and lower regions exhibited a curtained morphology.
- Sidewall roughness characteristics did not depend on die location on the wafer.
- The fraction of the surface exhibiting the rougher curtained morphology increases linearly with aspect ratio if the etch reached the bottom of the device layer.
- The curtained region roughness for the 1.25 aspect ratio was 2-3 time rougher than that for the 8.33 aspect ratio.

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Acknowledgments

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