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Quantum Information S&T

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Silicon enhancement mode nanostructures for quantum computing

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Albuquerque, New Mexico, USA

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LDRD LABORATORY DIRECTED RESEARCH & DEVELOPMENT

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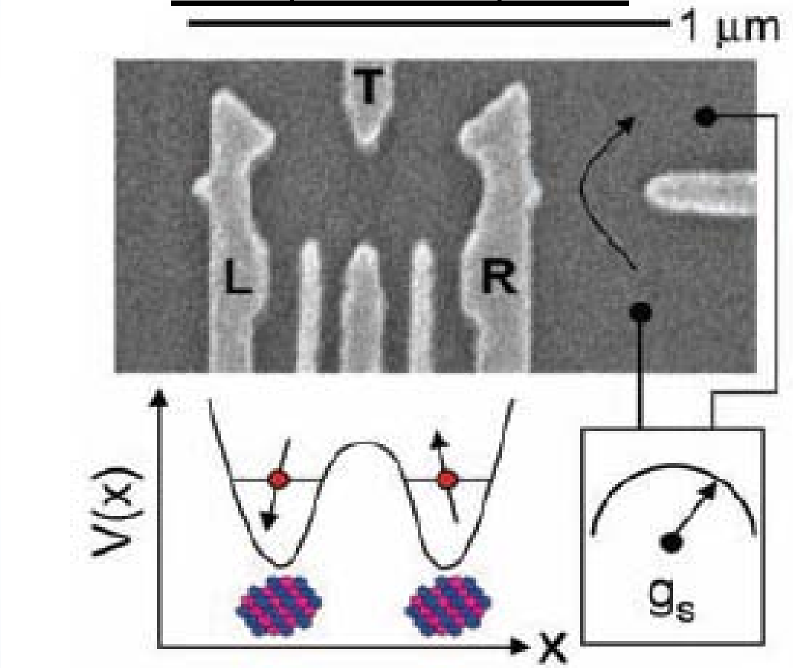
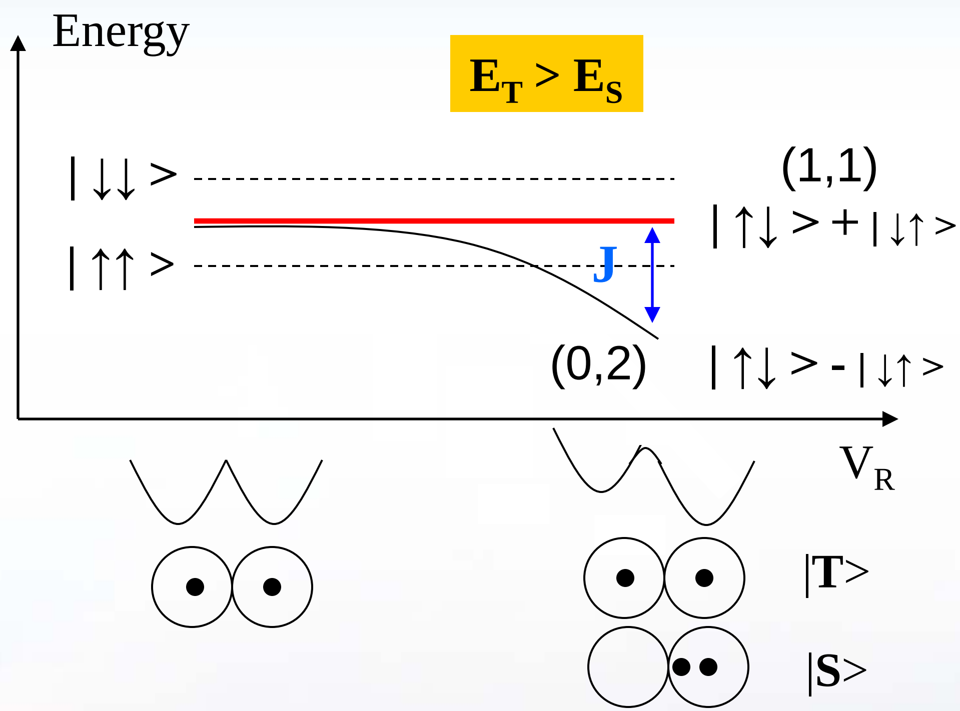
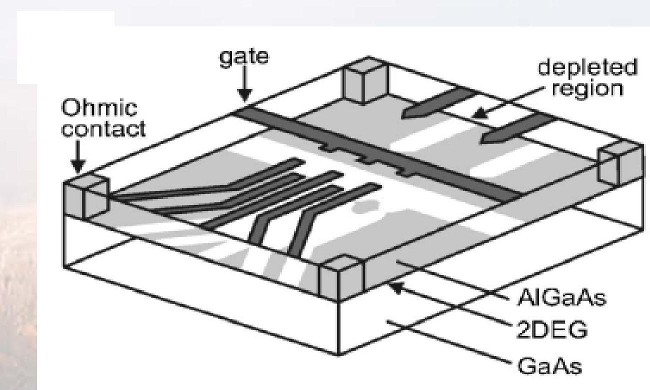
One inspiration for semiconductor quantum computing

Petta, Science, 2005





Elements:
- Two level system
  - m=0 subspace of 2 electrons
- Electrically tunable (tunnel coupling)
- Charge sense

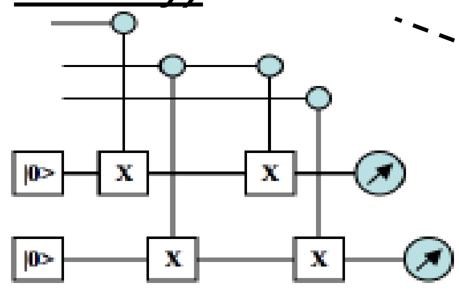


Quantum error correction needed for circuit model approach to QC

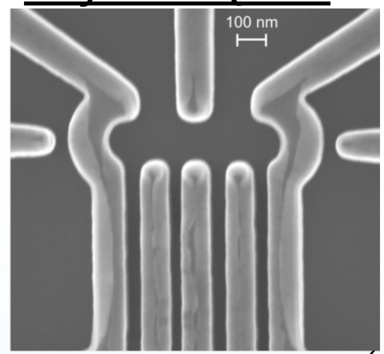
Some conclusions from logical memory

- Number of operations necessary to complete a QEC cycle => ballpark 10^{-4}
- Scheduling conflicts lead to more idles and gates (electronics, t_msr & DD)
- Circuit would show benefit at p~$5x10^{-4}$ assuming negligible idle error
- You want p/p_th as low as possible to reduce amount of QEC
- Fast high fidelity gates is made difficult in system (e.g., jitter on MUX/DEMUX clock)
- Long T2 really helps both idle as well as minimizing error in gates w/out DCG

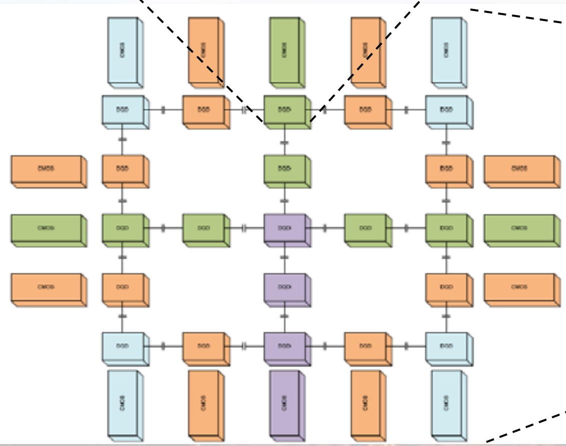
Quantum Circuit (Logical Memory)



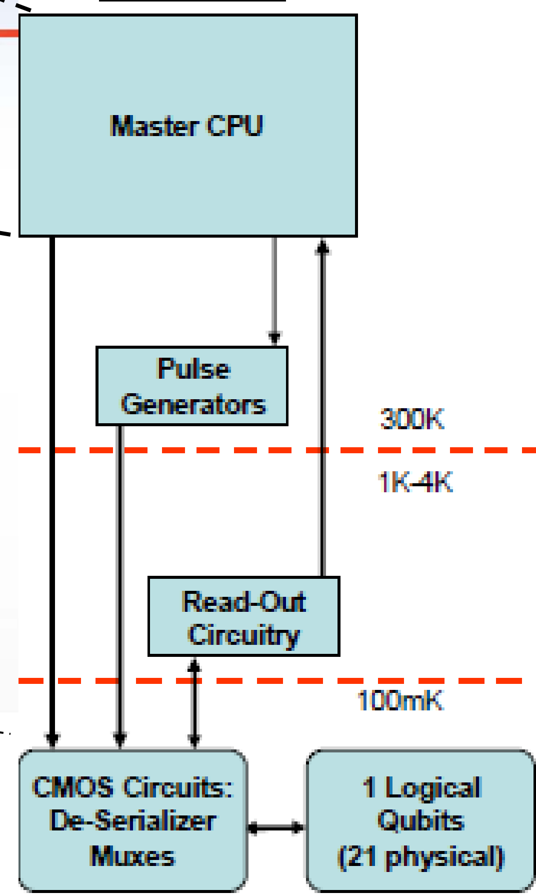
Physical Qubit



Chip Level Circuit (21 qubits)

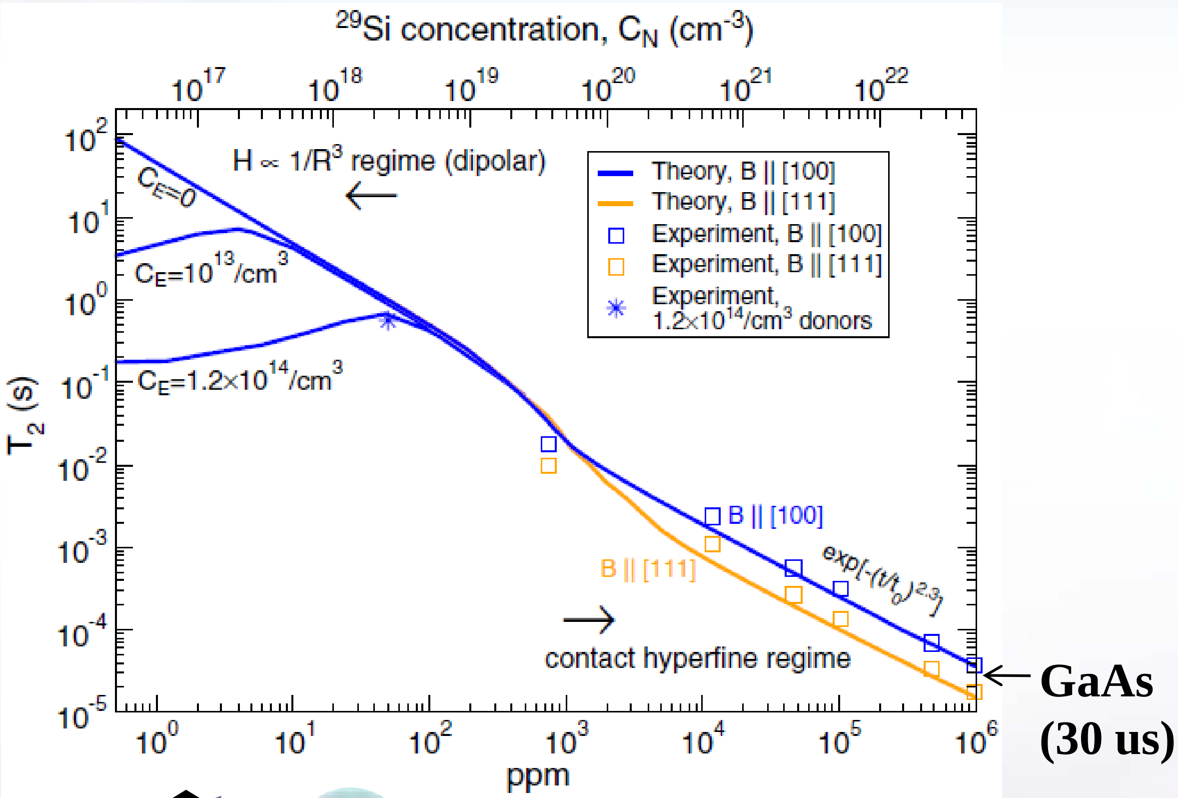


Classical-Quantum Interface

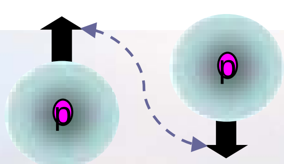


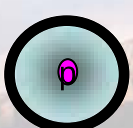
Levy et al. SPAA (2009)
Levy et al. J. New Phys. 13 083021 (2011)

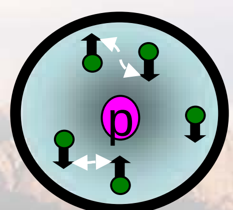
Motivation for Silicon Qubits



- GaAs has non-zero nuclear spin isotopes shorten T_2
- Si isotope enrichment removes nuclear spin, long T_2
- Nuclear spins can be useful for rotations between S & T0 but it limits T_2 , introduces errors on other gates
- Recent device progress in electron spin manipulation (spin read-out & evidence of coherence)
  - UNSW (donors)
  - UCLA (MOS)
  - HRL (SiGe mod. doped)
  - U. Wisconsin (SiGe mod. doped)

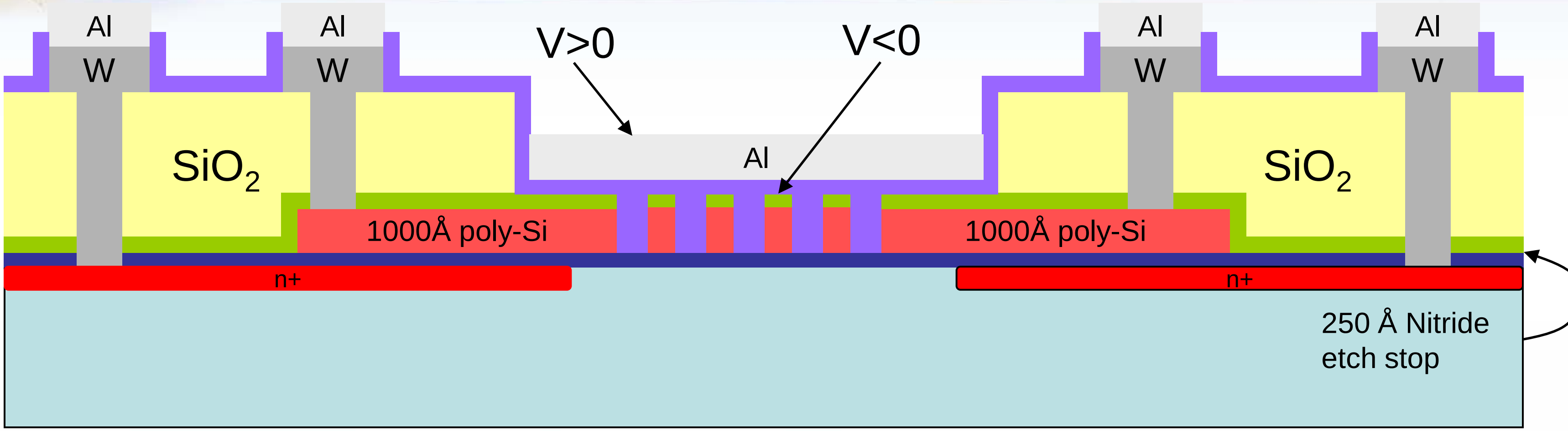






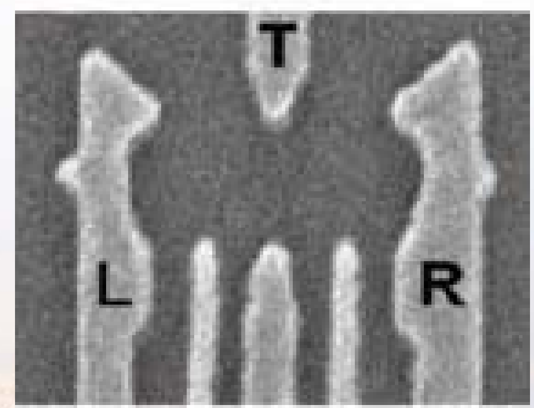
Witzel et al, PRL 105, 187602 (2010)

Silicon Enhancement Mode Quantum Dots



- Many silicon approaches
- SNL looking at enhancement mode & Si foundry approach
- This talk: MOS, SiGe/sSi and donors

GaAs design to Si?

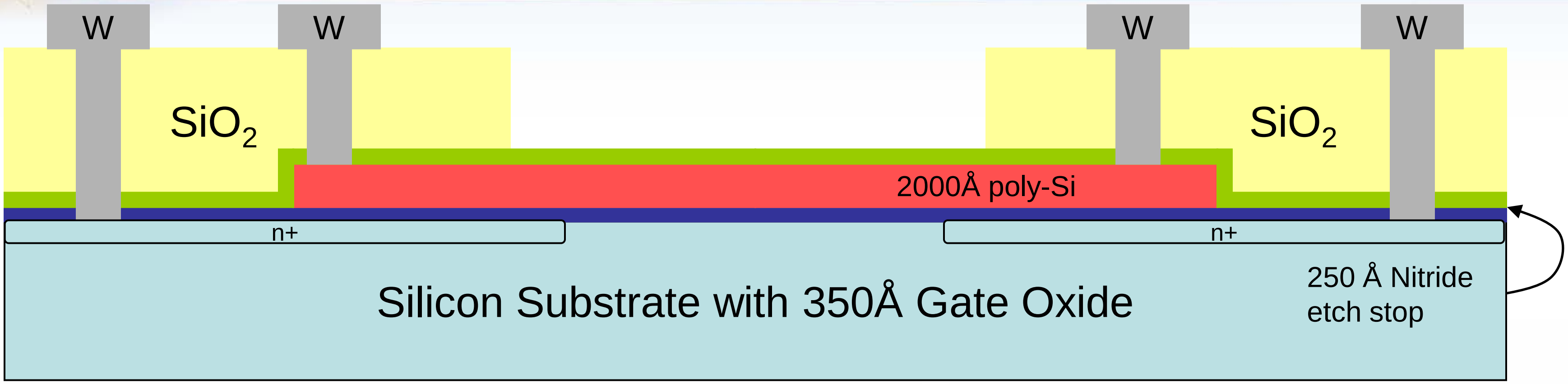


Petta et al. [2005]

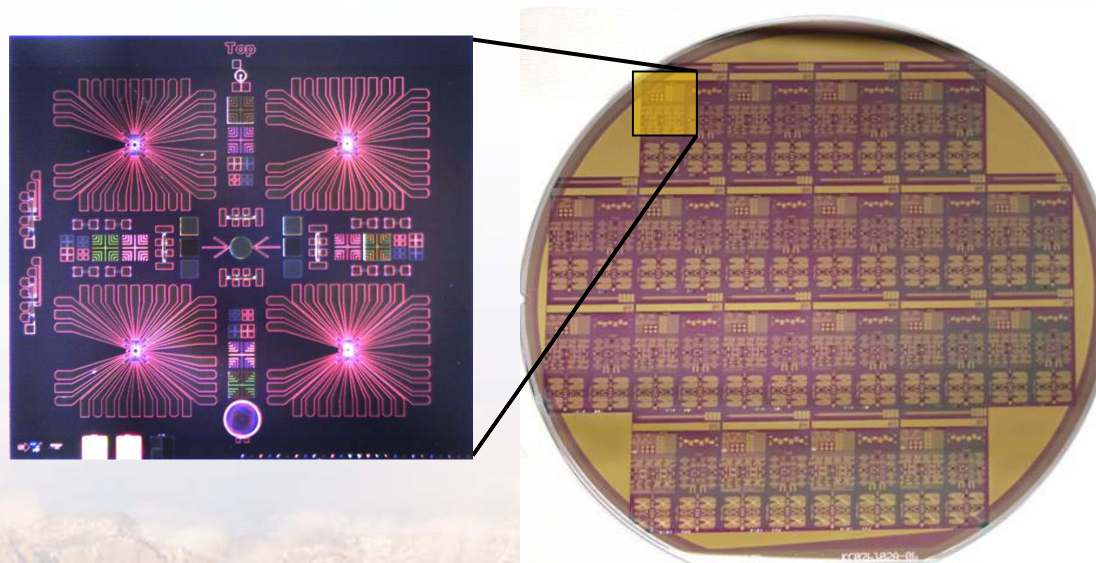
<u>Motivations</u>

1. Platform is modular design for both donors and SiGe/sSi
2. Tunable parameters (density, valley splitting, g-factor?)
3. No dopants
4. Start with MOS:
   - well understood material system
   - overlapped interests for other Si approaches
5. CMOS compatible (MOS)

Silicon foundry

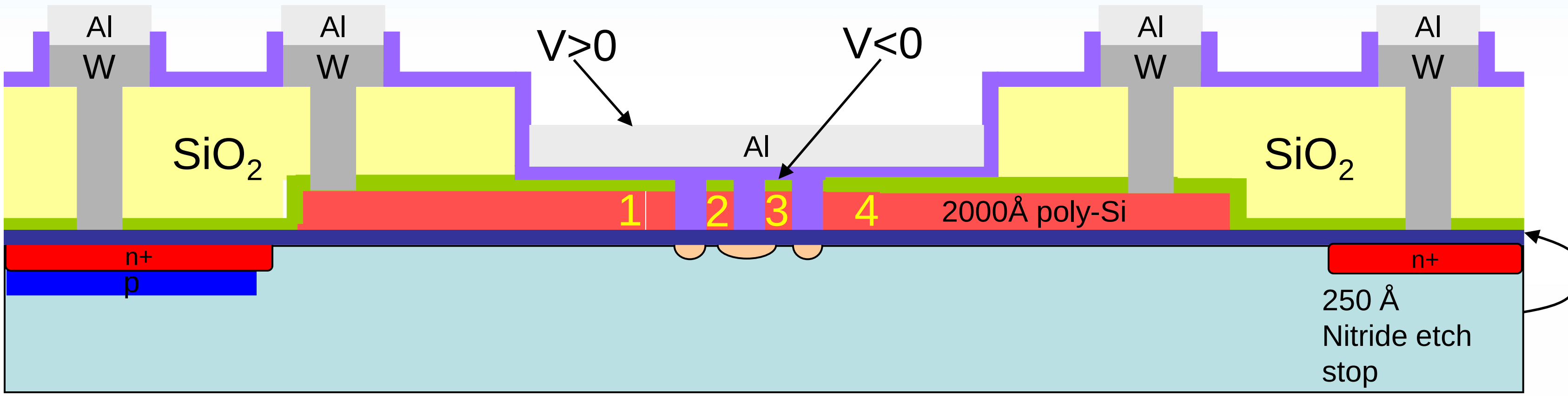


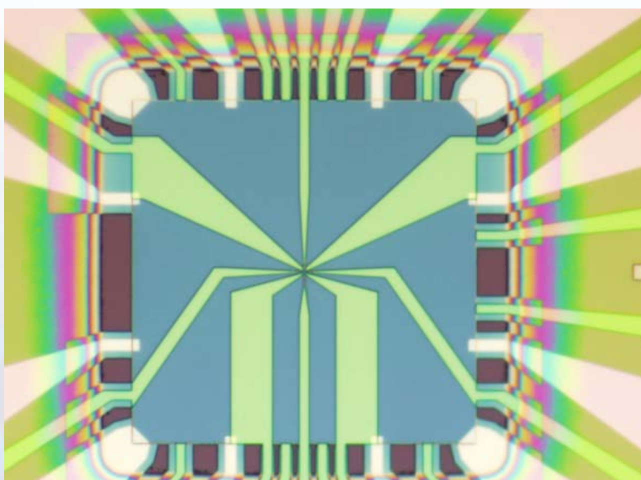
<u>MOS Stack from Si fab</u>
Deep UV lithography (0.18 um)
7,500 – 15,000 mobility cm2/Vs
QDs possible with 0.18 um litho
Smaller features w/ EBL in/out of fab
Standard MOS material set only



T. Pluym

Back-end processing

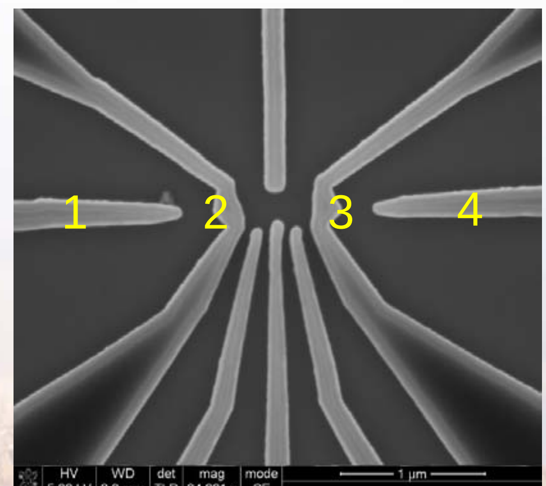




<u>Micro-fab facility</u>
Rapid turn-around EBL
Poly-silicon etch
Aluminum oxide
Top Al gate

<u>Low parasitic RF die</u>

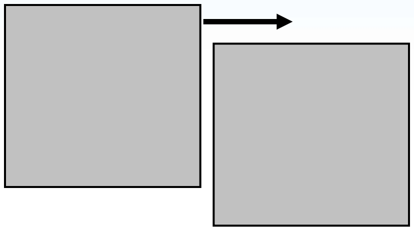
GaAs design to Si



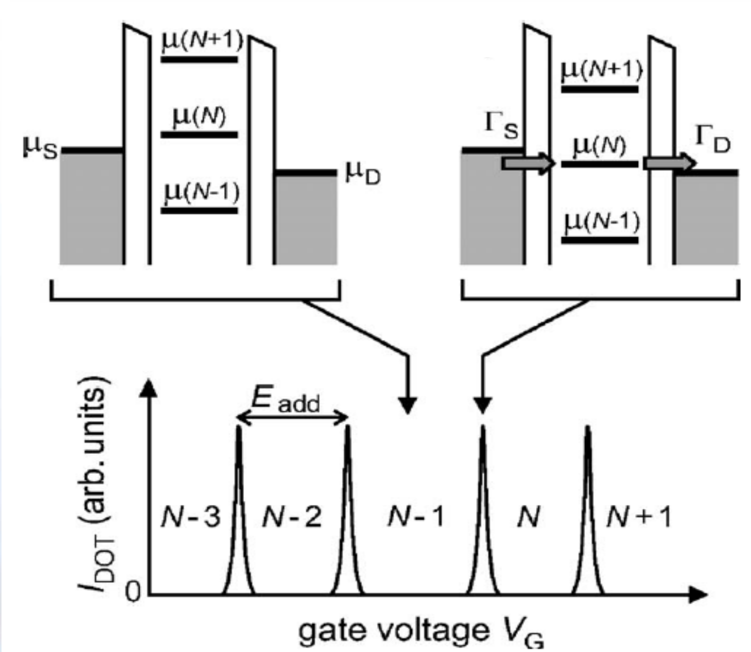
T. Pluym, B. Silva, J. Dominguez, N. Bishop

Coulomb blockade

Imbalance in chemical potential produces current



Current goes through QD when levels lines up

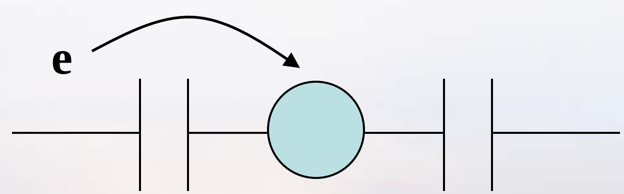


$$V = \frac{q}{C}$$

- Equally spaced energy levels related to charging energy of capacitance
- Periodic current resonances produces – "Coulomb blockade"
- Low temperatures required (T << 4K)

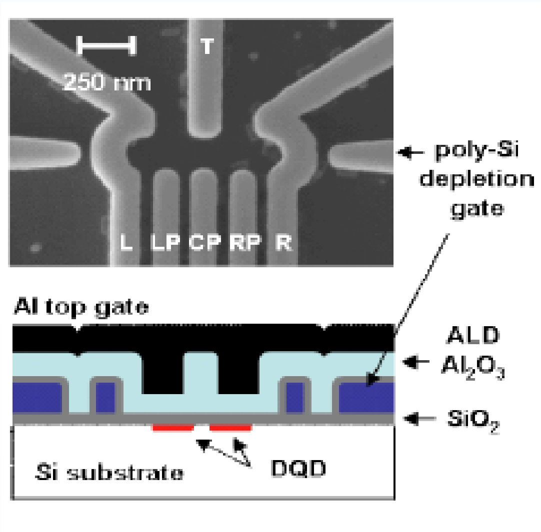
C_{sum} ~ 16 aF

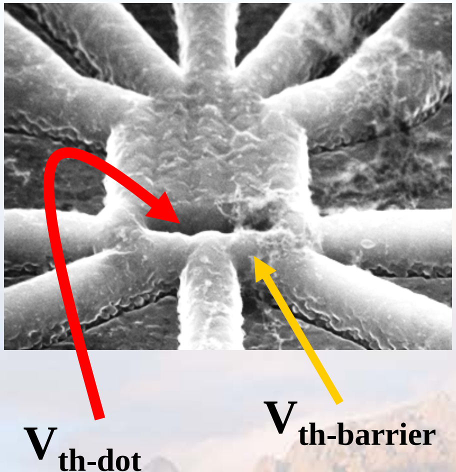
$$\Delta V = \frac{q}{C} \sim 1\text{ mV}$$



Chemical potential levels are spaced by charging energy

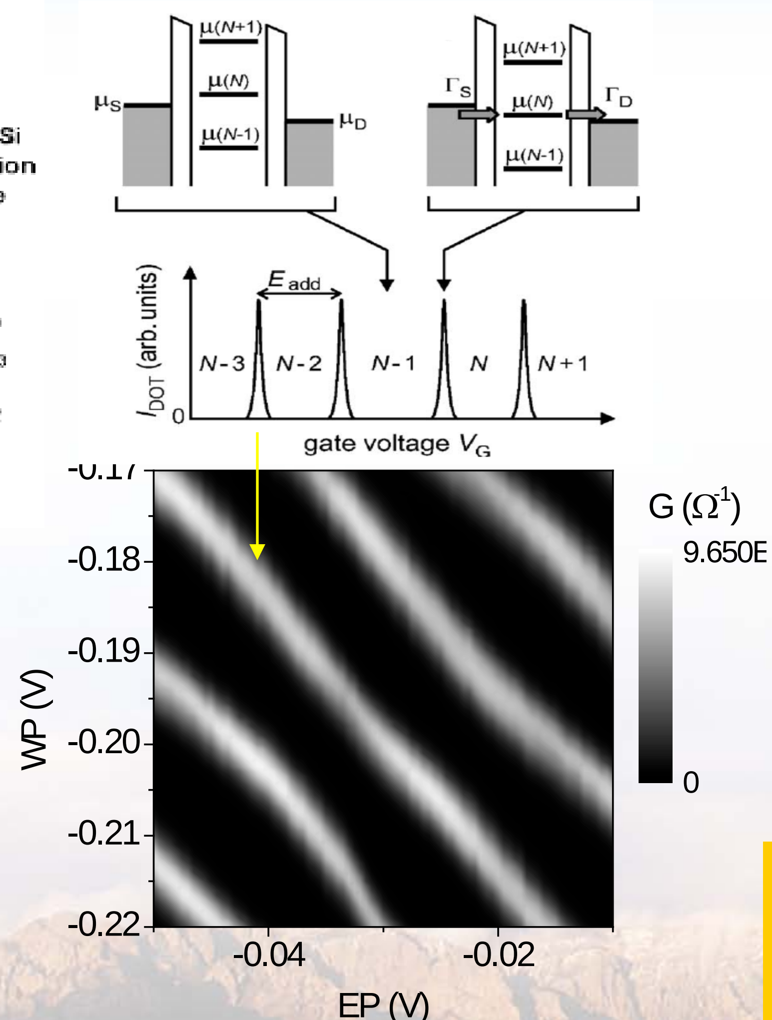
Reconfigurable Dot with Gates



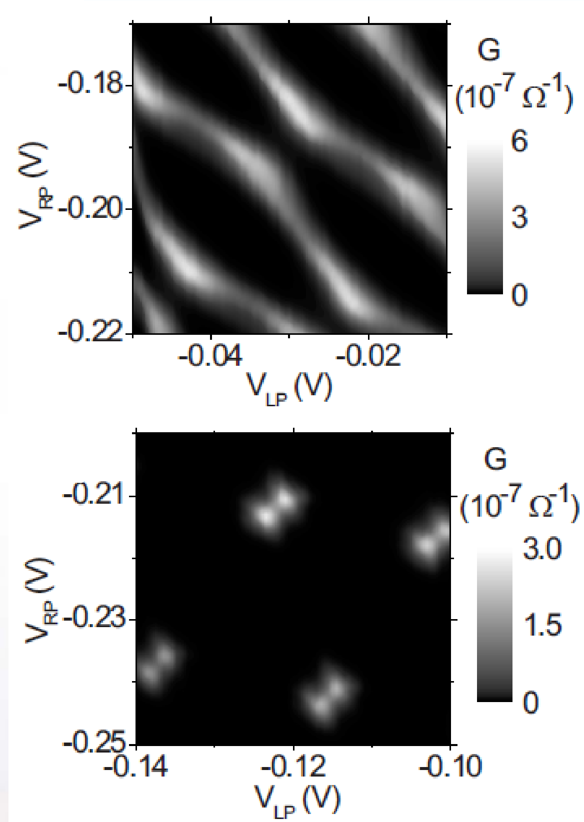


L. Tracy, et al. APL 2010

Coulomb blockade



Tunabilty

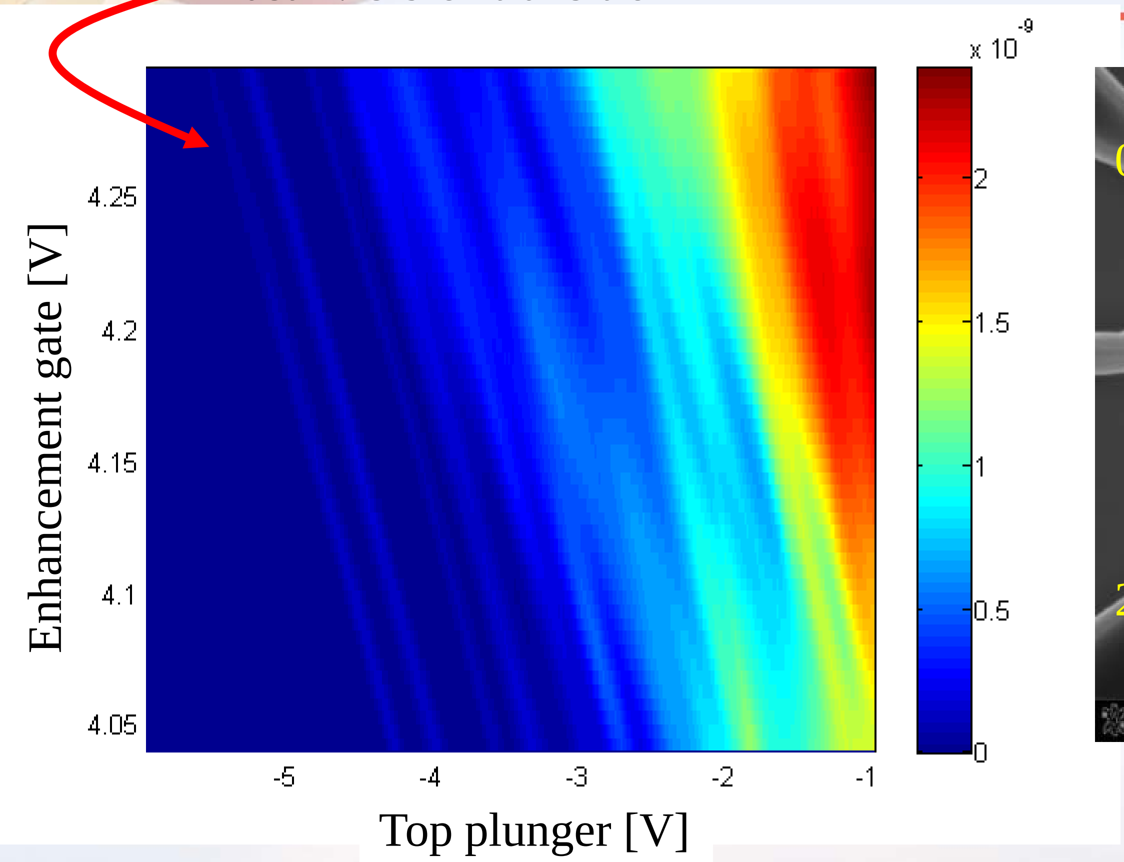


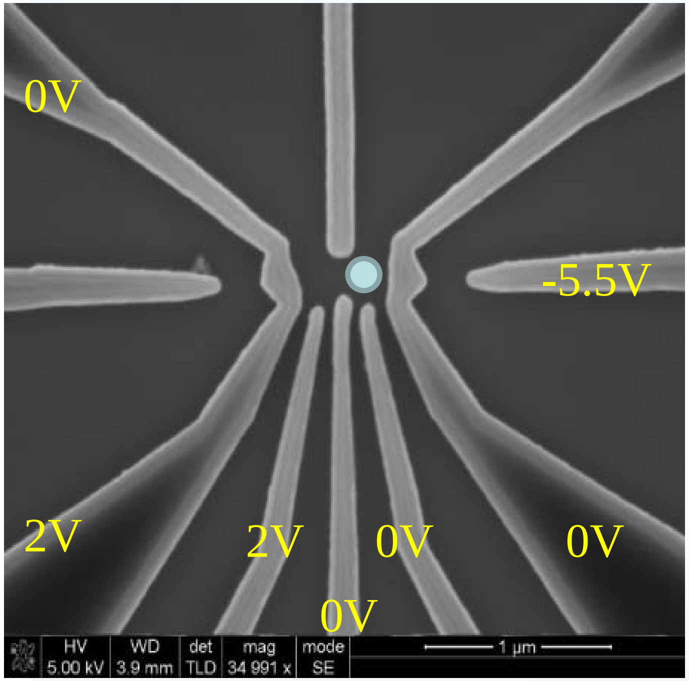
Problems:

1. Charge sensor constriction too thin
2. Top gate coupling imbalance to barrier/dot

Few electron single QD

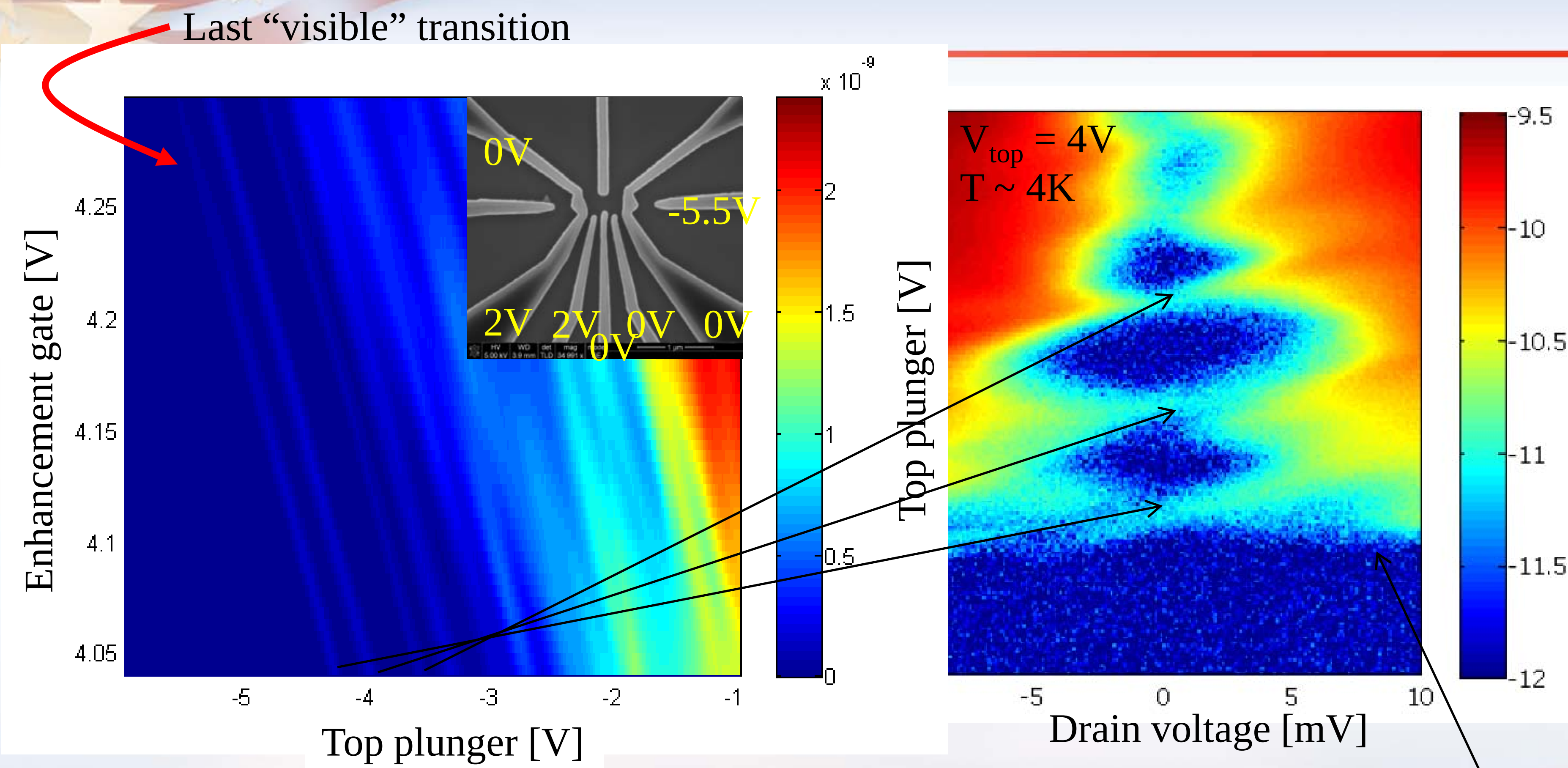
Last "visible" transition





- Edge of transport through dot observed
- Several possible reasons
  - tunnel barrier is gradually turning off (often the case)
  - Last electron
- <u>This case</u> is not gradual and no additional transitions are observed over reasonably large V_{top} scan and Vsd

Wider tunnel barrier



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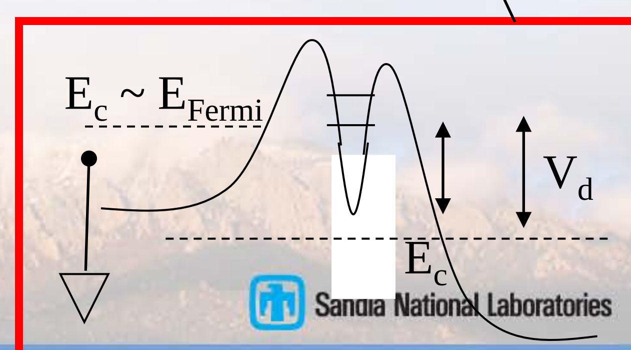
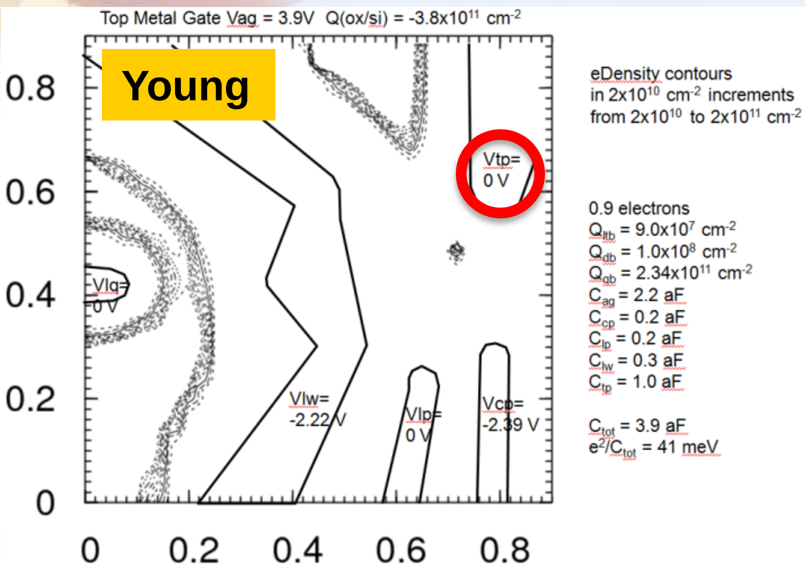
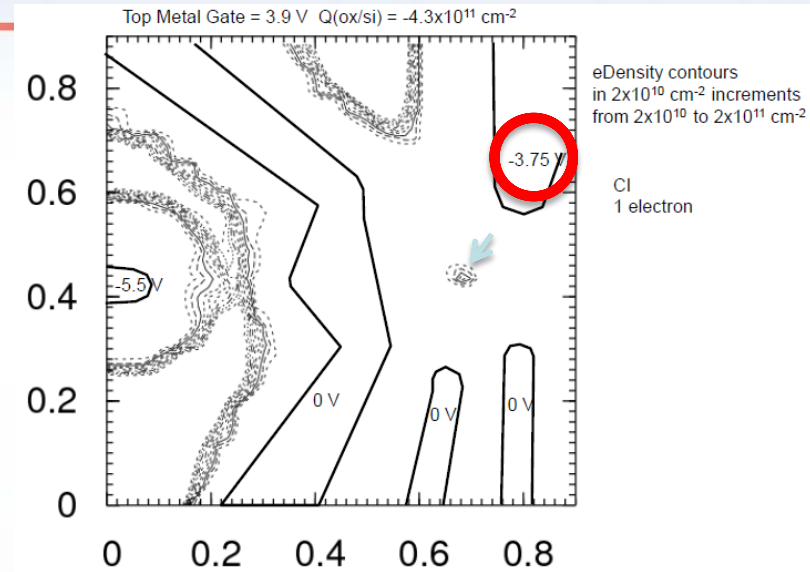


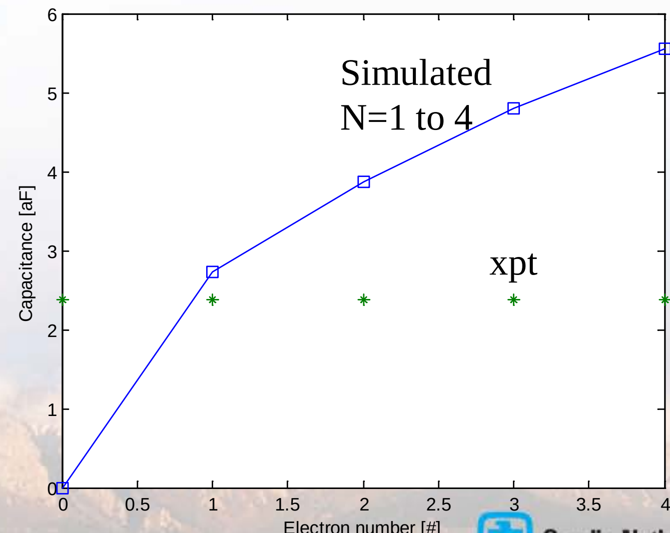
Simulation calibration





Gate	Measured [aF]	CI (N=1) [aF] TP=-3.75/ 0	Semi-classical [aF] TP=-3.75
AG	2.37	2.73 / 2.2	3.13
TP	0.48	0.29 / 1.0	0.3
L	0.56	1.56 /0.3	1.9
LP	0.29	0.45 /0.2	0.49
CP	0.54	0.59 /0.2	0.66

Carroll, Young



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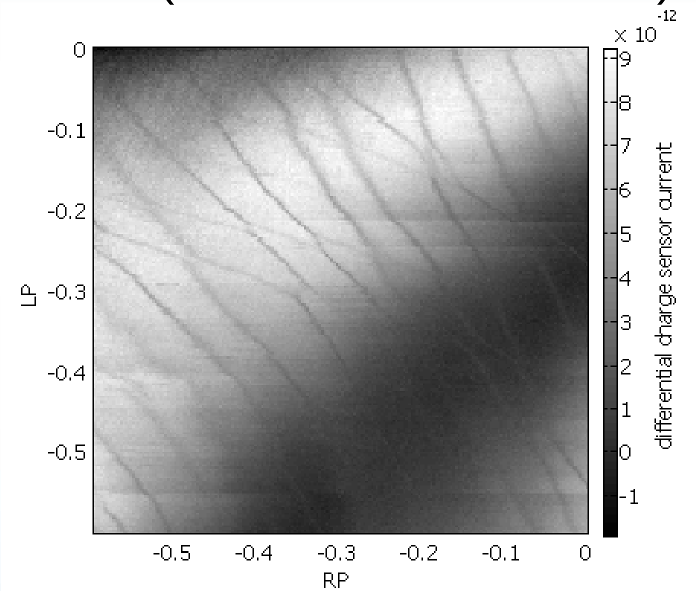
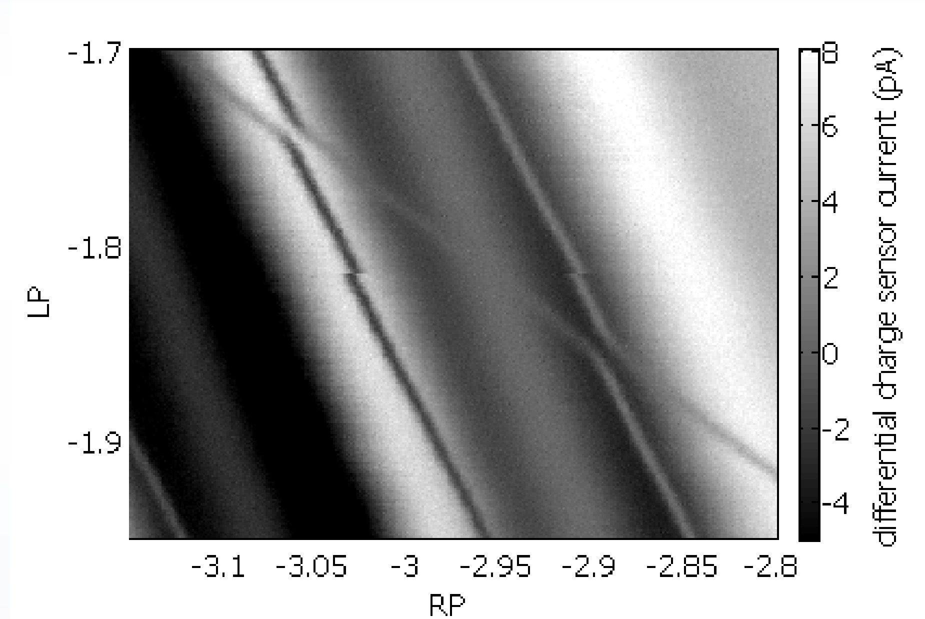
- Simulation is consistent with observed magnitudes in experiment at N=1

Double dot and charge sensing

MOS (same device as before)

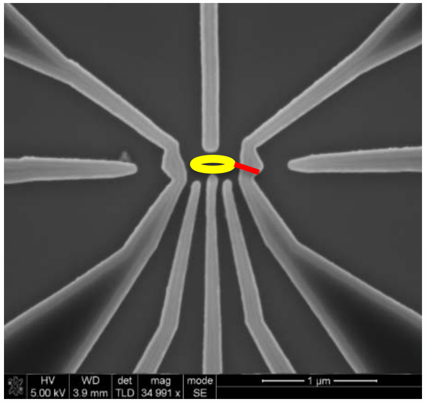




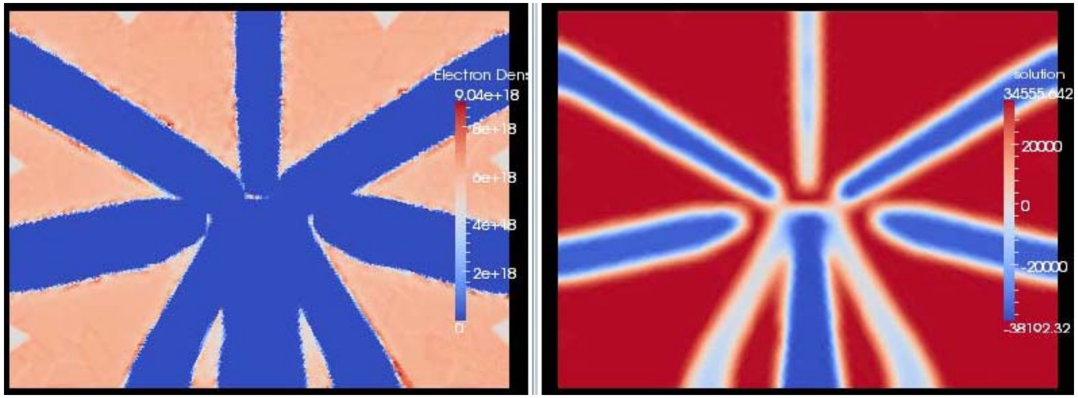
- Primary concern is to isolate a singlet and T0 subspace for qubit => tune DQDs
- Beginning to look for Pauli-blockade in many electron cases and few electron when possible
- Challenges:
  - Sensitivity
  - Reduce chance of defects
  - Fewer electrons
  - => smaller size designs

Lilly

Smaller dot designs and path dependent tunability

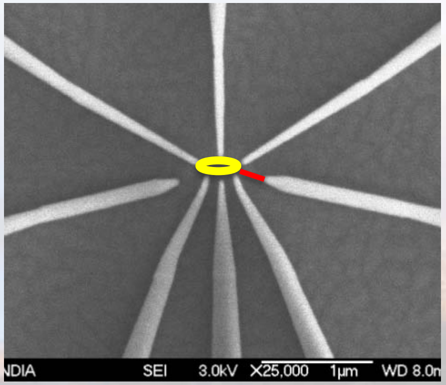


Modeling optimization: few electron DQD possible



Smaller dot size & proximity

1. Better charge sensitivity
2. Fewer defects



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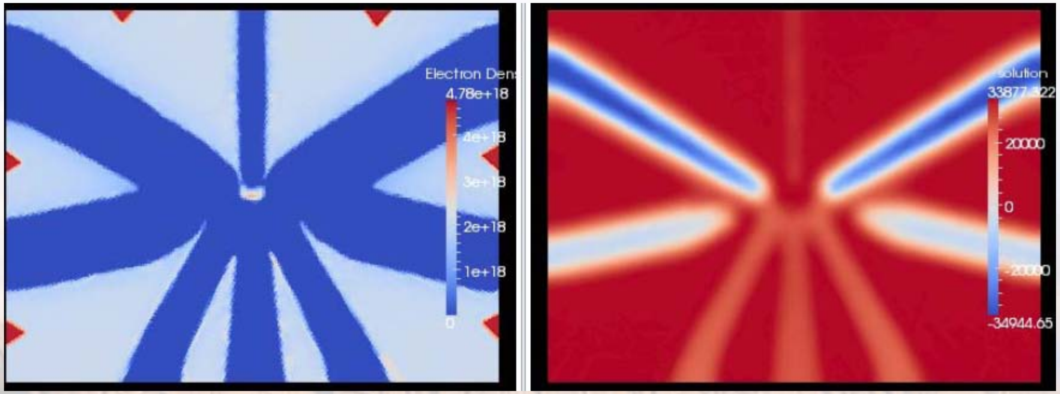
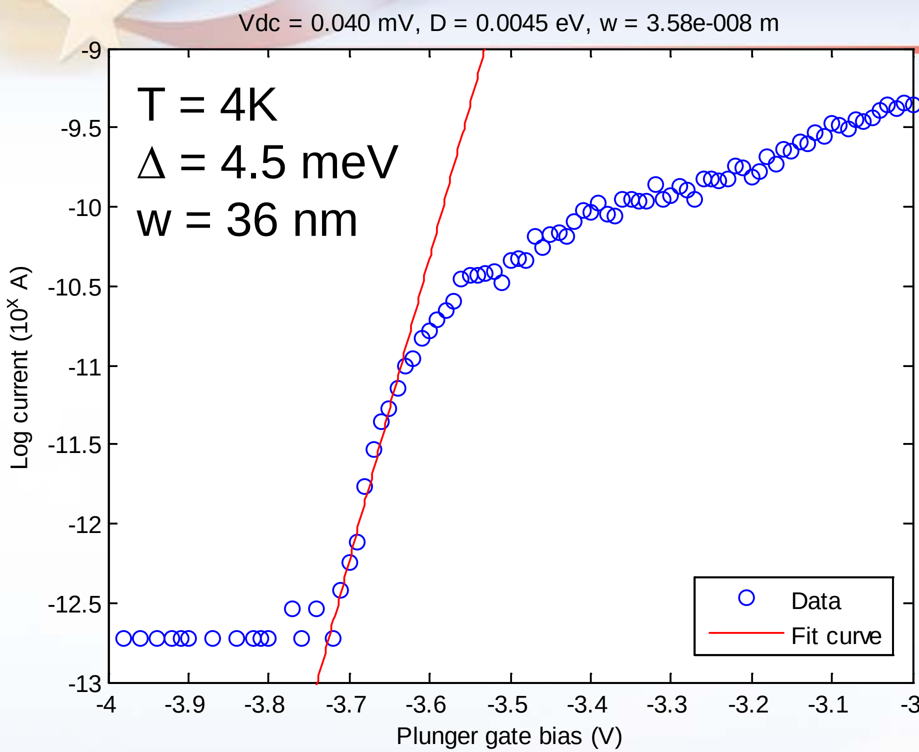
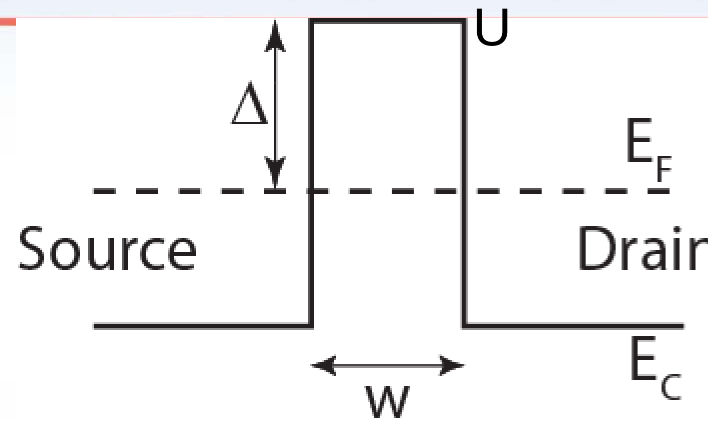
Modeling optimization: experimental path has non-ideal minima



Nielsen, Muller, Young (synergistic research)

Tunnel barrier model





$$I = q\Gamma \approx f_0 e^{-\frac{2w}{\hbar}\sqrt{2m^*\Delta}}$$

<u>Limitations</u>

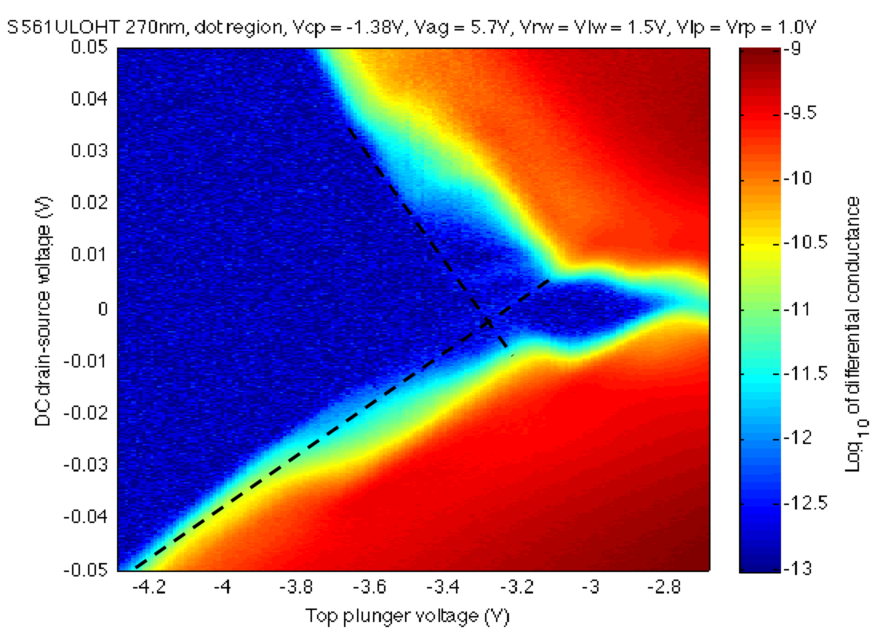
- Square barrier
- WKB approximation
- Linearize the radical
- Phenomenological parameter f_0

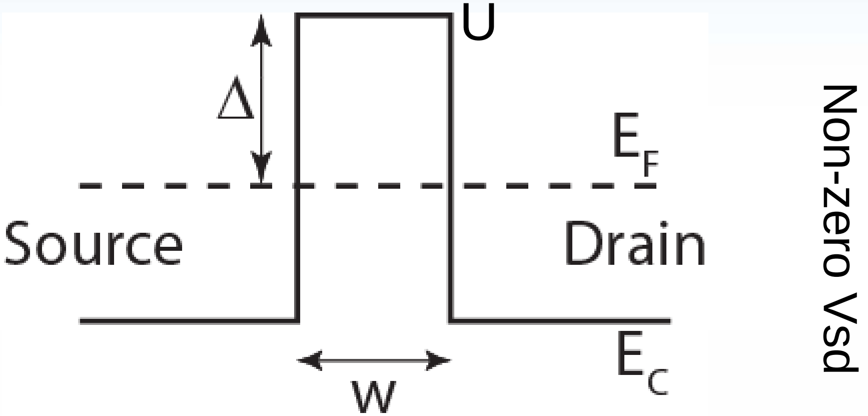
$$\ln(I) = \ln(qf_0) - \frac{w}{\hbar}\sqrt{\frac{2m^*}{\Delta}}\left(2\Delta + q\frac{C_{gate}}{C_\Sigma}(V_0 - V)\right)$$

$$y = mx + b$$

MacLean et al., PRL 2007

Consistent results





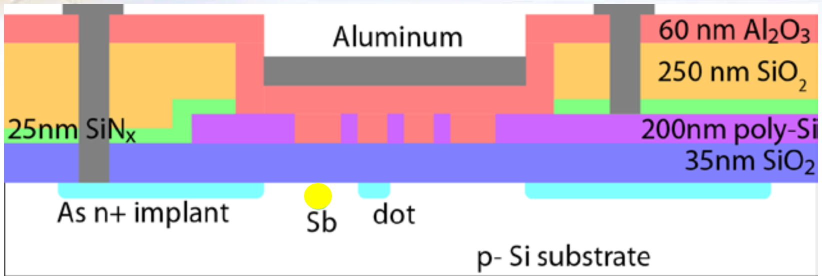
Vds (mV)	Vg (V)	Δ (meV)	W (nm)	Δ@ Vds = 0V Vg = -3.4V (meV)
-11	-3.26	4.63	21.9	15.6
-10	-3.24	4.42	22.9	13.7
10	-3.12	2.79	26.8	13.8
11	-3.13	2.69	26.7	13.7

$$dU = \frac{\partial U}{\partial V_{sd}} dV_{sd} + \frac{\partial U}{\partial V_{gate}} dV_{gate}$$

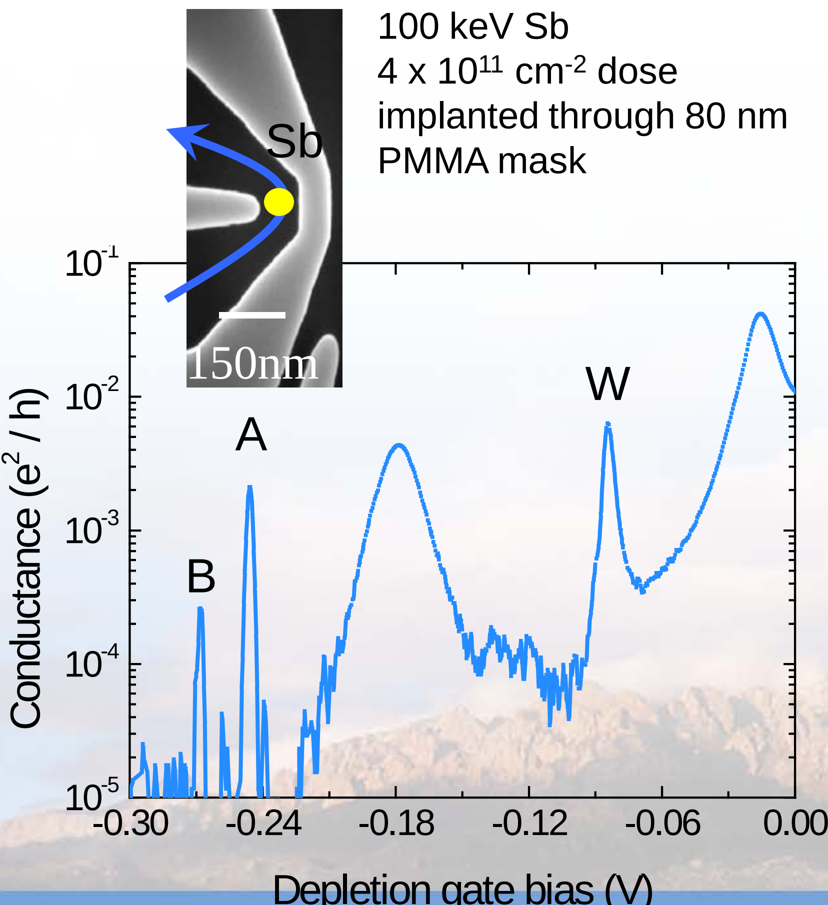
$$dU = \Delta - \Delta_0 - q|V_{sd}|$$

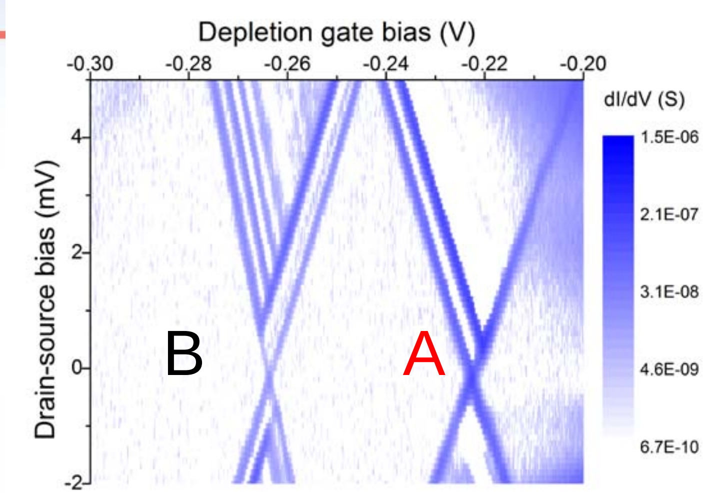
$$\Delta = \Delta_0 + q|V_{sd}| + \frac{C_S}{C_\Sigma} dV_{sd} + \frac{C_G}{C_\Sigma} dV_{gate}$$

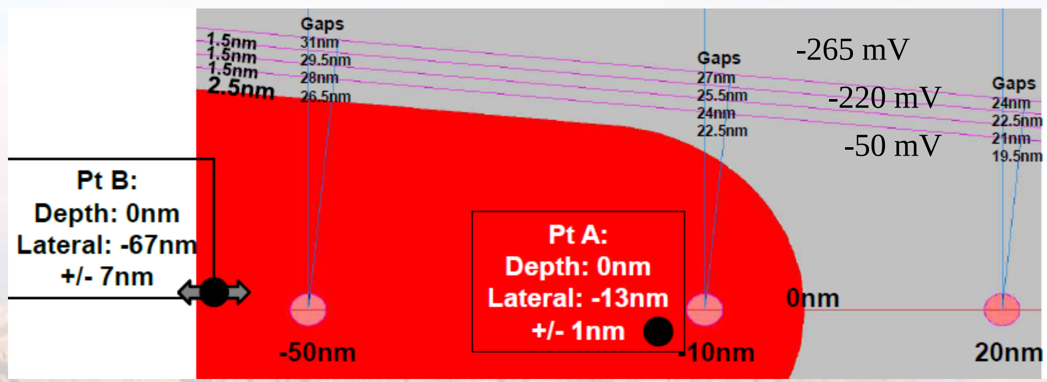
Triangulation of resonances in implanted split-gates



100 keV Sb
4×10^{11} cm^{-2} dose
implanted through 80 nm
PMMA mask







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Comparison of tunnel barrier model to triangulation

Resonance B

Vsd (mV)	Vg (V)	Δ (meV)	W (nm)
25	-0.3805	2.21	48.4
22	-0.3745	2.53	45.6

For V_{SD}= 0V and V_g = -0.27V, Δ = 9.12 meV

dU/dV_{SD} = -0.4203 eV/V (C_s/C = 0.4468)

Resonance A

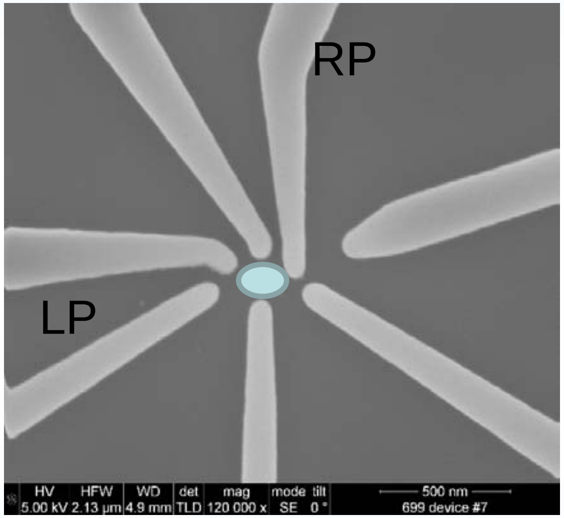
Vsd (mV)	Vg (V)	Δ (meV)	W (nm)
25	-0.353	1.65	39.1
22	-0.345	1.82	38.6

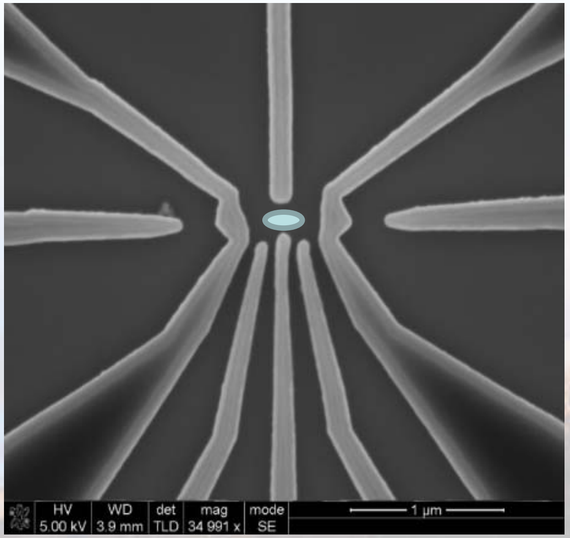
For V_{SD}= 0V and V_g = -0.24V, Δ = 6.05 meV

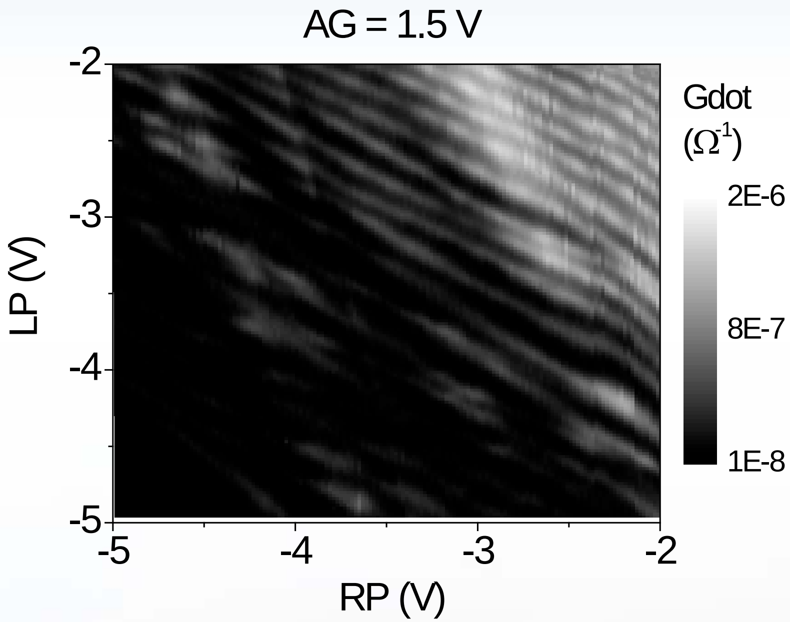
dU/dV_{SD} = -0.3825 eV/V (C_s/C = 0.3899)

Method	Width (A) [nm]	Width (B) [nm]
Triangulation to 1.5x10^11 cm^2 edge	29	34
Square barrier	39	46.5

Smaller design

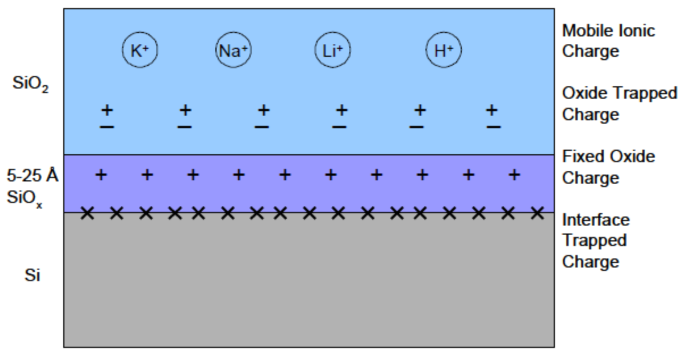




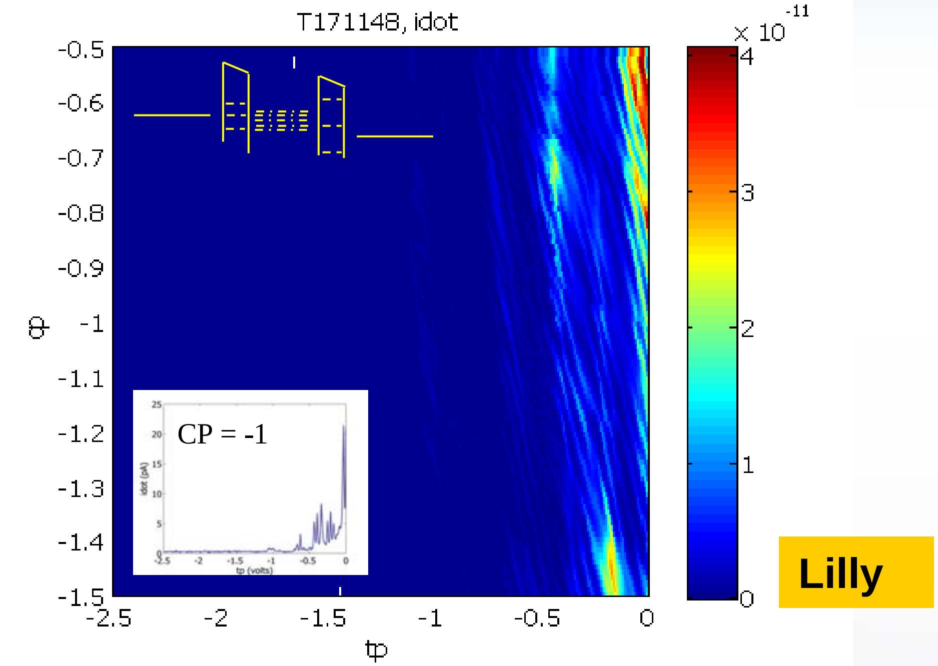


Persisting doubt about MOS DQDs for qubits

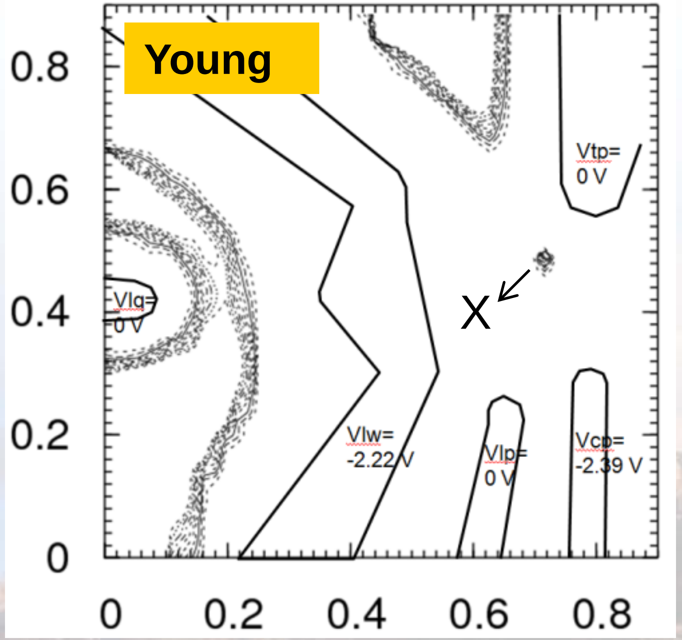
Defects



Coulomb blockade with disorder



Uncontrolled localization



Assume: DQD Area ~ 100 nm x 25 nm

Number of defects in DQD area

1×10^{10} → 0.25 per QD

1×10^{11} → 2.5 per QD

1×10^{12} → 25 per QD

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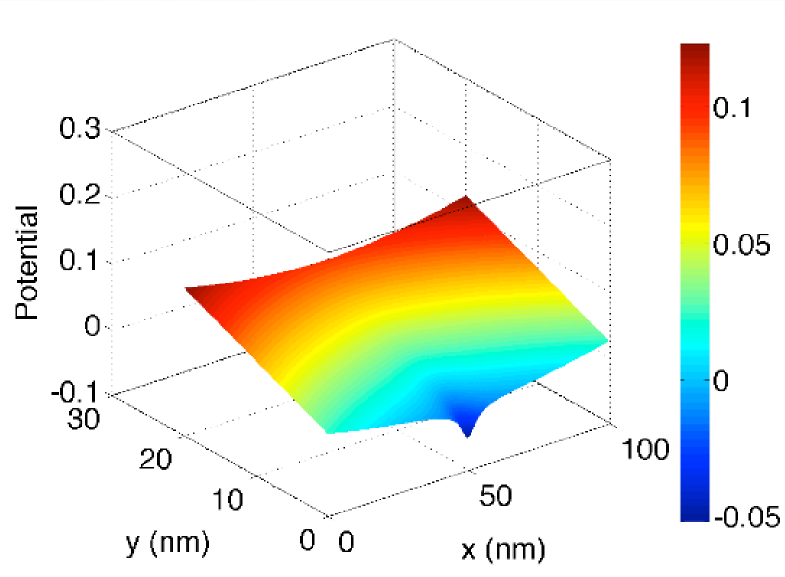
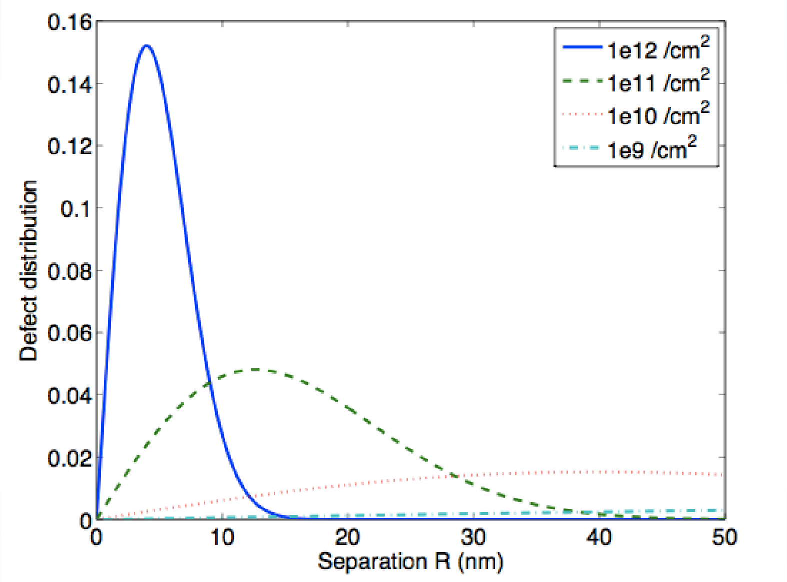
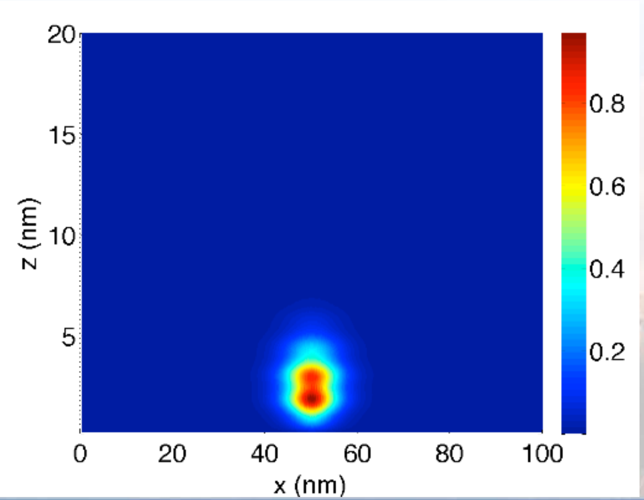
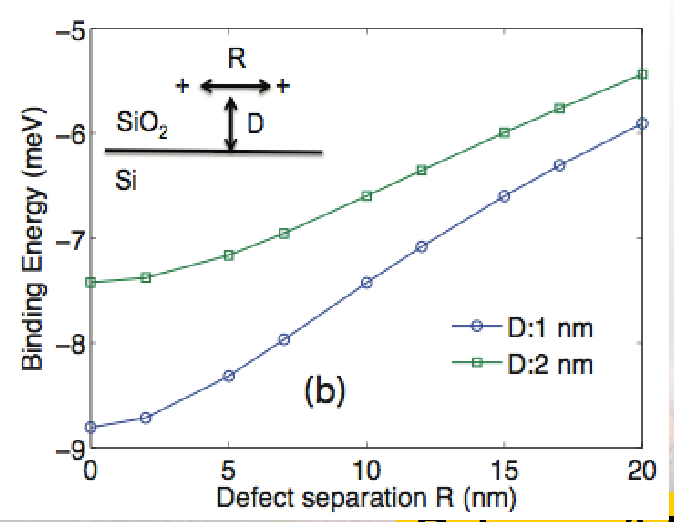
Implications of positive fixed charge



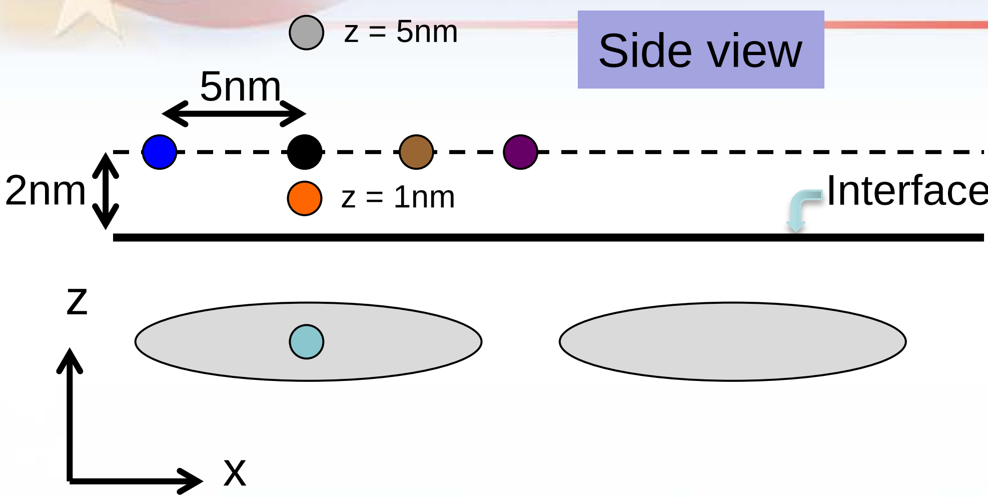


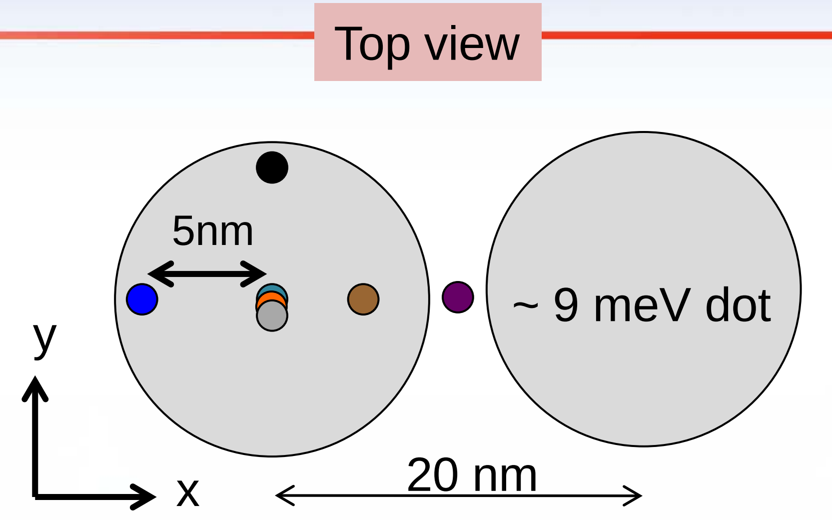


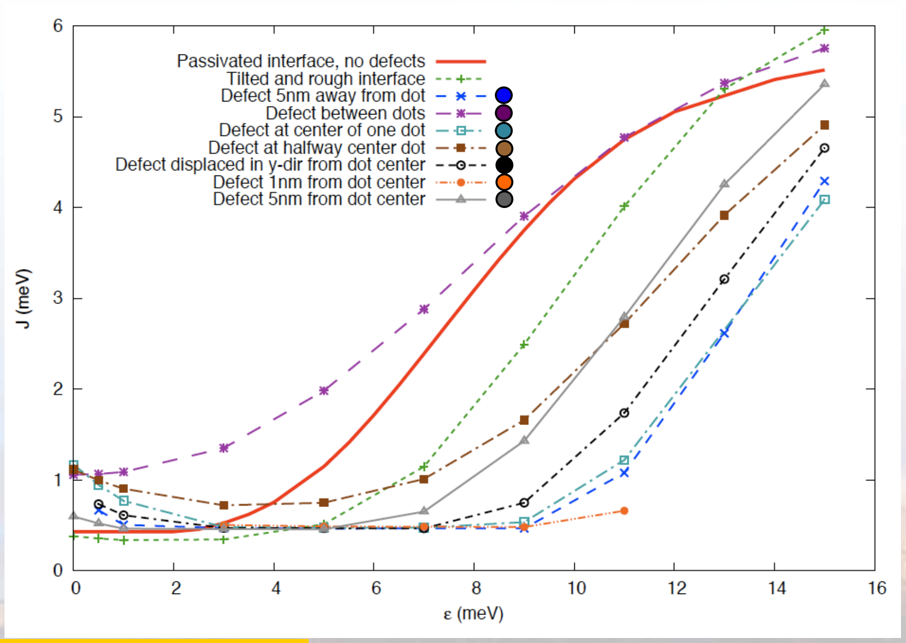


Rahman & Muller

Implications of defects for DQD control







Conclusions:

1. Defect produces offset in detuning
2. Tunnel coupling (slope of curve) can be perturbed
3. Result is statistical variation that will require tuning.
4. Possible challenges to turning off tunneling
5. Valley physics also perturbed

Rahman, Nielsen

Other considerations: Decoherence near Oxide

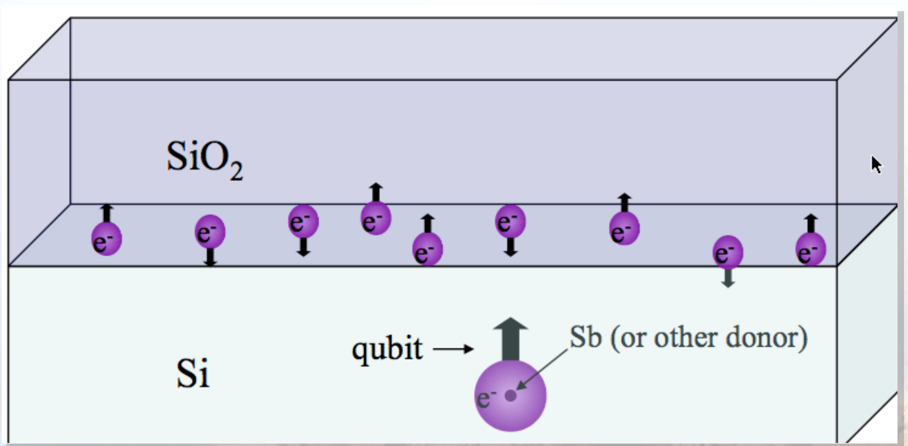
Schenkel et al. APL (2004)

Sample	Interface	Peak depth (nm)	T_1 (ms)	T_2 (ms)
120 keV	Si/SiO_2	50	15±2	0.30±0.03
120 keV	Si—H	50	16±2	0.75±0.04
400 keV	Si/SiO_2	150	16±1	1.5±0.1
400 keV	Si—H	150	14±1	2.1±0.1

SiO_2 from SNL **(2010)**

d (nm)	**T_2 ($SNL\ SiO_2$)**
25	**490 μs**
100	**520 μs**

99.95% ^{28}Si



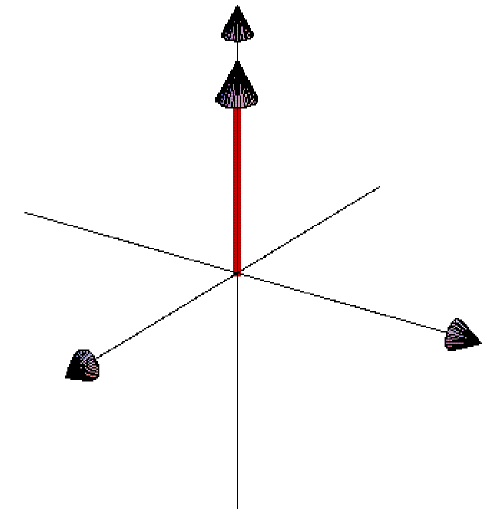
- T_2 not as long as bulk
- Solution: sufficient B-field and low enough temperature?

Doubt: decoherence just not well understood

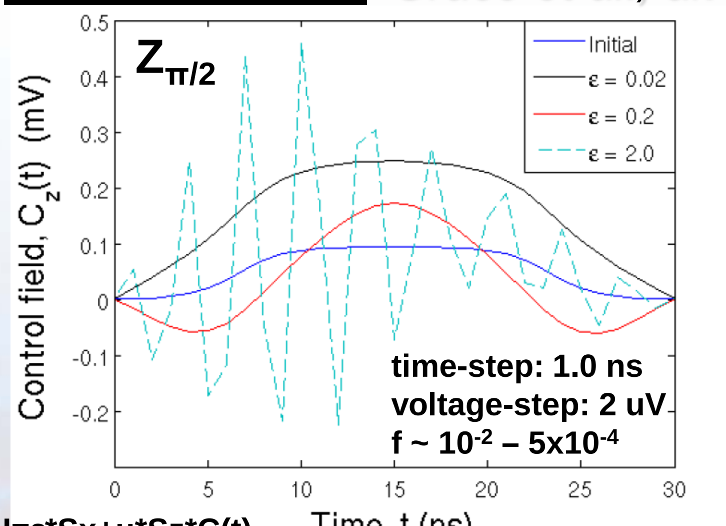
- understand problem
- eliminate decoherence

More robust gates

- Voltage fluctuations (1/f ~ 5 ueV)
  - fidelity of Z gate ~ […]
- J-flat proposal to suppress sensitivity to fluctuations
- Slow varying X-rotation <u>during all gates</u> due to background spins
- Hahn-echo and other DD suppresses this kind of error for idle
- Optimal control or DCG suppress X-rotation in the gate itself

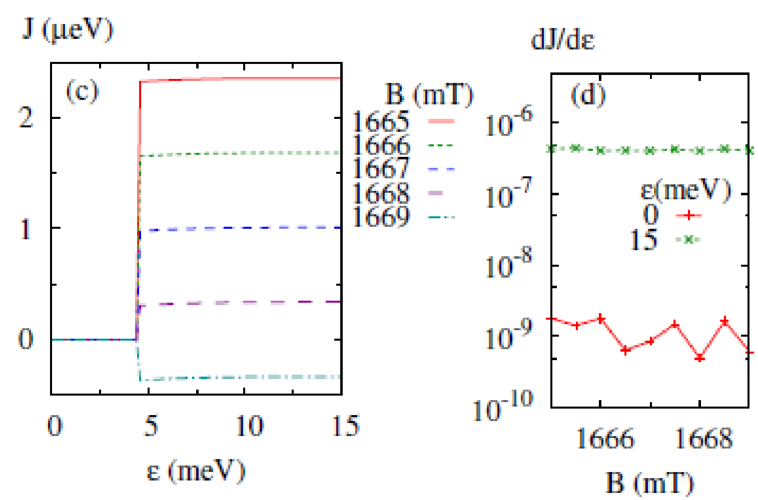


<u>Optimal Control</u> *Grace et al., arXiv*



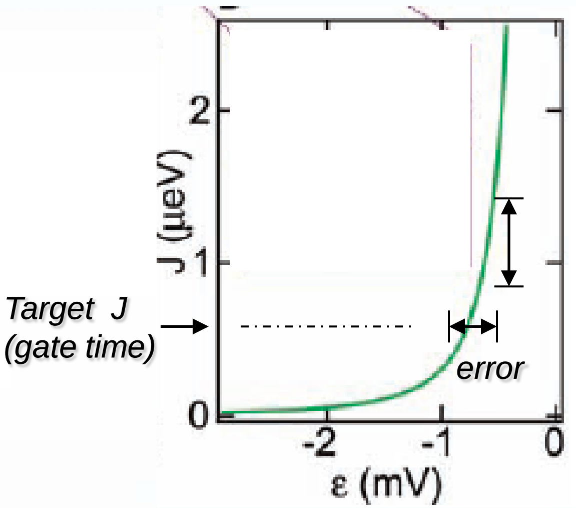
H=ε*Sx+μ*Sz*C(t)

<u>J-flat</u> *Nielsen et al., PRB 2010*

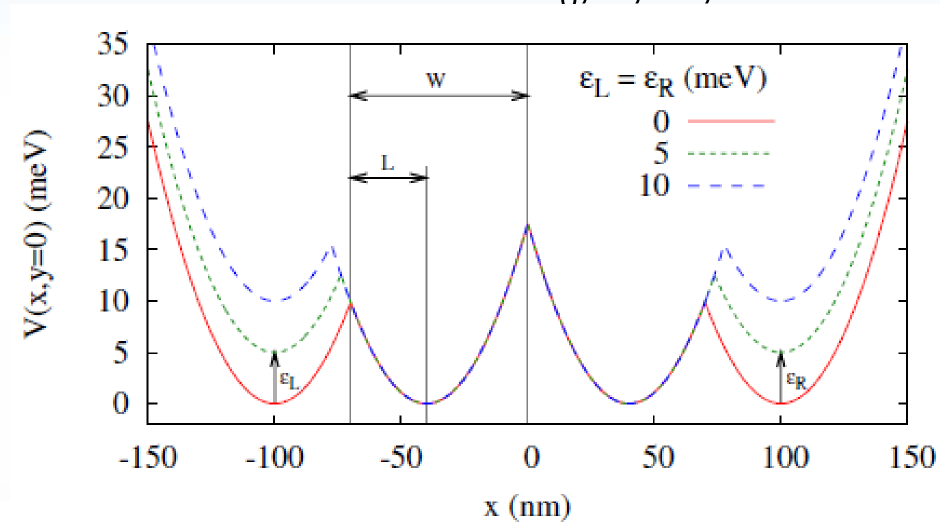


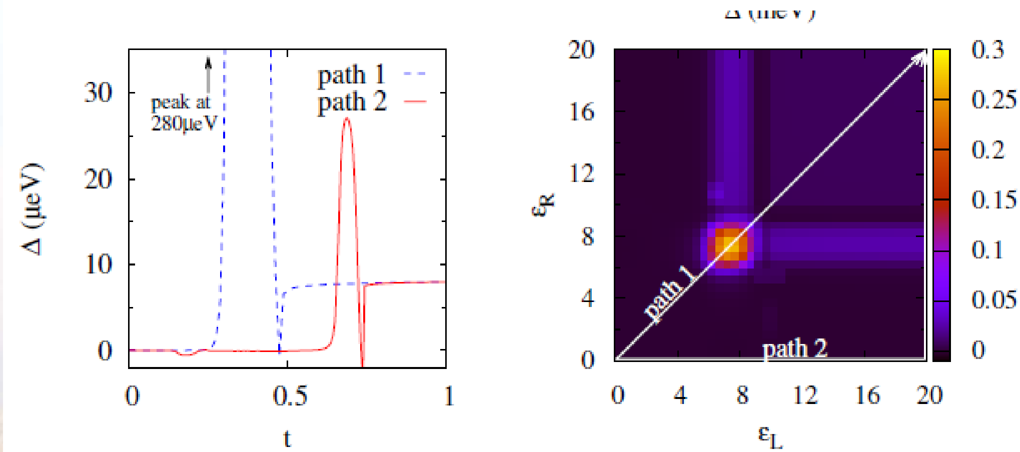
Tuned DQD Potentials for Robust CPHASE-Gate

Petta, Science 2005



Parameters: E_0, L, W, B





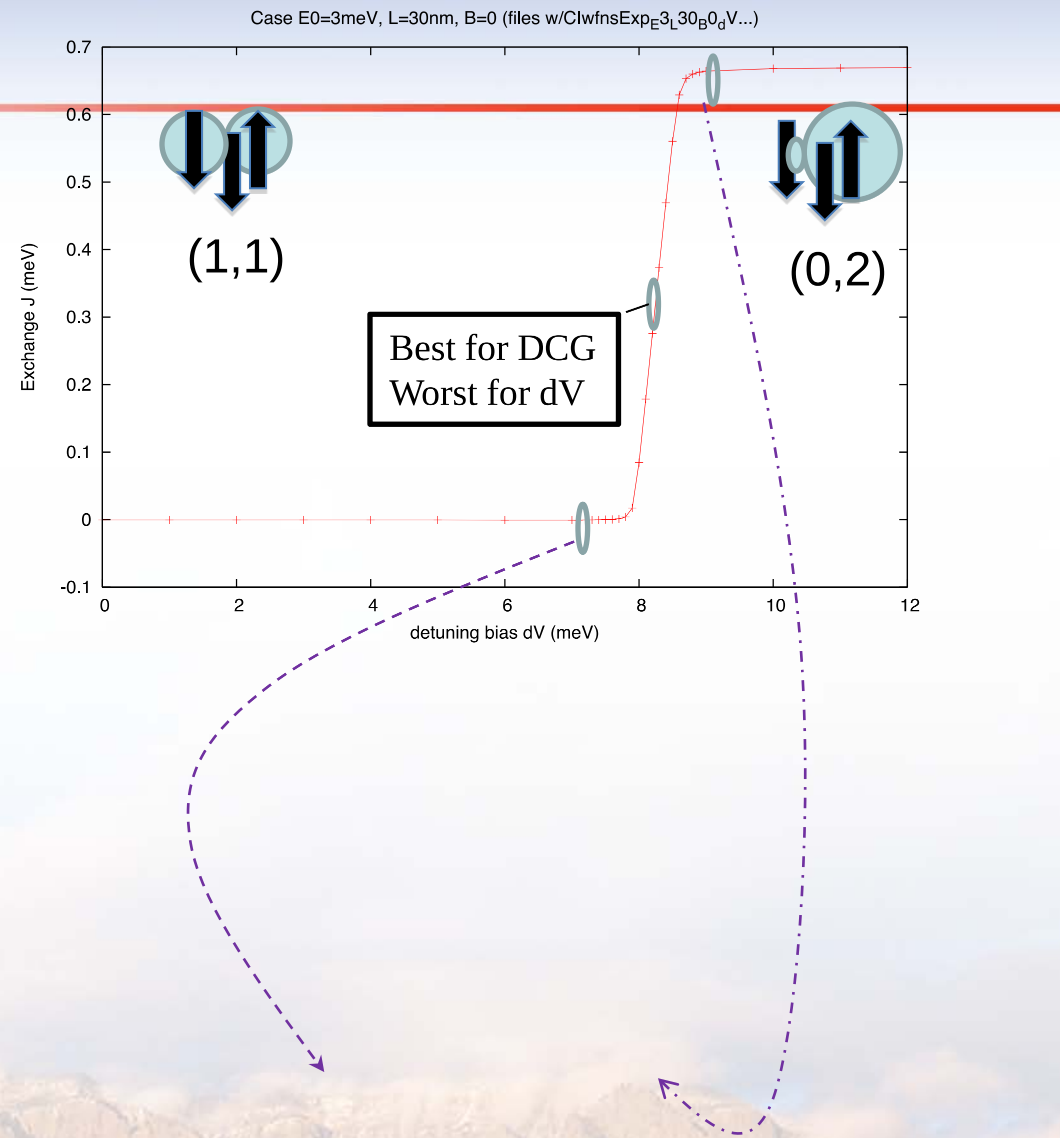
- Robust gate design desirable for CPHASE
- Effective mass calculations and CI used
- Robust regions to applied voltage do exist
- ueV coupling energies are predicted when dots are ~ 60 - 90 nm separated
- <u>High tunability of QD potential necessary!</u>

Nielsen et al., PRB 82, 075319 (2010)
Nielsen et al., arXiv 1106.1441

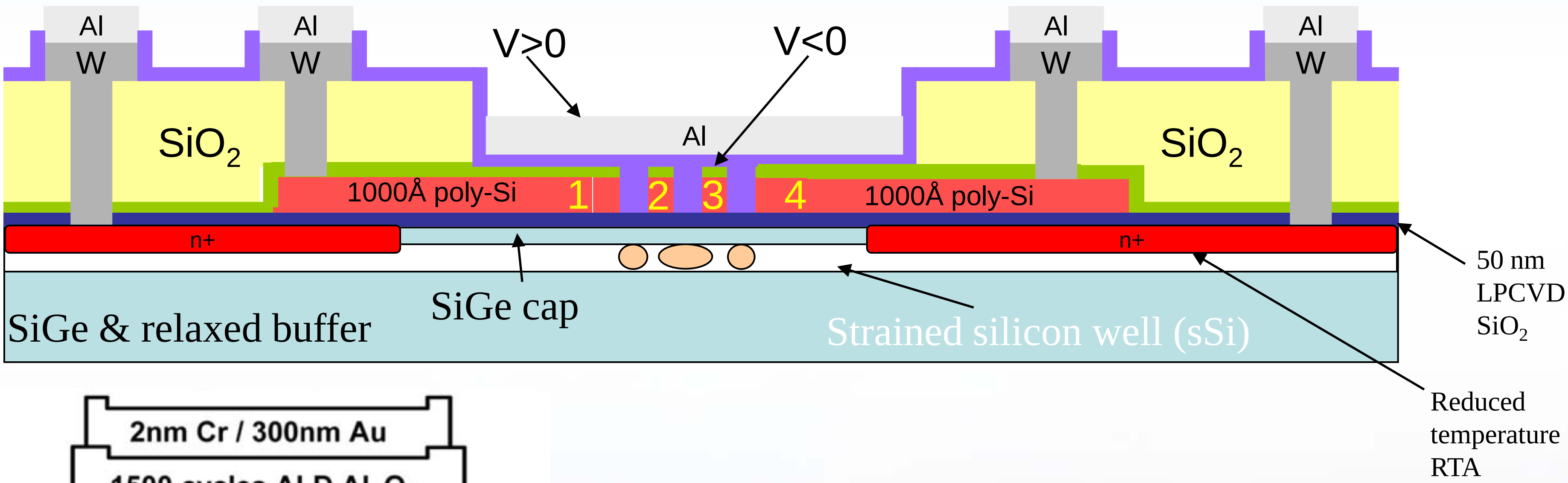
Value of more levels of DD: milestone scope expansion

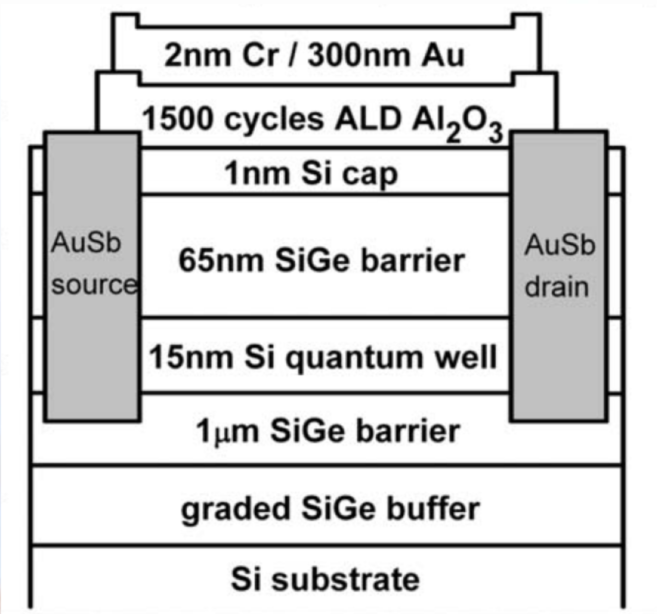
Observation:

1. X rotation during Z gate due to inhomogeneous field
2. DCG sequence to suppress unknown X rotation could be I-Z-I
3. Correlated noise might not be the same for entire sequence I – Z – I



Enhancement Mode SiGe/sSi: High Mobility & Modular Change to MOS Flow





Undoped SiGe Heterostructure

Lu et. al., APL **94**, 182102 (2009)

Mobility ~1.6×10^6 cm^2/Vs

Get the spin away from the surface and defects related to dielectric/crystal interface

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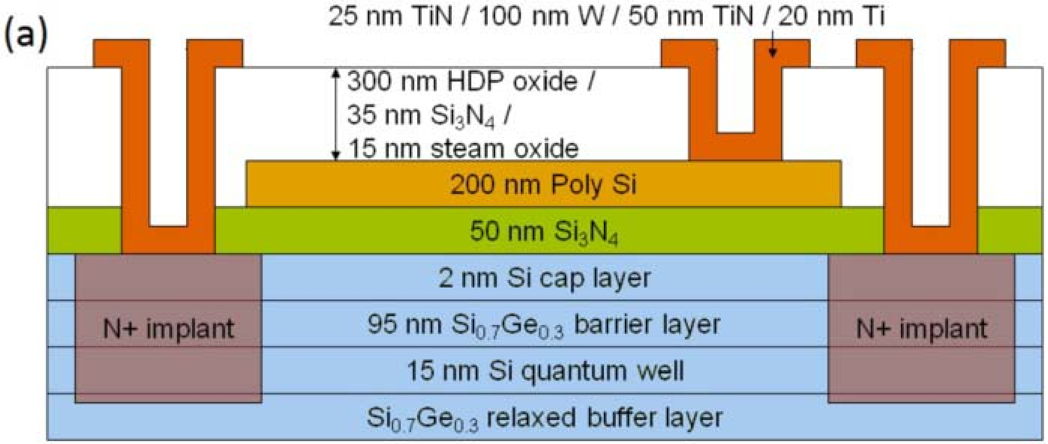
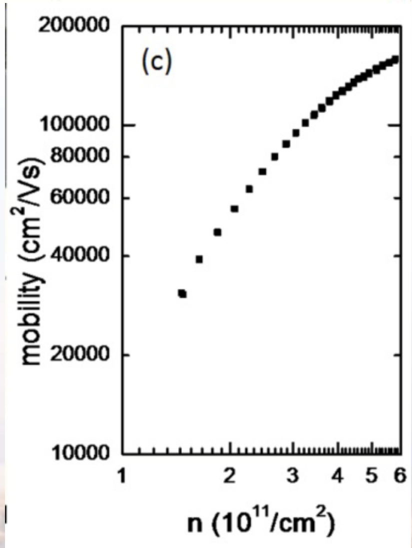
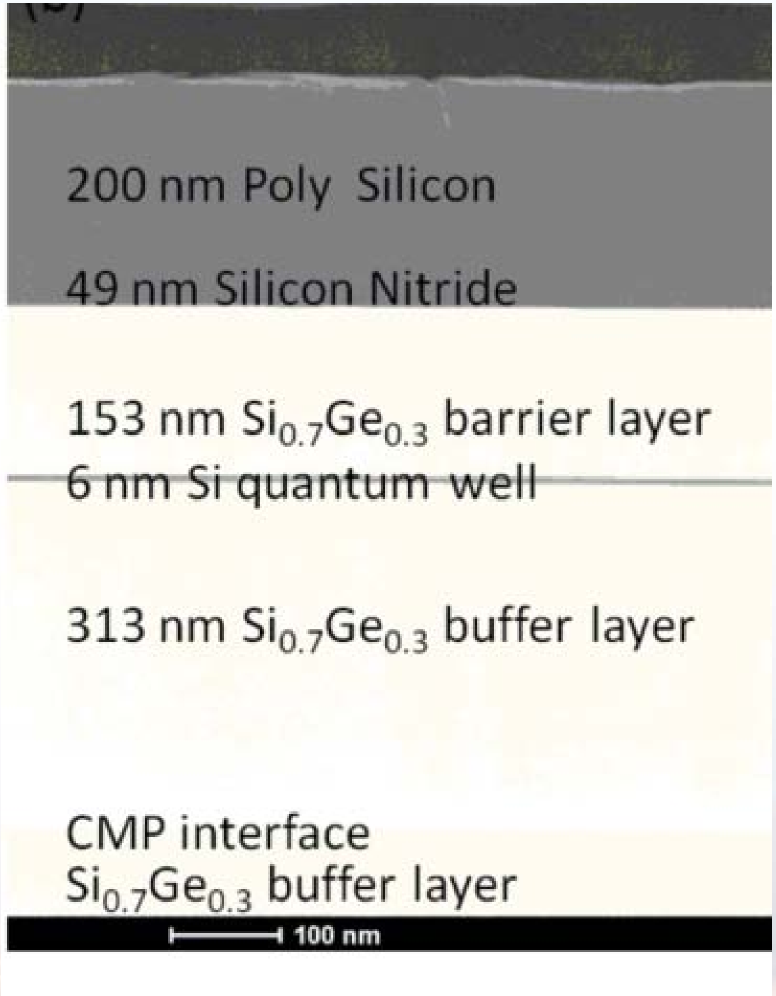
Back to the fab: SiGe/sSi



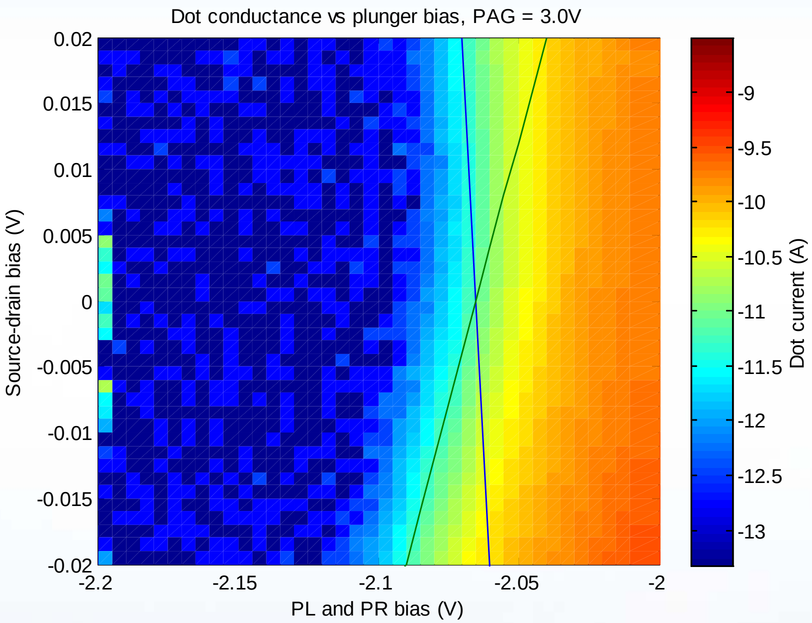


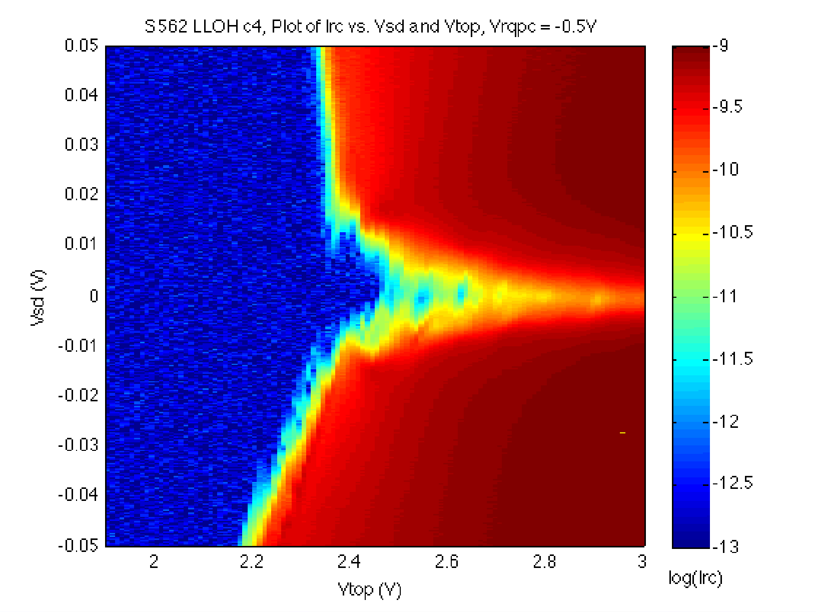


- Modifications:
  1. Substrate
  2. Gate dielectric
  3. Implant & anneals
- Questions:
  1. Ge/Si diffusion
  2. Surface pinning
  3. Mobilty

Pluym, Bishop, Lu, Carroll

Smooth SiGe barriers at 4K

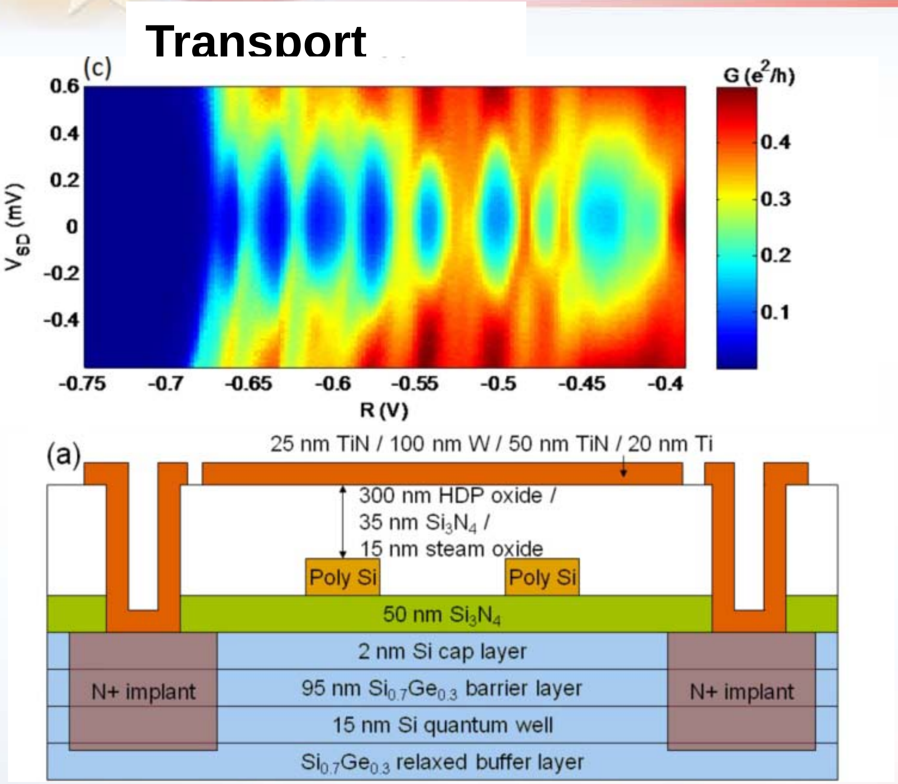


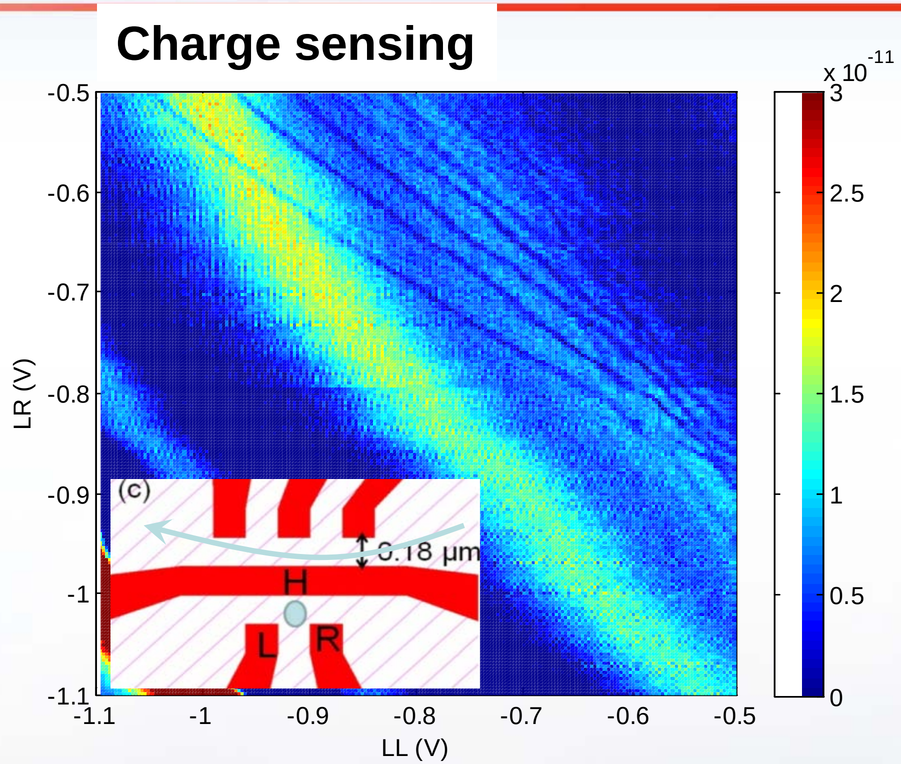


Vdc (mV)	Δ (meV)	w (nm)
+20	35 +/- 8	15 +/- 2
+10	34 +/- 8	16 +/- 2
0	35 +/- 8	15 +/- 2
-10	37 +/- 8	13 +/- 1
-20	35 +/- 8	12 +/- 1

Biggest source of uncertainty is choice of fitting parameter V0 (point of linear expansion)

Charge sensing: last transition

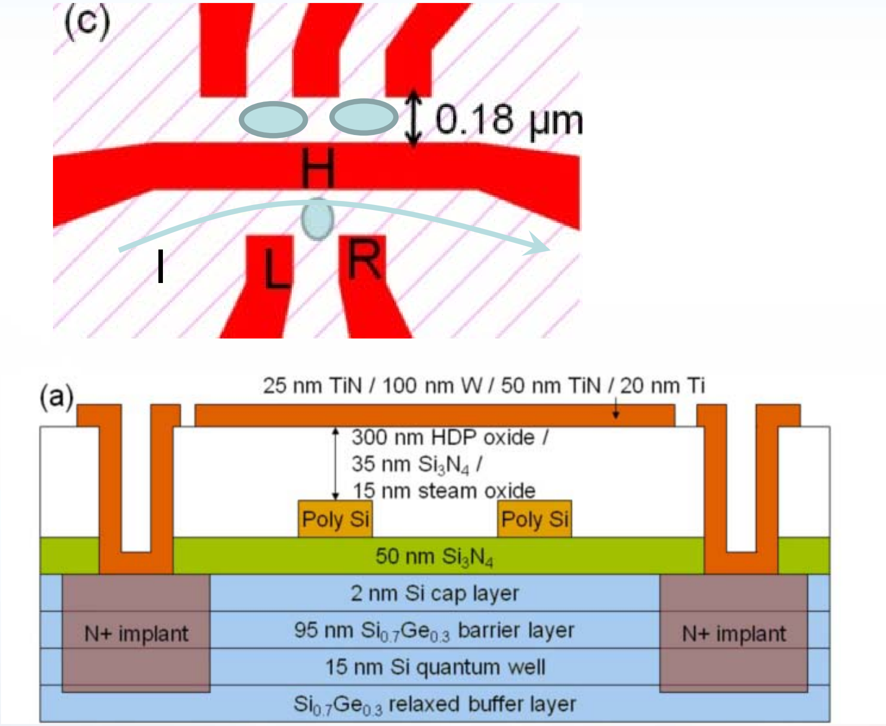


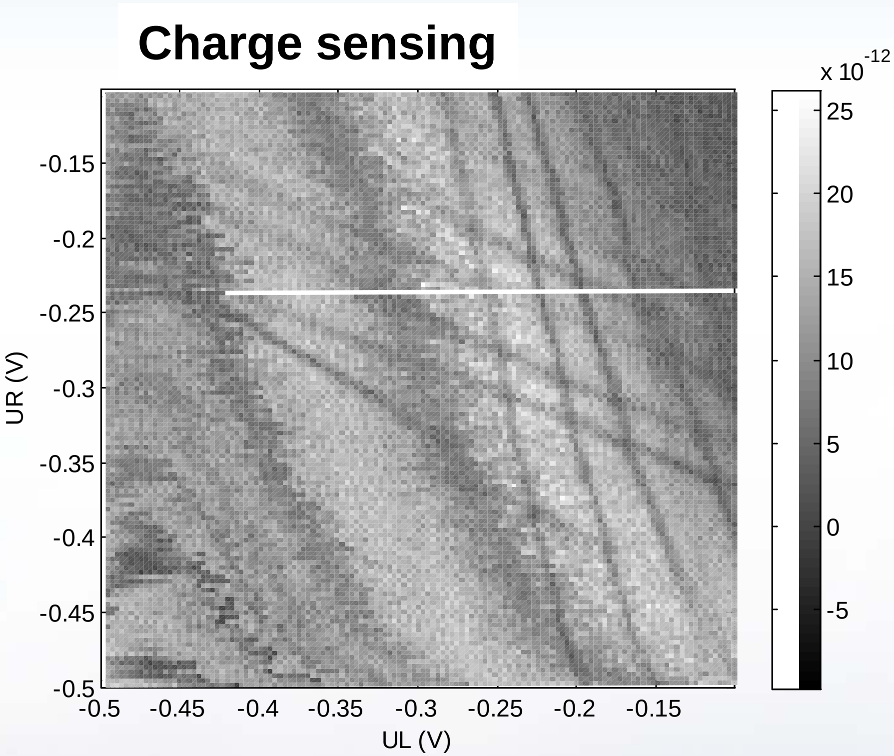


- Opposite channel used as charge sensor
- Last transition in region of high sensitivity of sensor
  - looks like the last electron
- DQD tuning also possible (charge sensed)
- <u>Problem:</u> charge stability

Lu et al., APL 2011

Charge sensing: last transition





- Double top gated quantum dot w/ DUV lithography
- Relatively regular CB observed w/ small charging energy

Lu et al., APL 2011

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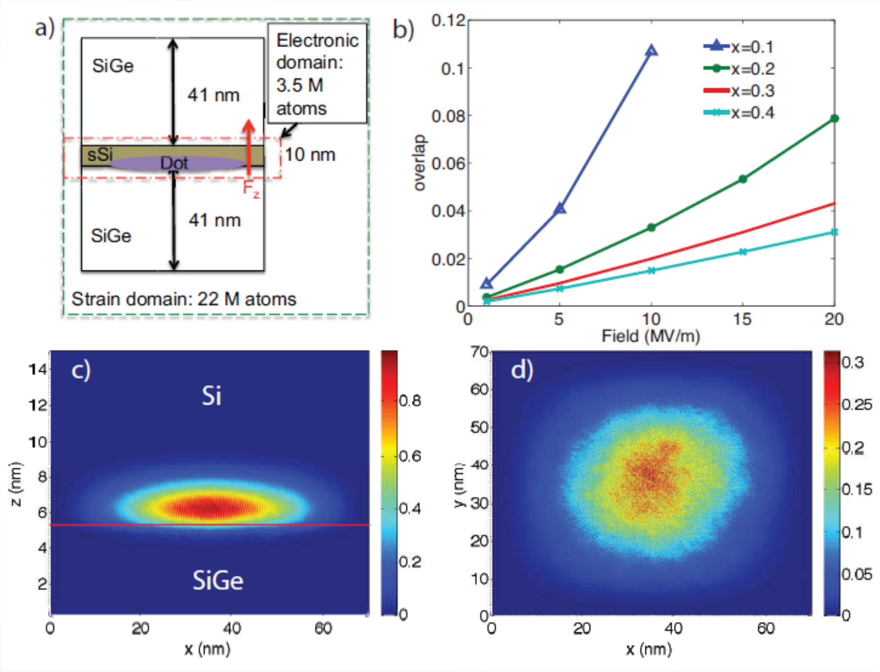
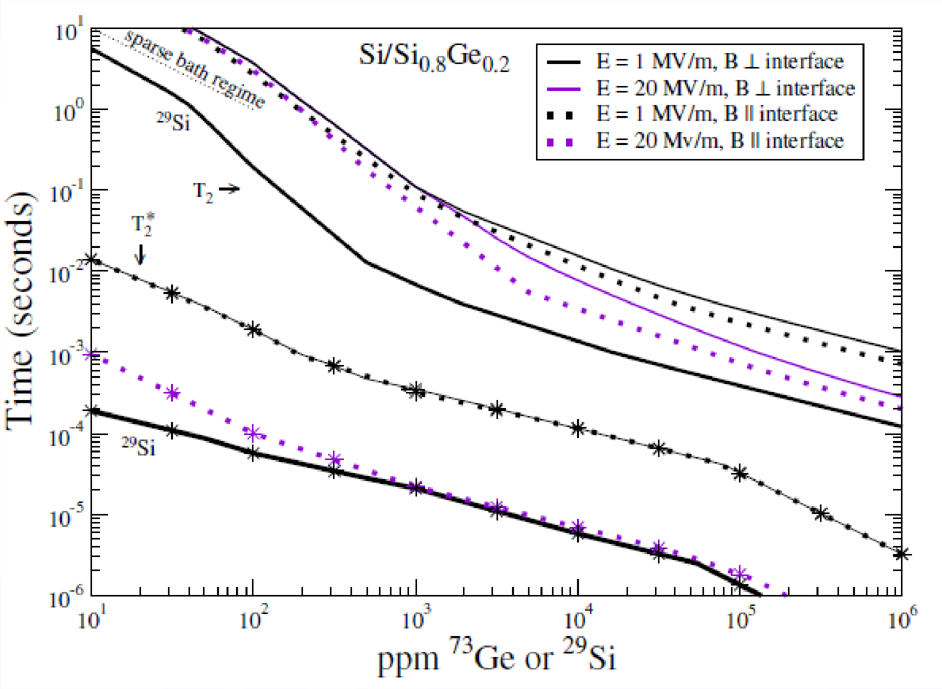
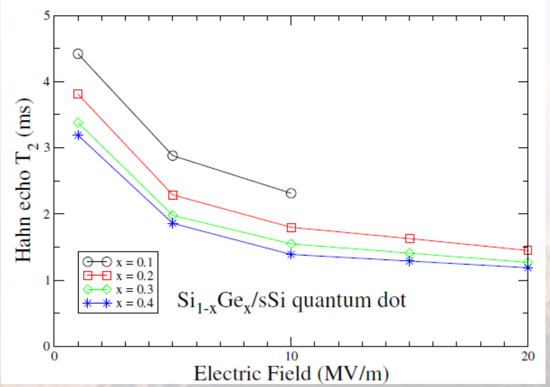
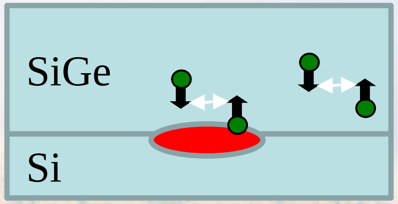
Silicon T2 vs. SiGe/sSi (unenriched)





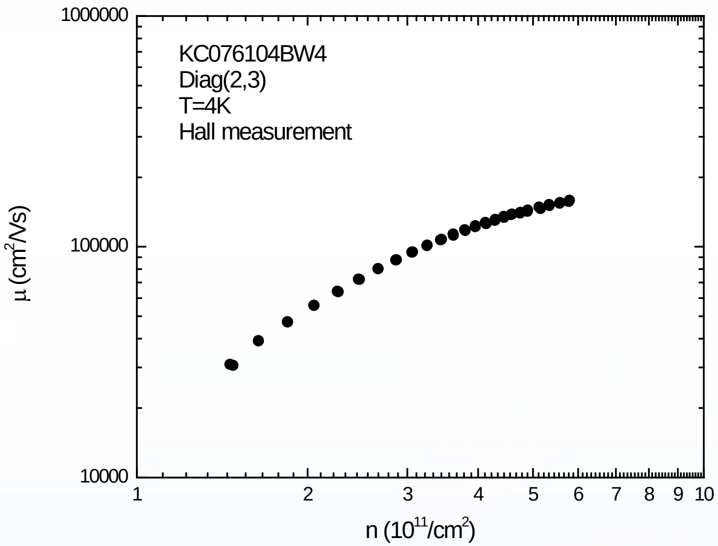




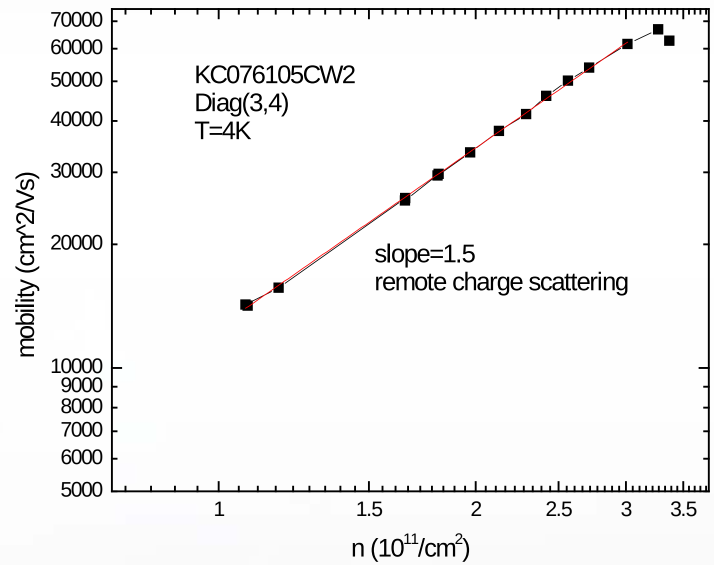
Witzel et al. (submitted to PRB rapid)

Reduced SiGe barrier thickness for increased stability

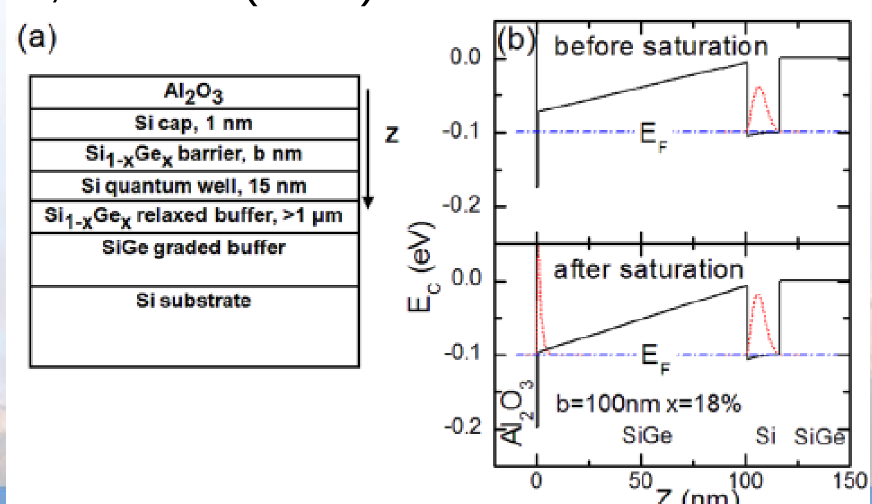
150 nm SiGe barrier (not stable)

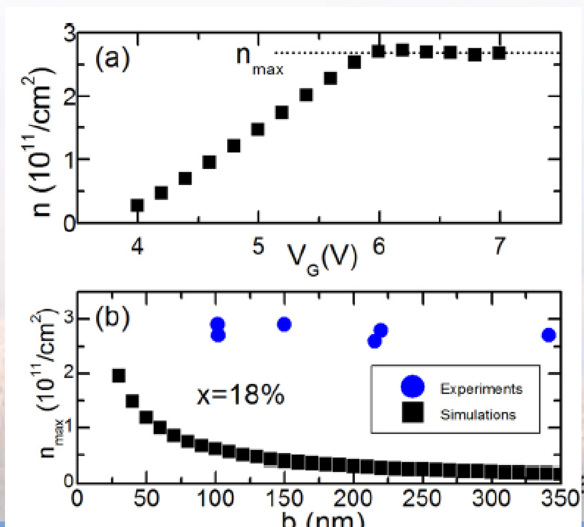


35 nm SiGe barrier (stable)

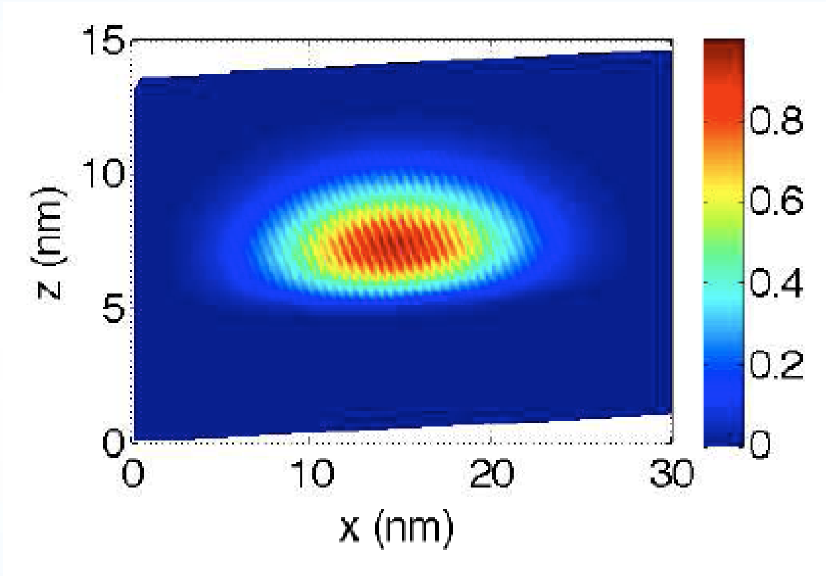


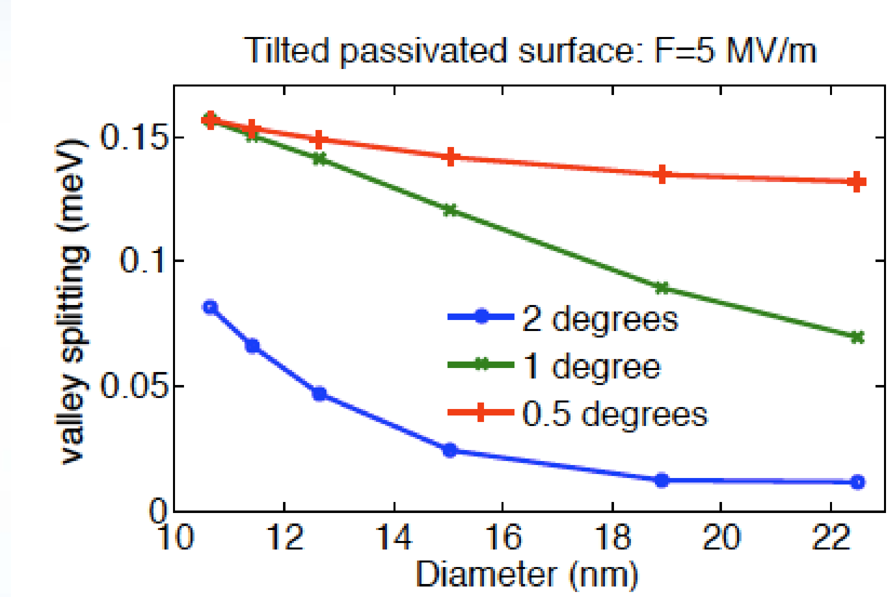
T. Lu, APL 99 (2011)



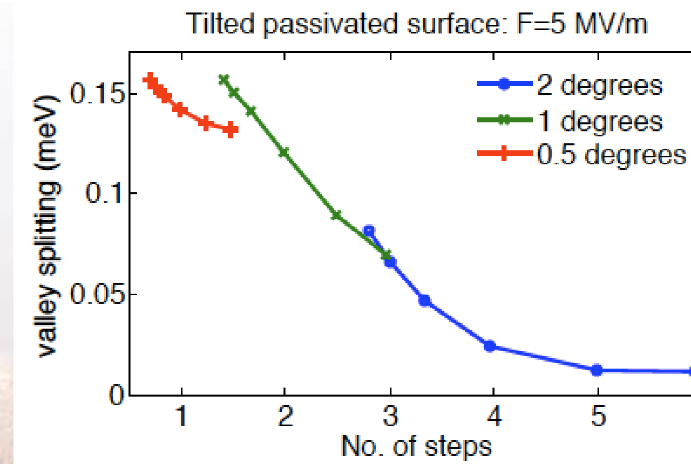


Few electron energies in SiGe

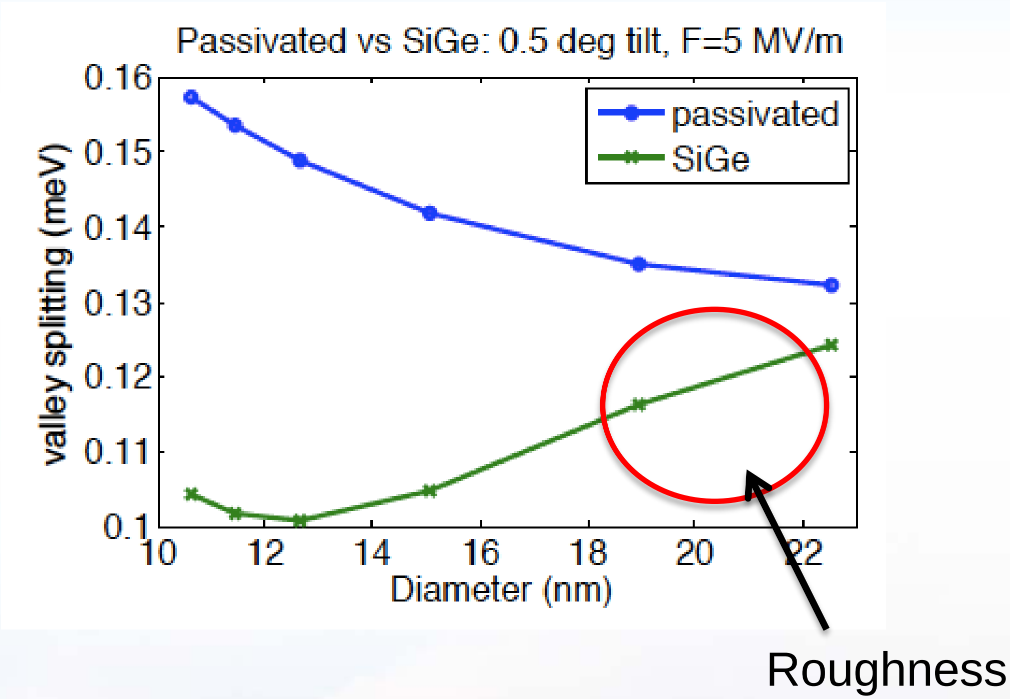




- Modeling of valley splitting at SNL
- Atomistic tight binding calculations (R. Rahman)
- Step edge dependence observed [Friesen et al]
- Calculations done for QD
  - Number of step edges appears to be determining factor



Valley physics still to better understand



- Evidence suggests that VS can be big enough
- Ge and Ge profile dependence not well understood
- Big phase space with E-field & processing

Summary

- Measurements and theory suggest very long T2 possible with enrichment and high purity [Witzel et al. PRL 2010]
- Tunable DQDs measured with transport [Tracy et al., APL 2010]
- Transport suggests new MOS design can achieve N=1
  - capacitances are consistent with CAD simulated N=1 capacitances
- Charge sensed MOS DQDs demonstrated
  - Balancing charge sensing, sensitivity and N=2 (DQD) is challenging
- CAD simulation tool being developed and calibrated to assist in design (smaller) and analysis
  - Good tunneling model for CAD needed for design
- Square barrier, WKB tunneling model produces self-consistent results with xpt. fits
- CI/TB calculations indicate positive charge defects can localize the DQD electrons, but tuning can work-around many defects
- J and CPHASE flats are predicted theoretically and are potentially more robust operation points [Nielsen et al., PRB and arXiv]
- T2 at surface near oxides is still not well established
- DCG might be inconsistent with J flat
- SiGe enhancement mode quantum dots have been developed (just get away from defects)
  - Measurements are consistent with charge sensed few electron QD and DQDs [Lu et al., APL 2011]
  - Barriers look cleaner
  - Sudden shut-off in 150K mobility material, thinner SiGe barrier, 70K mobility, has fewer abrupt shut-offs
  - Ge isotopes are predicted to limit T2 [Witzel et al., submitted PRB rapid]

Acknowledgements

- The technical teams

  Silicon quantum dot: M. Lilly, N. Bishop, S. Carr, T.-Z. Lu, L. Tracy, K. Nguyen, T. Pluym, J. Dominguez, J. Wendt, J. Stevens, B. Silva, E. Bower, R. Gillen

  Donor and donor-dot: E. Bielejec, E. Bussmann, D. Perry, B. McWatters, A. MacDonald

  Device modeling: R. Muller, R. Young, W. Witzel, E. Nielsen, R. Rahman, K. Young, J. Verley

  Cryogenic electronics: T. Gurrieri, J. Levy, R. Young, J. Hamlet, K. Barkley

  Architecture and quantum error correction: A. Ganti, M. Grace, W. Witzel, U. Onunkwo, A. Landahl, C. Phillips, R. Carr, T. Tarman

- Joint research efforts with external community:
  - U. Wisconsin (M. Eriksson, D. Savage, M. Friesen, R. Joynt)
  - Australian Centre for Quantum computing Technology (L. Hollenberg, D. Jamieson, M. Simmons, A. Dzurak, A. Morello)
  - Princeton University (S. Lyon)
  - NIST (N. Zimmerman)
  - U. Maryland (S. Das Sarma, M. Peckerar)
  - Lawrence Berkeley National Labs (T. Schenkel)
  - National Research Council (A. Sachrajda)
  - U. Sherbrooke (M. Pioro-Ladriere)

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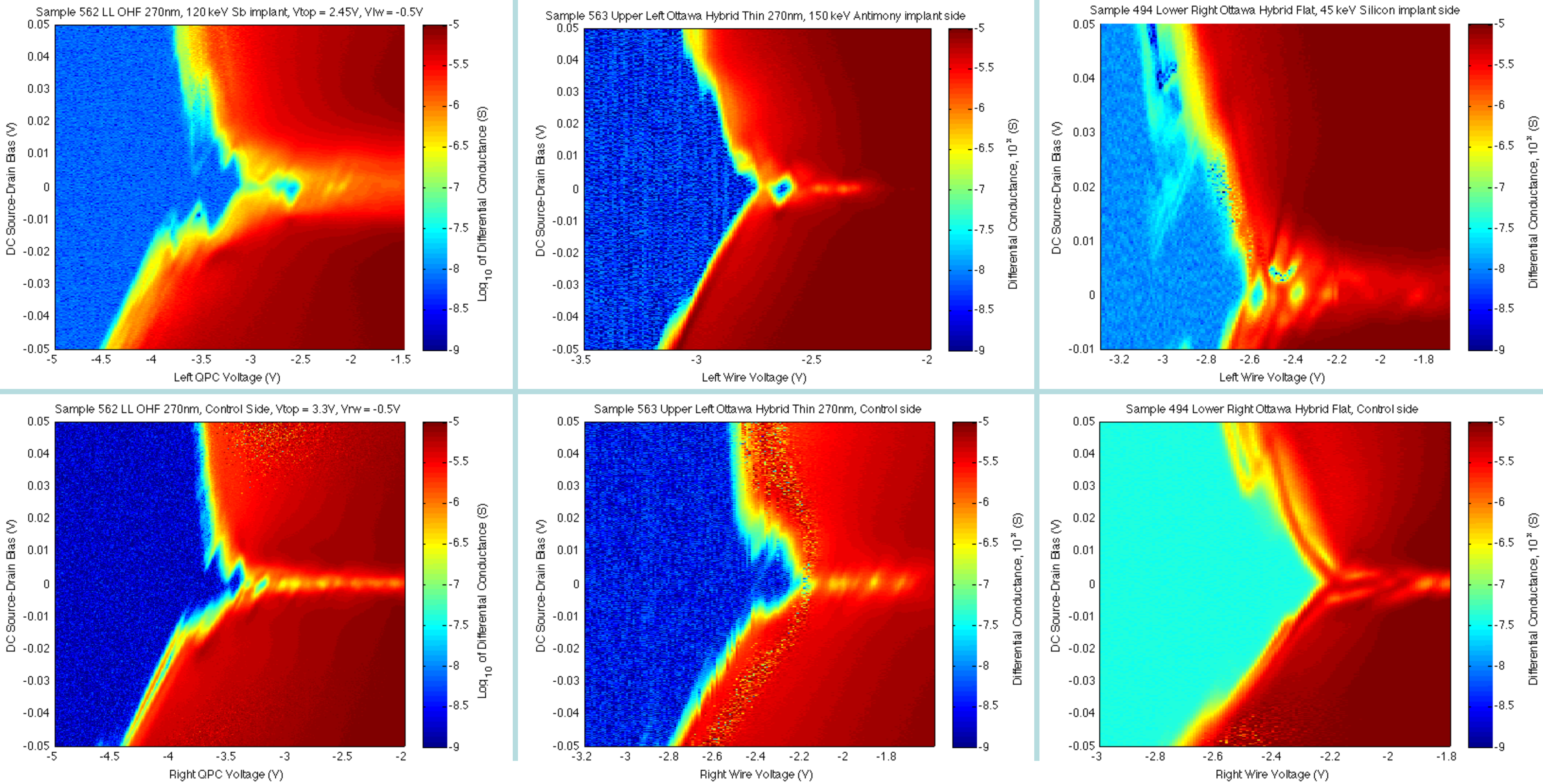
Statistical analysis of implanted tunnel barriers

120 keV Sb implant	150 keV Sb implant	45 keV Si implant

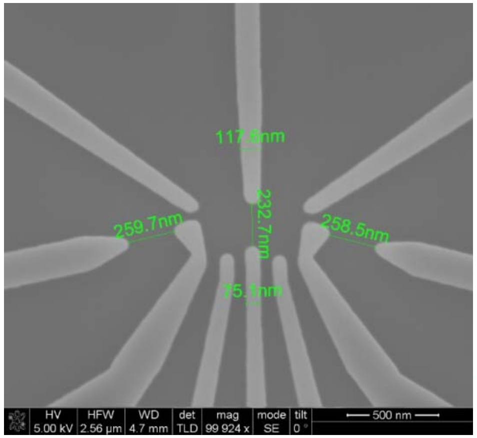
Implant / Control

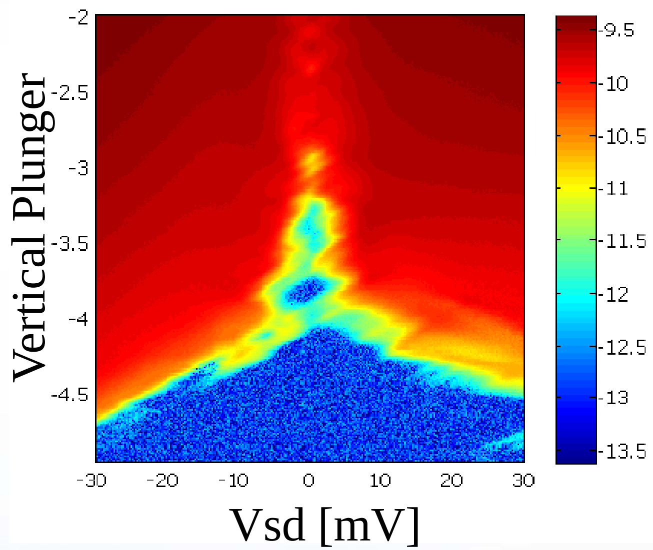


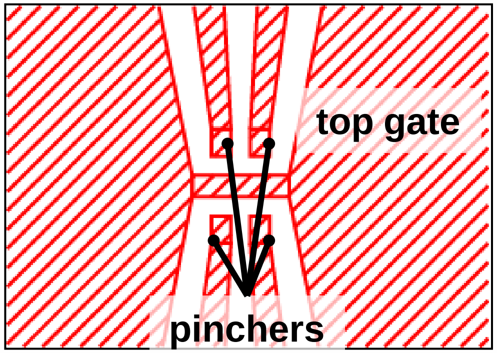
Donor signature difficult to find, but very useful for modeling tunnel barrier.

Shirkhorshidian, Carroll, Bishop

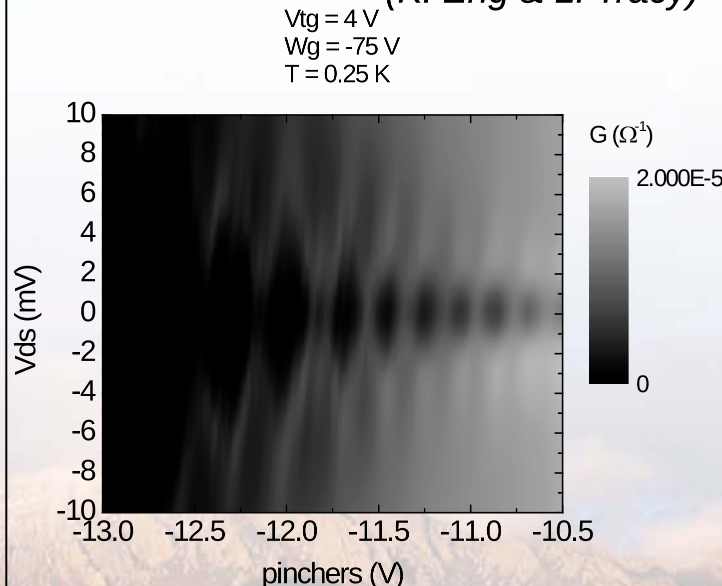
Qualitative differences between disorder in different structures





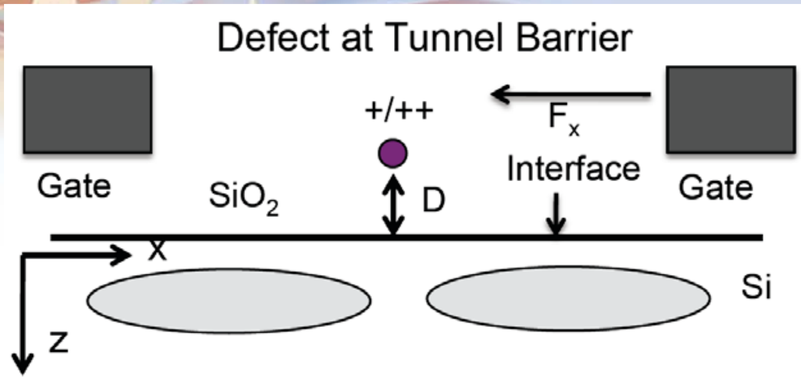


(K. Eng & L. Tracy)

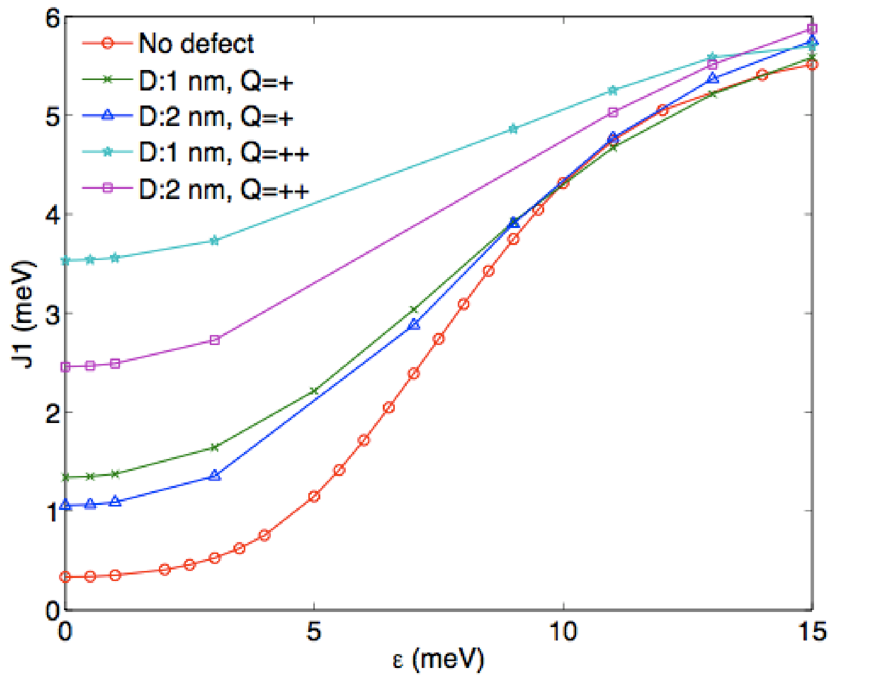


- Common in MOS for charging energy to rapidly increase as N => 1
- Charge sensing also detects outlier(s)
- Large area devices produce small dot charging energies?

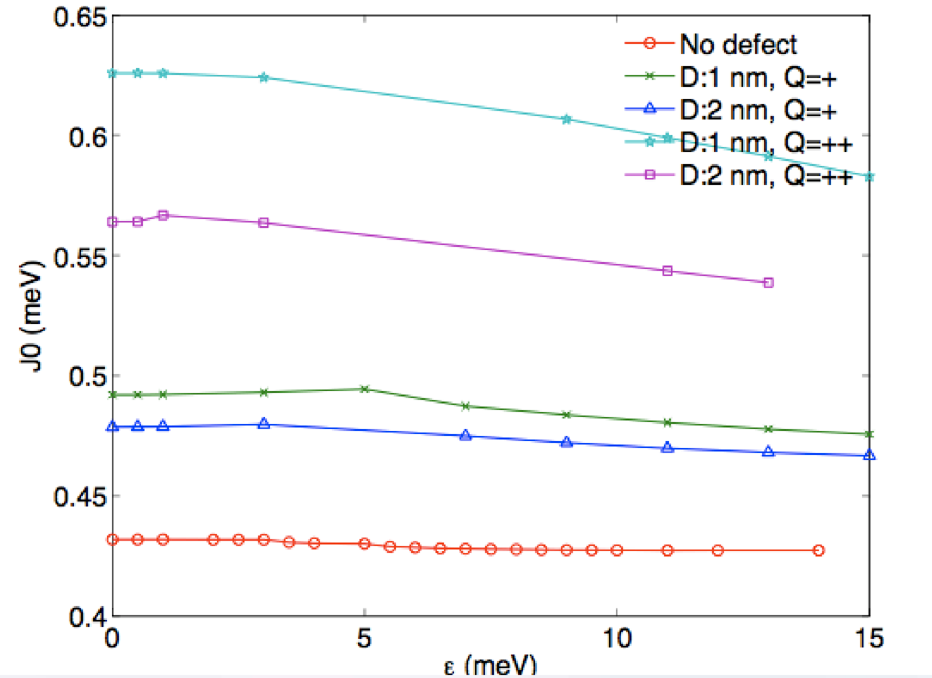
Fig. 3a) Defect at Tunnel barrier



J1



J0



Stronger the effect of the defect potential, the greater is the valley splitting, hence the curves move up

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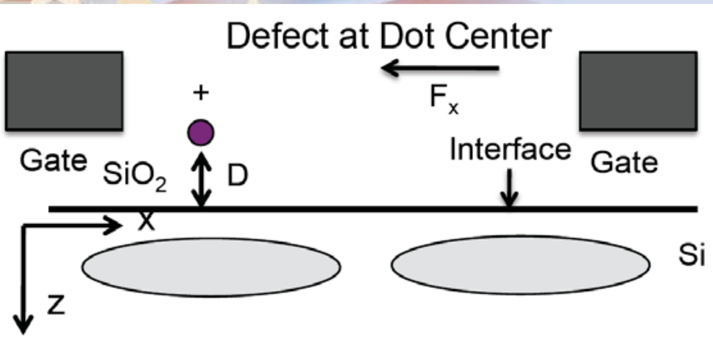
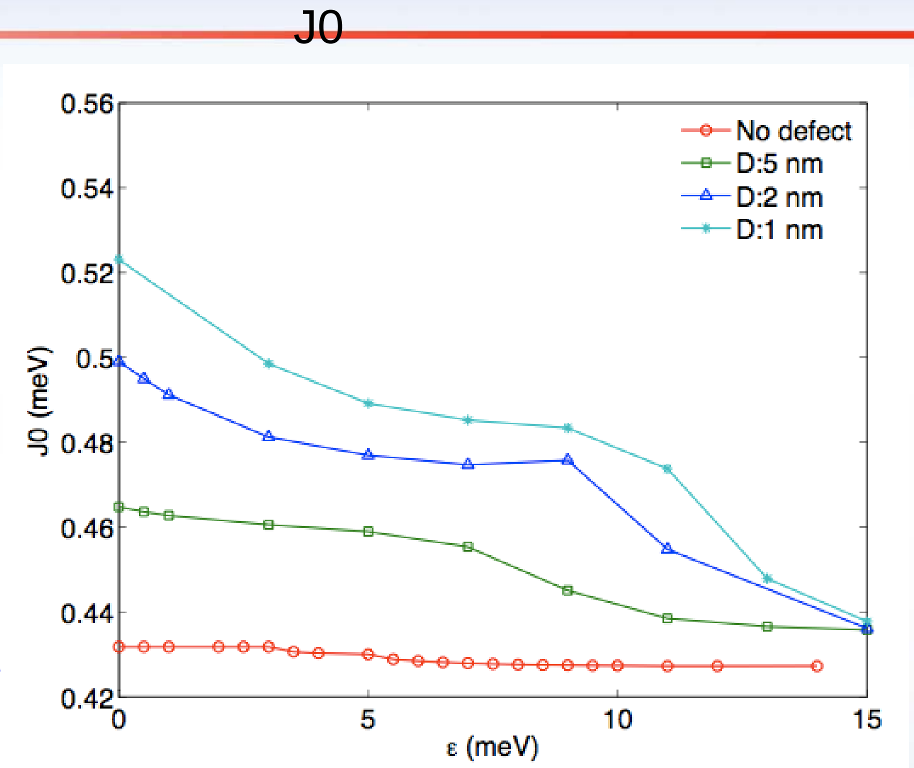
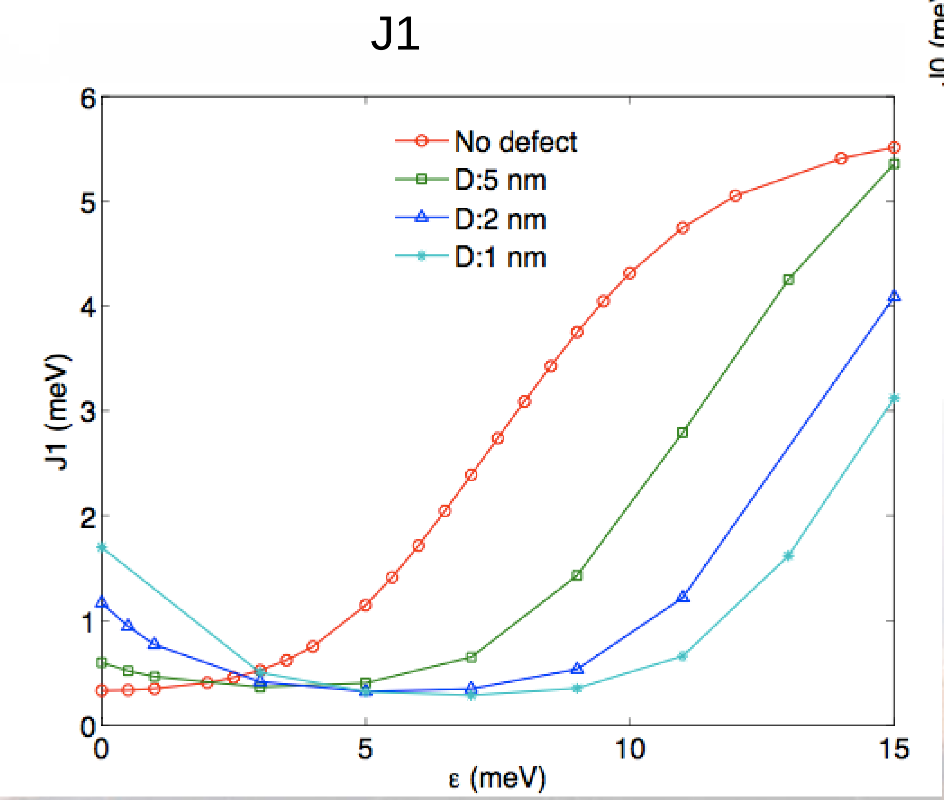
Fig. 3b)Defect at center of one dot

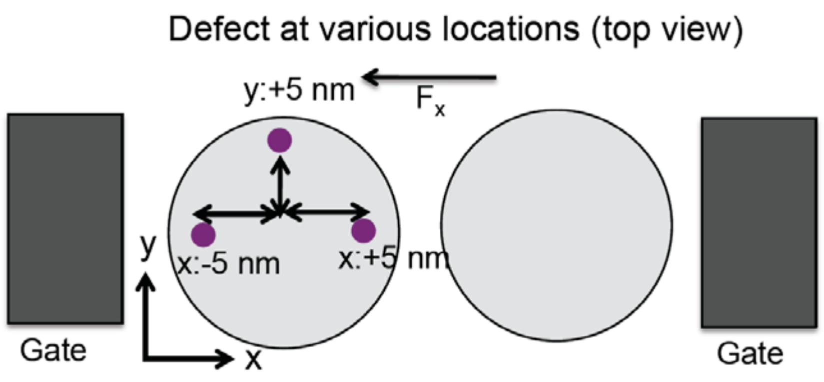


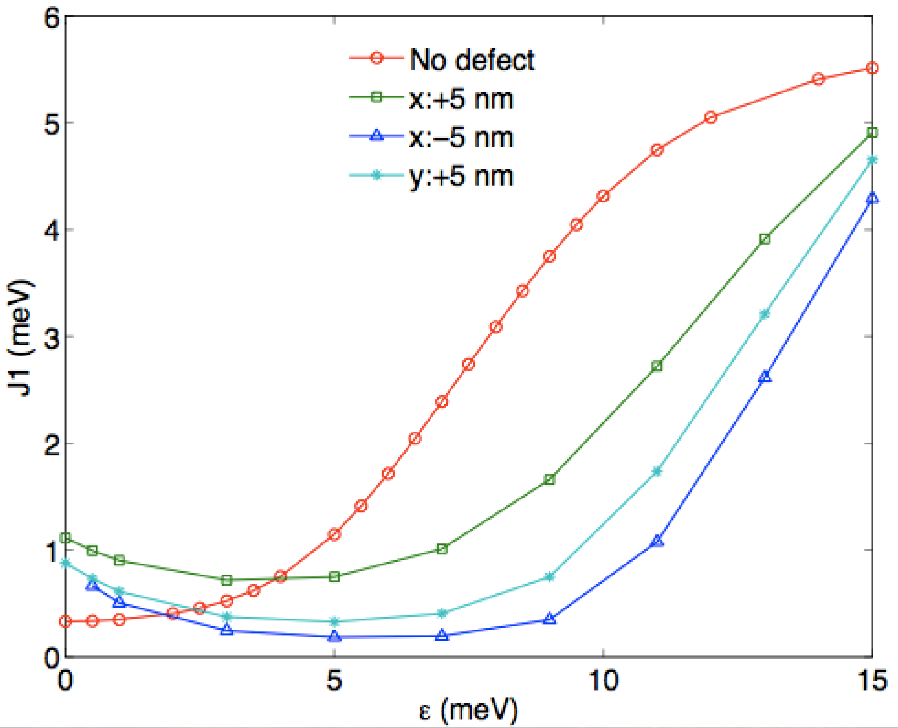


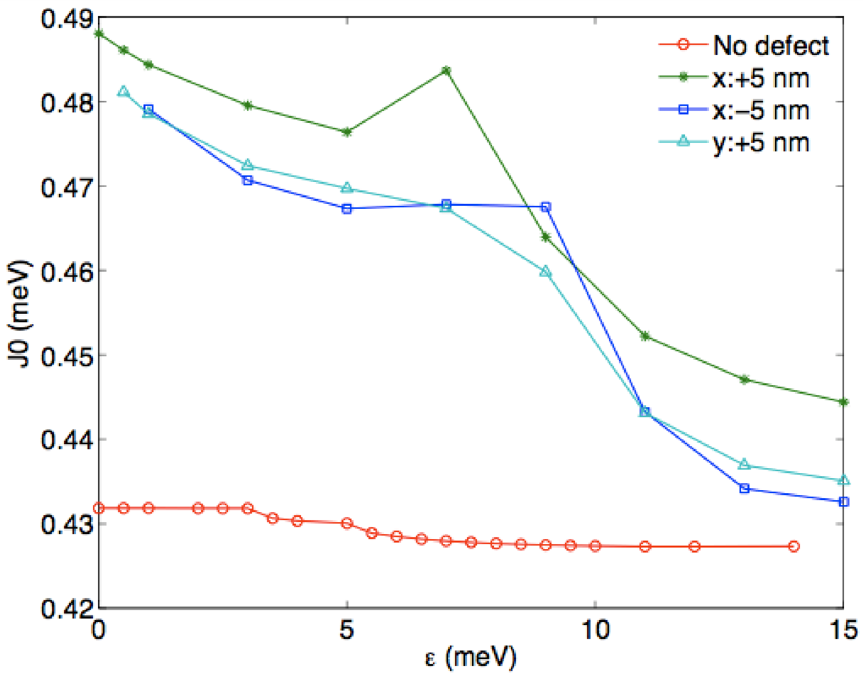


Defect cause VS to be different in two dots, hence the slope of the curve. The “hump” is a bit mysterious and doesn’t seem to be a numerical artifact.

Fig. 3c) Defect at various locations







Same effect: Asymmetric VS

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