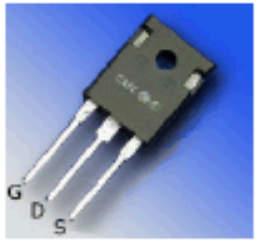
SAND2013-5268C

Performance and Reliability Characterization of 1200 V Silicon Carbide Power MOSFETs at High Temperatures



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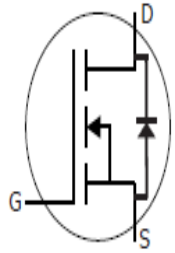

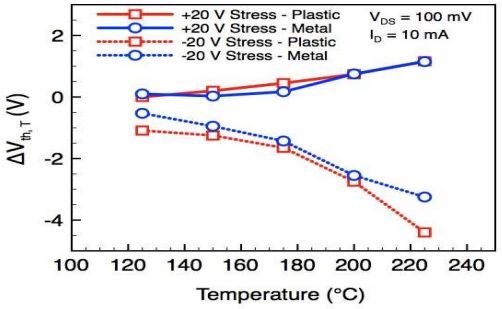

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R. J. Kaplar, D. R. Hughart, S. Atcitty, J. D. Flicker, S. DasGupta, and M. J. Marinella

The authors gratefully acknowledge the support of Dr. Imre Gyuk of the United States Department of Energy, Office of Electricity Delivery and Energy Reliability, Energy Storage Program

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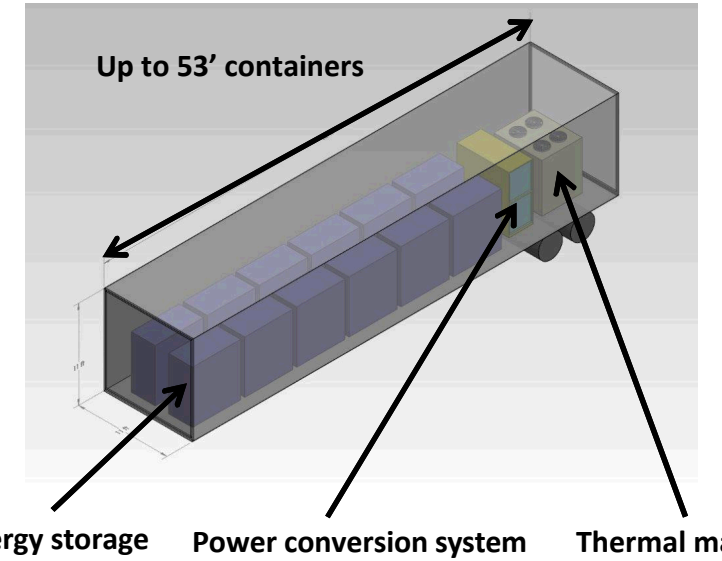
Overview

- ***Wide-bandgap semiconductors have material properties that make them theoretically superior to Silicon for power electronics applications***
  - Lower power loss and reduced cooling requirements would increase the efficiency and reduce the size and complexity of power conversion systems for stationary and mobile applications, *thus reducing overall system cost*
  - However, wide-bandgap materials and devices are far less mature than their Si counterparts; many questions remain regarding their reliability, *limiting their implementation in systems*
- ***Goal: Evaluate the gate oxide reliability of several different 1200 V SiC MOSFETs under various bias-temperature stress conditions***

Example of Motivation for WBG Power Electronics: Portable Energy Storage



Typical Applications

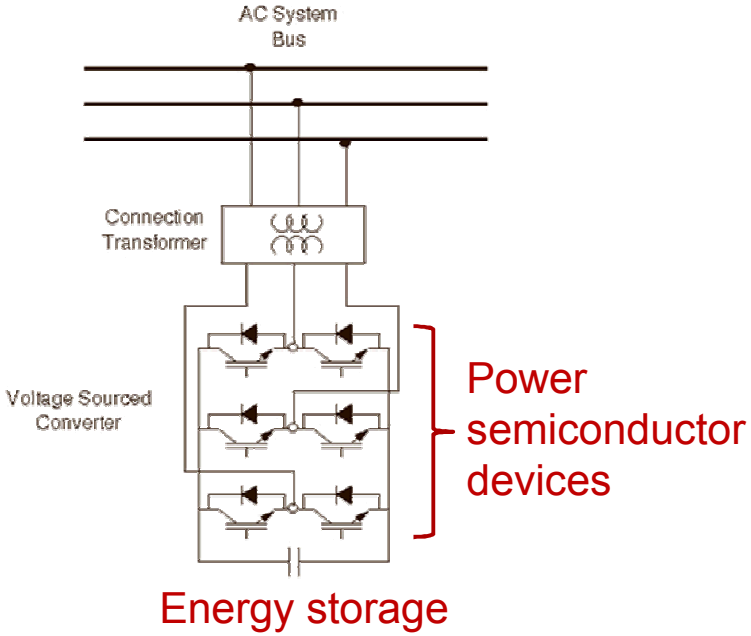
- Grid stabilization
- Frequency regulation
- Renewable integration
- Peak shaving
- Voltage support

Benefits of portable storage

- Low installation cost
- Short time from installation to operation
- System is optimized for use at multiple sites

Typical portable power conversion system

- PWM voltage sourced converter
- Silicon-based power electronics
- Water cooled (*complex, bulky, and expensive*)



SiC Has Superior Material Properties for Power Devices

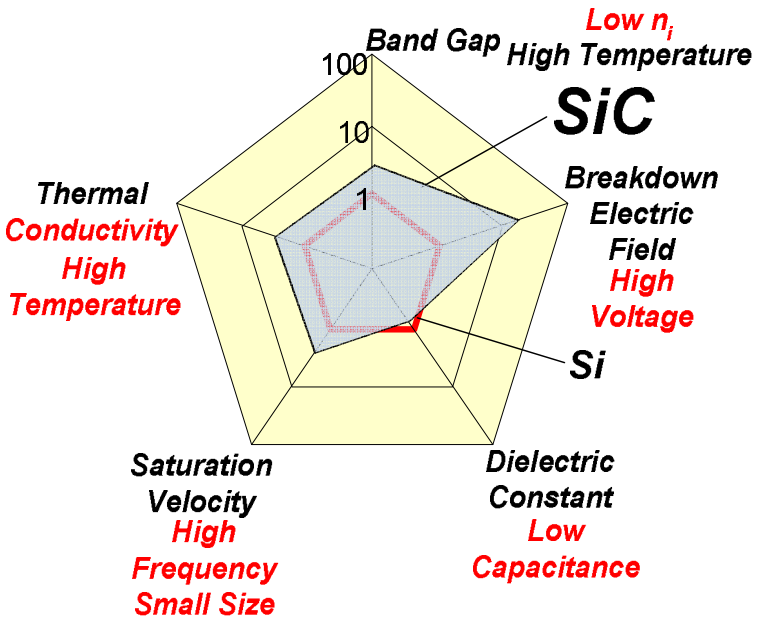
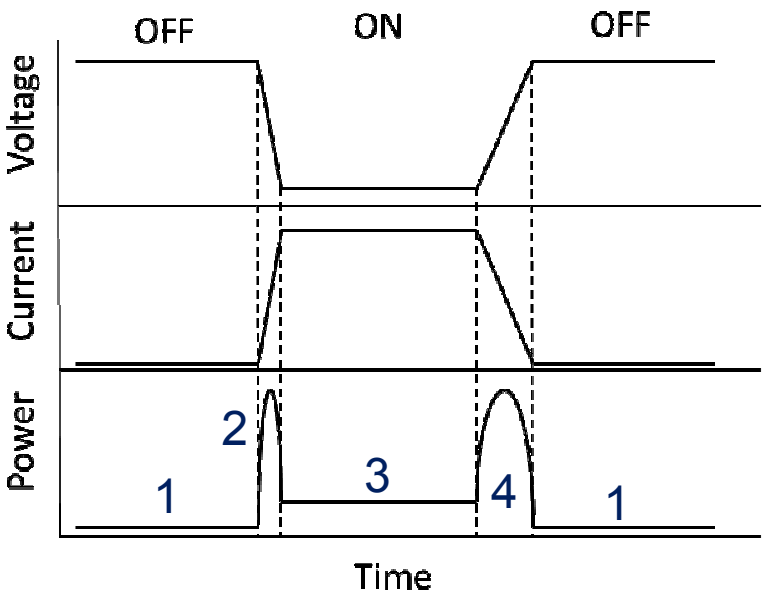


Figure courtesy of Prof. D. K. Schroder, ASU

Property	Si	4H-SiC
E_G (eV)	1.1	3.2
E_C (MV/cm)	0.3	3.0
ε_r	11.8	10.0
v_s (10^7 cm/s)	1.0	2.0
κ (W/cm˚K)	1.5	4.5

Source: T. P. Chow, "High-Voltage SiC Power Rectifiers," in *Wide Energy Bandgap Electronic Devices*, edited by F. Ren and J. C. Zolper (World Scientific, 2003).

Potentially Lower Power Loss for SiC Compared to Si



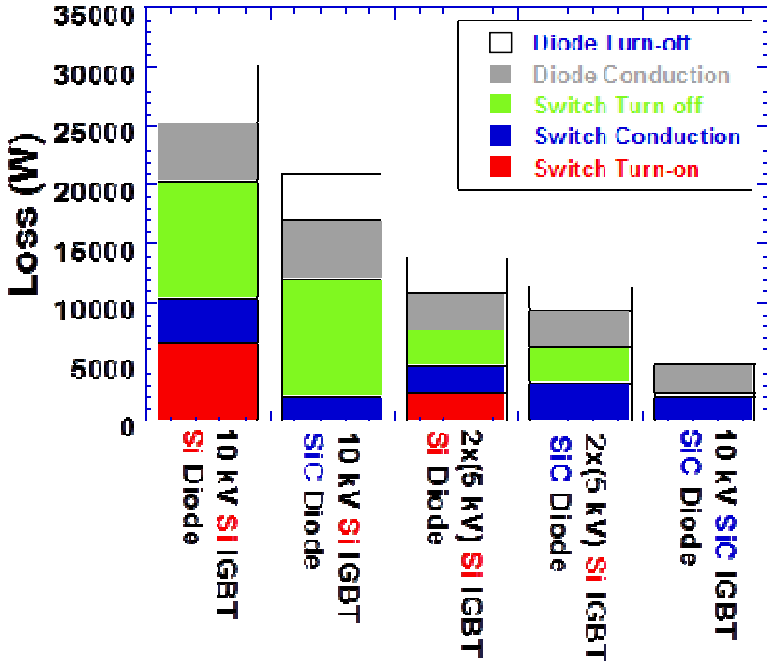


Figure courtesy of Prof. D. K. Schroder, ASU

Power loss mechanisms:

1. Leakage
2. Turn-on
3. Conduction (R_{ON})
4. Turn-off

We have characterized the reliability of several commercially available 1200 V SiC power MOSFETs

Gate Oxide Reliability Has Limited the Adoption of SiC MOSFETs

Critical gate oxide interfacial region

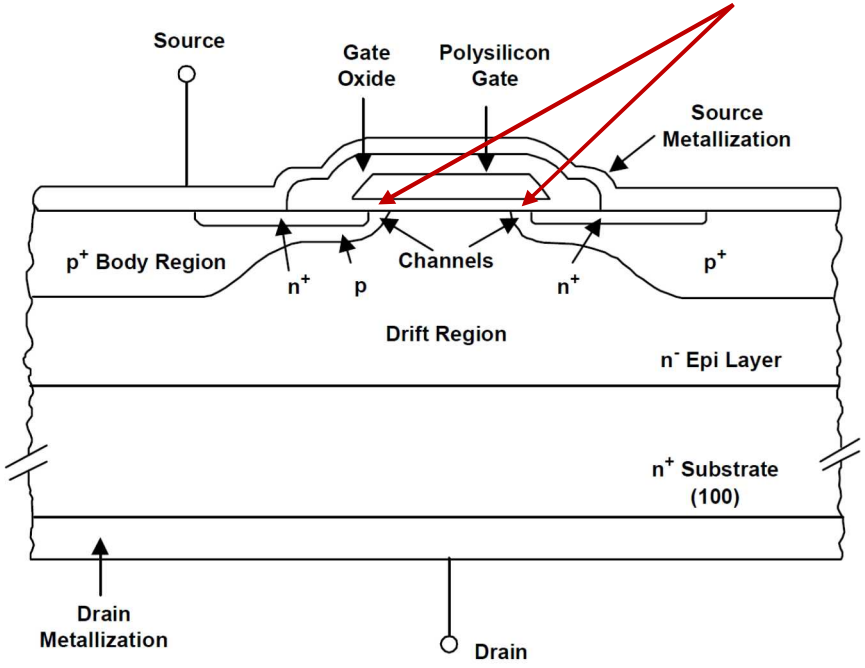


Diagram source: International Rectifier, "Power MOSFET Basics"

Charge injection due to small band offset at SiO_2/SiC interface enhances V_T shift

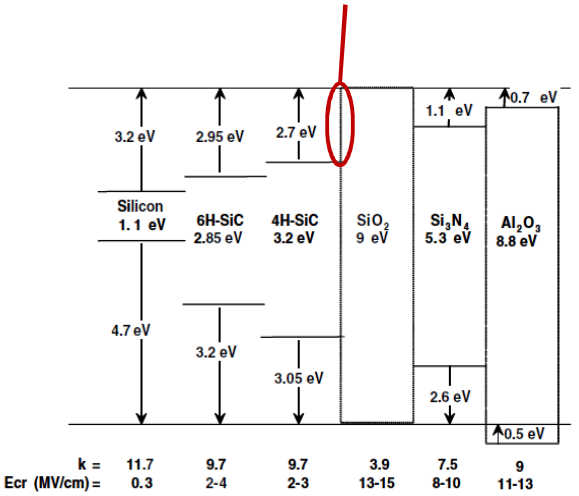


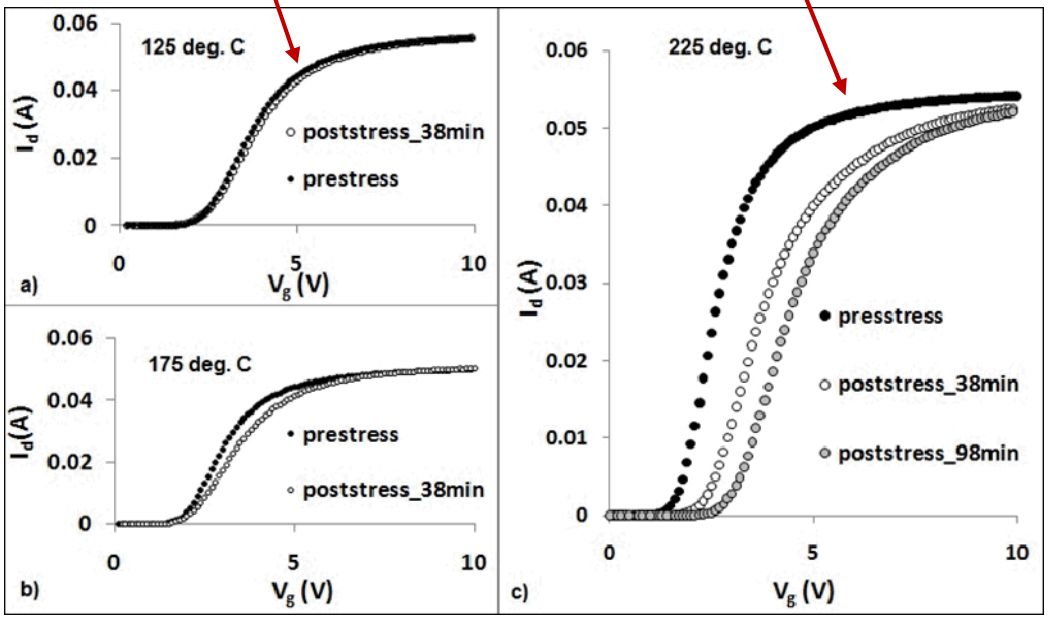
Fig. 1. Dielectric constants, and critical electric fields of various semiconductors (Si, 6H-SiC, 4H-SiC) and dielectrics (SiO_2, Si_3N_4 and Al_2O_3). Conduction and valence band offsets of these are also shown with respect to SiO_2.

R. Singh, *Microelectronics Reliability* **46**, 713 (2006).

Bias-Temperature Stress: ΔV_T and Increase in MOS Bulk and Interface State Density

Minimal degradation at rated temp (125˚C)

Severe degradation at high temp



Stress: V_{GS} = +20 V, V_{DS} = 0.1 V

S. DasGupta et al., *Appl. Phys. Lett.* **99**, 023503 (2011).

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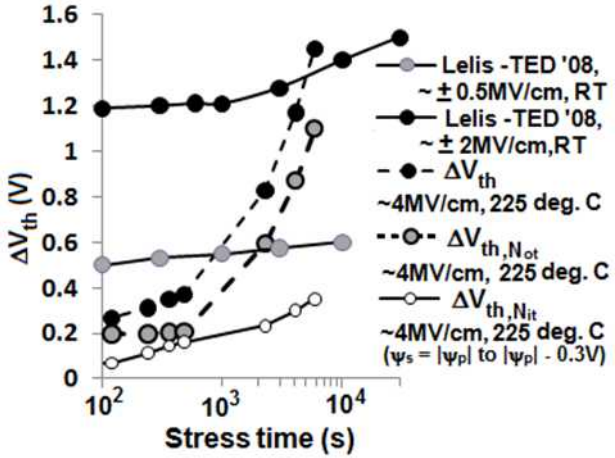
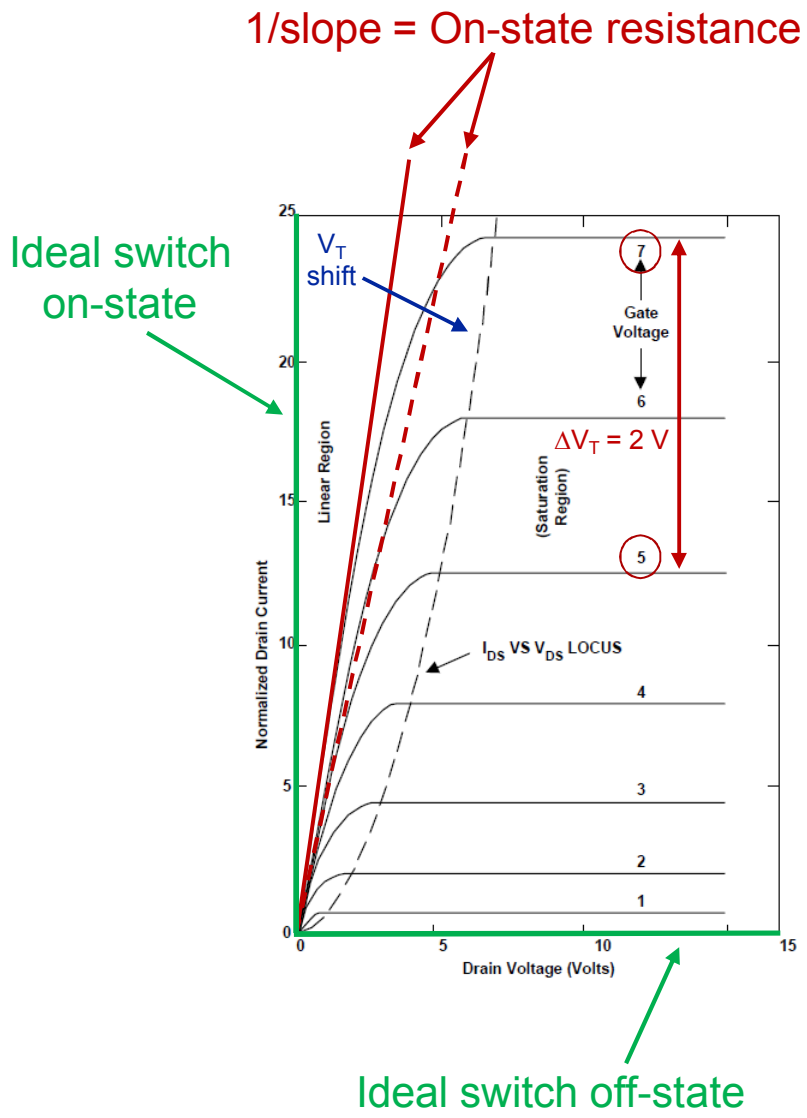
Commercial 1200 V SiC MOSFET



Evolution of interface and bulk trapping components vs. time

Impact of ΔV_T on MOSFET I-V



Threshold voltage shift can change gate drive (equivalent to larger/smaller applied gate voltage) and result in changes in on-state resistance (e.g. higher conduction loss, reduced system efficiency)

Non-ideal switch model:

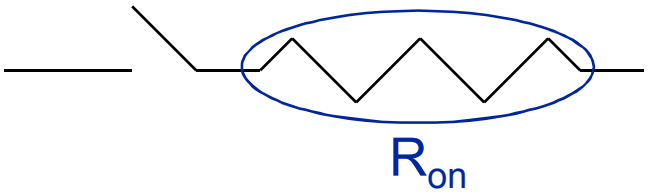


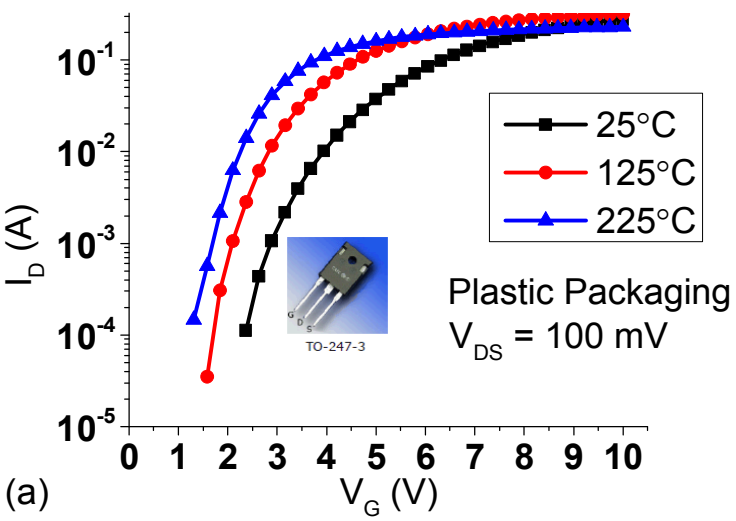
Diagram source: International Rectifier, "Power MOSFET Basics"

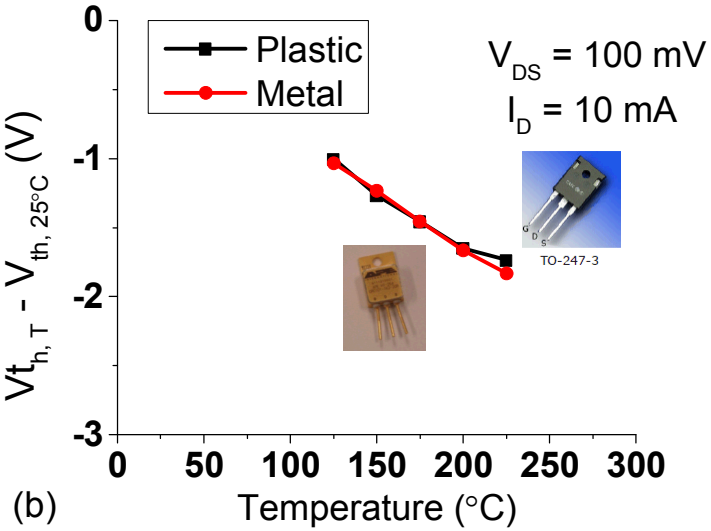
Commercial SiC MOSFETs Evaluated Under Various Conditions

- 1200 V SiC MOSFET from a single manufacturer
- First- and second-generation devices examined
- Plastic and metal packaging
  - Both package types for first-generation device
  - Plastic only for second-generation device (just got metal-packaged samples)
- Evaluate leakage current under forward-blocking conditions ($V_G = 0$ $V_G < 0$)
- Evaluate threshold voltage shift ΔV_T under DC gate stress as a function bias polarity and magnitude, and temperature
- Evaluate ΔV_T under AC gate stress as a function of duty cycle
- Temperature ratings: 1st gen. plastic = 125˚C, 1st gen. metal = 225˚C, 2nd gen. plastic = 150˚C

GEN1

Impact of High Temperature on MOSFET I-V (No Stress)

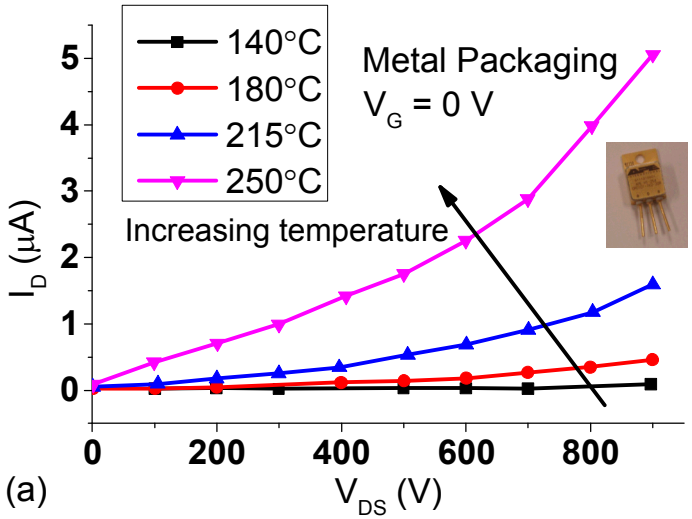




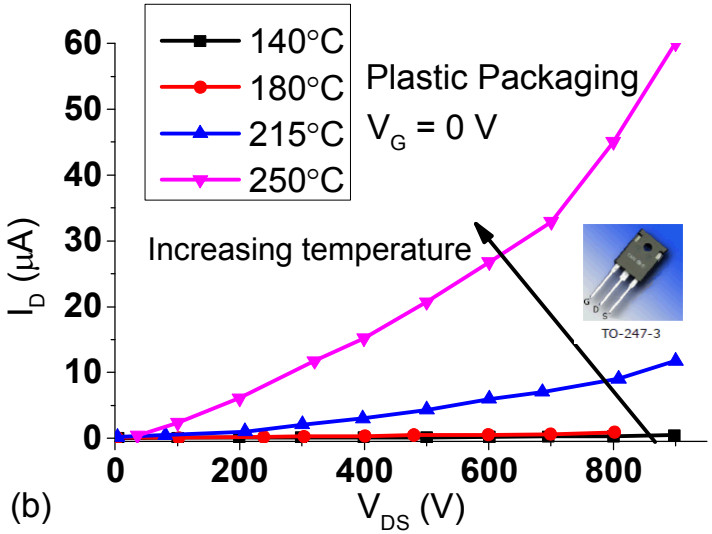
Non-constant sub-threshold slope and negative ΔV_T with increasing temperature are consistent with a high density of interface traps

GEN1

Blocking State Bias Condition: Plastic vs. Metal Package



(a)

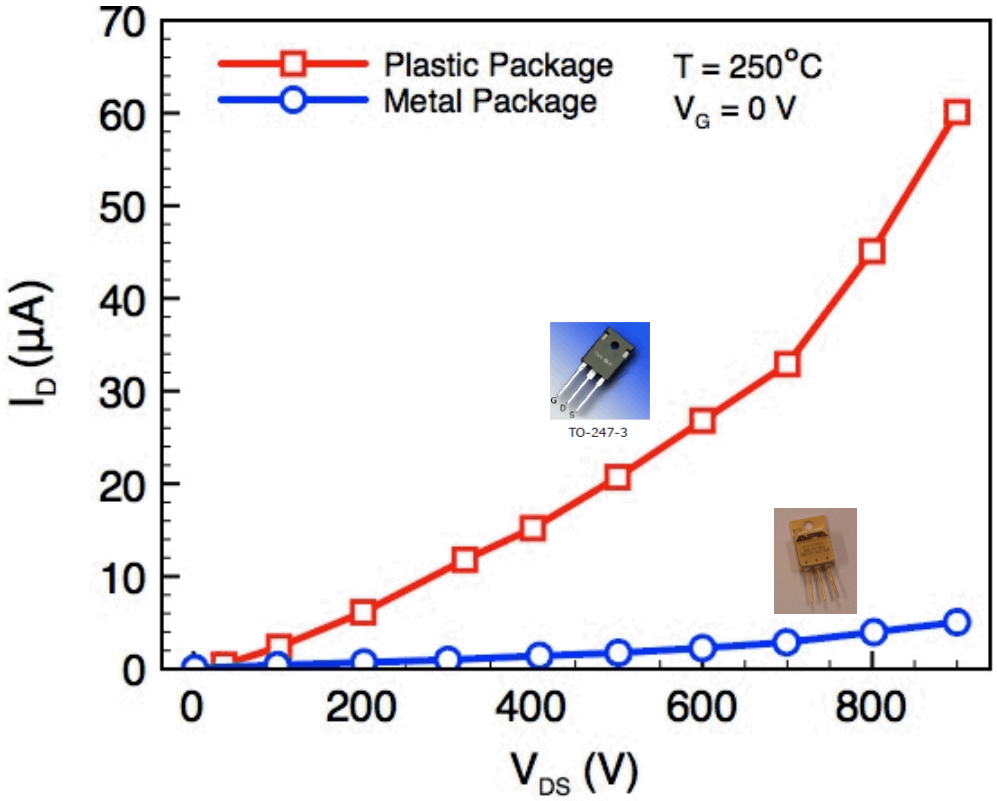


(b)

- **Plastic part is rated to 125˚C, metal part is rated to 225˚C**
- **Leakage current is reasonably low below rated temperature**
- ***Plastic-packaged part shows significantly higher leakage at high T***

GEN1

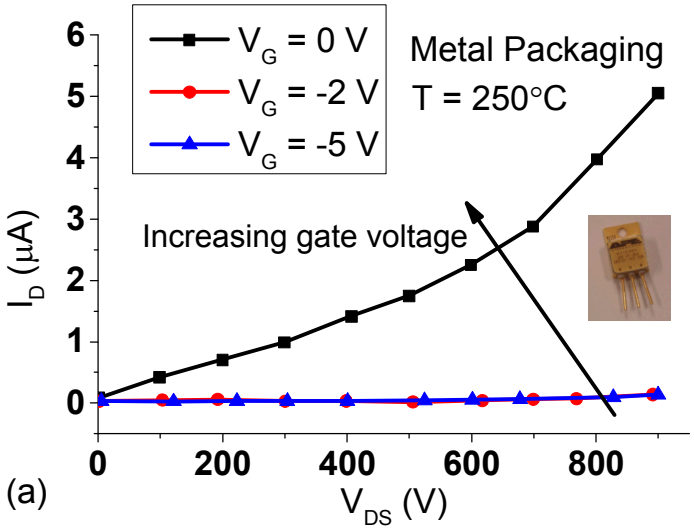
Direct Comparison of Plastic vs. Metal Packaging in Forward-Blocking State



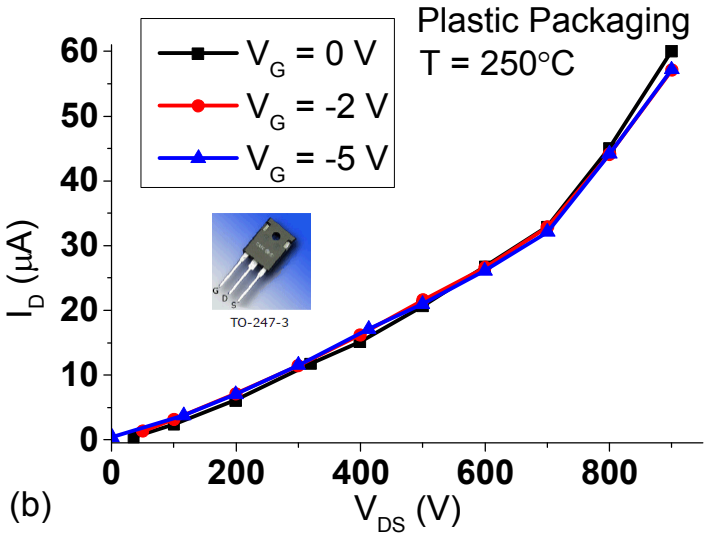
- *~10× higher leakage current for plastic-packaged part*
- *Plastic packaging appears to introduce an extrinsic drain-to-source leakage path*

GEN1

Gate Voltage Dependence of Off-State Leakage Current



Metal package:
Strong V_G dependence



Plastic package:
No V_G dependence

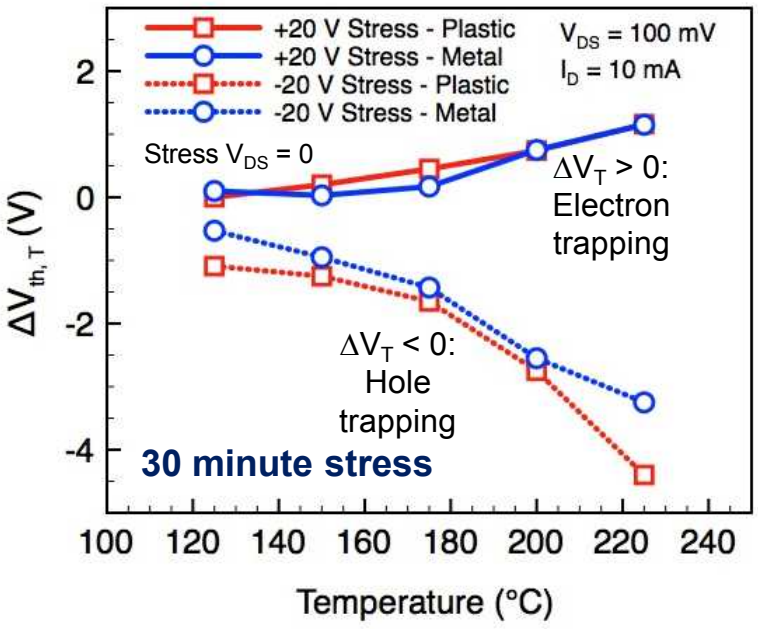
- **Negative gate voltage may be used to turn device completely off *for the metal-packaged device only***
- ***Plastic packaging appears to introduce an extrinsic drain-to-source leakage path that is not controlled by the gate***

Threshold Voltage Instability for Positive and Negative Gate Stress

GEN1

Plastic

Metal



Threshold voltage shift is independent of packaging type

- Shift in threshold voltage ΔV_T (likely due to charge trapping in the gate oxide) will change R_{ON} and thus the ON-state conduction power loss

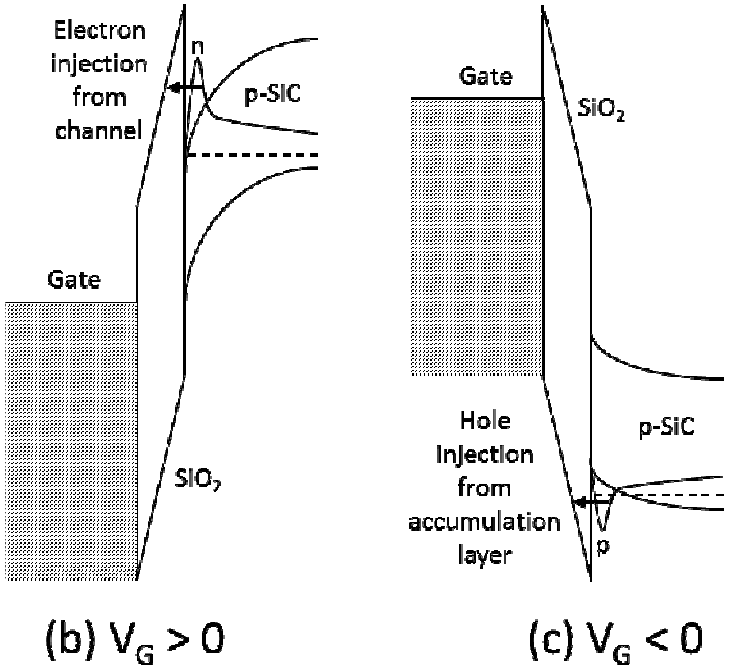
- ΔV_T is a function of time t, gate voltage V_G, and temperature T

- Assume a power-law dependence on t and V_G, and an Arrhenius dependence on T

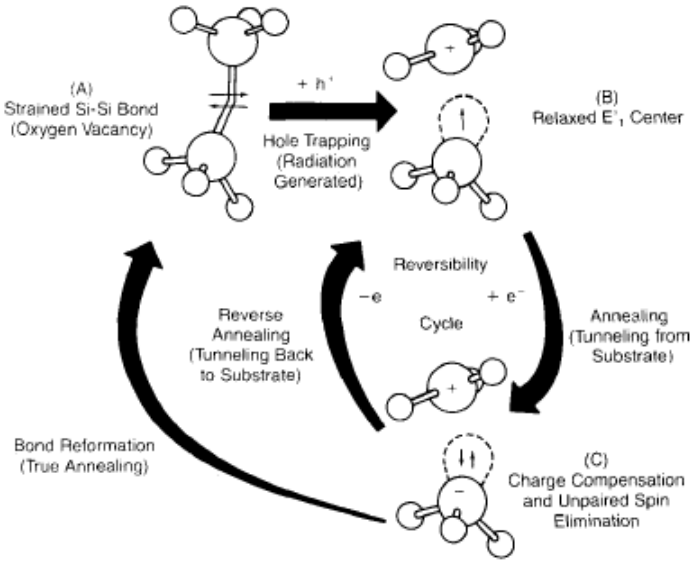
- **For *positive* V_G:**
  $$\Delta V_T = 8.5\times10^{-3} t^{0.40} V_G^{3.8} \exp(-0.34/kT)$$

- **For *negative* V_G:**
  $$\Delta V_T = -1.4\times10^{2} t^{0.42} \left| V_G \right|^{0.79} \exp(-0.33/kT)$$

Electron vs. Hole Injection into Gate Oxide



Possible bulk defect: E' center (oxygen vacancy)

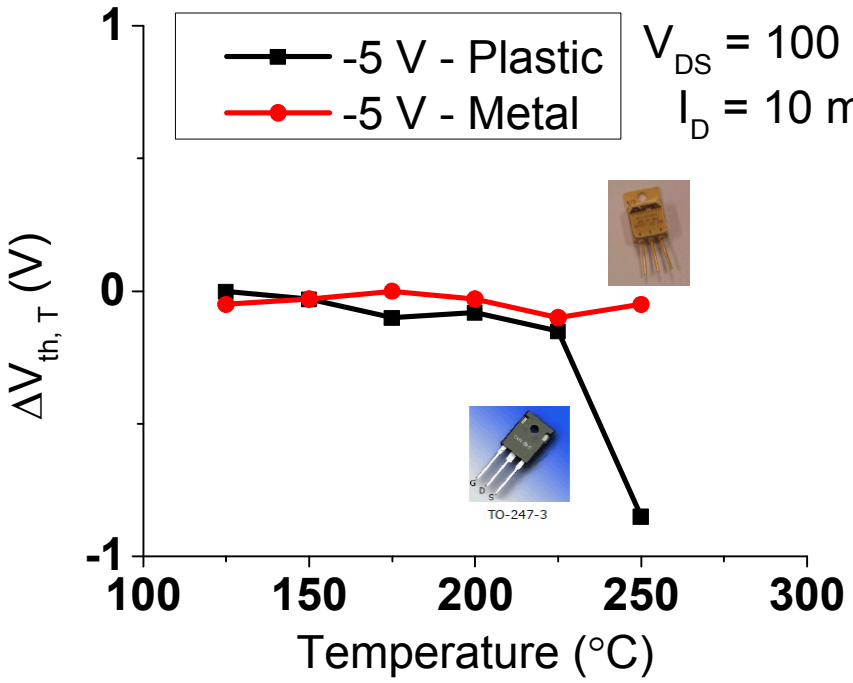


A. J. Lelis et al., *IEEE Trans. Nuc. Sci.* **36(6)**, 1808 (1989).

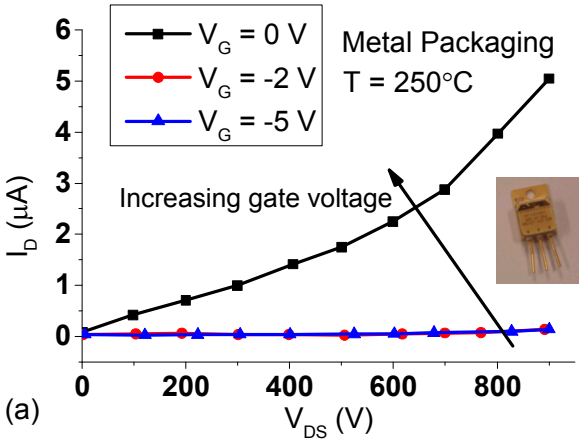
Hole injection under negative gate bias appears to result in greater instability than electron injection under positive gate bias

ΔV_T vs. Temperature at -5 V Gate Voltage

GEN1



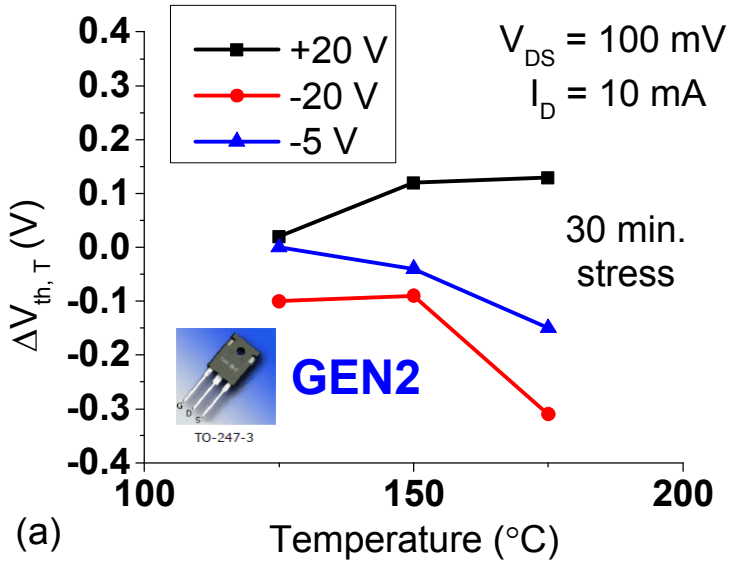
Manufacturer recommends -5 V on gate for complete turn-off (recall data from three slides ago and reproduced below)

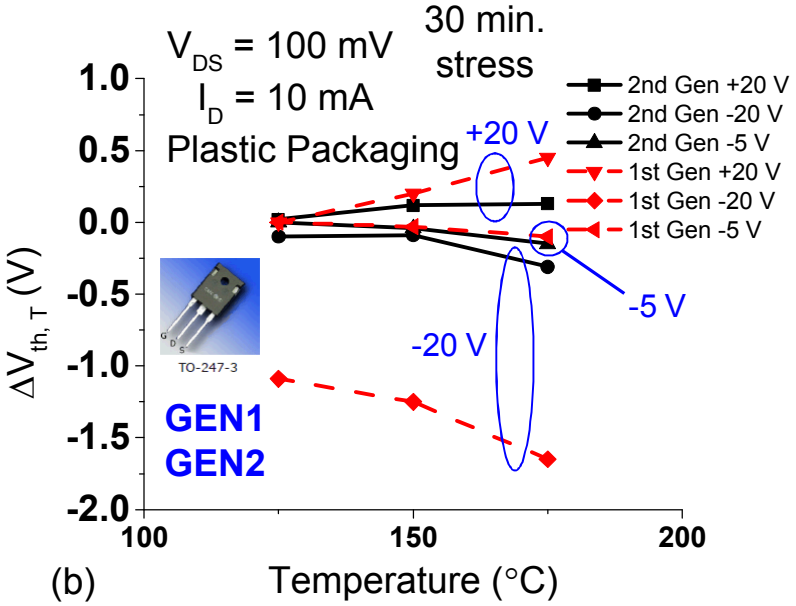


-5 V signal on gate results in negative ΔV_T in plastic-packaged part at very high temperature (250˚C = double the rated temperature) indicating good reliability under recommended off-state gate voltage

Comparison of 1st and 2nd Generation SiC MOSFETs

GEN1
GEN2





- *A huge improvement is seen in V_T stability for the 2nd generation parts, especially for the -20 V gate stress condition*
- *Likely due to design and/or processing improvements in the Gen2 device compared to the Gen1 device*

GEN2

AC Gate Stress on 2nd Generation SiC MOSFET

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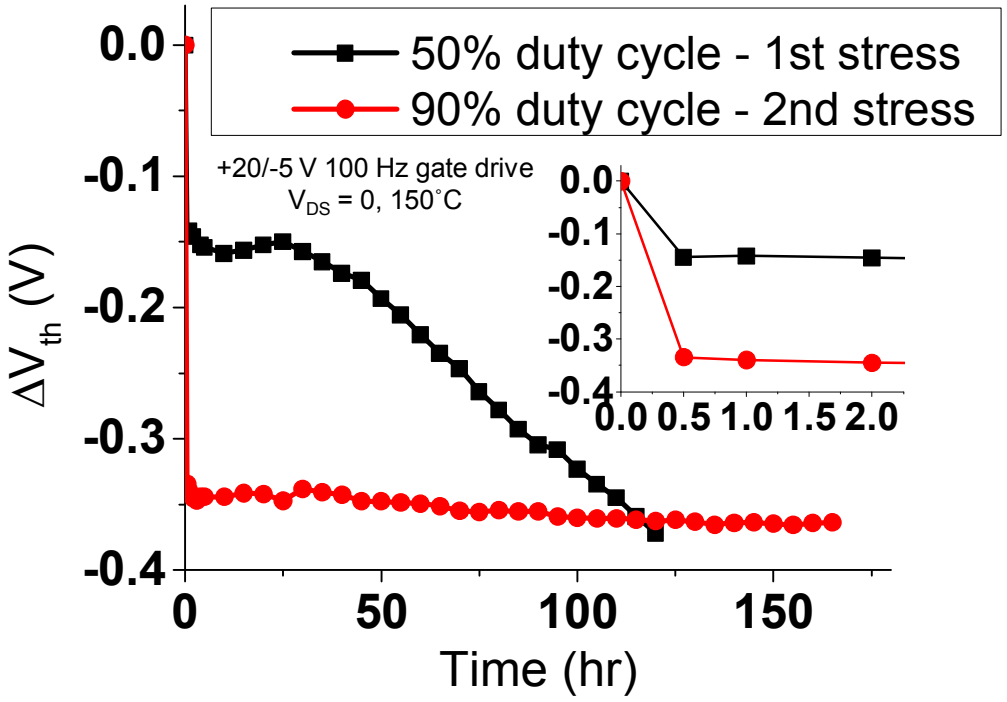

- ΔV_T is negative, suggesting that hole injection dominates electron injection
- True even for 90% duty cycle, i.e. when hole injection occurs only 10% of the time
- A very fast negative shift is observed, followed by a much slower negative shift

Much more study is needed to understand the complex injection, capture, and emission properties of electrons and holes into bulk and interface states to understand SiC MOS reliability under AC stress

Summary / Conclusions

We have demonstrated that:

- Plastic packaging of a 1200 V 1st generation SiC MOSFET increases off-state leakage current compared to metal packaging, especially at high temperature
- Compared to zero gate voltage, negative gate voltage may be used to reduce leakage current *in metal-packaged devices only*
- Gate electrical and thermal stress changes the MOSFET's threshold voltage, and we have developed models for $\Delta V_T(t, T, V_G)$ for positive and negative V_G
- The 2nd generation SiC MOSFET shows greatly improved VT stability, especially under hole injection conditions (VG << 0)
- AC gate stress results in very complex V_T degradation with a two-phase shift in V_T observed and apparent dominance of hole injection

Contact Information

Dr. Robert Kaplar (Bob)
Sandia National Laboratories
Advanced Semiconductor Devices
and Reliability Physics, Dept. 1748
Phone: 505-844-8285
Email: rjkapla@sandia.gov

Dr. Stanley Atcitty (Stan)
Sandia National Laboratories
Energy Storage Technology
and Systems, Dept. 6111
Phone: 505-284-2701
Email: satcitt@sandia.gov

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