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Influence of Barrier Design on Current Collapse in High Voltage AlGaN/GaN HEMTs

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***Abstract*— Simultaneous measurements of surface potential and drain current detrapping transients in AlGaN/GaN HEMTs, performed on devices with two different epitaxial structures, show that the predominant location of charge trapping is affected more strongly by device design than by surface passivation or buffer defects. Experiments also show that AlGaN traps dominate current collapse in devices with thick AlGaN barrier layers.**

Keywords – Galium Nitride; Power HEMT; Kelvin Force Microscopy, Trapping.

I. Introduction

High voltage GaN HEMTs promise major performance improvements compared to silicon IGBTs under high power switching operation. A major hurdle in the development of a high voltage lateral GaN HEMT is the achievement of both high breakdown voltage (V_{BD}) and low charge trapping in the AlGaN/GaN materials system. Specifically, this has been hindered by uncertainty regarding which layer or interface traps the preponderance of charge [1]-[4].

In this work, Kelvin Force Microscopy (KFM) is used to characterize surface potential changes *in situ* during drain current detrapping transients (Fig. 1). It is shown that under gate bias stress, the dominant component of current collapse in devices with thick AlGaN barrier layers (as suitable for devices with high V_{BD}) is due to traps associated with the AlGaN barrier layer, as opposed to bulk GaN defects. In contrast, the thinner, higher Al content barrier (giving lower V_{BD}) results in charge trapping near the channel, irrespective of surface passivation.

II. Device Structures

TABLE I. Synopsis of the epitaxial layer structure and composition for the two device types used.

Device Type	AlGaN Barrier	GaN Buffer	Passivation
A	50 nm thick, $Al_{0.15}Ga_{0.85}N$	Carbon Doped	ALD $Al_2O_3/SiO_2/Al_2O_3$ stack
B	20 nm thick, $Al_{0.26}Ga_{0.74}N$	Undoped	None

Table I summarizes the composition of the two equally sized (L_{gd} = 15 µm, W_g = 100 µm, L_g = 2 µm) device types used. Both devices were fabricated at MIT on silicon (111). Device A used a 50 nm $Al_{0.15}Ga_{0.85}N$ barrier, a carbon doped buffer, and an $Al_2O_3/SiO_2/Al_2O_3$ stack deposited by atomic layer deposition. The passivation is extremely effective in reducing charge trapping. Device A had a $V_{th} \approx$ -3.6 V ($V_{BD} \approx$ 1800 V). Device B used a 20 nm $Al_{0.26}Ga_{0.74}N$ barrier, an undoped buffer, and no passivation, and had $V_{th} \approx$ -1.8 V ($V_{BD} \approx$ 500 V). From physical intuition, device A was *expected* to have less surface trapping and more buffer trapping, while device B was *expected* to have more surface trapping and less buffer trapping. However, this was not the case, for reasons discussed in the following.

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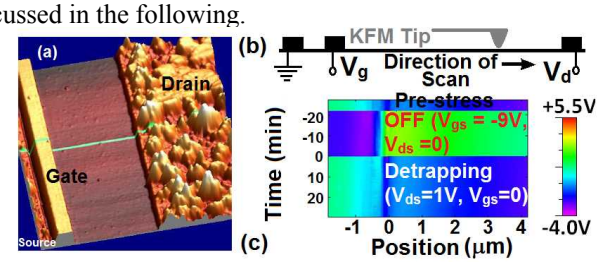

Fig. 1. (a) Device topography, acquired by AFM. (b) Schematic diagram of KFM and simultaneous bias setup. (c) Surface potential measured over a period of time as cantilever repeatedly scans from gate to drain.

III. Simutaneous Surface Potential and Detrapping Transient Characteristics

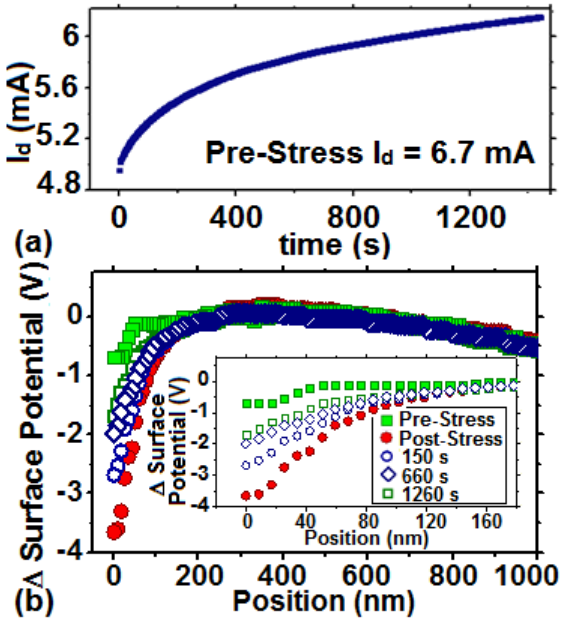

Fig. 2. (a) Detrapping transient recorded at V_{gs} = 0 V, V_{ds} = 1 V in device A following OFF-state bias stress (V_{gs} = -9 V, V_{ds} = 0 V). (b) Simultaneously measured surface potential before and immediately after stress, and at various times during detrapping. Zero position denotes gate edge on the drain side. Inset figure shows the 180 nm of scan closest to the gate edge.

Results of simultaneous KFM surface potential measurements and I_d detrapping transients are shown for devices A and B in Figs. 2 and 3, respectively. Devices were biased in OFF-state (V_{gs}= -9 V, V_{ds} = 0 V) for 20 min. to

induce charge trapping. Following this, detrapping transients were recorded at V_{gs} = 0, V_{ds} = 1 V simultaneously with surface potential measurements in a region of the device surface between the gate and the drain, from the gate edge to 2 μm from the gate edge.

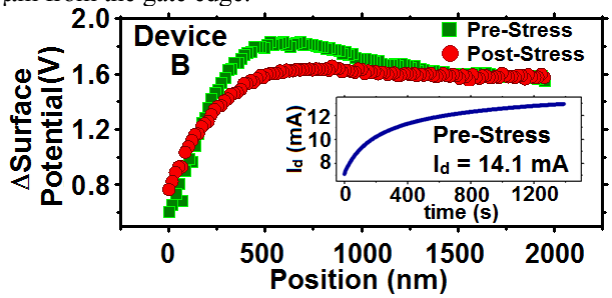

Fig. 3. Simultaneously measured surface potential before and after stress, and detrapping transient (inset) recorded at V_{gs} = 0 V, V_{ds} = 1 V in Device B following OFF-state stress (V_{gs} = -9 V, V_{ds} = 0). Zero position denotes gate edge on the drain side.

While the surface potential shifts by ~ 3 V near the gate edge for device A, it causes a peak change of only ~ 0.25 V along the channel for device B, even though device B exhibits greater current collapse (both in terms of absolute I_d and the fraction of pre-stress I_d).

IV. Impact of AlGaN Barrier Thickness

Physical insight into these results is provided by V_{th} shift measurements and simulations of surface potential shift (ΔSP) and current collapse for different locations of the trapped charge in the AlGaN/GaN/passivation stack (Fig. 4). For charge trapping at a given location to be consistent with the experimental data, *it is critical that both ΔSP and the current collapse be simultaneously satisfied.* Trapped charge closer to the AlGaN surface gives greater ΔSP and smaller current collapse (as observed for device B). Conversely, for charge trapping closer to the AlGaN/GaN interface, current collapse is larger and ΔSP is smaller (as observed for device A). Thus, contrary to the expected behavior considering surface passivation and buffer doping, device A traps more at or near the surface, whereas device B traps almost entirely at the AlGaN/GaN interface or in the GaN buffer (to be explained in greater detail in the final paper).

In OFF-state, AlGaN surface or bulk states in the access region trap electrons injected from the gate. If the electric field in the AlGaN barrier is very high in the direction normal to the AlGaN/GaN interface, it is possible for the injected electrons to gain enough energy while traversing the AlGaN barrier to reach the channel access region below, without becoming trapped in the AlGaN layer (Fig. 5). As is also shown in Fig. 5, the vertical electric field is much larger in the thinner barrier of device B, making this process much more probable in device B compared to device A. If most electrons injected from the gate in device B reach the channel without being trapped in the AlGaN, their trapping mechanism should show a ΔSP signature similar to that shown by ON-state trapping, where electrons travel in the channel from the gate edge towards the source or drain until they gain enough energy to tunnel into either the AlGaN or the GaN buffer, close to the channel, and become trapped there. ΔSP for Device A after ON-state bias stress is indeed very similar to that of Device B after OFF-state stress (to be shown in detail in final paper).

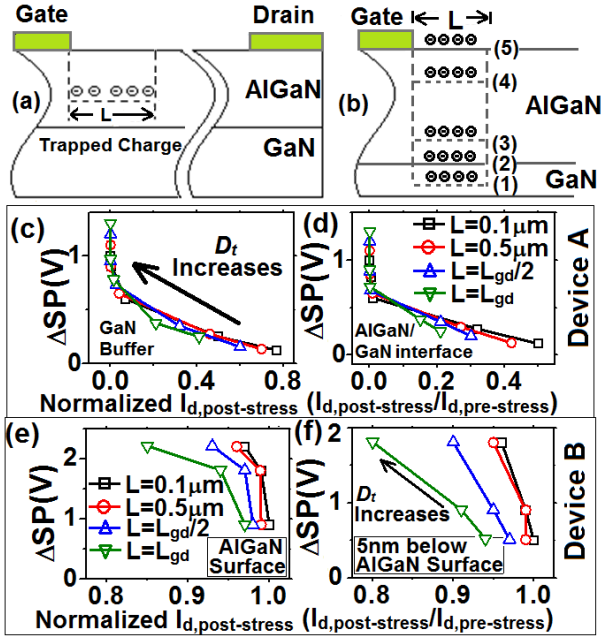

Fig. 4. (a) Position of trapped sheet of charge, from gate edge into the drain side access region (length L and density D_t). (b) 5 vertical positions of trapped charge in the AlGaN/GaN stack. Peak change in surface potential (ΔSP) of Device A vs normalized $I_{d,post\text{-}stress}$ for L = 0.1μm, 0.5μm, $L_{gd}/2$, and L_{gd} (D_t = 0.65D_0, 0.8D_0, 0.9D_0 and 0.95D_0 with D_0 = 1.2 × 10^{13} cm^{-2}) simulated for (c) GaN buffer and (d) AlGaN/GaN interface (positions 1 and 2 in Fig. 5b). D_t = 0.75D_1, 0.5D_1 and 0.25D_1 (D_1 = 8 × 10^{12} cm^{-2}) simulated for (e) AlGaN surface and (f) 5 nm below AlGaN surface (positions 5 and 4 (Fig. 5b) of Device B.

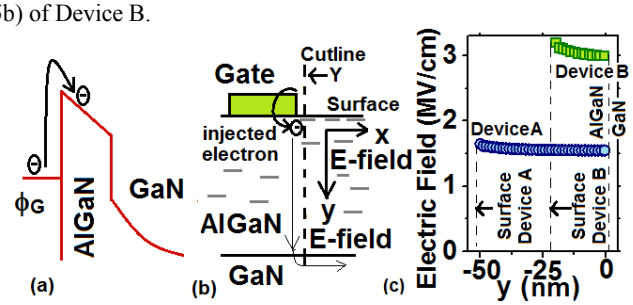

Fig. 5. (a) Schematic illustration of thermal emission from gate into AlGaN during OFF-state. (b) Under very high electric field in y-direction, injected electrons can gain enough energy to travel through the AlGaN barrier and reach the channel without being trapped. (c) Simulated electric field (cutline Y) at the gate edge for Device A and Device B in OFF-state.

Thus, the results strongly suggest that the location of charge trapping in AlGaN/GaN HEMTs is affected more by the design of the device and the electric field profile than by the actual trap distribution resulting from a given passivation or doping scheme. The dominant component of current collapse in devices with a thick AlGaN barrier layer is shown to come from AlGaN traps.

References

[1] H. Kim, **Phys. Stat. Sol.** A 188, 203 (2001)
[2] S. C. Binari, **Proc. IEEE**, 90 (6), 1048 (2002)
[3] R. Vetury, **IEEE Trans. Electron Dev.** 48, (3), 560 (2001).
[4] G. Meneghesso, **IEEE Trans. Electr. Dev.** 51 (10) 1554 (2004).