Exceptional service in the national interest

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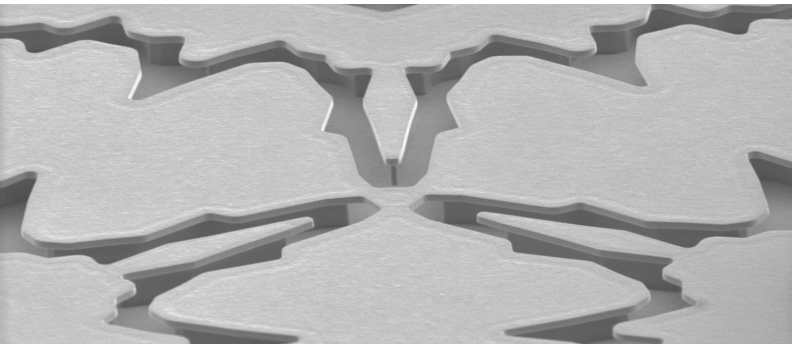

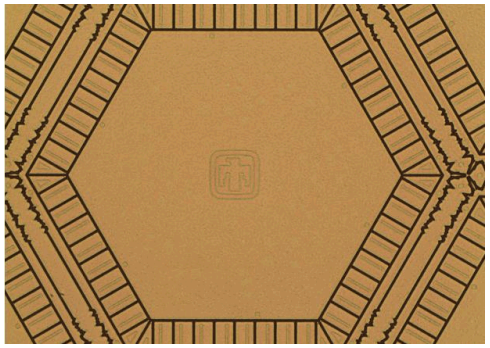

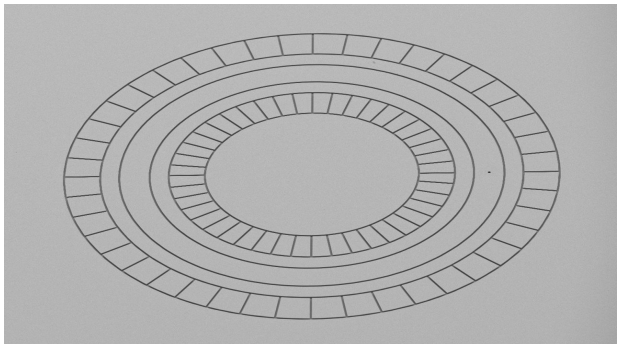

Surface Electrode Ion Trap Device Technology for Quantum Information Science

Peter Maunz, Matthew Blain, Amber Young, Daniel Stick, Chris Tigges, Daniel Stick

September 23, 2013

IARPA

UNM

U.S. DEPARTMENT OF ENERGY

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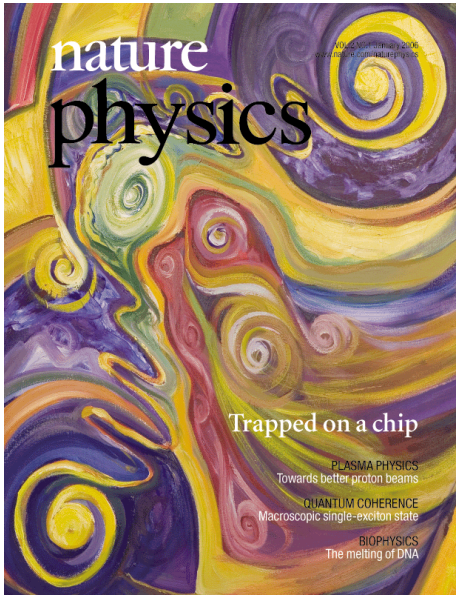
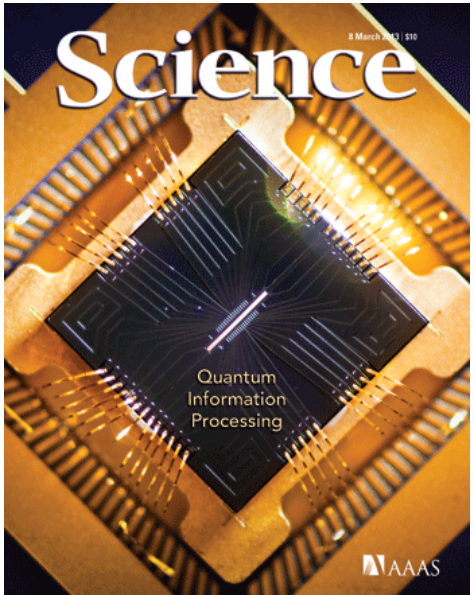
Trapped Ion Quantum Information Processing

- Fulfill all of DiVicienco's criteria
- Long trapping and coherence times
- High fidelity state preparation, detection and single qubit operations
- High fidelity two-qubit gates
- Entangled state of up to 12 ions have been demonstrated
- All basic quantum





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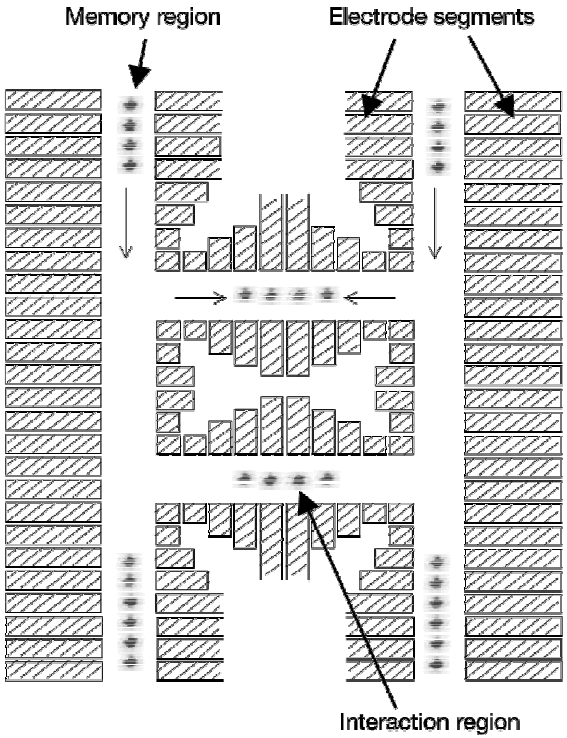
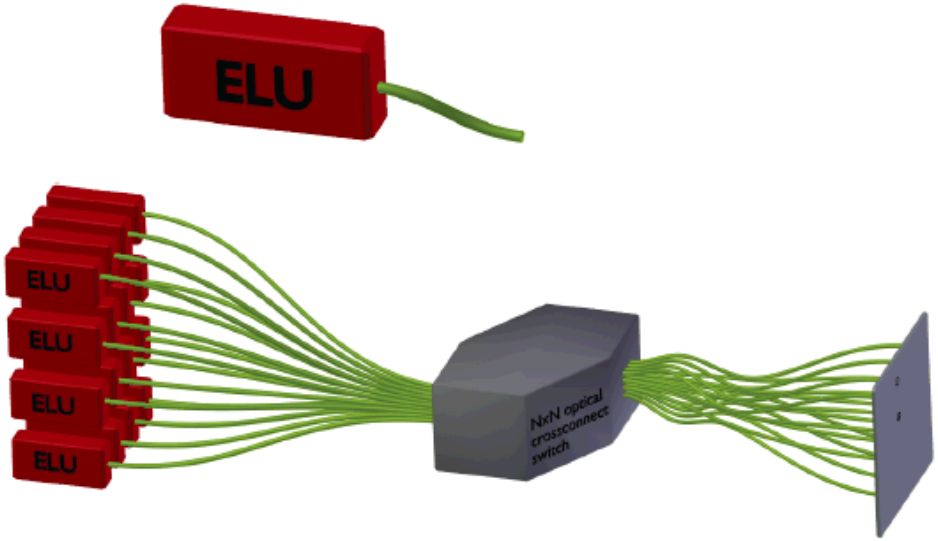
Ion Traps
scaling trapped ion QIP



Kielpinski, Monroe and Wineland, *Nature* **417**, 709 (2002)

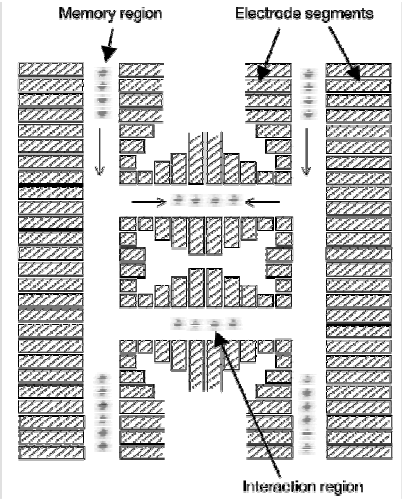
Remote entanglement

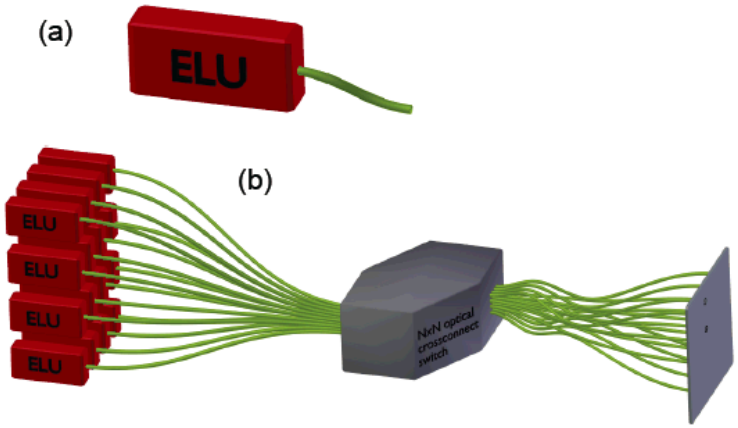


Monroe et al., quant-ph/1208.039 (2012)

Scaling trapped ion QIP

requirements





- Linear segments for processing and storing QI in ion chains
- Junctions
- Optical access for individual addressing of ions

- Efficient light collection
- Integrated optics to allow remote link and processing closeby

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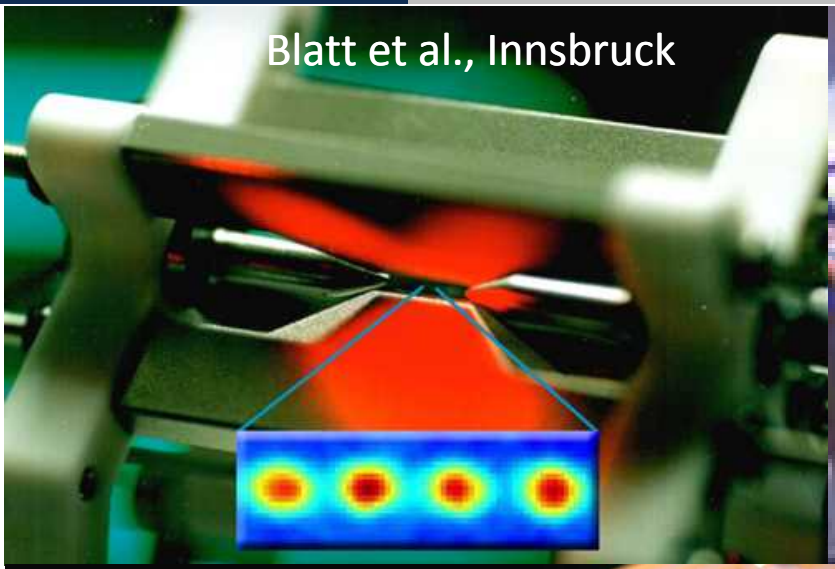
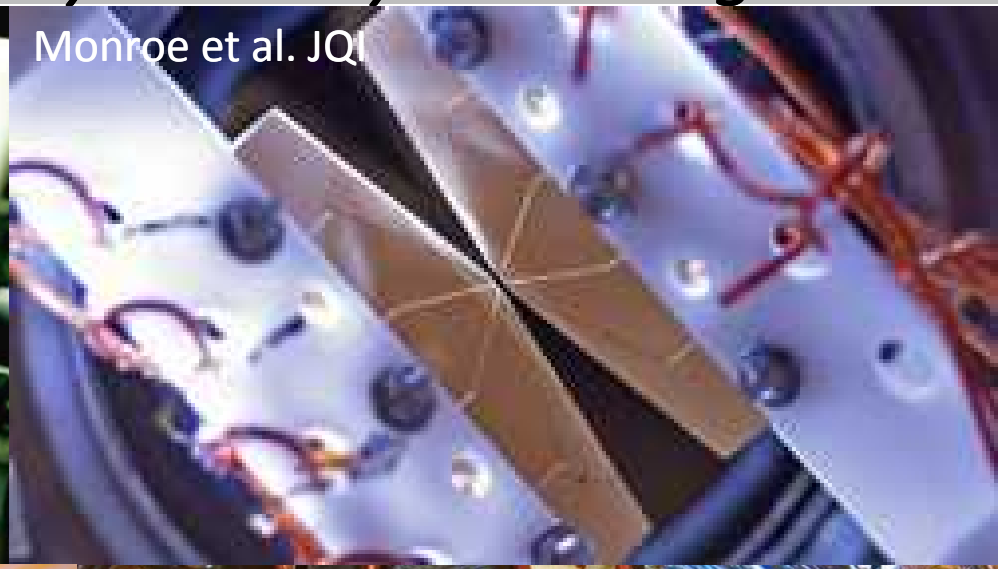
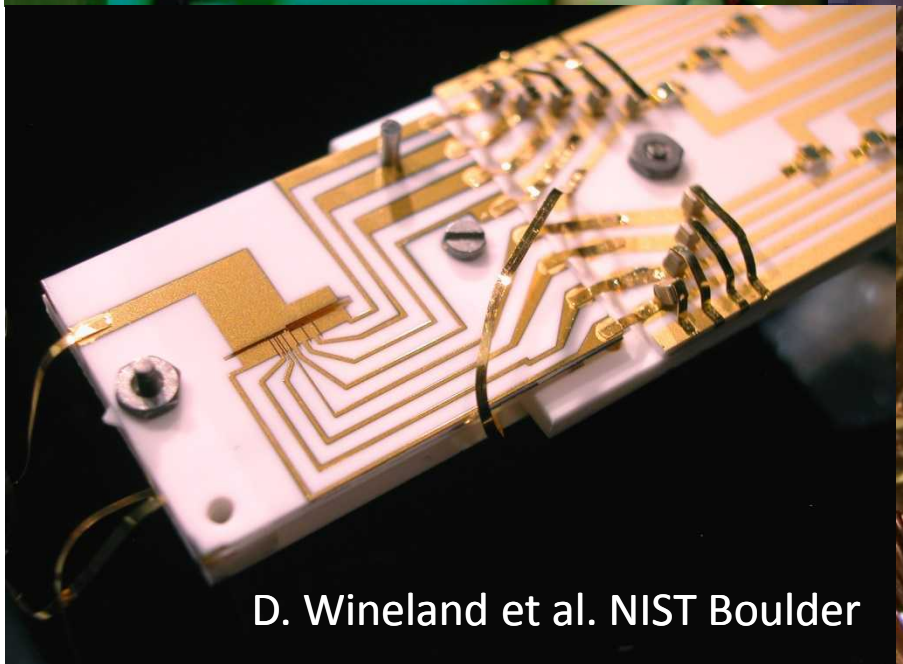
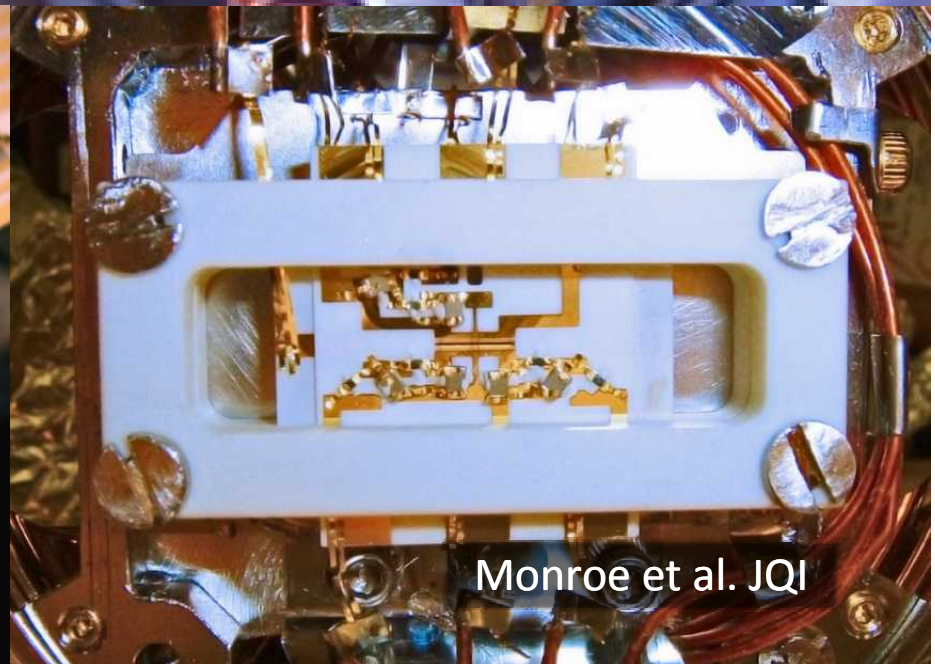
Macroscopic ion traps

why are they still being used?









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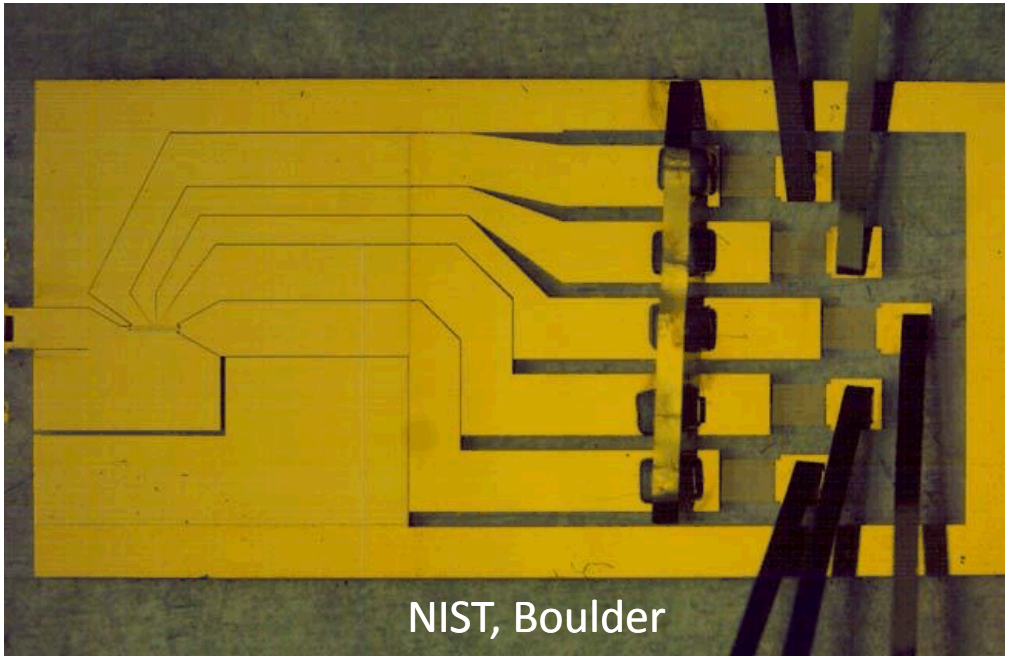
Surface Ion traps *the first steps*

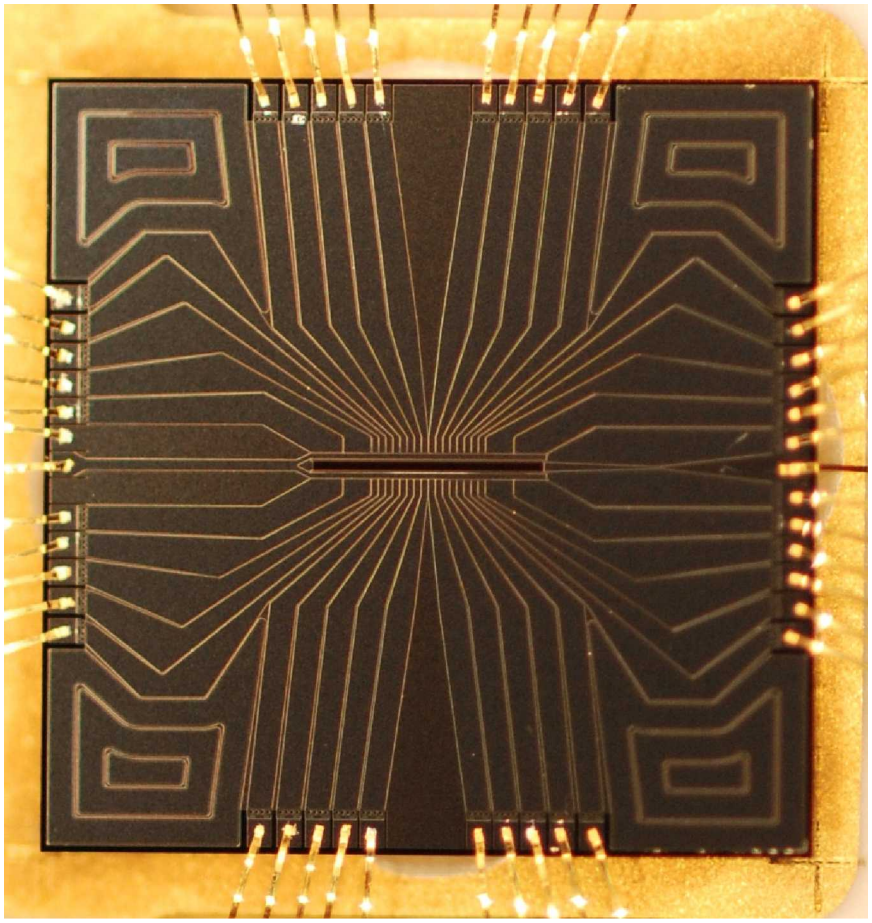
First Surface ion trap:

- Gold on fused silica
- Few electrodes
- Exposed dielectric



Seidelin et al. *PRL* **96**, 253003 (2006)

Thunderbird trap
the workhorse



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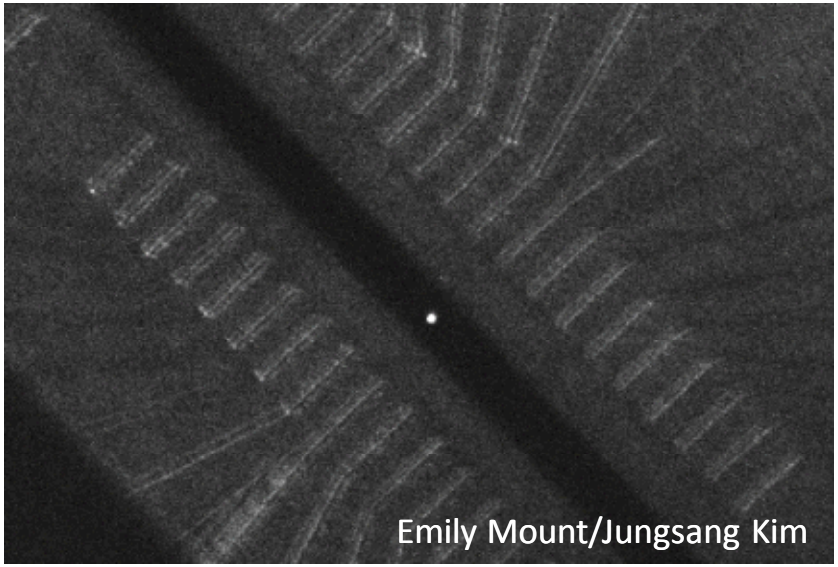
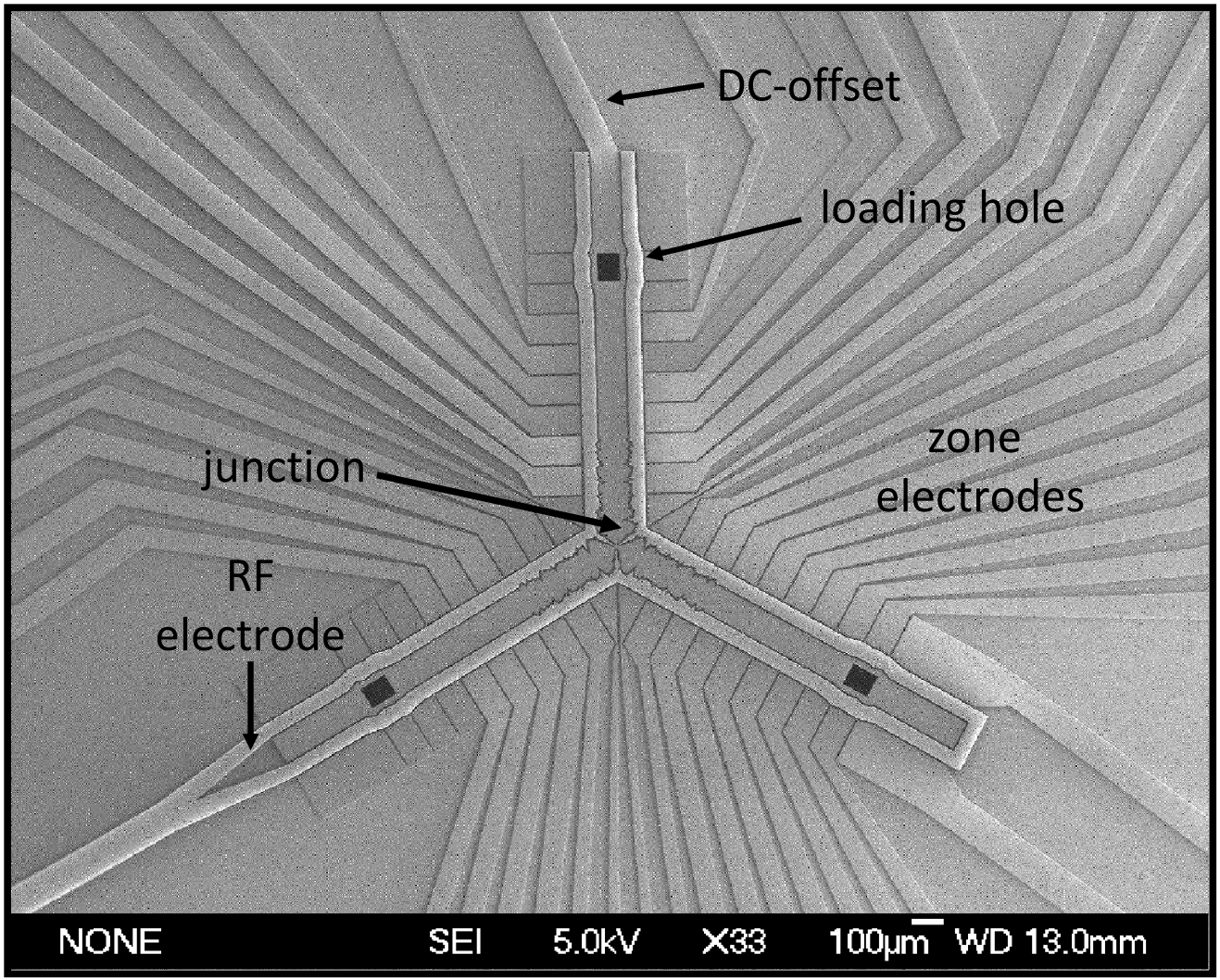
- 2-layer design
- though chip slot
- in operation around the world
- can be equipped with chip capacitors

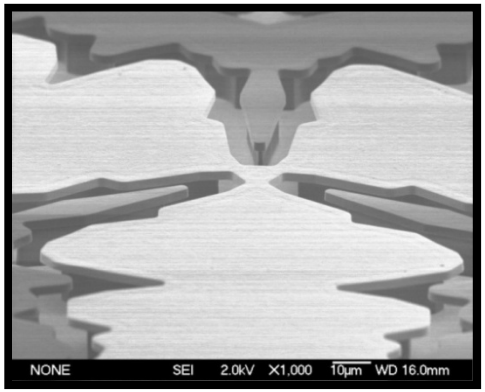
Excellent trapping times proven @ Duke

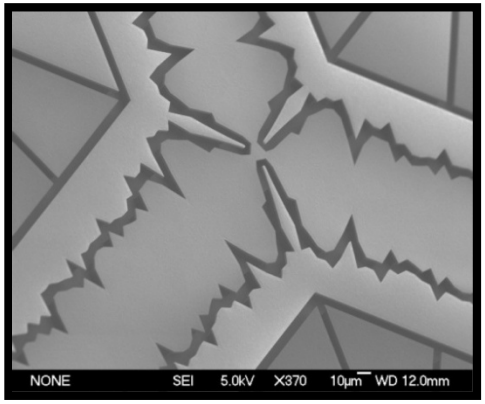
- > 8h cooled
- > 30min dark
- Heating rates (Yb, 2MHz) 0.5 q/ms

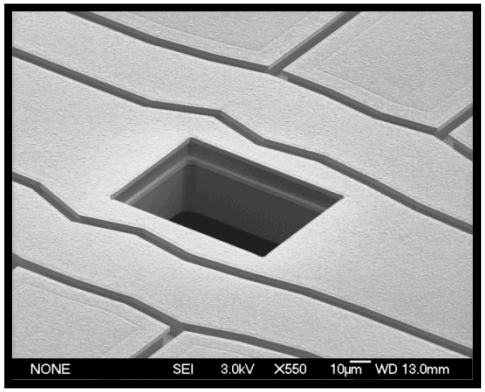


Sandia Y-junction trap



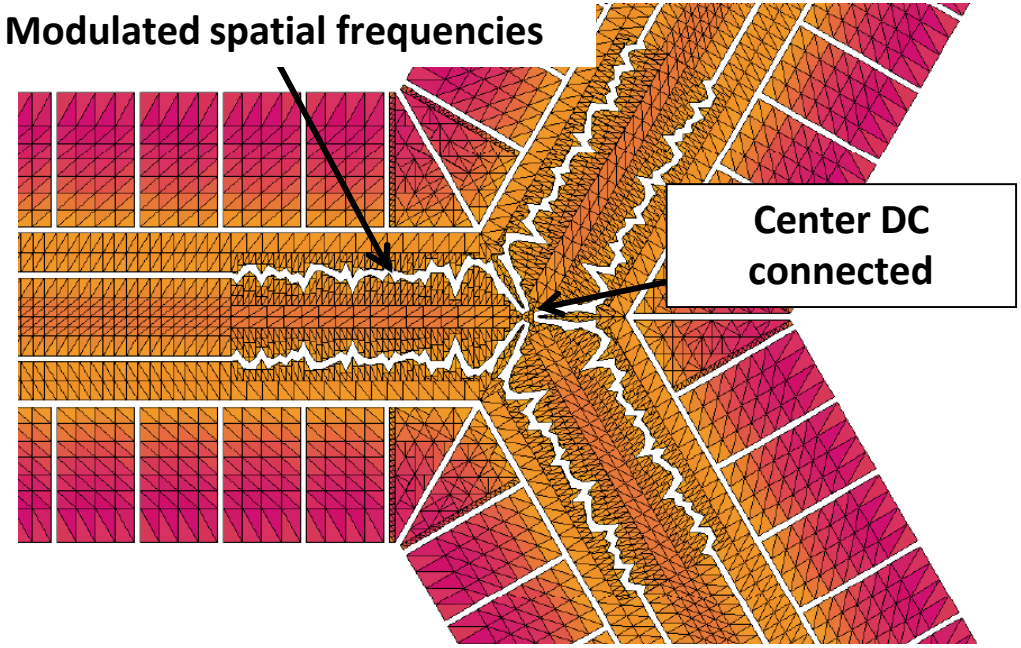


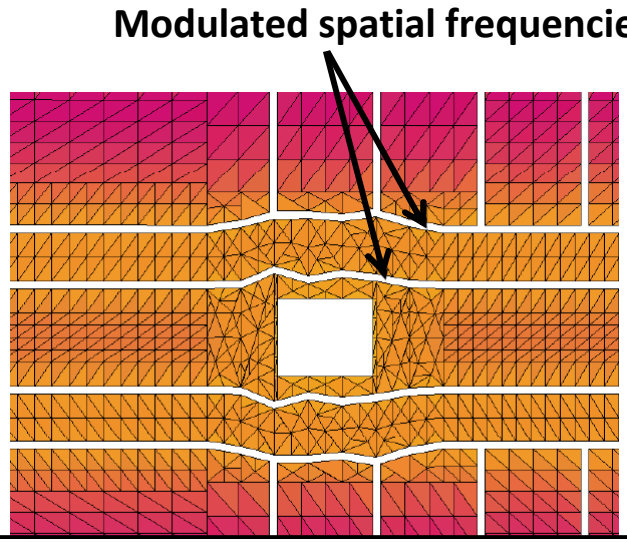


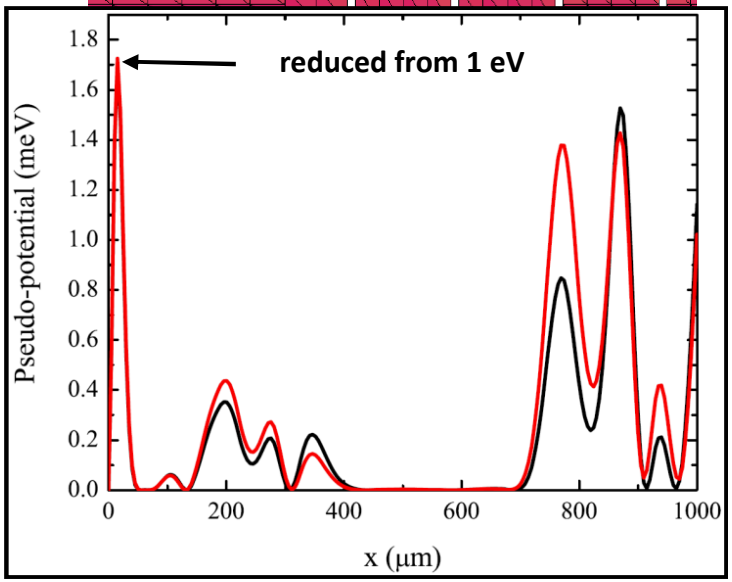


D. L. Moehring, *et al.* **New J. Phys** 13, 075018 (2011).

Y-junction trap
making shuttling work







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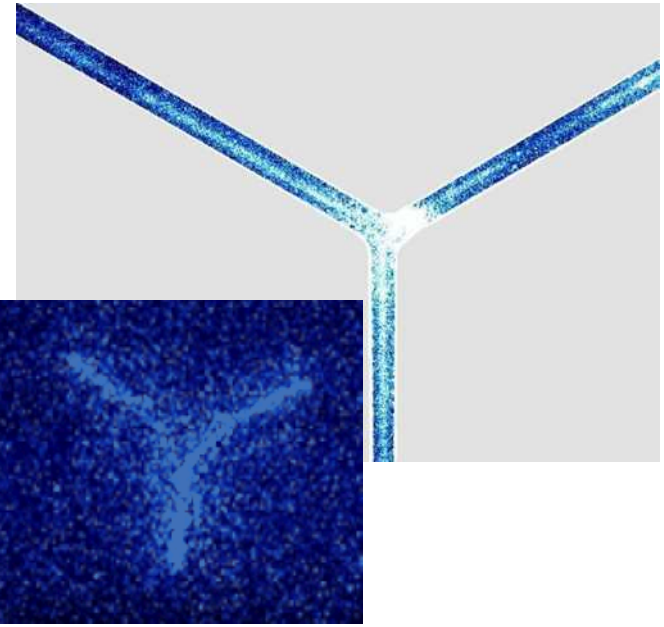
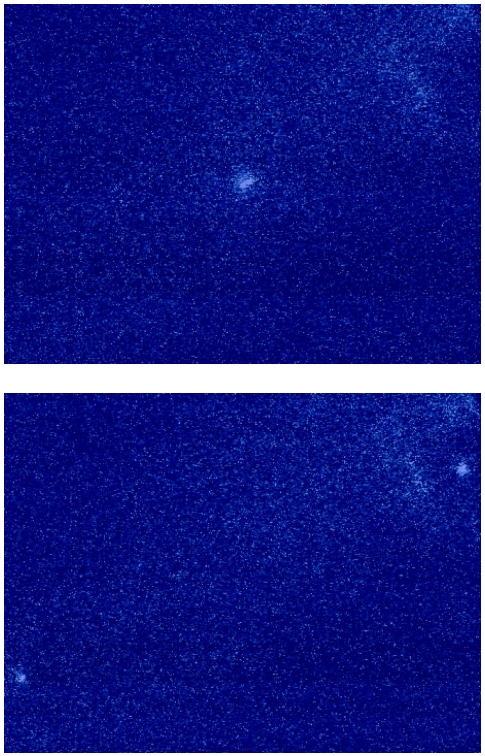
Y-junction trap *ion transport*

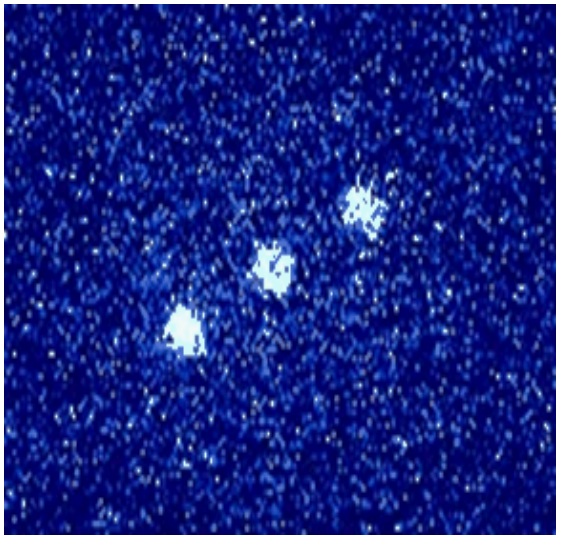
Shuttling



Splitting/Recombination

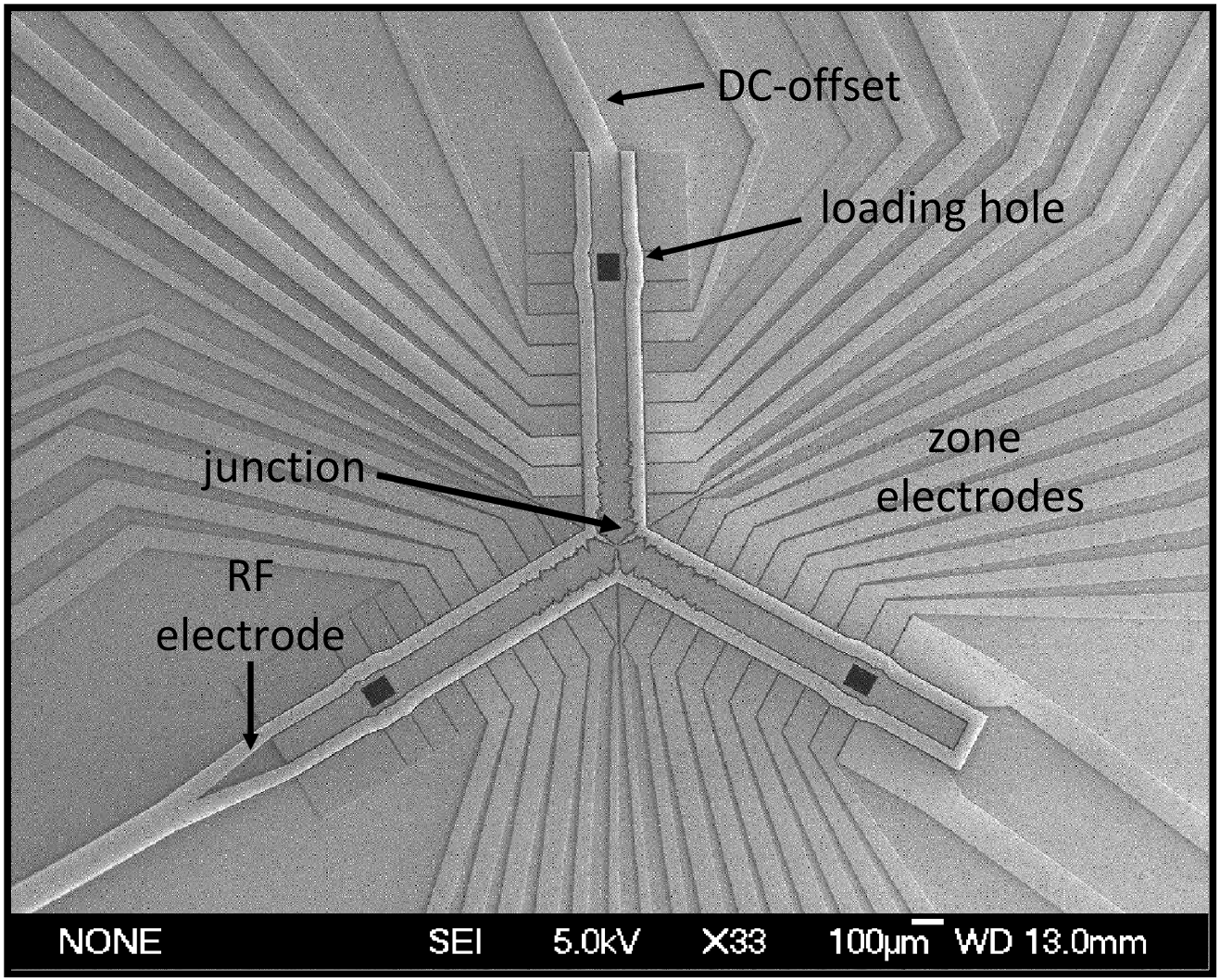


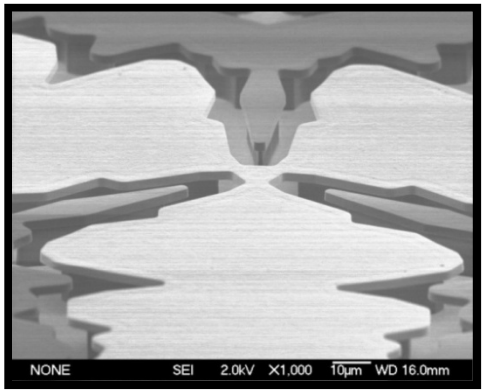
Multiple ions

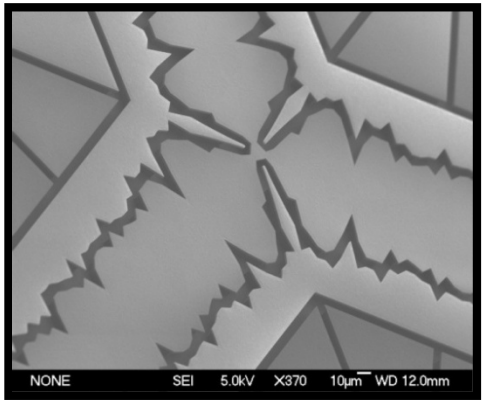


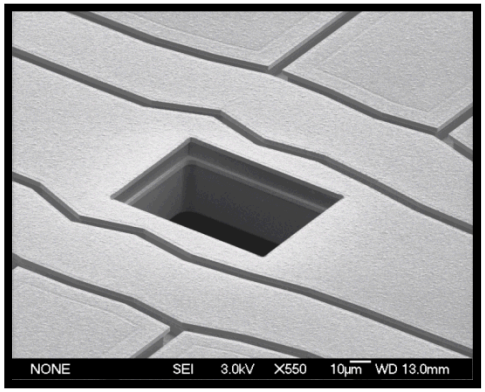
Successful shuttling in multiple independent systems with identical voltage solutions.

Sandia Y-junction trap





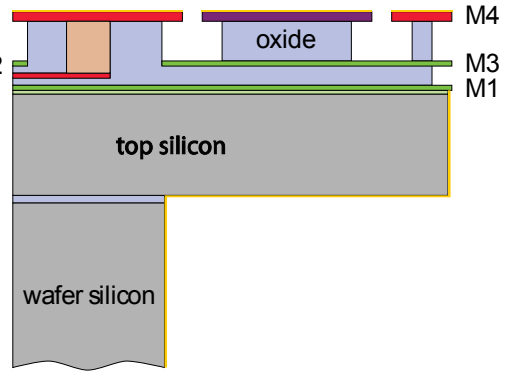


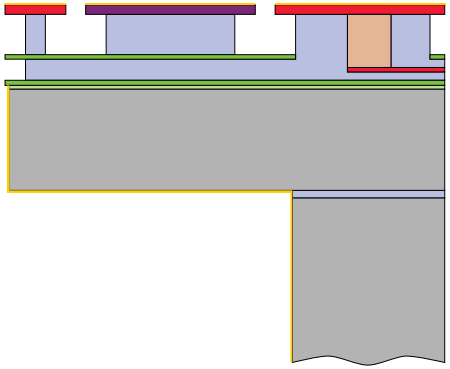


D. L. Moehring, *et al.* **New J. Phys** 13, 075018 (2011).

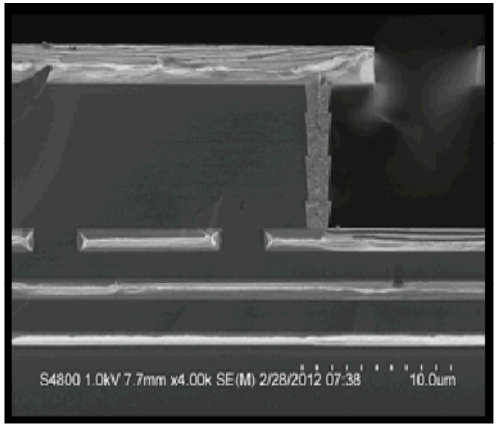
Fabrication capabilities

four metal layer process





- precisely recessed oxide
- Grounded M3
- Routing on M2
- Gold coating from front and back side



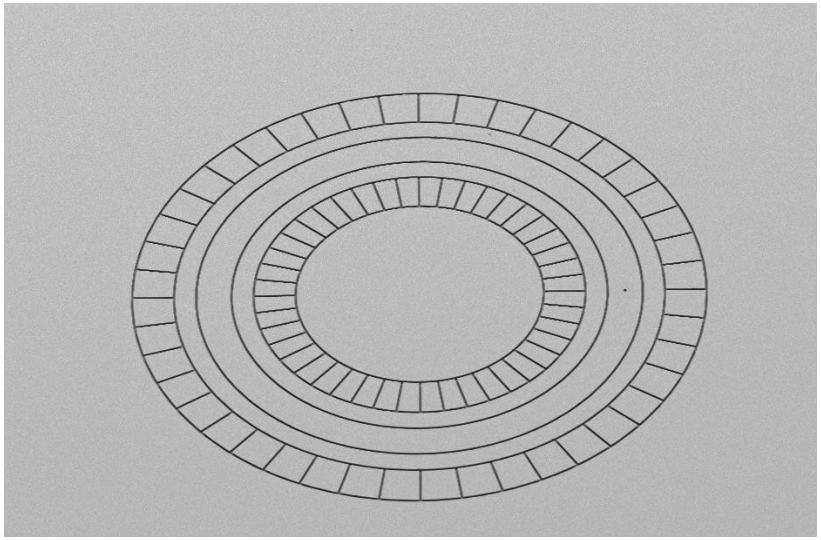
Modern 4-layer traps

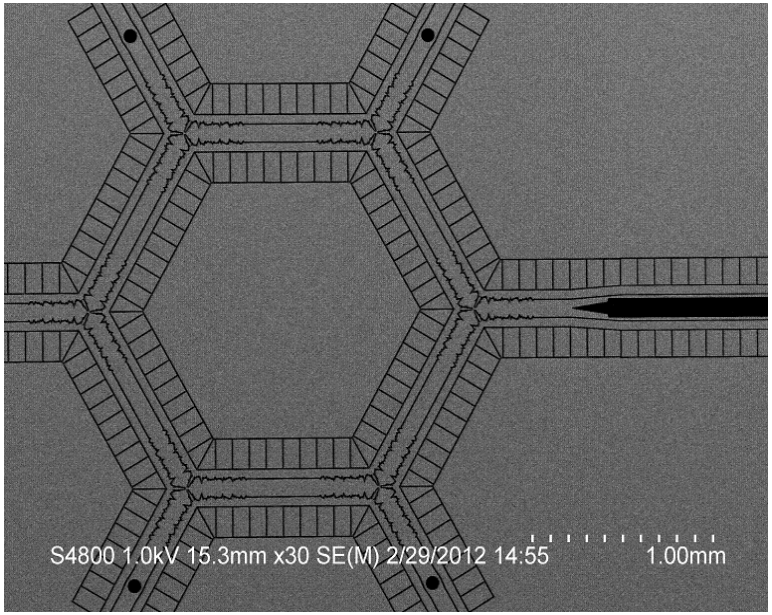
any trap topology possible

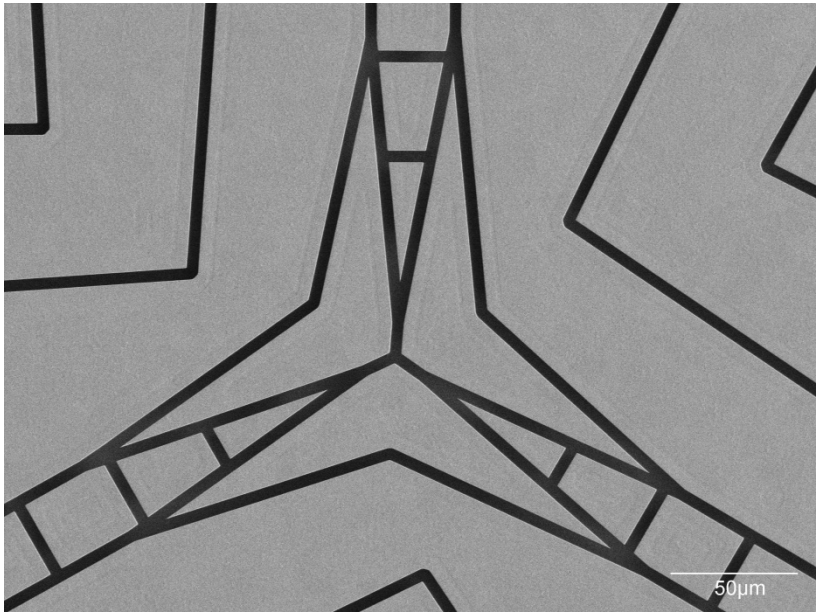
4-layer process:

- No exposed routing
- Islanded electrodes
- New topologies

Imagine your trap geometry:
it can be realized

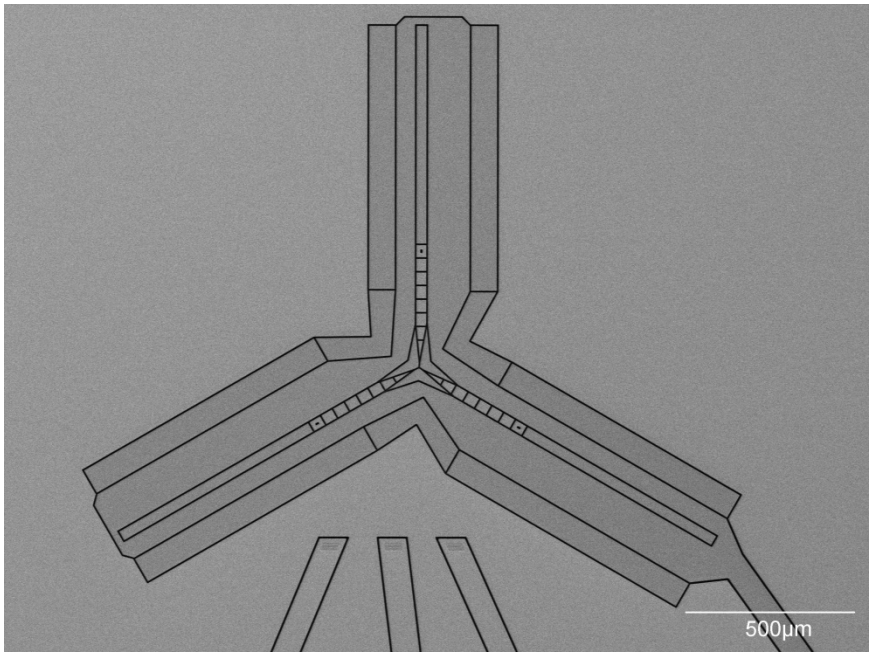


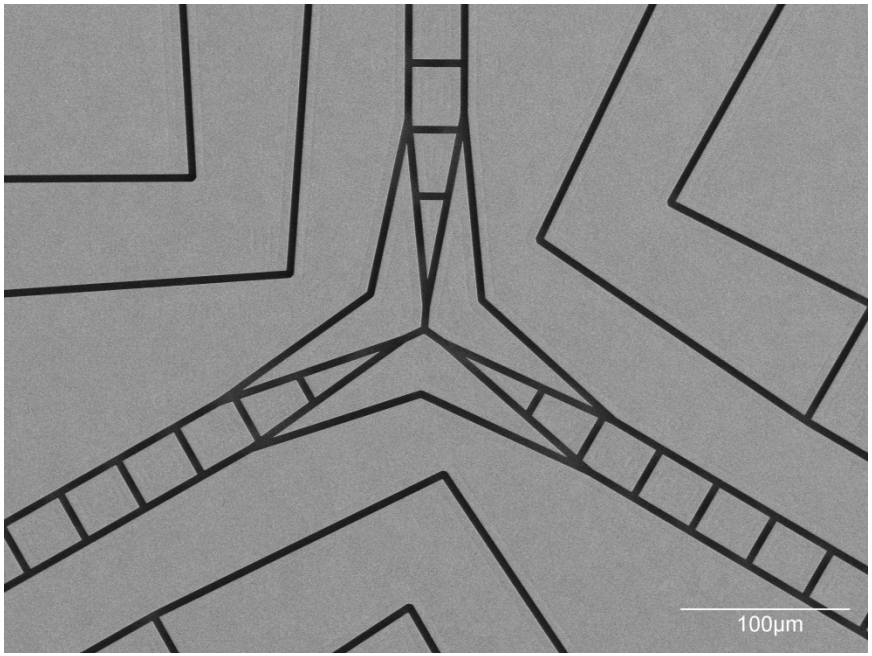


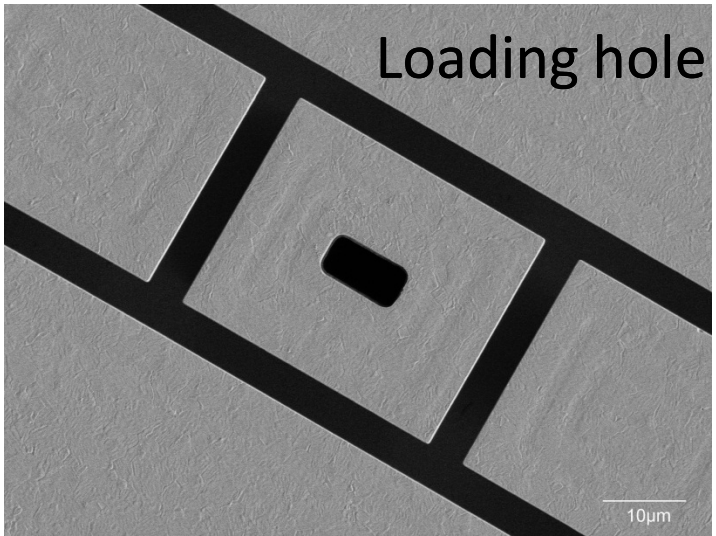


Switchable Y (NIST)

optimus prime





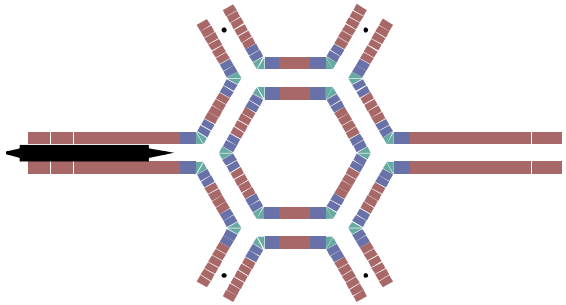


- Only realizable in 4-layer design
- Greatly reduced rf ripple
- 3 switchable rf electrodes
- Engineered for low capacitance and improved phase control

Circulator trap

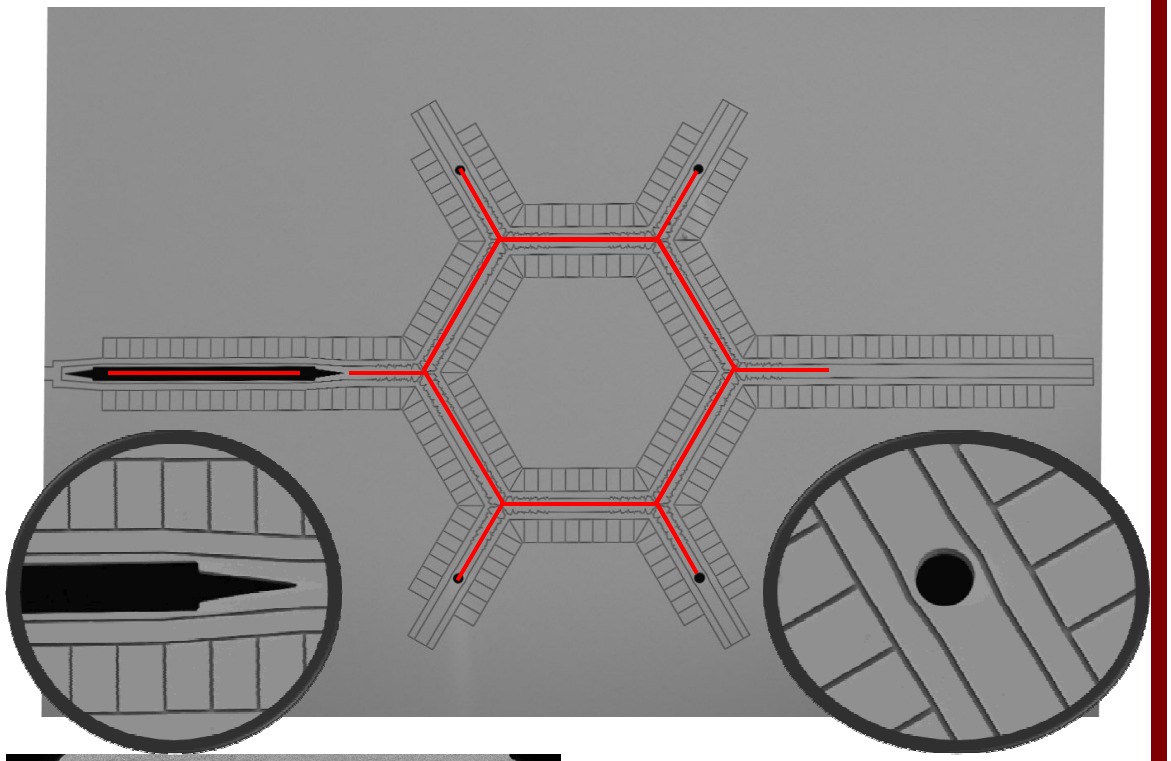
Y-junction circulator

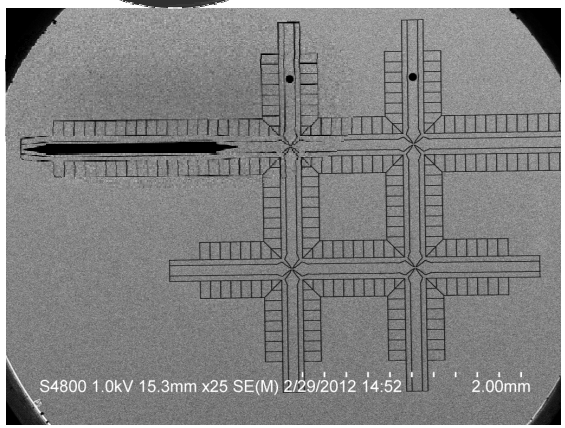
- Junctions based on demonstrated Y trap (SNL and GT)
- 93 independent electrodes; 216 electrodes all junctions co-wired
- Slot for vertical optical access, 4 loading holes
- Shuttled around Y trap with identical shuttling voltages in each turning direction

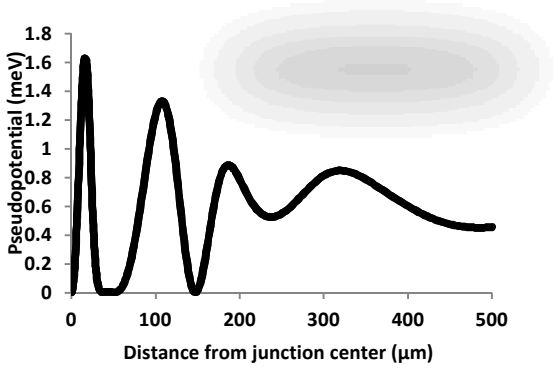


X-junction circulator

- Designed in collaboration with GT and Duke
- 93 independent electrodes; all junctions co-wired

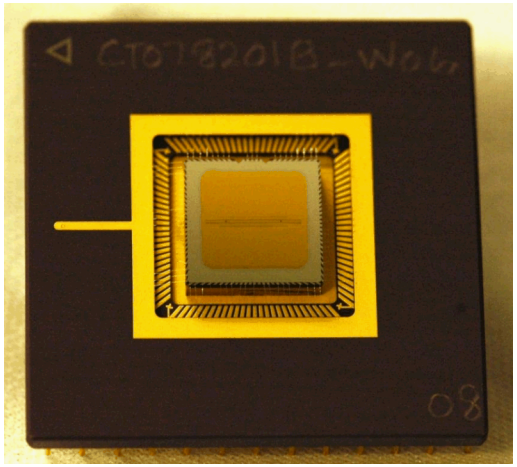




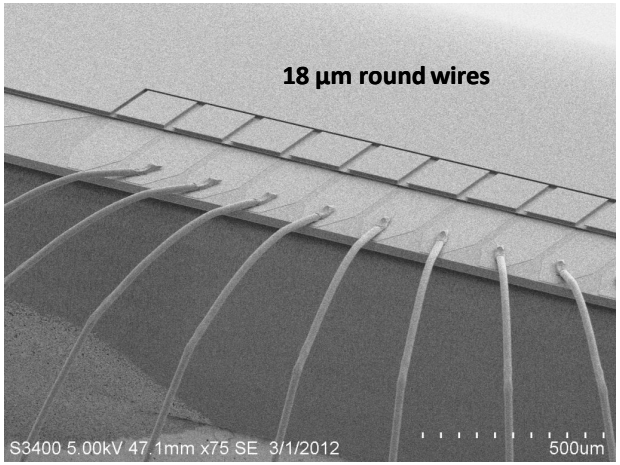


Packaging and testing

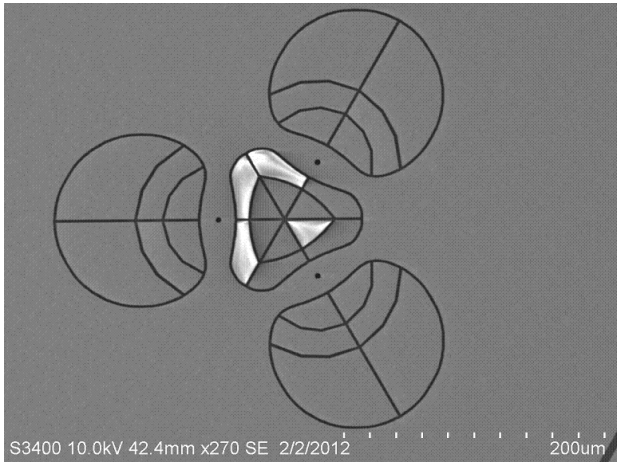
Plug-and-trap design

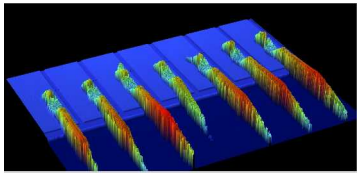


Low profile wirebonding



Parametric verification





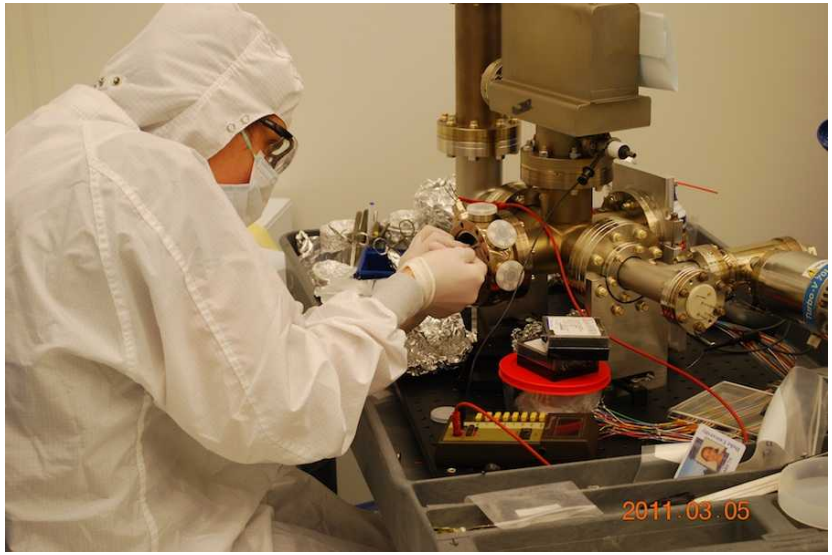
Features:

- Plug-and-trap design:
  most trapping groups can accommodate the package
- Standard for chip ion traps
- Low profile wirebonds: good optical access
- Checks for opens and shorts > 40 MΩ

working with chip traps
the details

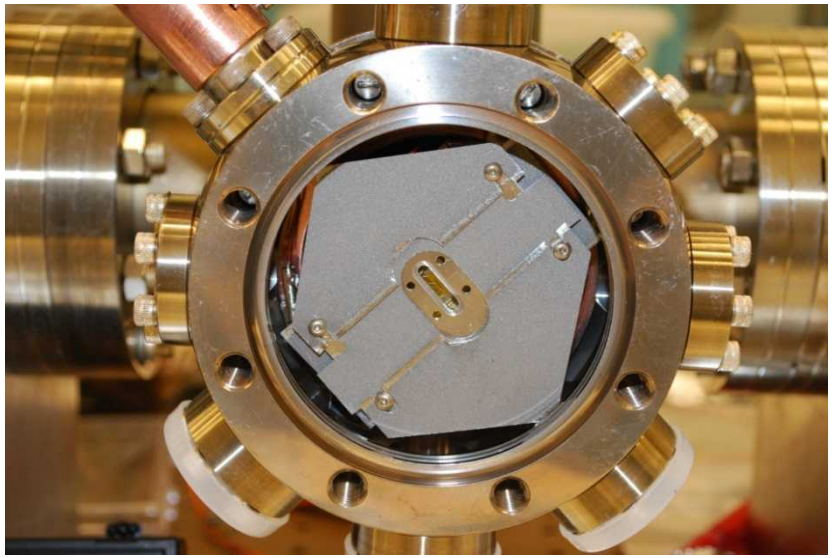
Dust-free handling of trap chips

- shorts and voltage breakdowns
- dust particles can charge: unreliable conditions



Ultra high vacuum

- helps realizing good trapping times
- lifetimes without cooling >20min
- Clean and absolutely grease-free handling of components
- NEG



Optical beam quality

- optical access is smaller
- optimal beam quality is essential to prevent scatter

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Surface Ion Traps for QIP

Optimizing surface traps for QIP

Challenges:

- Geometry and optical access:
  - Individual addressing
  - Resonant excitation for remote entanglement
  - Quantum gates with Raman beams
- Trap parameters
  - Trap frequencies > 2MHz (Yb) facilitate ground state cooling and quantum gates
  - Low residual micromotion for photon generation and quantum gates

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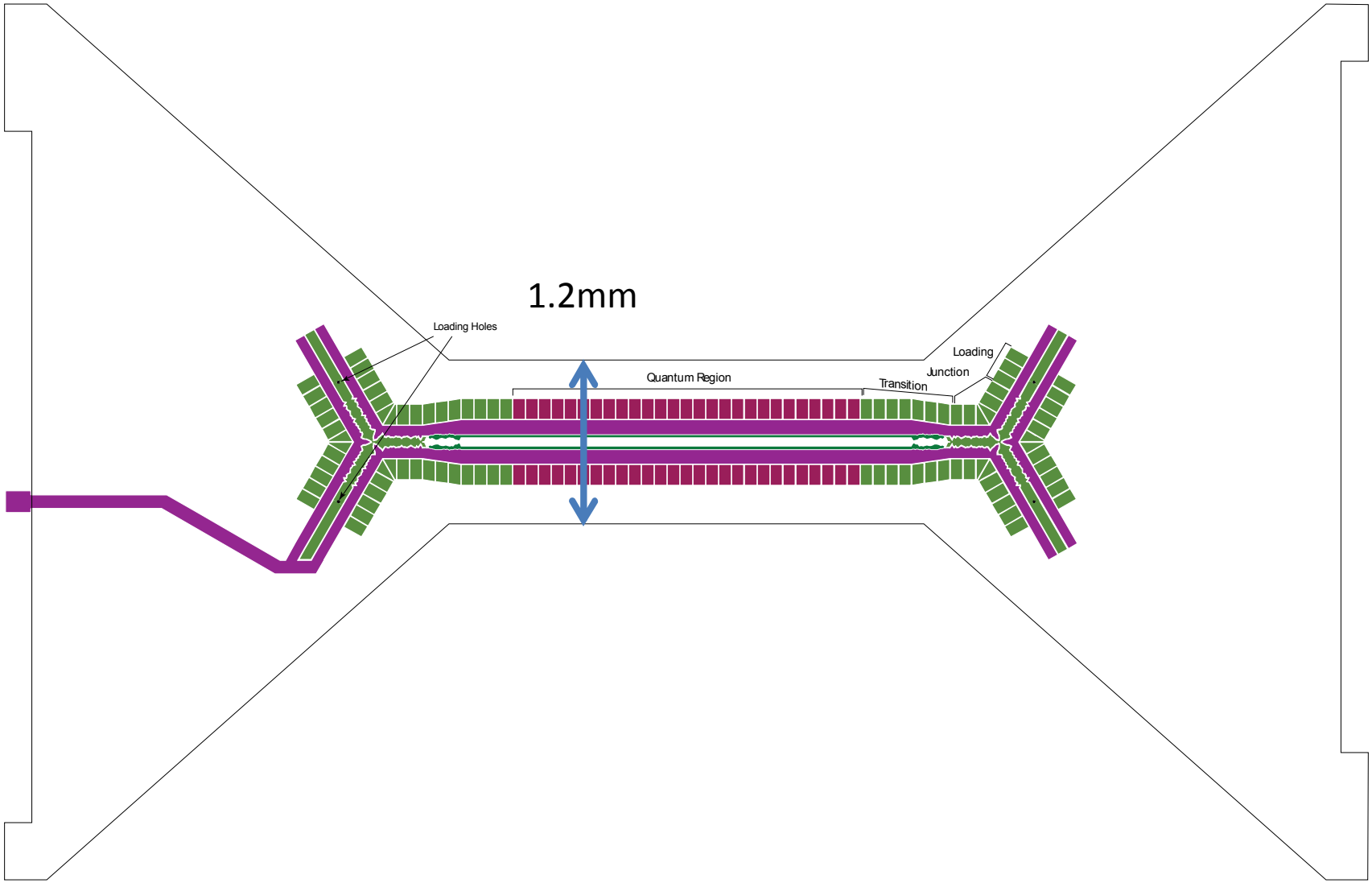
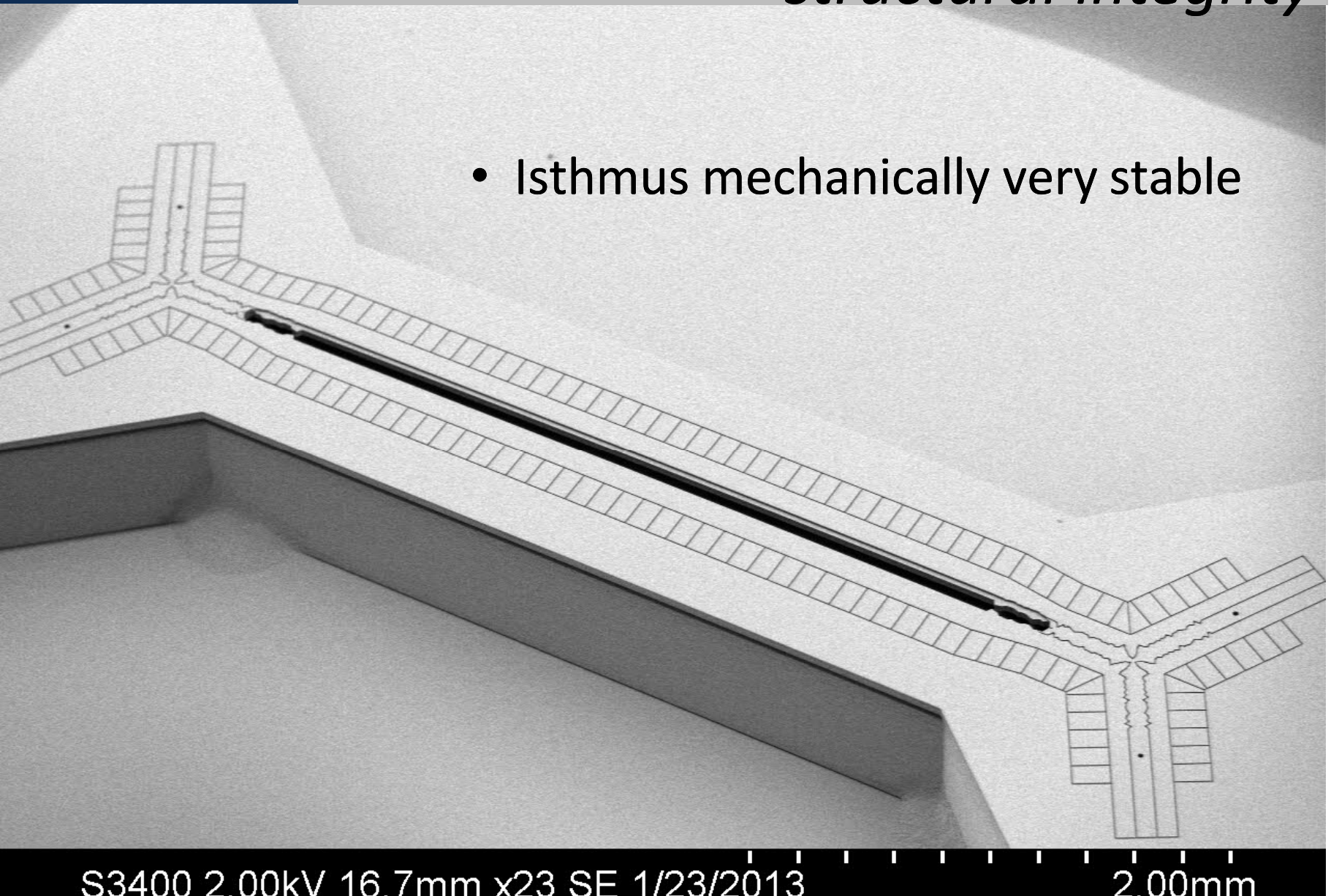
Schematic



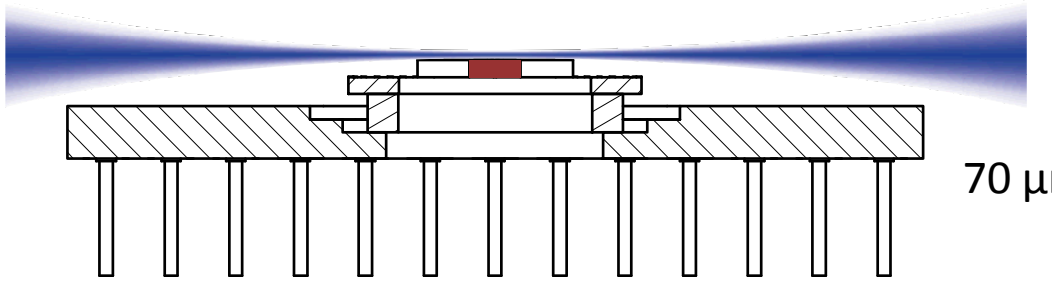
Bowtie trap

structural integrity

- Isthmus mechanically very stable

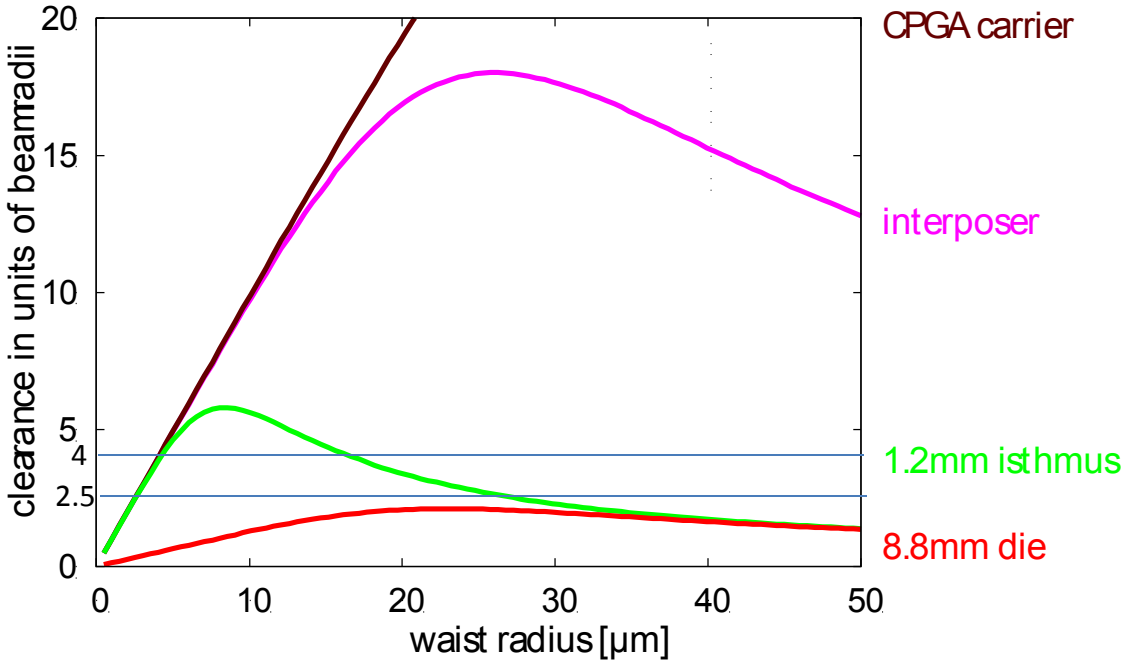


High Optical Access trap
beam clearance



70 µm ion height

clearance for a surface skimming beam



4: $<2\times10^{-14}$

3: $<2\times10^{-8}$

2.5: $<3\times10^{-6}$

4 µm waist is possible

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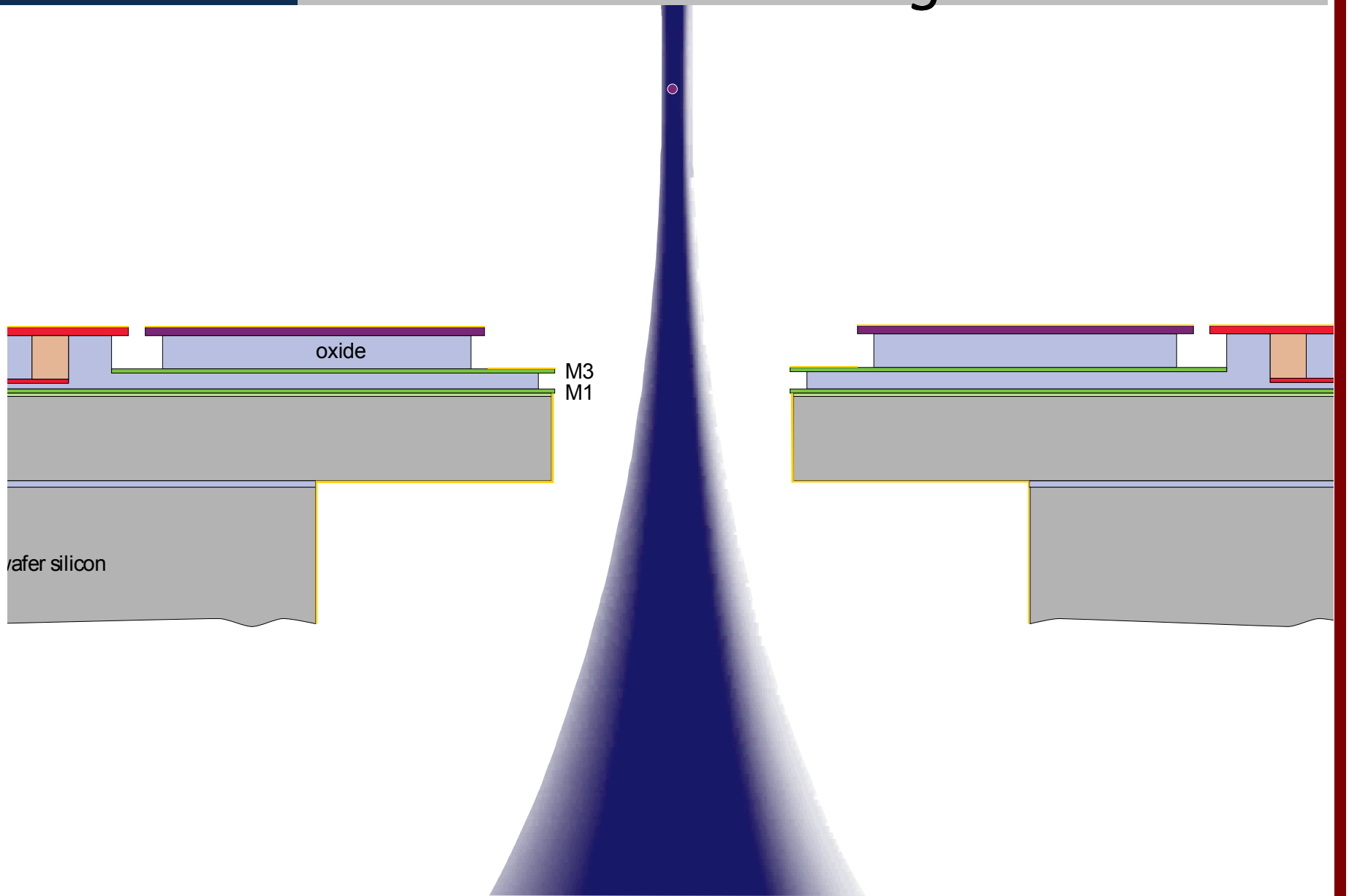
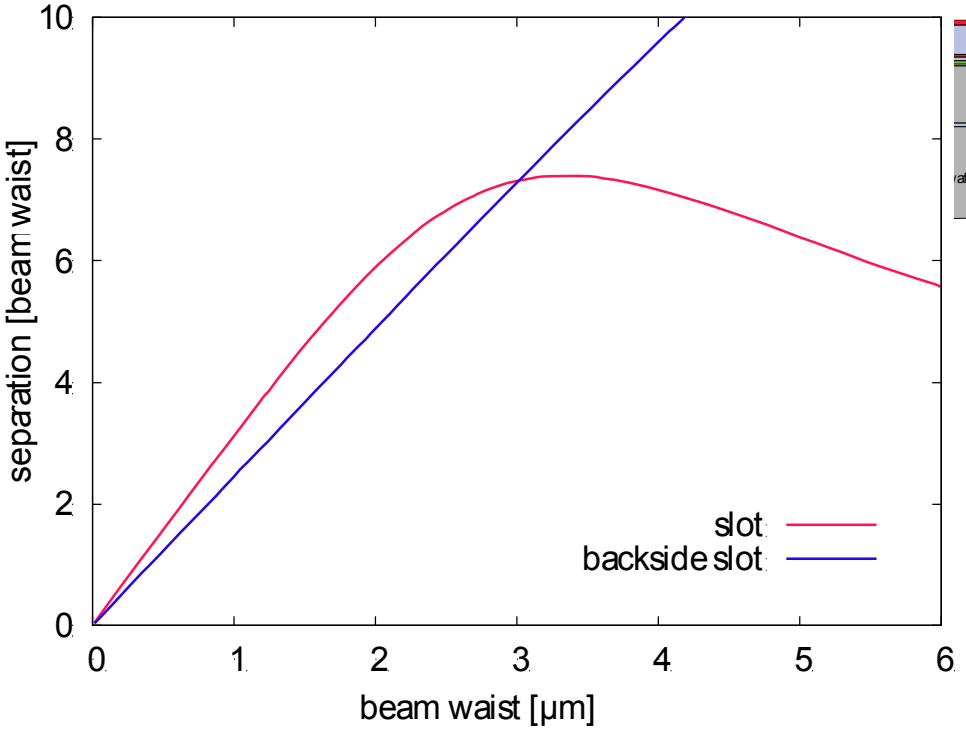
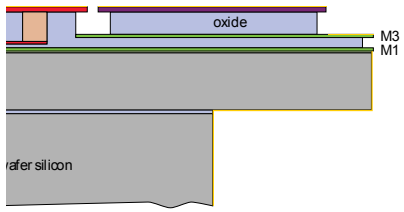
Optical access
through central slot

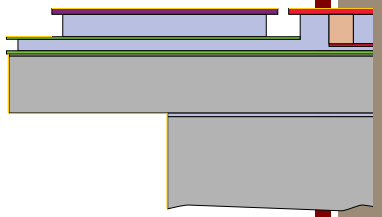


Optical access
through central slot

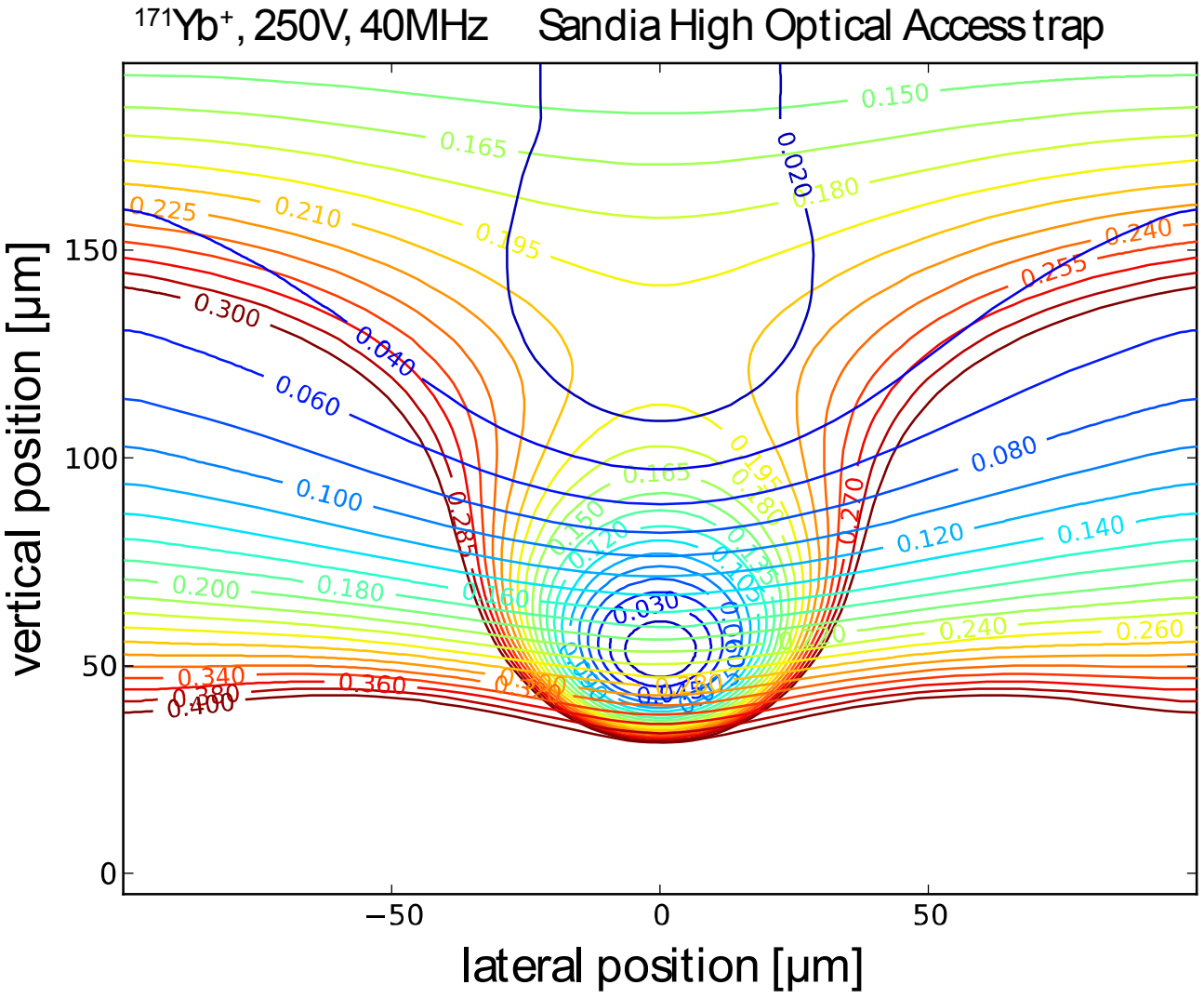
Clearance of vertical beam







Trap parameters



$$V = \frac{q^2 E_0^2}{4m\Omega^2}$$

$$V_{\text{trap}} = 200\,\text{meV}$$

$$\eta = 2q\frac{|\nabla E_0|}{m\Omega^2}$$

$$\eta_{\text{center}} = 0.22$$

$$\eta_{\text{max}} = 0.38$$

Thunderbird:

$$V = 50\,\text{meV}$$

$$\eta_{\text{center}} = 0.1$$

$$\eta_{\text{max}} = 0.22$$

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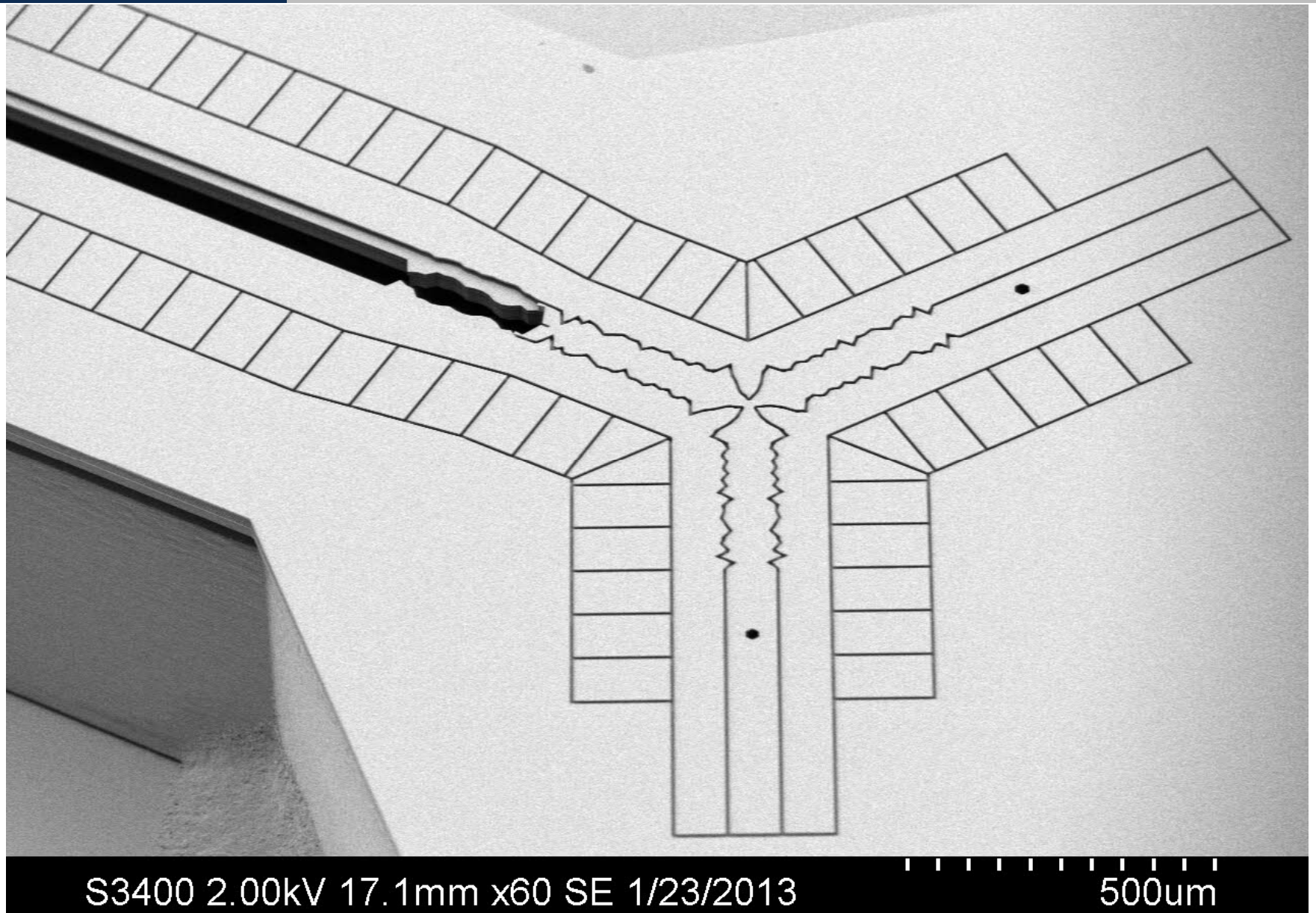
Geometry optimization

linear section



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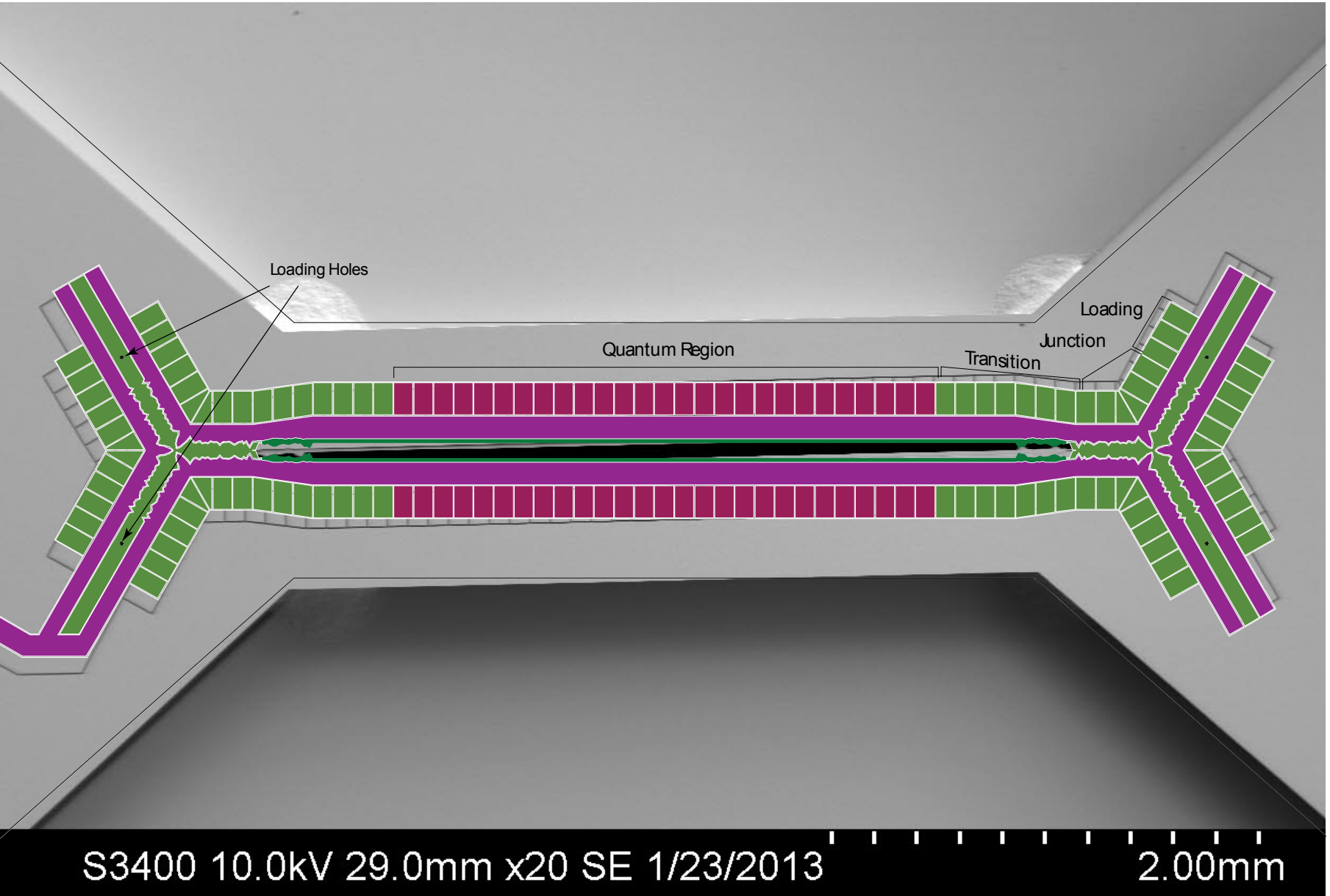
Schematic



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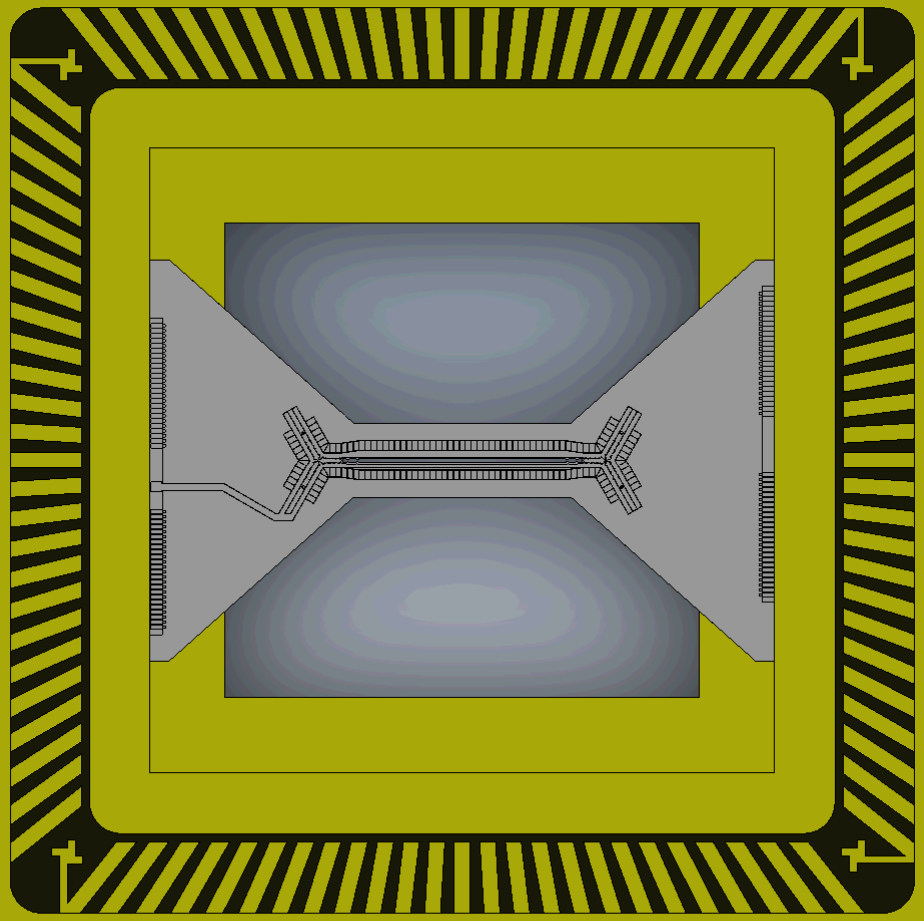
Interposer



- Connections to package
- Unobstructed optical access

Interposer also serves:

- Filter (rf shunt)
- RC filter
- Universal from future and existing traps

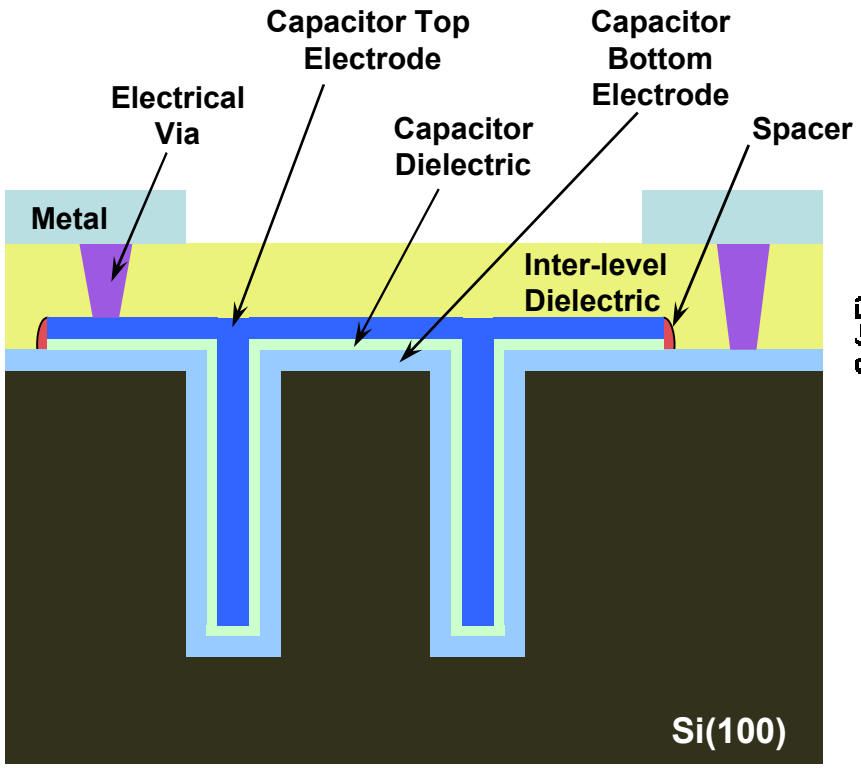
Integrated Trench Capacitors

Trench v. Surface Capacitors for Surface Ion Traps

- **High-k dielectric surface areas: still large**
- **Thin dielectric challenges: yield, reliability**
- **Vertical surfaces: more available area**

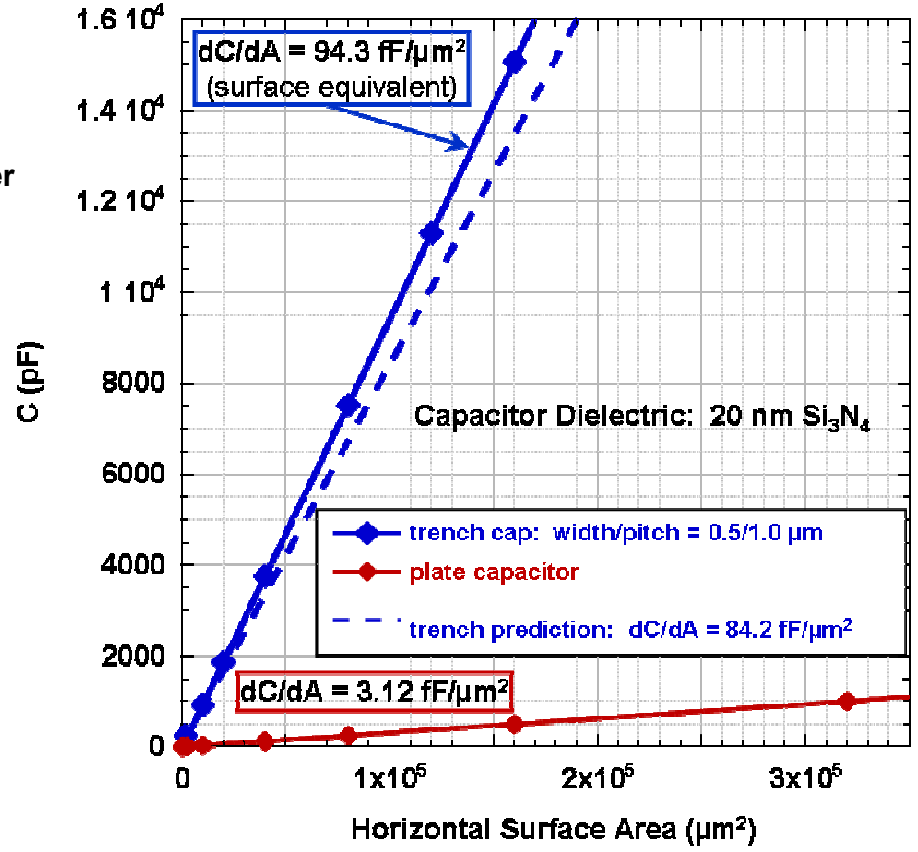
ATC 116 Series Microcaps
Surface mount: 1.27 x 1.27 mm², 821±20% pF

Trench Capacitor Architecture



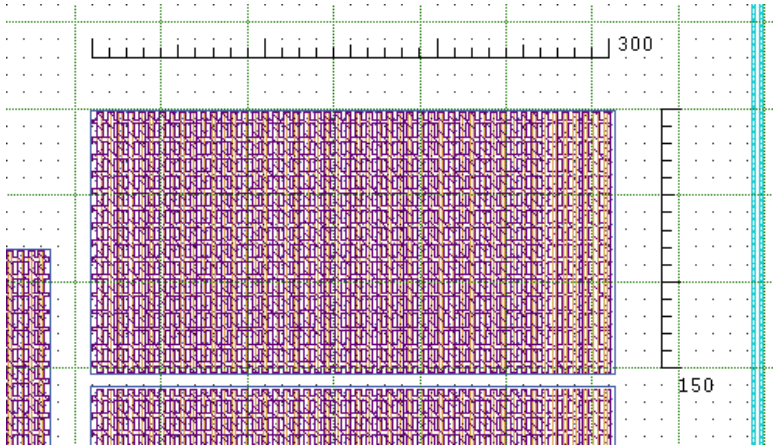
D.T.C. Allcock, *et al.*, Appl Phys B (2012) 107:913-919

Area relationship for trench v. horizontal plate capacitors

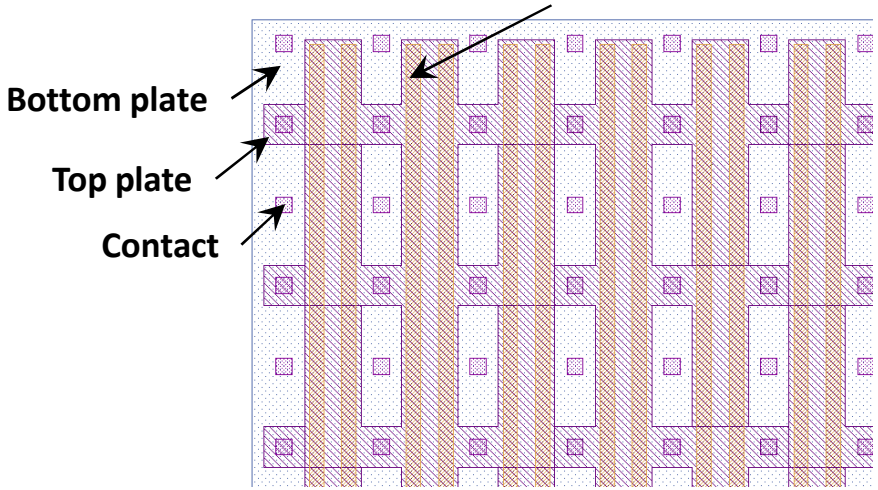


Integrated Trench Capacitors

1.05 nF trench cap, 0.045 mm^2/cap



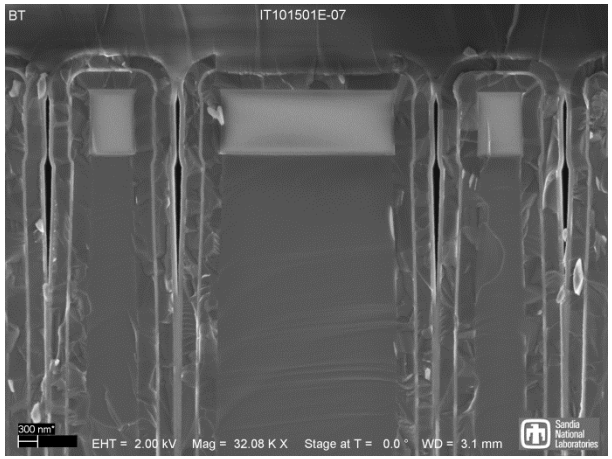
Trenches: 1 µm wide, 150 µm long, 19 µm deep



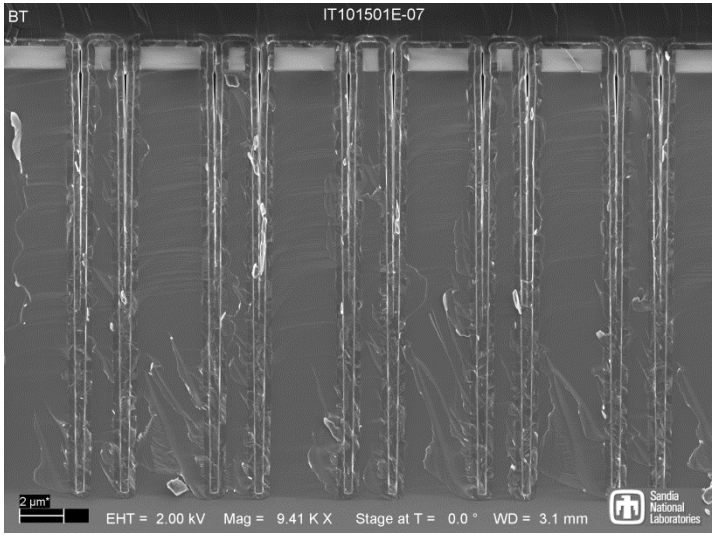
Top plate: 250 nm n-type a-Si

Dielectric: 40 nm Si_3N_4

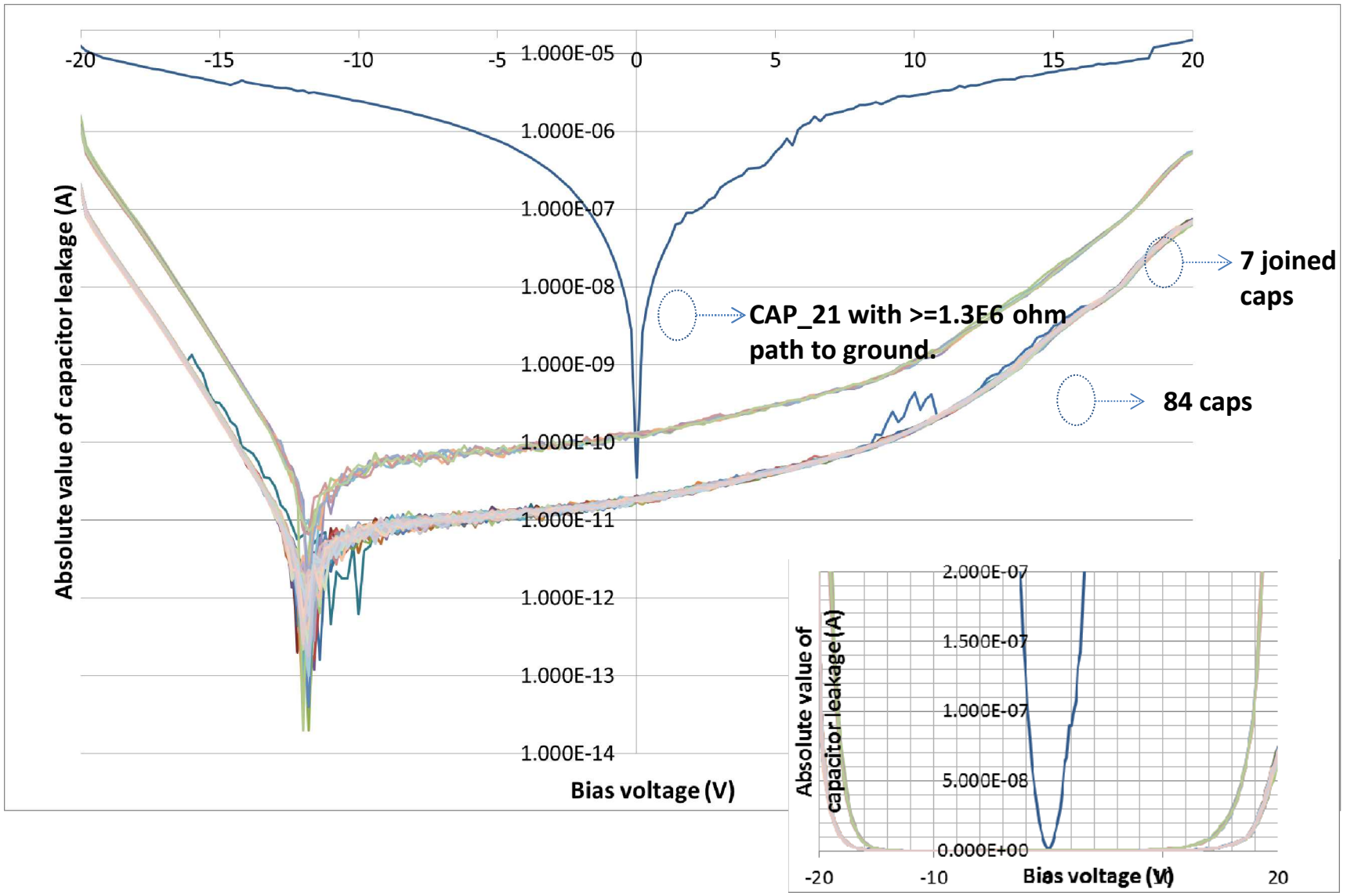
Bottom plate: 300 nm n-type a-Si



19 µm



Integrated Trench Capacitors
Capacitor I-V leakage



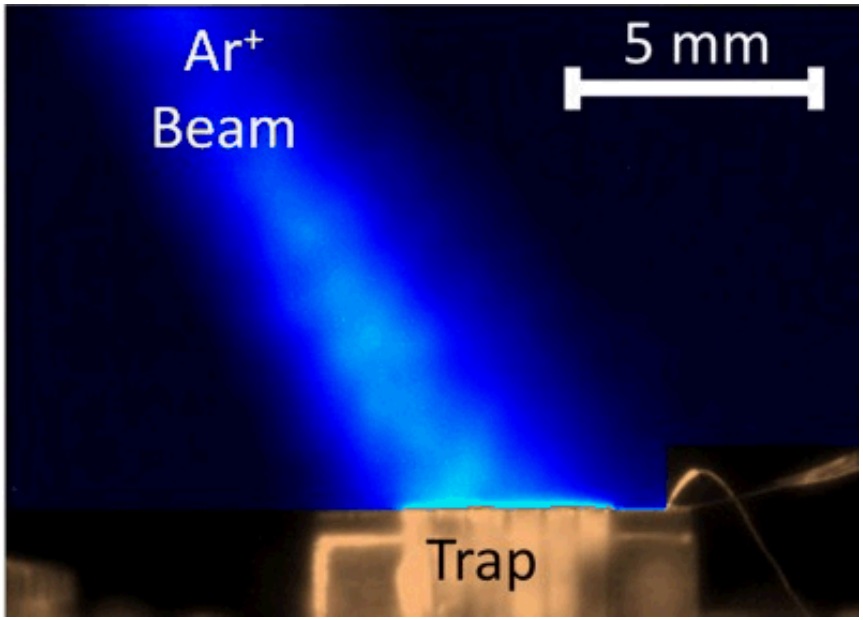
Anomalous heating in surface traps
and how to fight it

Problem:

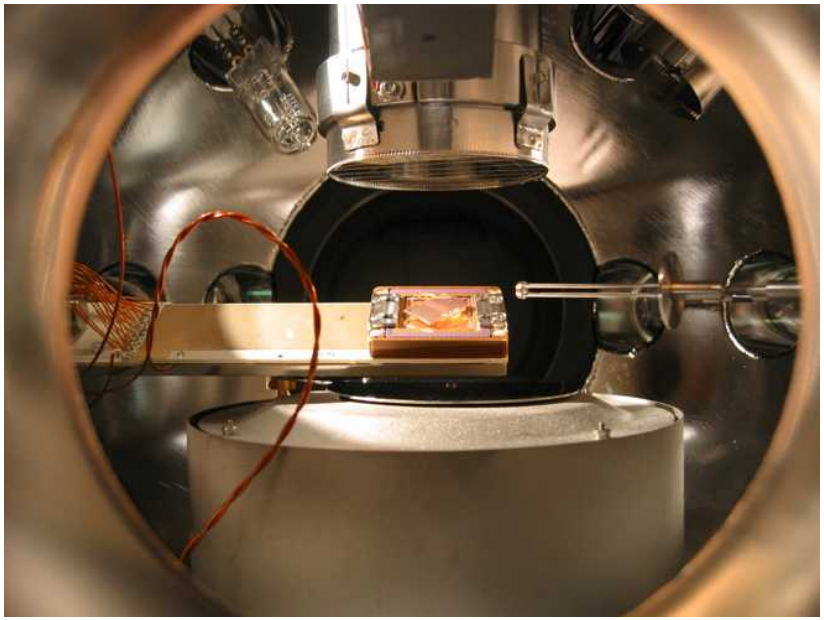
- Anomalous heating in ion traps $\propto d^4$
- Due to electrical flield noise of patch potentials

Remedies:

- Operate at Cryogenic temperatures
- Surface cleaning



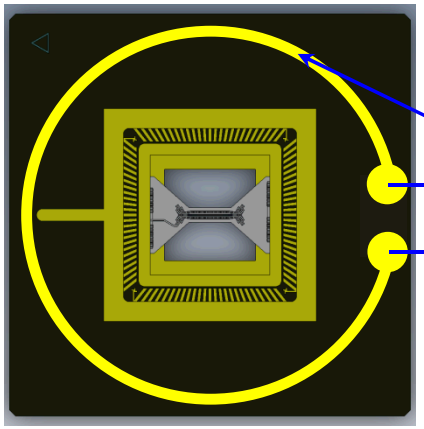
D.A. Hite et al. *PRL* **109**, 103001 (2012)

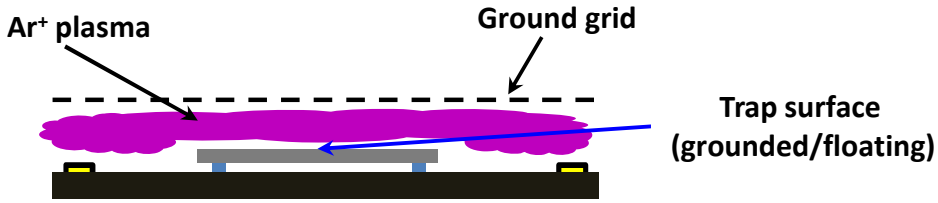


H. Häffner et al., UC Berkeley

Ion Trap Chip Packaging
surface cleaning

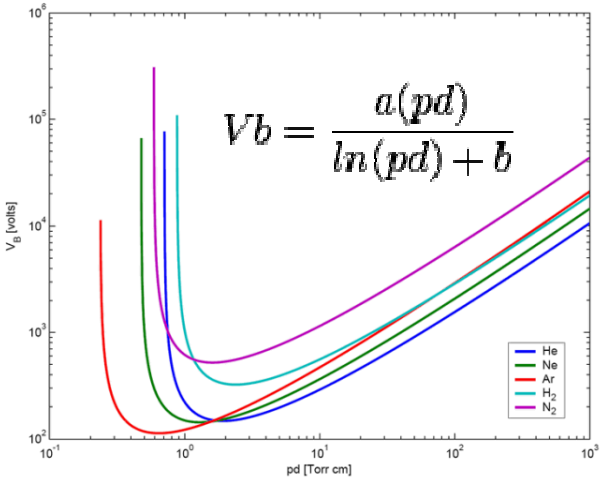
Is *in situ* Ar plasma trap cleaning feasible? One possible implementation





Energies should stay below sputter thresholds of trap materials

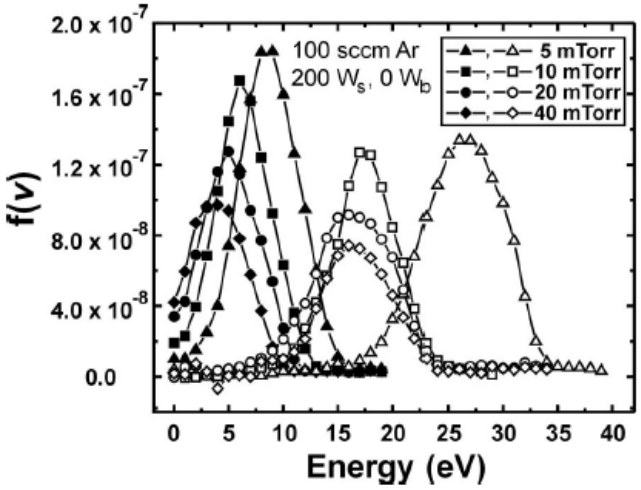
Can a micro-plasma be established in such a small place?



Paschen Curve for inert gases:
Ar: 10 Torr, 100 V, 1 mm

Inductively coupled plasmas: control of ion energies.

- **Surface adsorbate bond energies ≤ 12 eV**



M.G. Blain, *et al.*, Appl. Phys. Lett., 75 3923 (1999)

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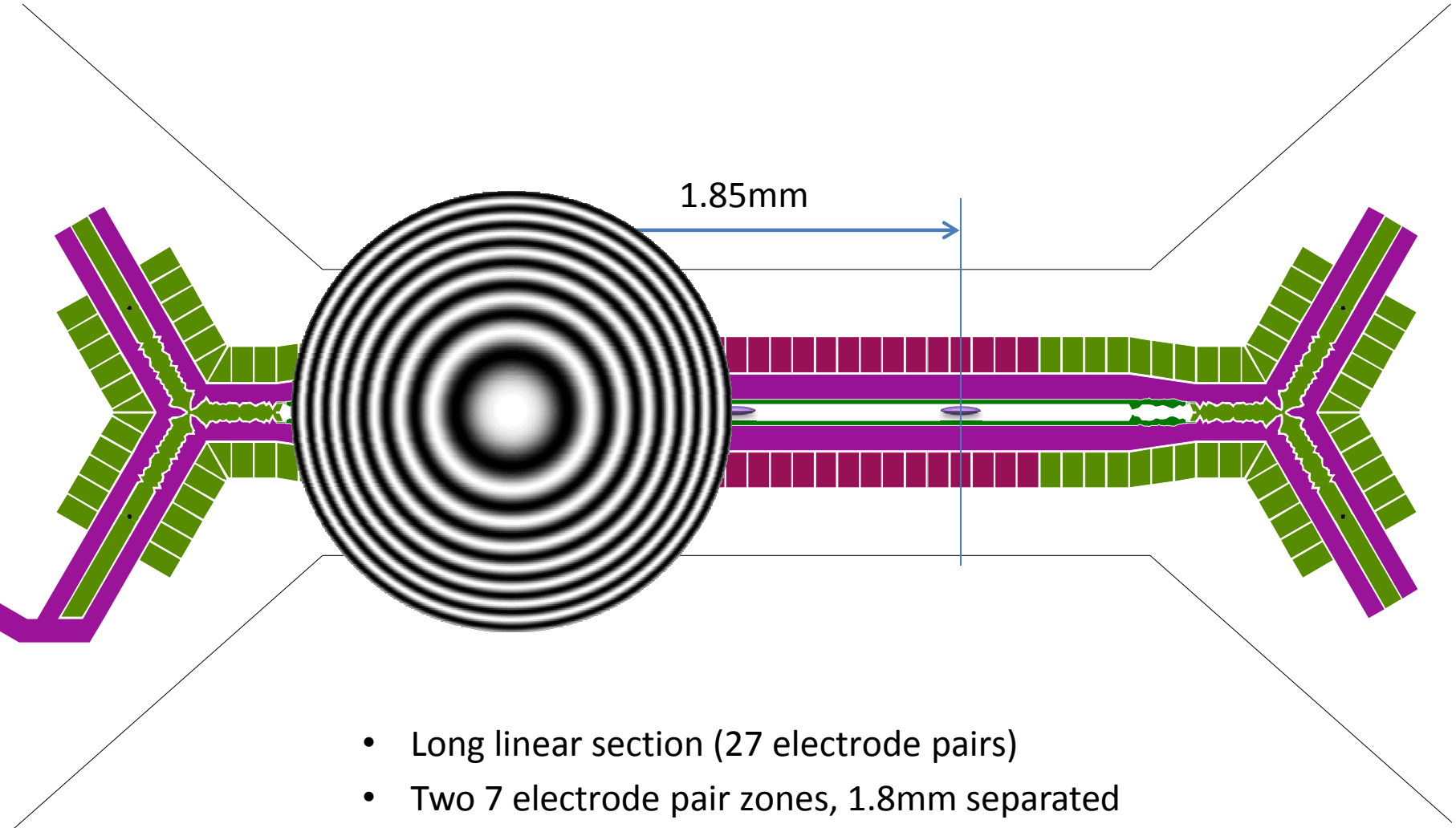
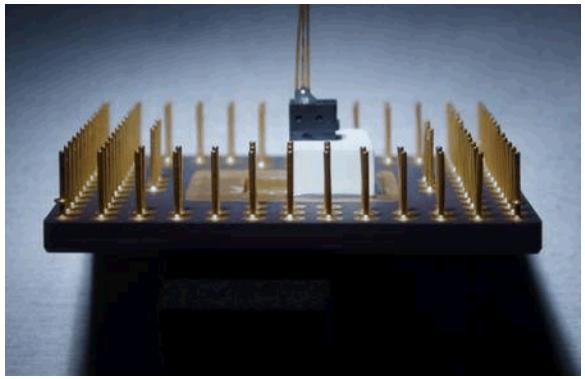
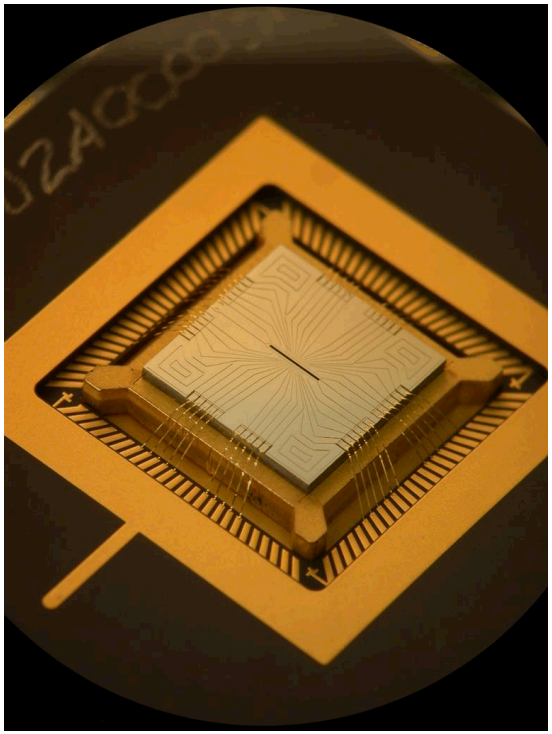
MUSIQC architecture



- Long linear section (27 electrode pairs)
- Two 7 electrode pair zones, 1.8mm separated
- Integrated optics can be used for separate imaging

Surface Ion Trap Packaging

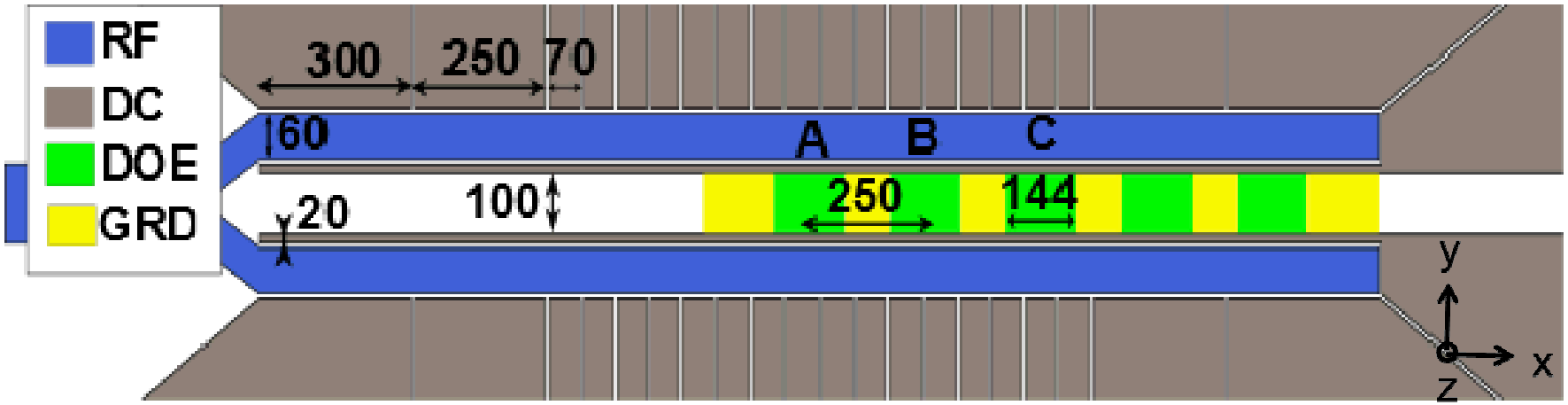


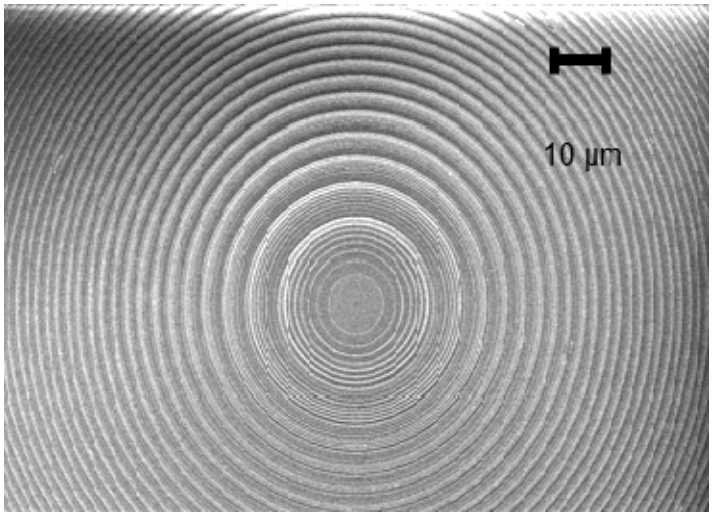


- **Package Requirements**
- **(Ion optical access/optics integration)**
- **Interposers and through substrate vias (TSVs):**
  - **“2.5D” integration**
- **Integrated capacitors**

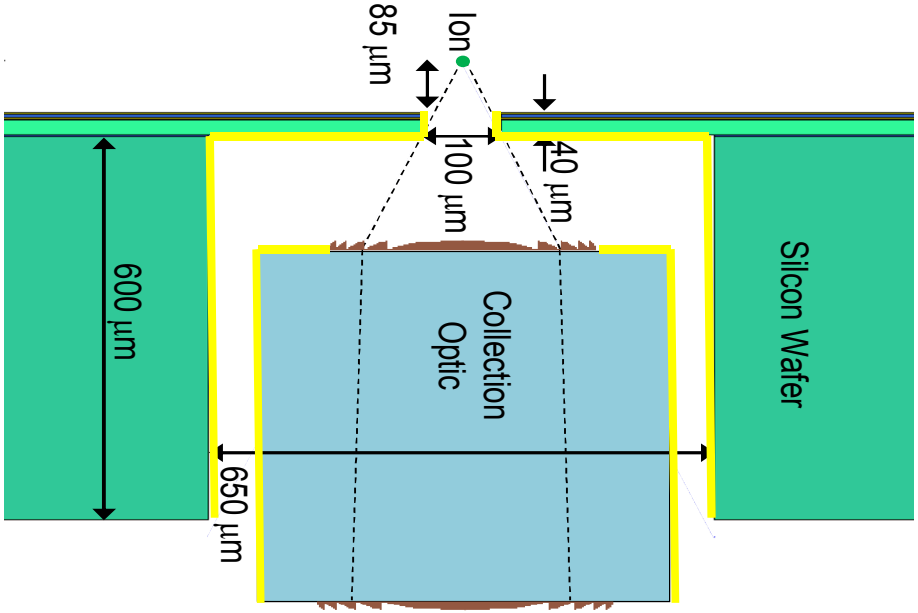
Thunderbird Trap

with integrated diffractive optic

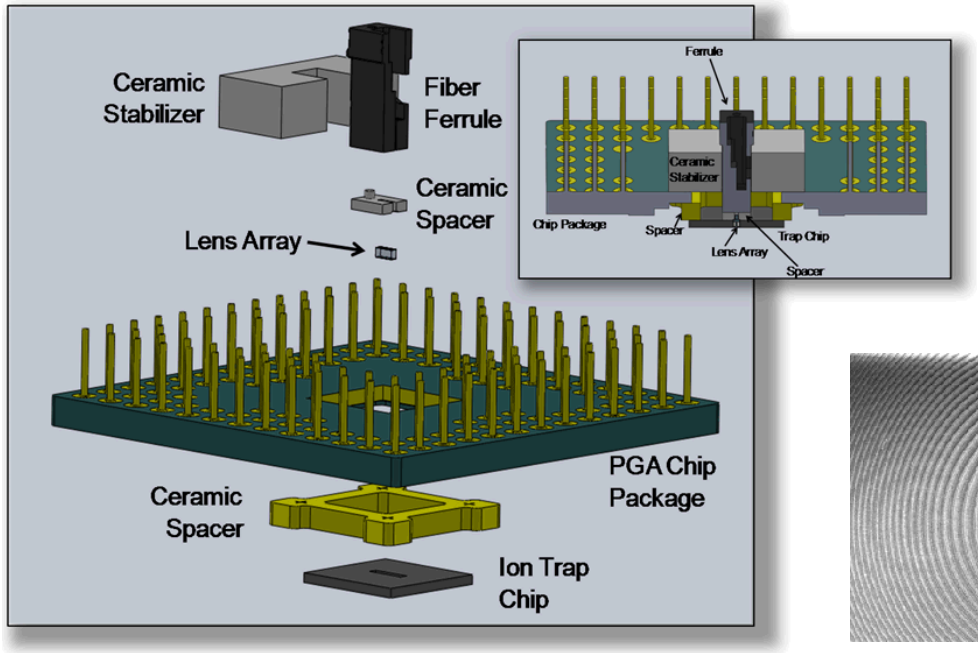


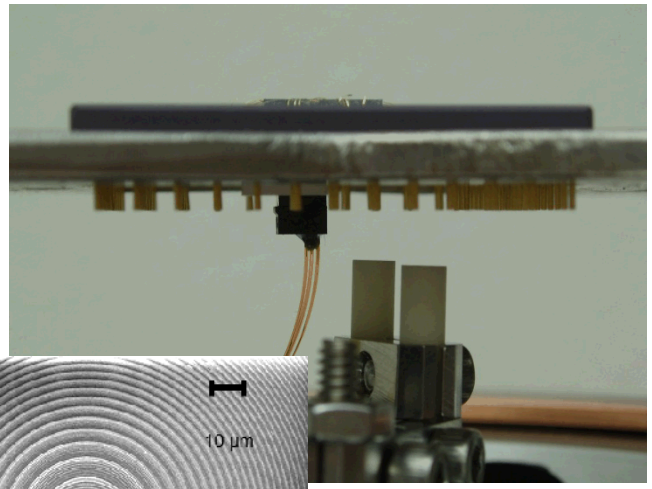


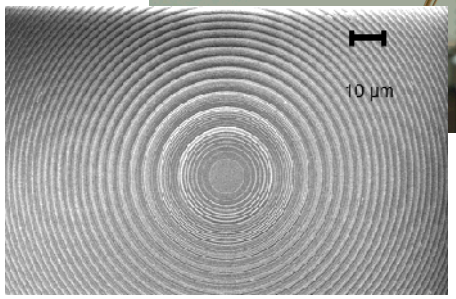
Eight level F/1 fused silica DOE



Integrated Optics

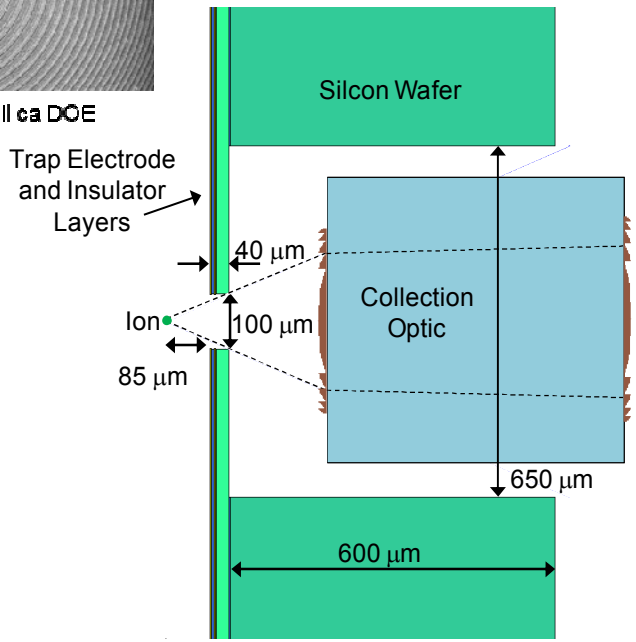






Eight level F/1 fused sil ca DOE

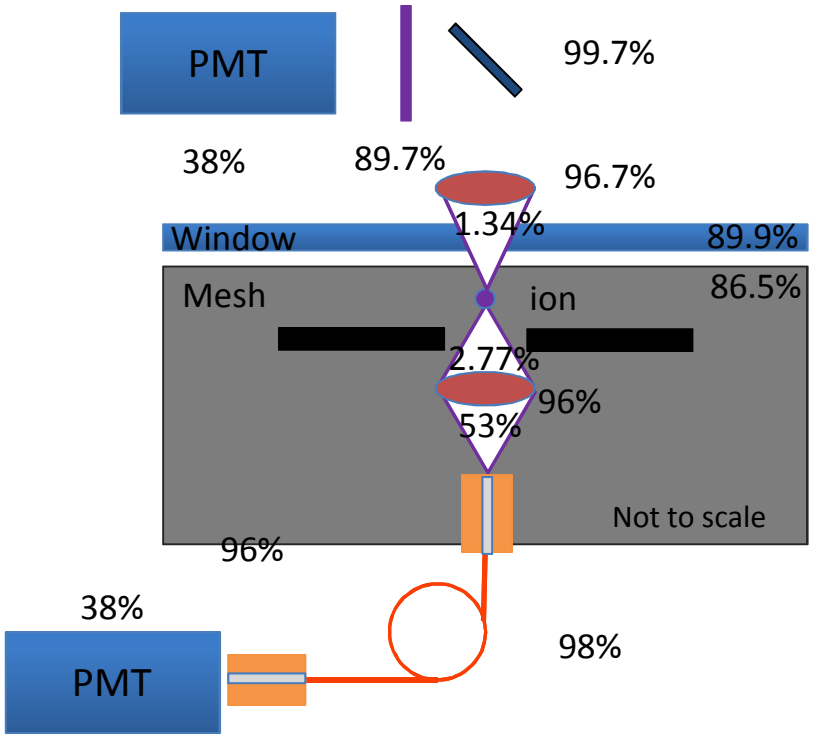
- **Optics have been integrated into linear ion trap.**
- **No detrimental effects to ultra-high vacuum.**
- **Successful shuttling with same voltage solutions as linear trap without integrated optics.**
- **Compensated any charging on dielectric lenses.**
- **Dielectric lenses ~150 microns away from ion.**



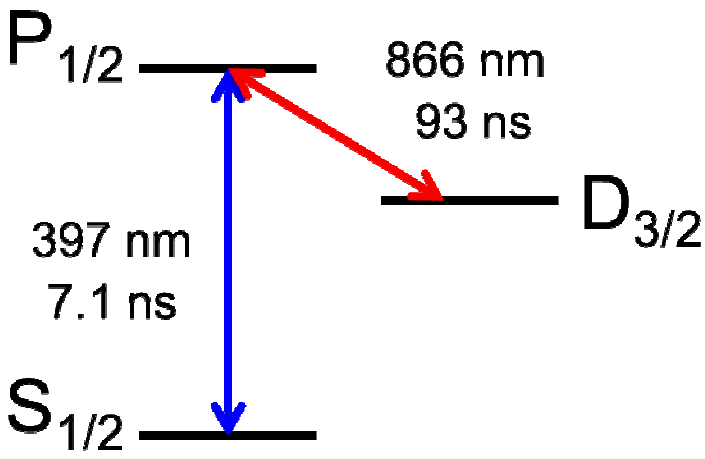
G. R. Brady, *et al.* Appl. Phys. B: Lasers and Optics 103, 801-808 (2011).

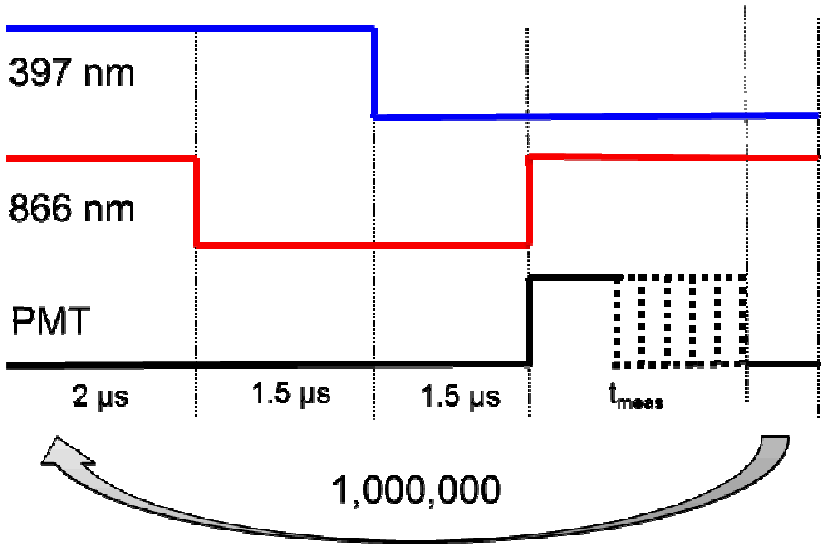
Light collection performance

DE_{fs} = 0.34%



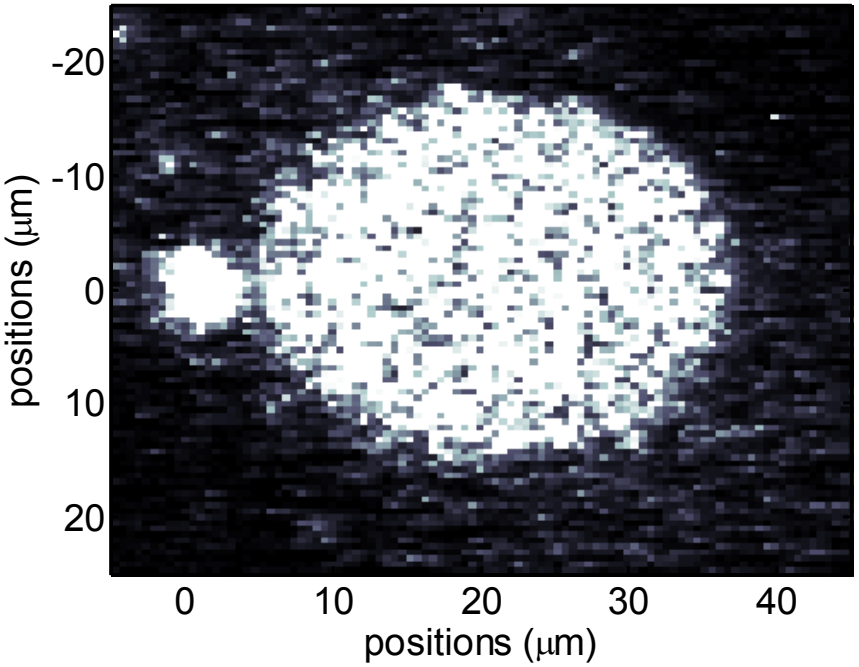
DE_{DOE} = 0.50%





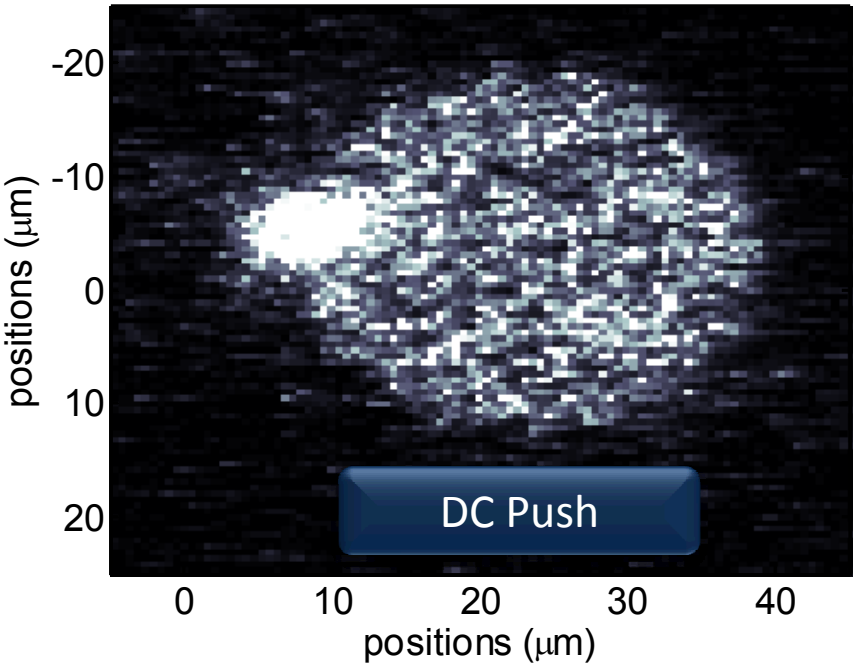
Detection measurements

DE_{fs}=0.341%



DE_{DOE}=0.023%

DE_{fs}=0.315%



DE_{DOE}=0.236%

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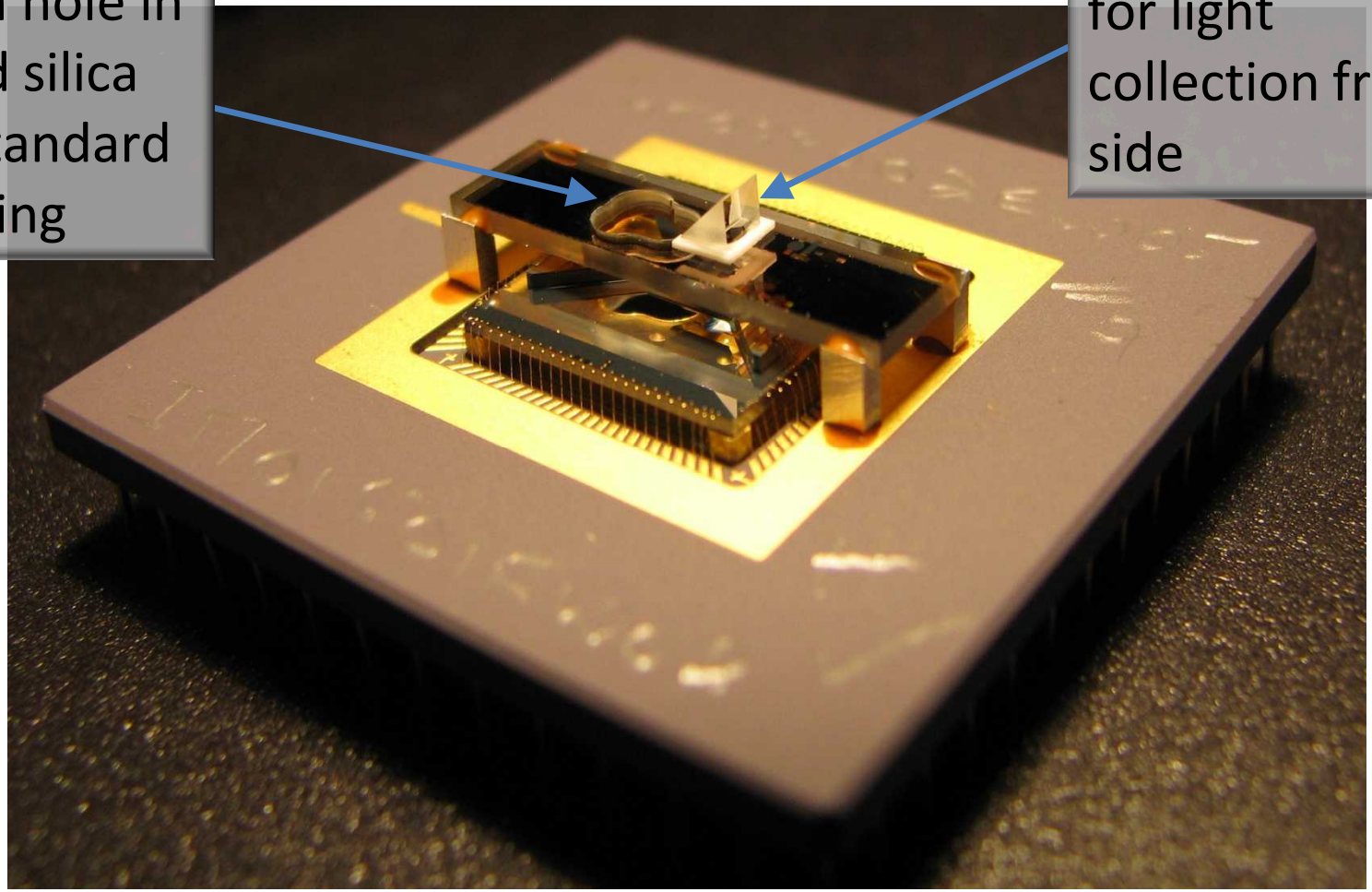
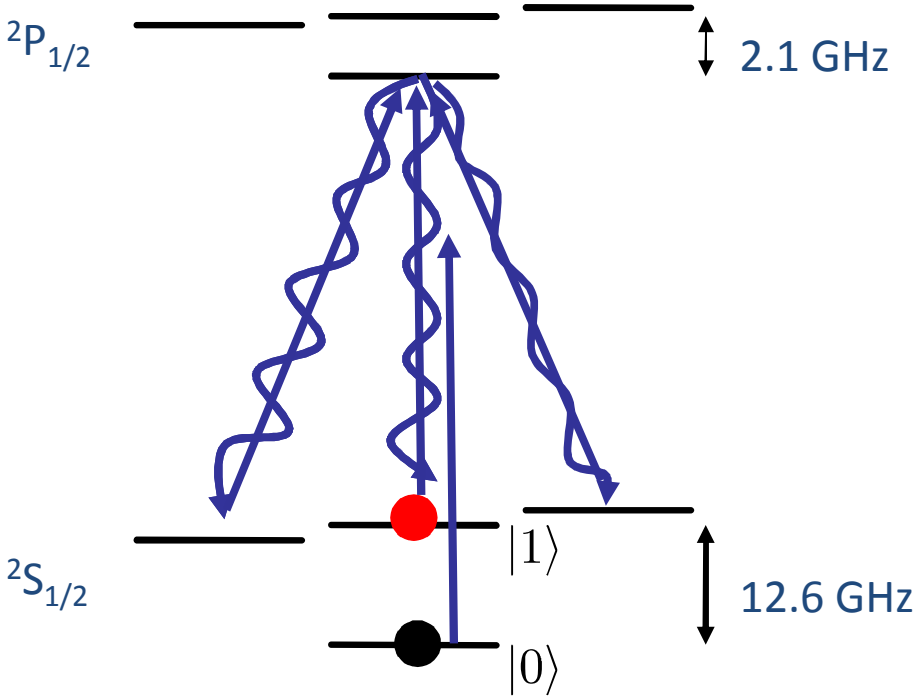
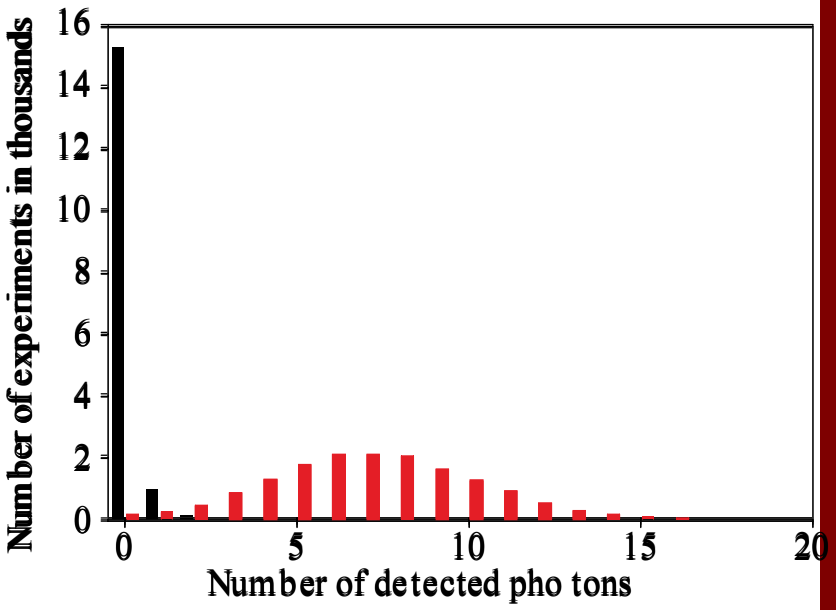
HOA + optic



Quantum State preparation and detection





- State detection fidelity >97%
- will be optimized further
- Expecting >98% fidelity

S. Olmschenk *et al.*, PRA **76**, 052314 (2007)

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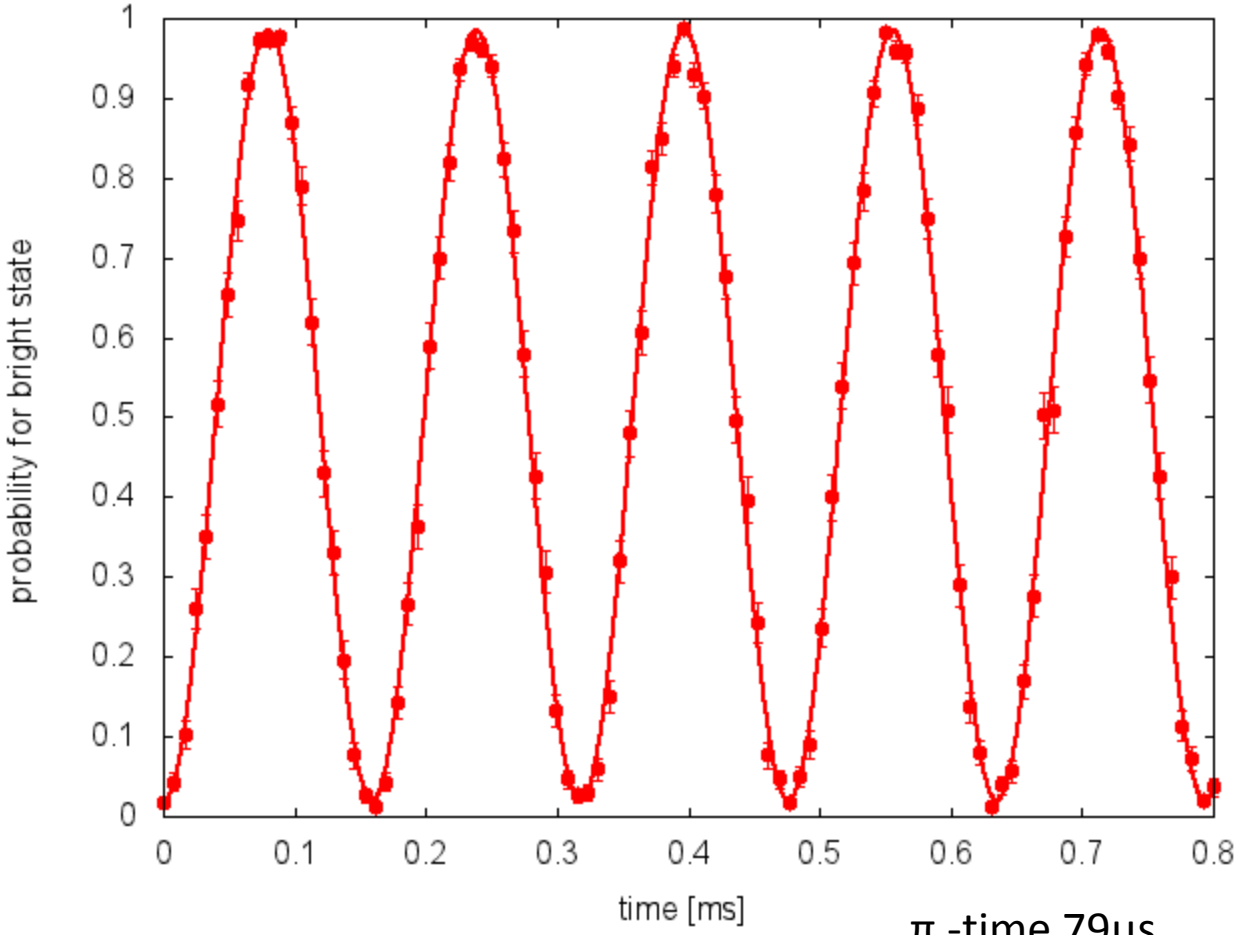
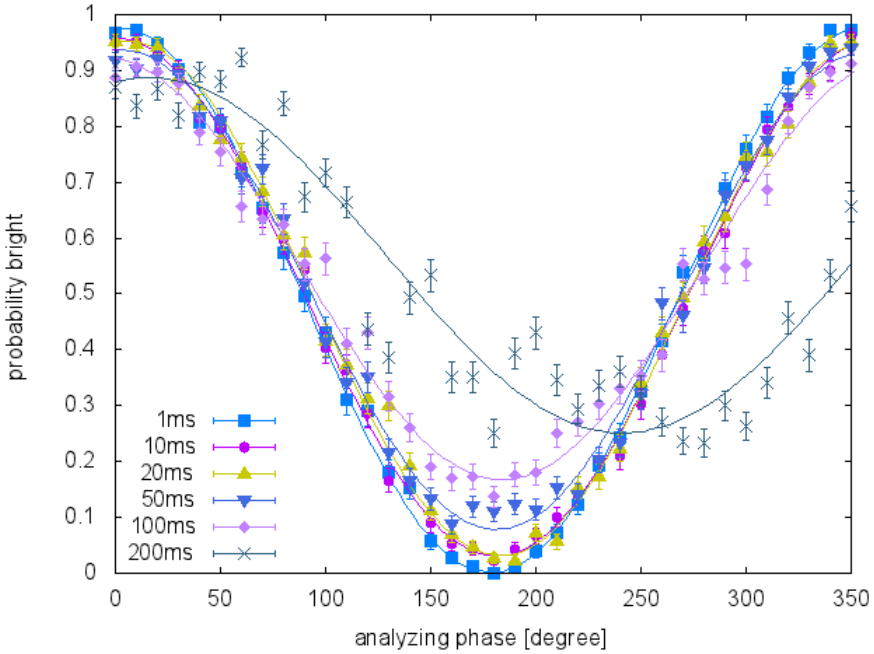
Single qubit manipulations

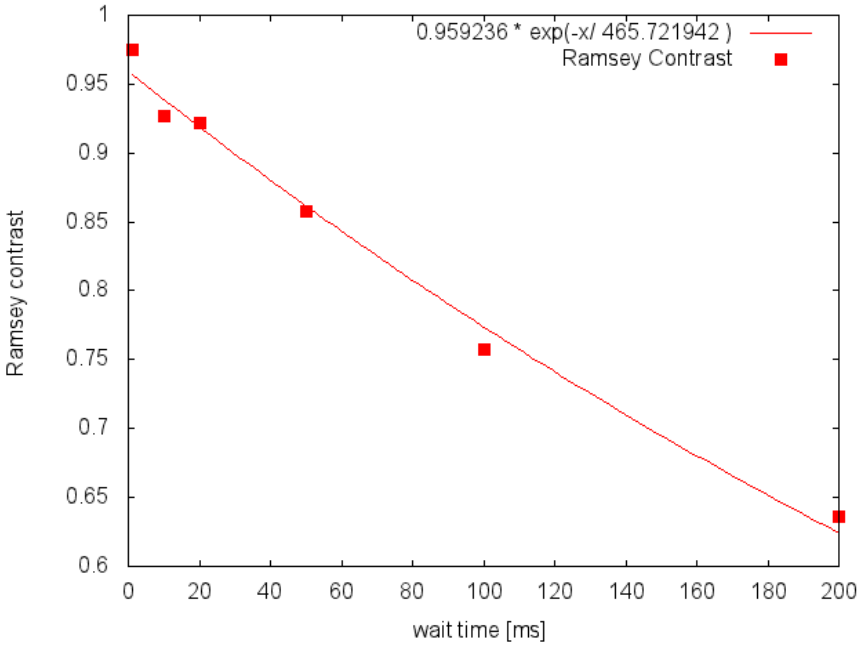
Rabi flopping



π -time 79μs

Single qubit manipulations
Coherence time



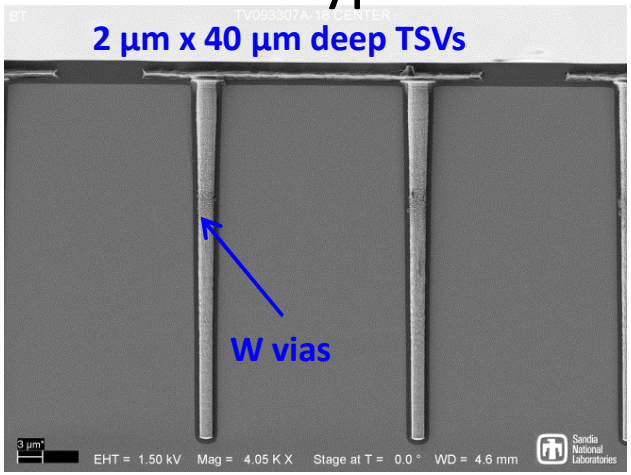


- Coherence time approx 400ms (expected >1s)
- Coherence time is currently limited by light leaking through the switches
- Verified that leaking light can be reduced by 30dB with additional single mode fiber
- System is upgraded, new measurement to follow this month

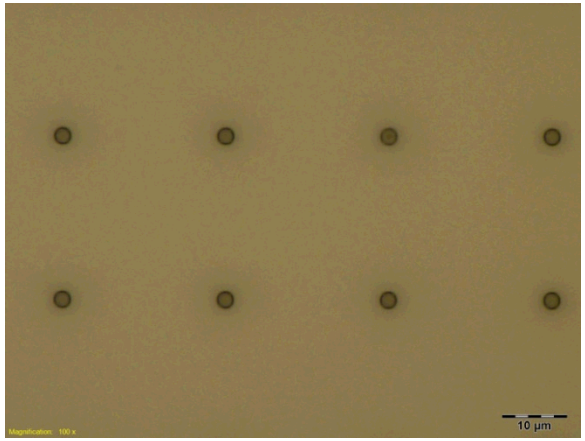
Outlook: future technologies

through substrate vias

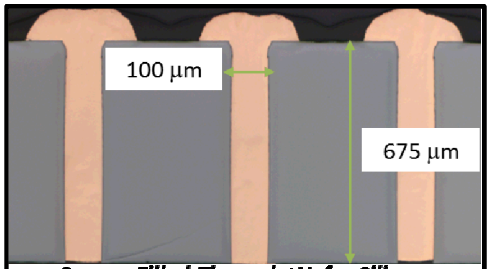
Types of through substrate vias: Cu and W



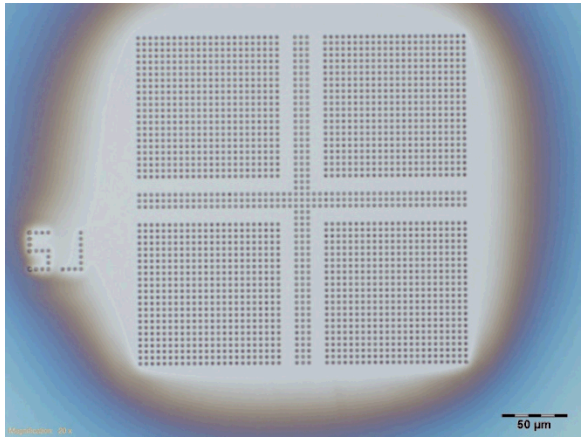
- Bond front to handle
- Backgrind to 75 µm
- Dry etch to reveal TSVs

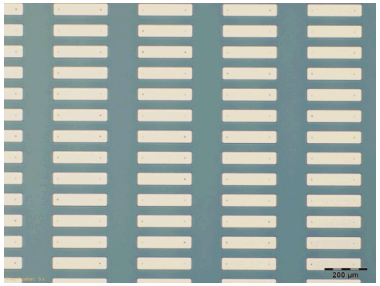


- Si recess
- PECVD oxide
- CMP

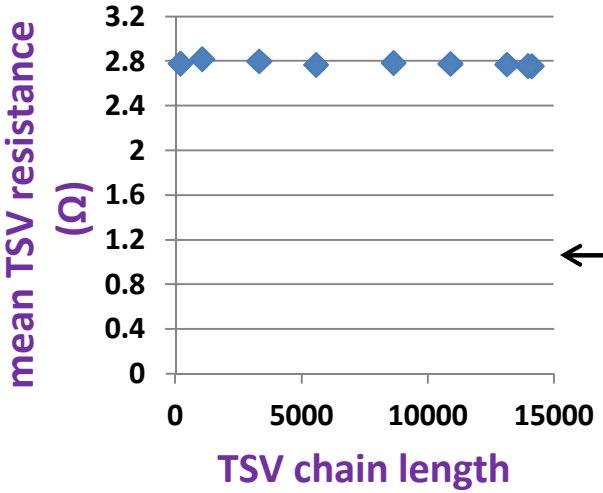


Copper Filled Through Wafer Silicon Vias





- Pattern metal



Acknowledgements

Funding

UNM

Collaborators

MUSIQC

CQuIC

Georgia Tech Research Institute
Problem. Solved.

MICHIGAN

The University of Sydney

WASHINGTON

Sandia National Laboratories

Pictures of traps