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CRADA Final Report
For
CRADA Number NFE-11-03404

Simulink/PARS Integration Support

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Abstract

The state of the art for signal processor hardware has far out-paced the development tools for placing applications on that hardware. In addition, signal processors are available in a variety of architectures, each uniquely capable of handling specific types of signal processing efficiently. With these processors becoming smaller and demanding less power, it has become possible to group multiple processors, a heterogeneous set of processors, into single systems. Different portions of the desired problem set can be assigned to different processor types as appropriate. As software development tools do not keep pace with these processors, especially when multiple processors of different types are used, a method is needed to enable software code portability among multiple processors and multiple types of processors along with their respective software environments.

Sundance DSP, Inc. has developed a software toolkit called "PARS", whose objective is to provide a framework that uses suites of tools provided by different vendors, along with modeling tools and a real time operating system, to build an application that spans different processor types. The software language used to express the behavior of the system is a very high level modeling language, "Simulink", a MathWorks product.

ORNL has used this toolkit to effectively implement several deliverables. This CRADA describes this collaboration between ORNL and Sundance DSP, Inc.

Statement of Objectives

The purpose of this CRADA is to advance the state-of-the-art in model-driven engineering through development of software tools.

ORNL's Software Defined Radio program, as a seasoned user of model based design tools, is very familiar with the limitations of the current state of the art of these tools as well as with ways to adjust the PARS framework to more effectively use these tools.

The goal of this project is to expand the types of processors that can be used with the PARS framework to include new types of processors such as multi-core CPU and Graphics Processor Units (GPU), new variants of Digital Signal Processor (DSP) and Field Programmable Gate Array (FPGA), as well as different communication links as appropriate and available on these processors. The benefits of this project are to streamline the (tedious) process of software and firmware development for heterogeneous multi-processing systems and enable scientists to generate trustworthy and functional systems from Simulink models.

The desired result is to achieve an integrated PARS framework that generates software/firmware for both Sundance DSP, Inc. supplied hardware as well as industry-standard hardware such as commodity multi-processor servers and application accelerators.

Benefits to the Funding DOE Office's Mission

The Ubiquitous High Performance Computing 2010 BAA [1] set a goal of 50GFlops/W (0.02 W/GFlop, pg. 17) for the HPL benchmark for a proposed system. Heterogeneous computing addresses the needs of these requirements:

"1) development and optimization of Extreme-Scale architectures, technologies, execution models, and the critical co-design of hardware and software; 2) low-energy architectures and protocols for logic, memory, data access, and data transport; 3) dynamic systems that adapt to achieve optimal application execution goals..." The International Exascale Software Roadmap [2] listed software tools for such architectures in its 2011 milestones. OMB Memorandum M-10-30, R&D on advanced vehicle technologies, particularly ***modeling and simulation***..." [emphasis added]. This research supports modeling and simulation efforts by enabling informed choices regarding the construction and selection of computing systems for these programs. As we described in our publications [3][4] prior to the establishment of this CRADA, such a framework can be used for incorporating arbitrary new computation architectures into high performance multiprocessor systems of interest to the DOE and DOD.

We envision a future capability in which **scientists and modelers** define a specification for a very large-scale sensor network and control system in a high- level modeling language [5][6] with which they are familiar. A computer program initially performs a design-space exploration [3] of a variety of computational models and their implementation on simulations of cyber-physical systems. Then the computer program produces a partitioning that implements the specifications in an **optimal** manner using specific components listed in a component database that is available to the computer program. A software tool performs a mapping **automatically** according to performance cost-functions {power/energy and code/data size}, determines the **optimal** architecture, chooses the partitioning between the various processor cores and verifies that each core implements the design correctly using enhanced simulators [7][8], etc. **The result of such an analysis/optimization is a repartitioned model and an interconnection diagram that will execute on all the processors of the system in the most power-efficient manner.** As an *artifact*, the source code produced represents a complete executable specification.

A model driven engineering tool such as PARS has the ability to create a radically new programming methodology based on analysis through synthesis combined with operations research and global optimization. Such tools condense the steps needed to translate simulation models from the scientists' specification into executable specifications. These tools do this by converting the high-level specifications into a global optimization problem, solved without human interaction, yet encapsulating the many years of embedded system implementation experience into a process.

Historical Development of this CRADA partnership

An integrated single-vendor tool for generating code for multiple types of programmable processors does not currently exist[1]. Each processor or system vendor supplies a compiler tool to translate computer source code into a machine executable specification. It is the hardware vendor's task to supply appropriate software drivers and application programming interfaces so that the hardware can be loaded with these executable programs and perform the function. Finally, if attempting to connect multiple types of disparate processors together, a physical and logical communication must exist to enable these several programs to communicate.

The approach that Sundance DSP, Inc. has taken is to use a multi-processor operating system vendor, 3L Ltd. and provide the necessary logic and drivers to enable code written for this operating system to span across multiple boards, devices, cores, etc. Upon this platform, the PARS toolkit is used to automate the process of converting Simulink model code (and its variations of embedded Matlab, stateflow coder and other methods) to one of two types of source code: C language code for von-Neumann machines and VHSIC[2] Hardware Description Language (VHDL) for programmable logic.

ORNL and Sundance DSP, Inc. originally came together as part of a DOD project entitled "Common Radar Environment Simulator" that operated from September 2005 thru March 2010. Sundance DSP, Inc. provided the PARS software as well as hardware for the system. While PARS had support for multi-FPGA using Xilinx's System Generator tool in earlier version, in 2008 support for HDL-Coder was also added in PARS versions 10.xx and later. PARS always had support for multi-DSP from very early on in its development.

[1] But efforts such as OpenACC [9] and OpenMP v4.0 [10] are closing the gap.
[2] Very High Speed Integrated Circuits (VHSIC)

Technical Discussion of Work Performed by All Parties

The technical objective of this CRADA is to complete and maintain an integration of UT-Battelle (ORNL)-developed software with Sundance DSP, Inc (SDSP)-developed software (PARS) such that both entities may use the combined function to their individual benefit.

Negotiations between ORNL and Sundance DSP, Inc. led to the establishment of three primary tasks to be accomplished for the CRADA. These are listed below, with narrative describing the task and the result.

Task #1:
- *Provide current source code of PARS, the AB105 board support package and additional driver support files as needed for a complete software system build.*
- *SDSP is to provide this software.*
- *Completed Oct 11, 2011*

This task formed the beginning of the CRADA work, and represented Sundance DSP, Inc. in-kind contribution to the CRADA. Sundance DSP provided PARS version 12 to ORNL on October 11, 2011.

Task #2:
- *Integrate 'PFIFO_to_HDLCoder' software into source code for PARS and provide quarterly updates to SDSP of any new capabilities and problem fixes as determined by ORNL or SDSP and provided by either.*
- *ORNL is to perform this task with input from SDSP, subject to available funds.*
- *Integration with PARS version 11 was completed on Nov 01, 2011*
- *Integration with PARS version 12 was suspended on Sep 13, 2013*

The effective parts of the October 2011 release were merged into ORNL's code base developed from PARS version 11 from August 2009 thru October 2011. This release was transmitted to Sundance DSP on November 1, 2011 entitled 'PARS V11 Beta 17(j)', and tagged in the ORNL internal source code control system[3].

In consultation with the partner, integration of PARS 12 with Matlab/Simulink R2009b+ began. This integration was intended to support Matlab/Simulink R2009b+ (Service Pack 1), Code Composer 4.2.4, Diamond 4.1.2 and Xilinx ISE 12.4. The partner selected three Sundance hardware platforms and their corresponding modules to be supported:

CRES: SMT417_5(PCI)+SMT365+SMT318SX+SMT368A
AIMMv1: SMT148(USB)+SMT361Q+SMT374+SMT318SX
EVP6472: SMT111(USB)+SMT372V2

One difficulty encountered was the fact that Diamond 4 did not support the modules in RED, while the platform/modules in ORANGE were claimed supported but not verified working. Correspondence with Sundance DSP, its affiliate Sundance Multiprocessor Technology, Ltd. and partner 3L, Ltd. occurred between December 2011 and July 2012. At that time, it became known that the SMT374, a module thought to have been supported by Diamond 4, was in fact *not supported*. Correspondingly, all effort to integrate PARS 12 with the tools above was suspended, and the remaining project funds were reserved to write the user guide of the 'PFIFO_to_HDL Coder' gasket. This document was provided to the partner for review in September 2012.

Task #3:
- *A final report will be filed at the termination of the CRADA.*
- *ORNL is to perform this task with input from SDSP.*
- *Completion 10/16/2013*

During the discussions in the first quarter of 2012, it became clear that Sundance DSP, Inc. was developing a business opportunity with another DOD agency, and requested an expansion of the scope of the CRADA to

[3] https://eesd-ls1.ornl.gov/svn/SDSP/PARS/tags/pars_v11b17j/

incorporate additional tasks on which ORNL would be able to provide unique expertise. These tasks were added as Addendum #2 to the CRADA and extended the period of performance of the CRADA to the end of fiscal year 2013.

Task #4:
Update digital beamformer software from the SDSP product DSP8080-AIMM to use the latest tool versions from Xilinx, Texas Instruments, 3L/Diamond, National Instruments and the PARS/Diamond software that is the subject of this CRADA:

- *SDSP is to provide the software, firmware and documentation for the DSP8080-AIMM.*
- *SDSP is to provide one hardware system with all cables, connectors and parts needed to operate the system. The system remains the property of SDSP and will be returned upon completion of this task.*
- *ORNL will implement the system using PARS pre-built tasks for all code and firmware modules used (two total configurations).*
- *ORNL will integrate and verify the correct operation of the system with the updated modules and modern version of intellectual property (IP) pulled in by the latest tool versions. This includes the Sundance Communication (SCOM) cores.*
- *ORNL will provide calibration, performance verification test and data integrity verification test for all the processors and SCOM links in the system.*
- *ORNL will update existing documentation to correspond to the new programming method.*
- *ORNL will update DSP9650 Labview Interface SW to work with the latest AIMM system described above and Labview 8.x, 2011 and 2012.*

Sundance DSP, Inc. provided ORNL with one DSP8080-AIMM hardware system in June 2012. As part of the development of the User Guide and as verification of the 'PFIFO_to_HDLCoder' software, ORNL ensured that all the processors of the DSP8080-AIMM hardware platform could be programmed from Simulink models. A device description file was created and several examples were provided to the partner on June 14, 2012.

Due to the volatile nature of the U.S. economic market, Sundance DSP, Inc. was unable to provide the necessary funds-in to ORNL to perform this task and the others that comprised the tasks for Addendum #2. Sundance DSP, Inc. internal engineering, according to the procurement contract issued by the DOD for upgrades to the DSP8080-AIMM system, performed the above Task #4.

Therefore, this CRADA closes with the delivery of the User Guide for 'PFIFO_to_HDLCoder' software module integrated with **PARS 11** { PARS 11.b17k, Diamond 3.1.10 update 7, Matlab R2007b, Code Composer 3.3 and Xilinx ISE 10.1.03 } and ***tested*** on the DSP8080-AIMM system. As a bonus, the 'PFIFO_to_HDLCoder' software module is also integrated with PARS 12 { Diamond 4.1.2, Matlab R2009b+ (Service Pack 1), Code Composer 4.2.4, and Xilinx ISE 12.4 }, but ***not tested on hardware*** due to the aforementioned difficulty encountered.

Subject Inventions (As defined in the CRADA)

UTB Case No. 50000053 for PFIFO_to_HDLCoder, submitted for copyright **PRECEEDED** the CRADA. The CRADA was developed to enable the commercialization of the ORNL developed software component.

Commercialization Possibilities

Negotiations with Sundance DSP, Inc include the possibility of licensing the software package under a commercially reasonable license. This CRADA was entered to further validate the materials in preparation for licensing. ORNL plans to commercialize the copyrighted materials within five (5) years of being granted the rights from DOE. It is expected that the 'PFIFO_to_HDLCoder' and the enhanced PARS as bundled with it, when commercialized, will have a positive effect on U.S. competitiveness. It is expected that this material will have an export market that will have a positive effect on U.S. industrial competitiveness in international markets.

Plans for Future Collaboration

ORNL is to provide a document describing the nature of PFIFO_to_HDLCoder and how it differs from the original interface used in PARS to help Sundance DSP make informed decision on the benefits before deciding to make use

of it. ORNL successfully integrated PFIFO_to_HDLCoder with PARS 11 under the CRADA, but since then Sundance DSP has moved on to PARS 13.

The below papers [11][12] presented at ICALEPS 2013 [13] may serve as food for thought. In [11] the European Xray Free Electron Laser (XFEL) facility is describing heavy investment on model-driven engineering process and use of Simulink/Xilinx System Generator and HDL Coder. In [12], they present an integrated software framework under development for communicating and coordinating multiple devices across the entire facility. This has the potential of becoming an open-source alternative to the Diamond operating system that has the potential for expanding the role and relevancy of the PARS software system to a far greater set of devices. In the meantime Sundance DSP has developed a RTOS called L7 which is a modern operating system with all the features of Diamond and more. Sundance DSP is planning to certify this by FAA DO-178. This development can also considerably open new avenues to PARS and enhance its position in the market place.

Another industry development that has occurred over the last 5 years is the standardization of VITA-49 [14][15][16] and its application to RF systems. Because of this work, it is now possible to construct self-synchronizing systems without a central arbitration of flow control. In essence, this is the heart of what the PARS system was attempting to achieve, albeit on top of a specific multi-processor operating system. The industry adoption of VITA-49, and its interest to the open source community [17] signal a landmark event toward the accelerated development of complex communicating multi-processor systems. Matt Ettus/National Instruments, in his keynote address at ICALEPCS 2013 [13] described a communication system code named “RF NoC” [18] that is being diligently worked on and has great relevance to PARS.

Conclusions

Large experimental physics laboratories, in order to further the frontiers of science are developing ever more complex systems composed of 1000s of heterogenous computing elements. Similar to the development of super computers at the end of the last century, these facilities are accumulating more complexity in every generation. The model driven engineering process, system engineering and automatic code generation are proven methods.

PARS is a toolkit that stands in relevance to all these activities. It has the ability to leverage the advances that OpenACC [9][20], VITA-49 [15][19] and “RF NoC” [18] standards provide with respect to code performance portability, packet communication and component interoperability. By incorporating these basic features into a model driven engineering environment it not only supports the generation of reliable and functional systems [21], but paves the way toward systems that can be optimized using the properties emergent in these systems.

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