

Directed Patterning and Fabrication of Functional Nanoscale Electronic Oxides

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Jon Ihlefeld

Matt George

Chris Shelton*

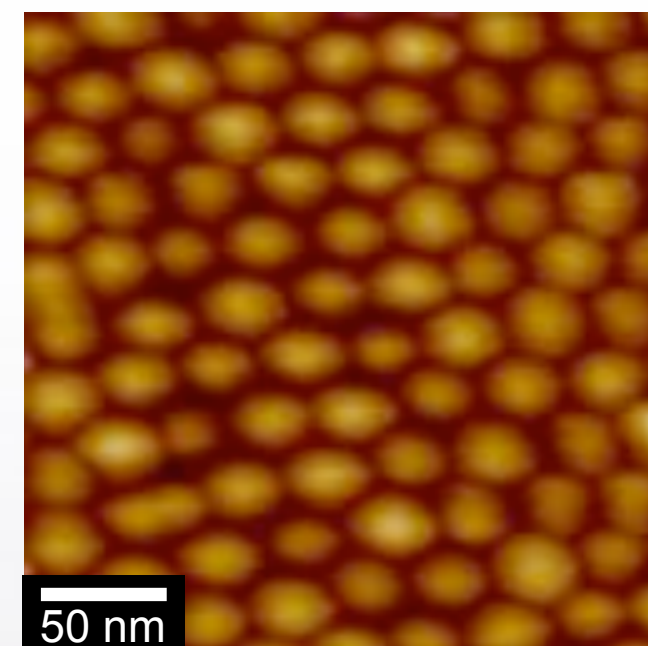
Sandia National Laboratories
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now at HP

Paul Nealey

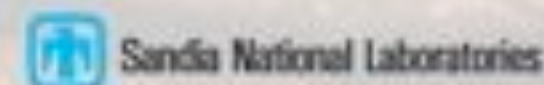
Shengxiang Ji

Chris Thode

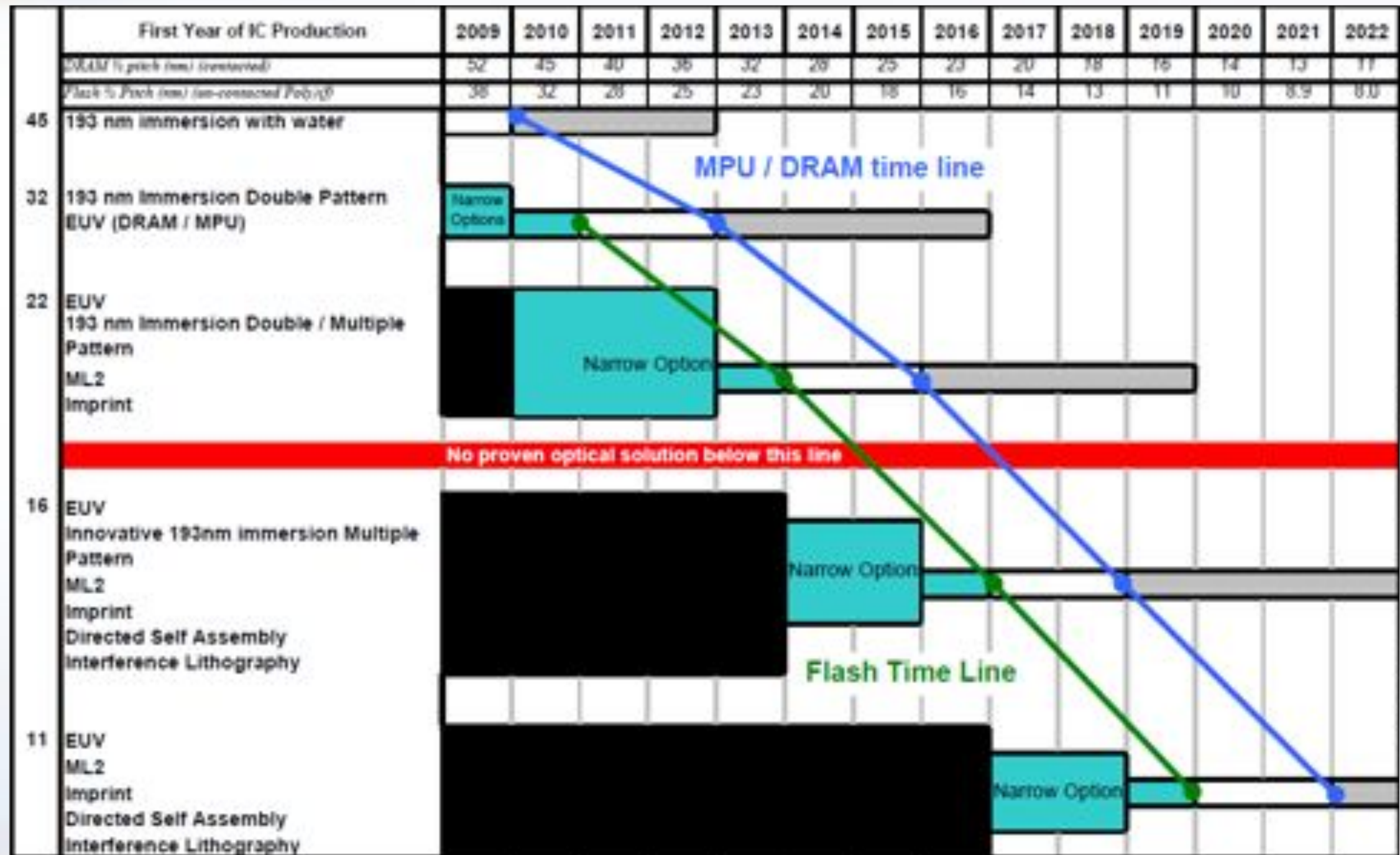
University of Wisconsin



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Doing Moore with the Same?



This legend indicates the time during which research, development, and qualification/pre-production should be taking place for the solution

Research Required

Development/Qualification

Qualification/Pre-Production

Continuous Improvement

ITRS 2009



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Doing More with the Same?

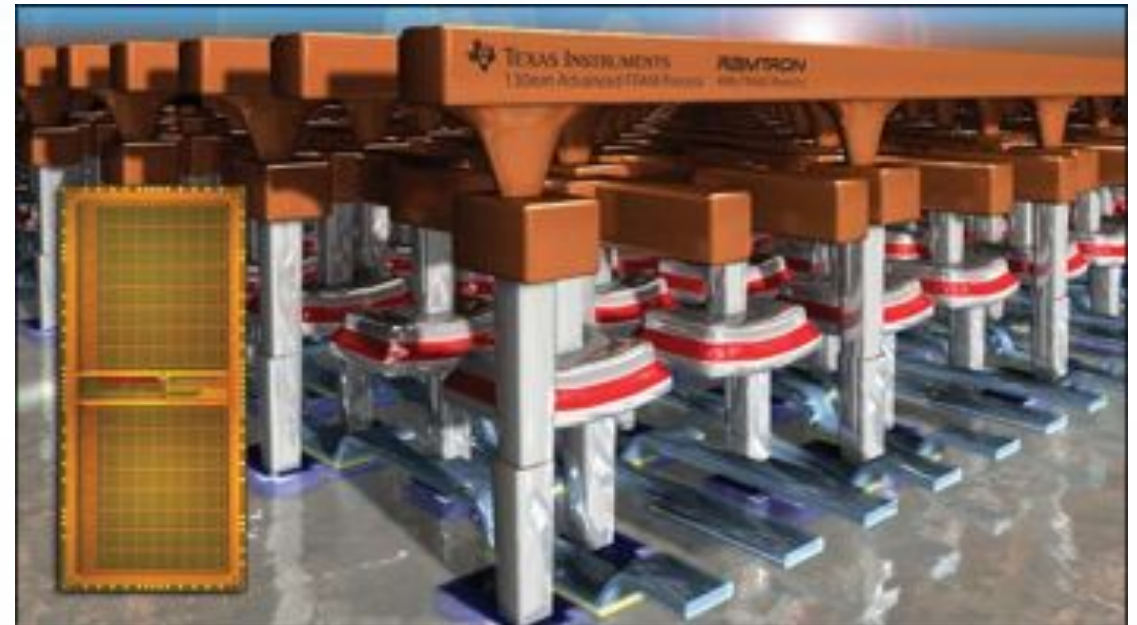
Integration of materials with new and/or increased functionality

General Fabrication Technique for Controlled Nanopatterning

- Any material, any substrate
- Arbitrary, addressable features/patterns
- Platform for size/interface effects studies, device development, etc.

Why Ferroelectrics?

- Demonstrate broad applicability
- Study fundamental lateral size and aspect ratio effects
- Ultrahigh density NVRAM



From MRS Bulletin v33 (2008), originally from TI, Ramtron

Target Demo Application Information Storage (NVRAM)

- Reduce physical size
- Reduce power consumption
- Improve operation through interface control

Micro-, Nano-Patterning of Arbitrary Materials

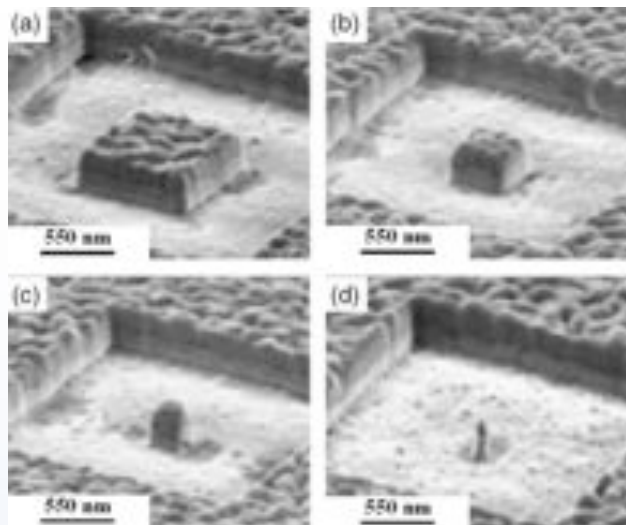
■ Challenges of expanding beyond 'standard' materials

Fabrication

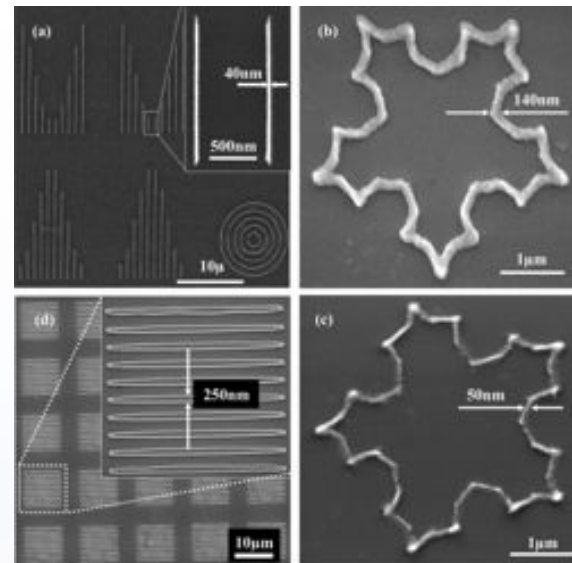
Patterning

Integration

Performance

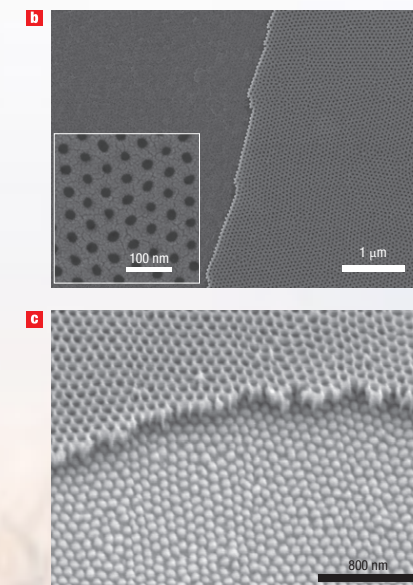
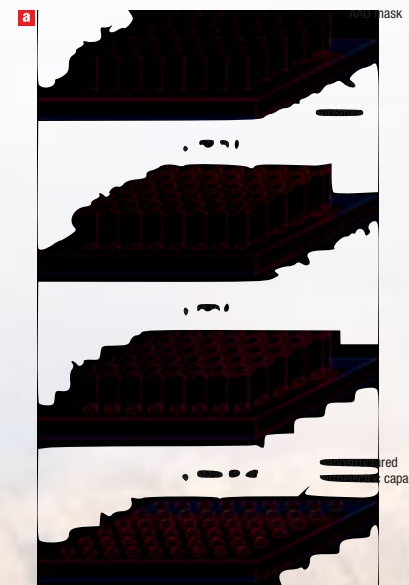
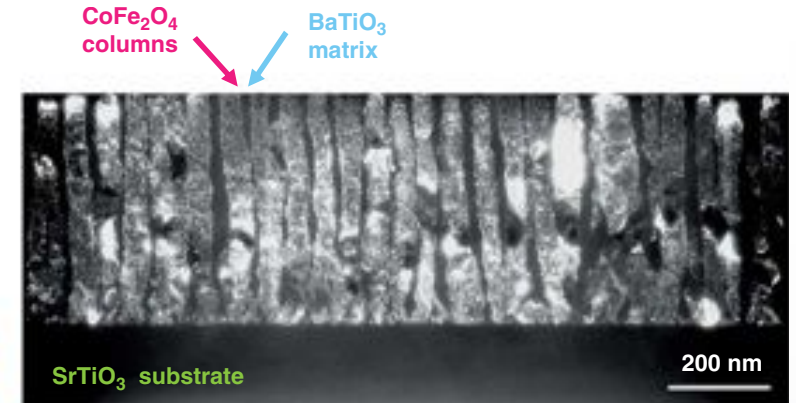
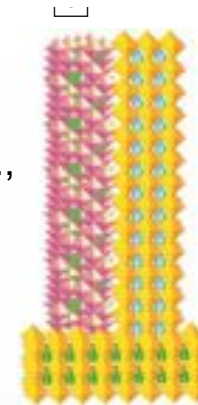


Ganpule et al., MRS Proc. (2001)



Donthu et al., Nano Lett. (2005)

Zheng et al.,
Science
(2004)



Lee et al.,
Nature Nano
(2008)

- Need functional crystalline nanostructures in predetermined locations without needing to develop new etching / integration approaches for each new material(s)

Overview of Our Approach

- Goal: Combine flexibility and functionality of chemical solution deposition with use of e-beam and BCP patterning capabilities

Solution Deposition

Fabrication

Patterning

Integration

Performance

Feature Definition

Fabrication

Patterning

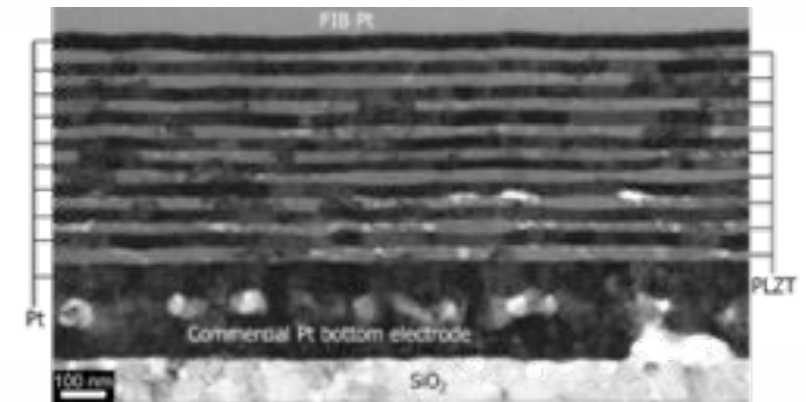
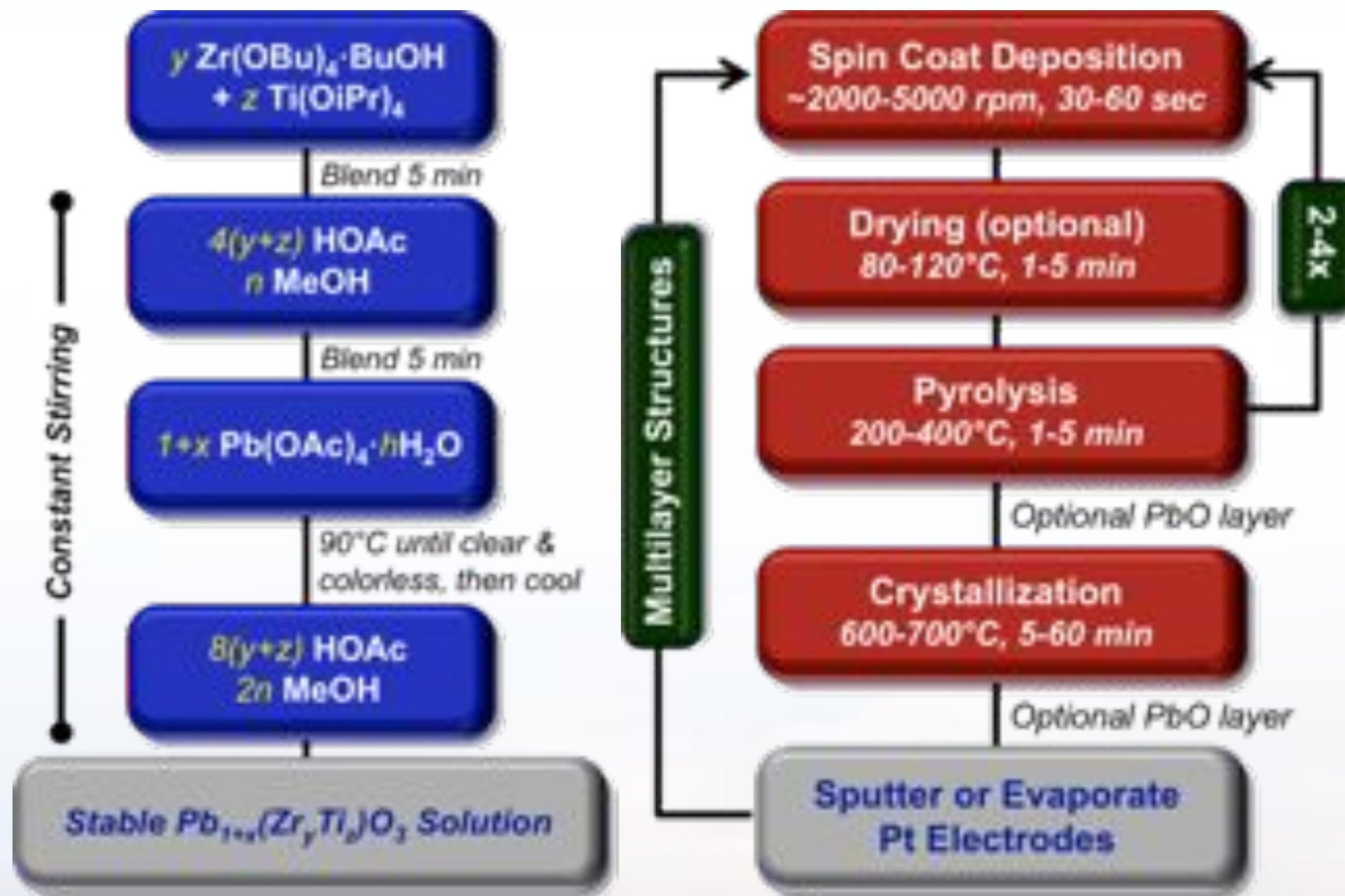
Integration

Performance

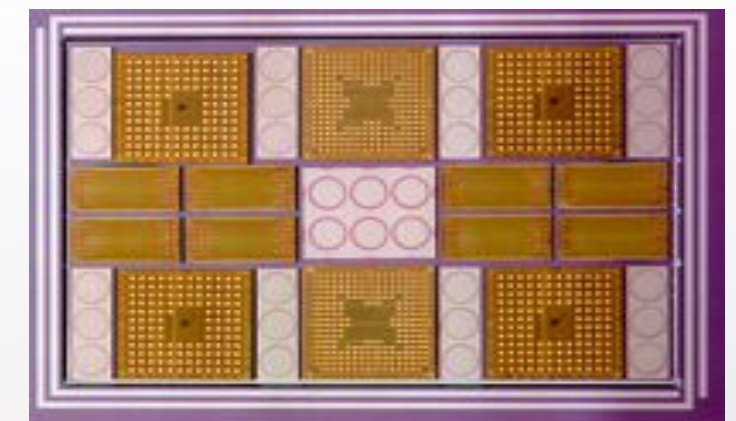
Challenges:

- Avoid etching functional materials
- Avoid any fab-based processes during/ after deposition of functional materials
- Maintain feature integrity after thermal treatment(s)
- Retain function in nanoscale features

SNL IMO-based Solution Route



Functional thin film multilayer capacitor structure



Multichip module with PZT thin-film capacitor arrays

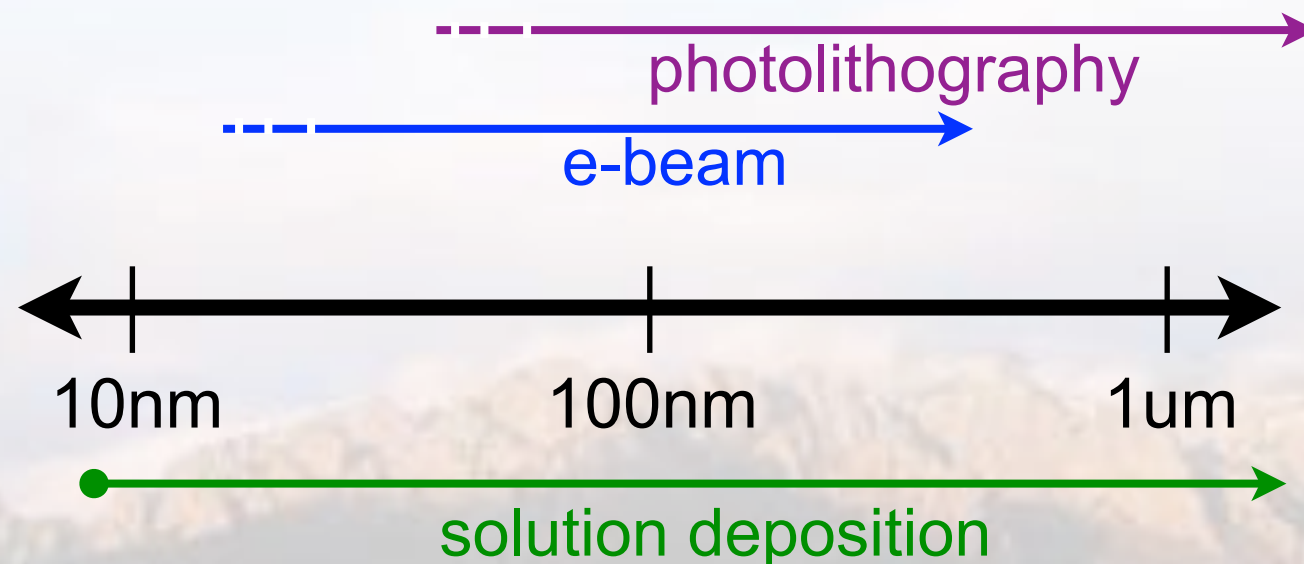
R.A. Assink and R.W. Schwartz; **Chem. Mater.** (1993)

G. Yi and M. Sayer; **J. Appl. Phys.** (1988)

Brennecka et al., **J. Am. Ceram. Soc. feature article** (2010)

Pattern Definition

- Continuous films are very limited in function
- Difficulties of etching PZT-based films
 - Access to tools...
 - Property/reliability degradation
- Alternative approaches to patterning/integration
 - Direct write
 - Microcontact printing
 - Various transfer techniques
 - PZT-friendly lithography
 - (Directed) self-assembly



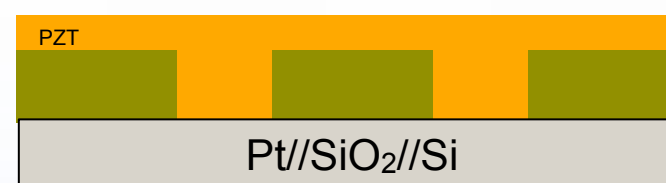
Microscale Patterning



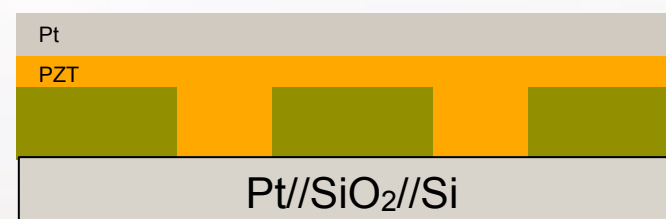
etch



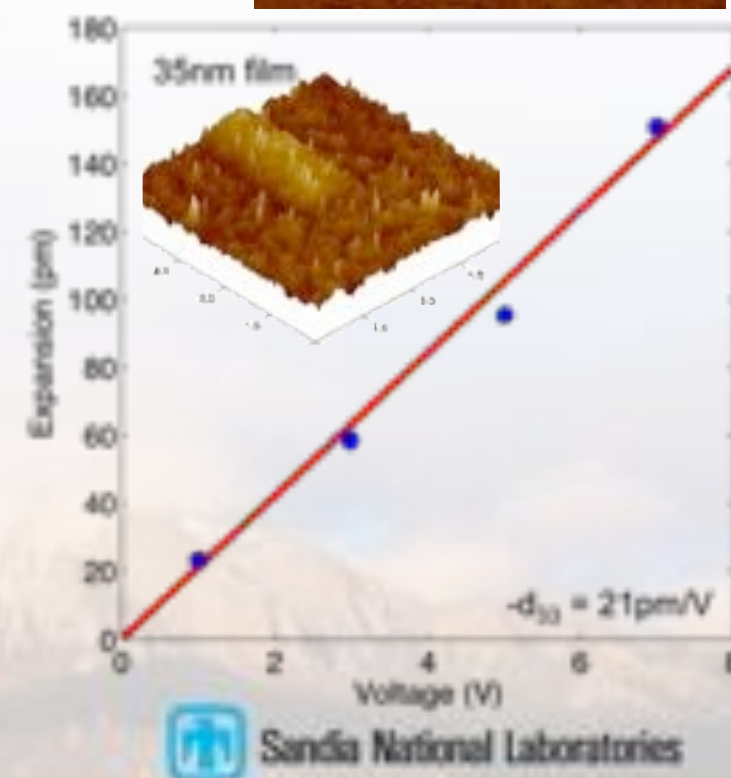
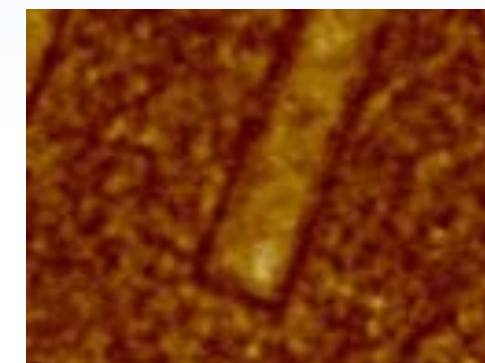
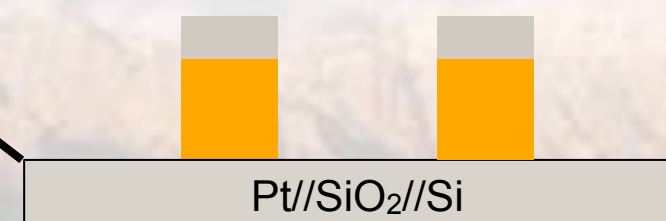
deposit, crystallize



sputter Pt

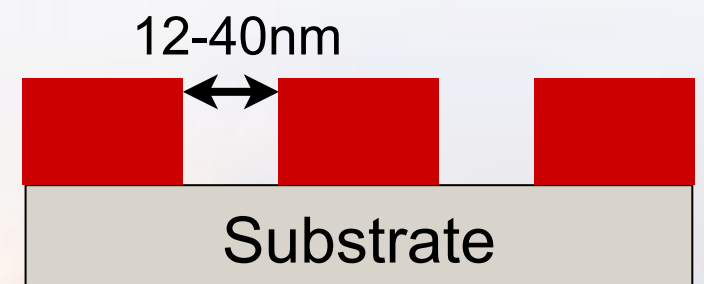
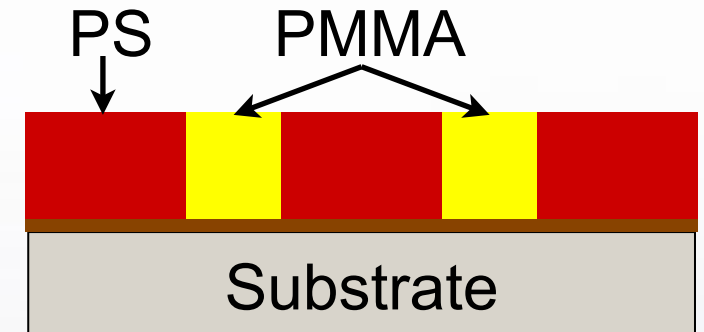
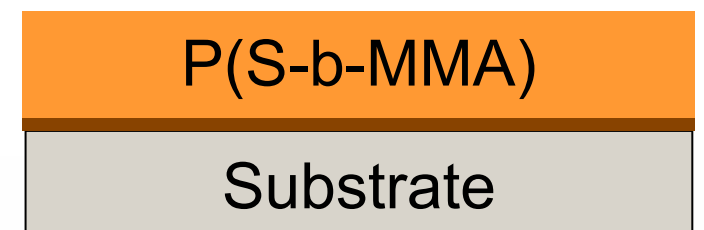
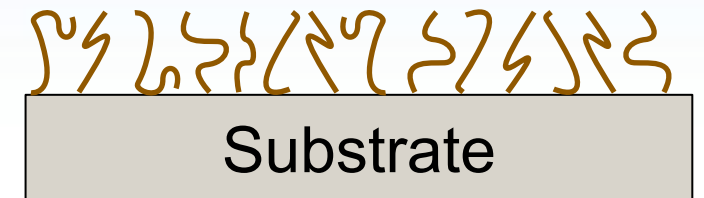
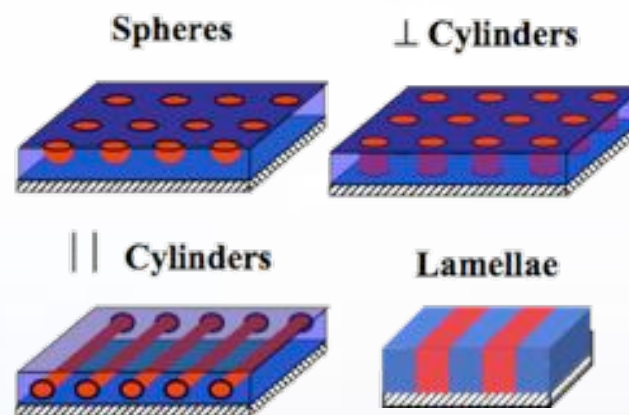


liftoff

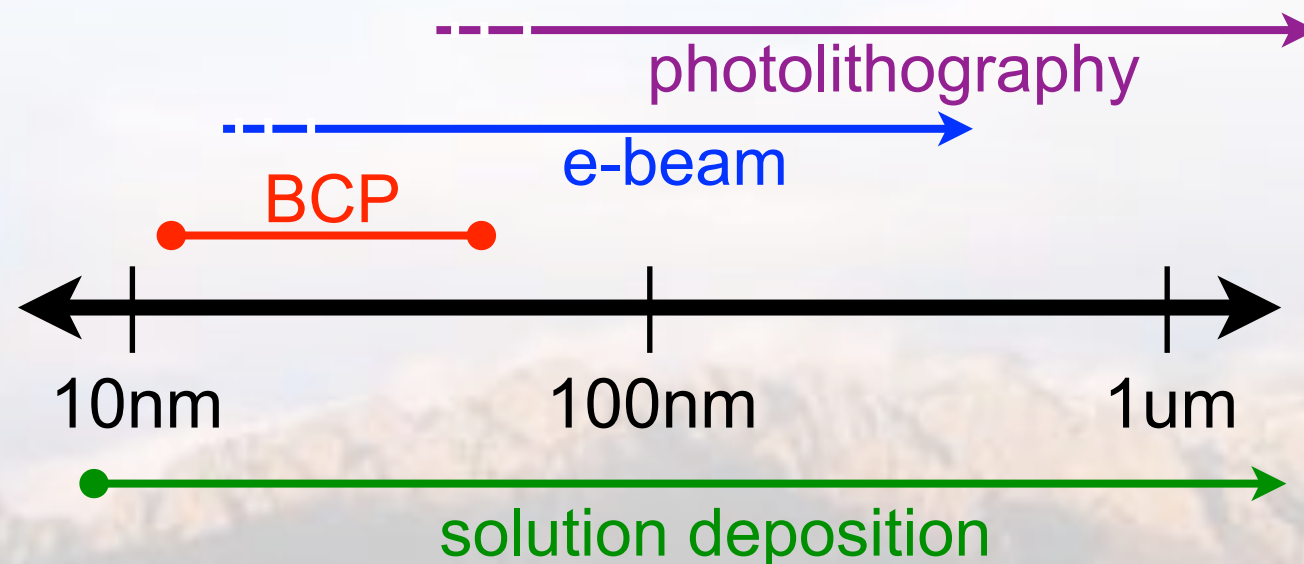


Pattern Definition

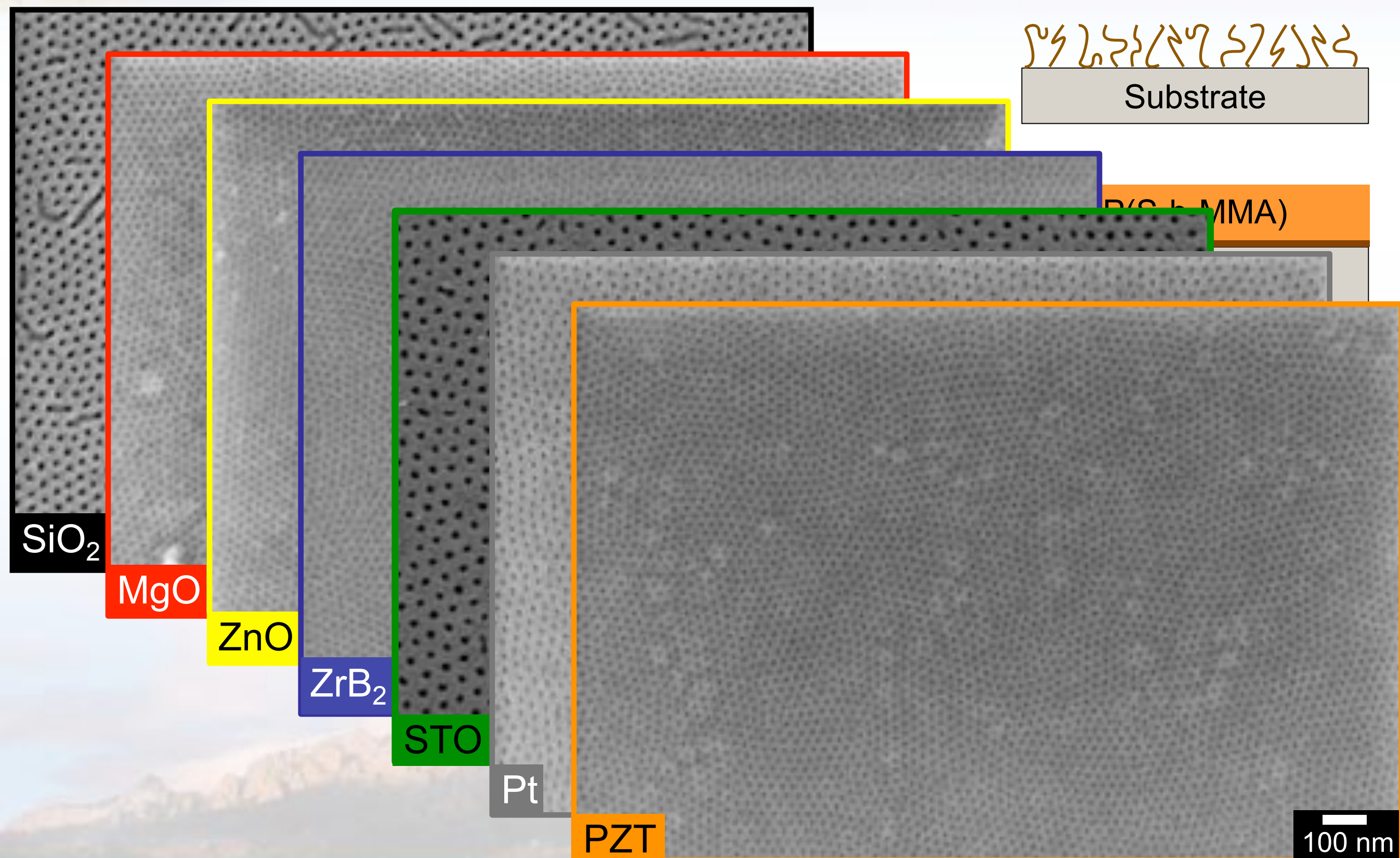
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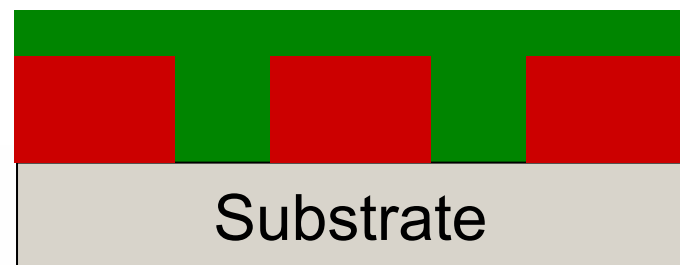
Guarini, K W, et. al., *J. Vac. Sci. & Tech. B*, 2001, 19 (6), 2784-2788



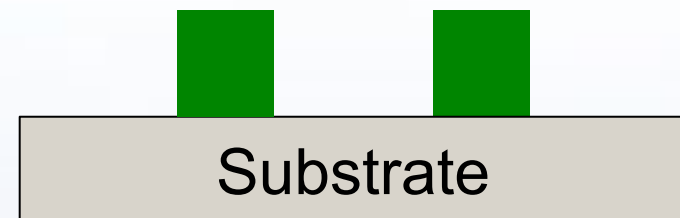
Diblock Assembly on Various Substrates



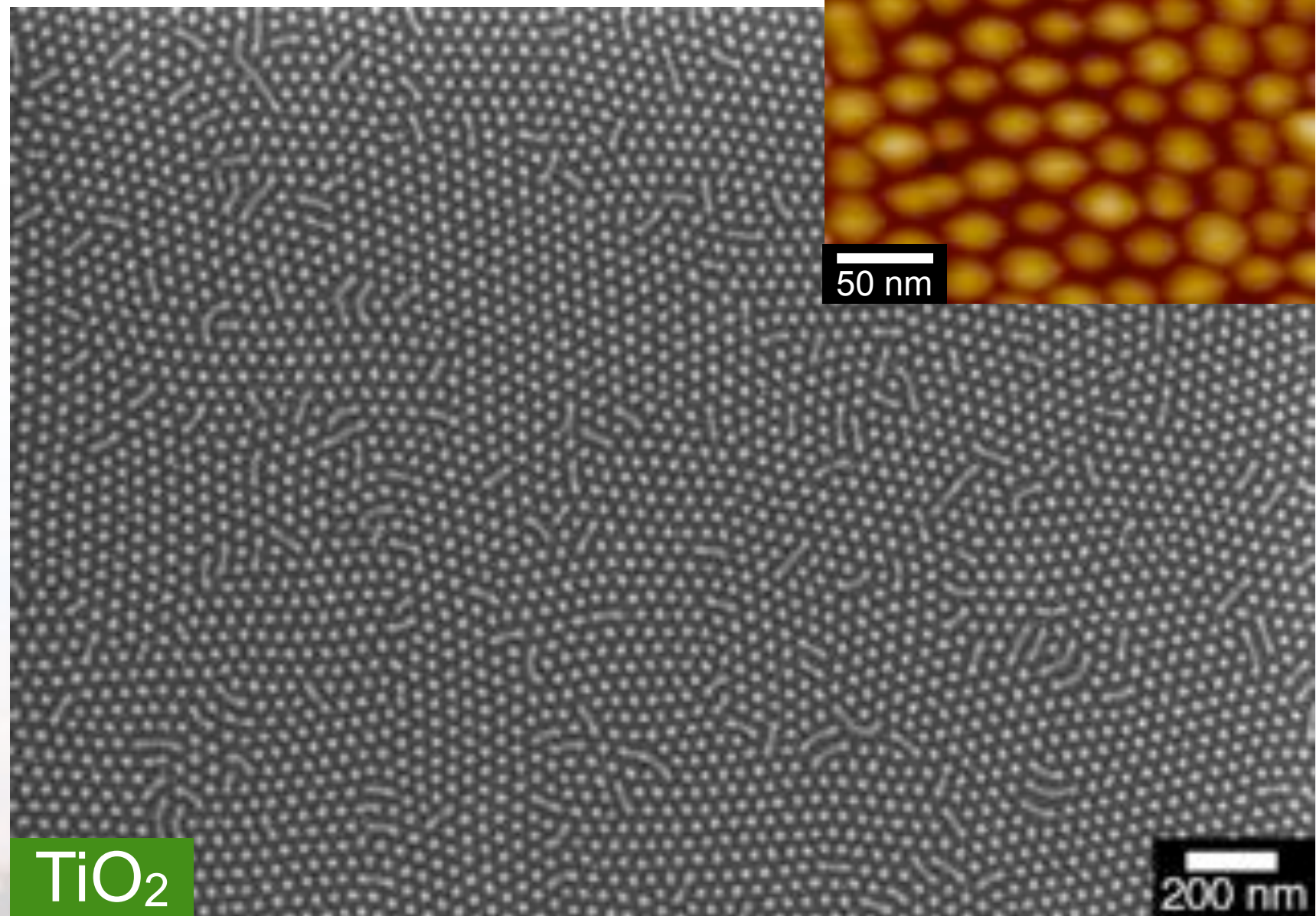
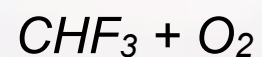
Additive Fabrication of Patterned Electronic Oxides



Fill, Gel

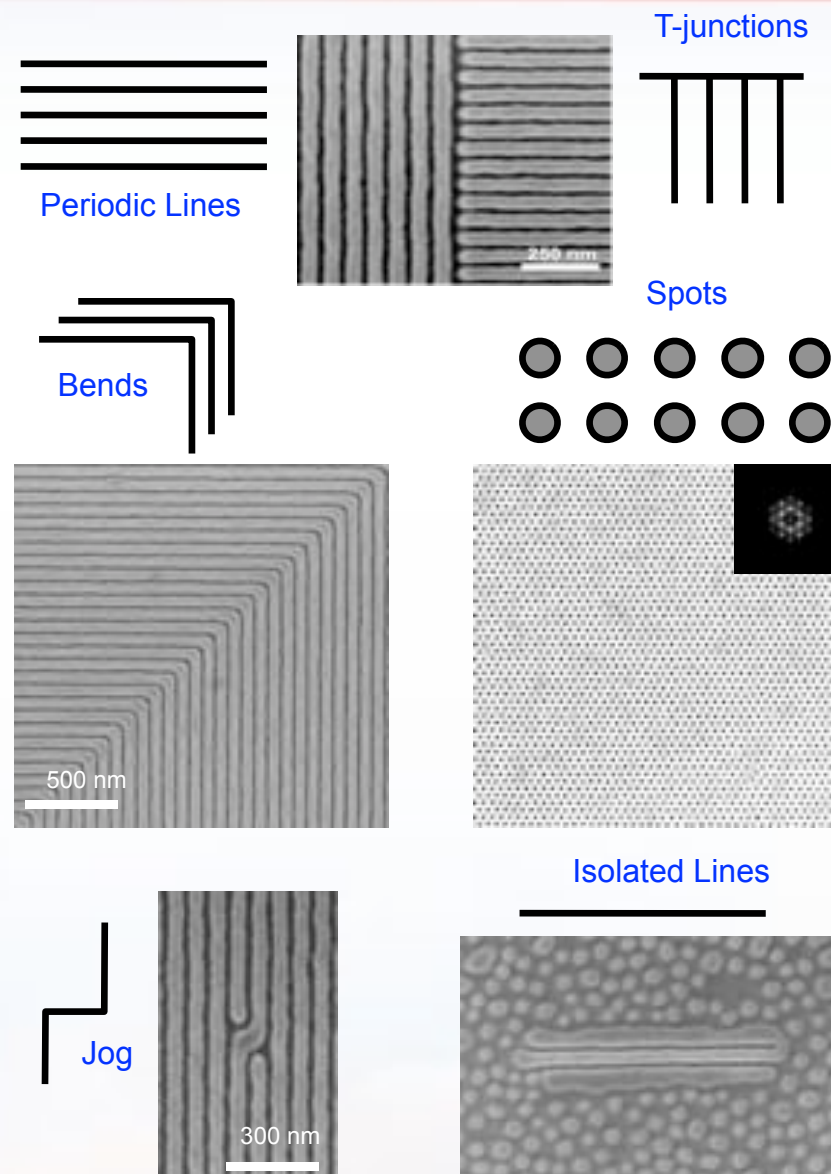
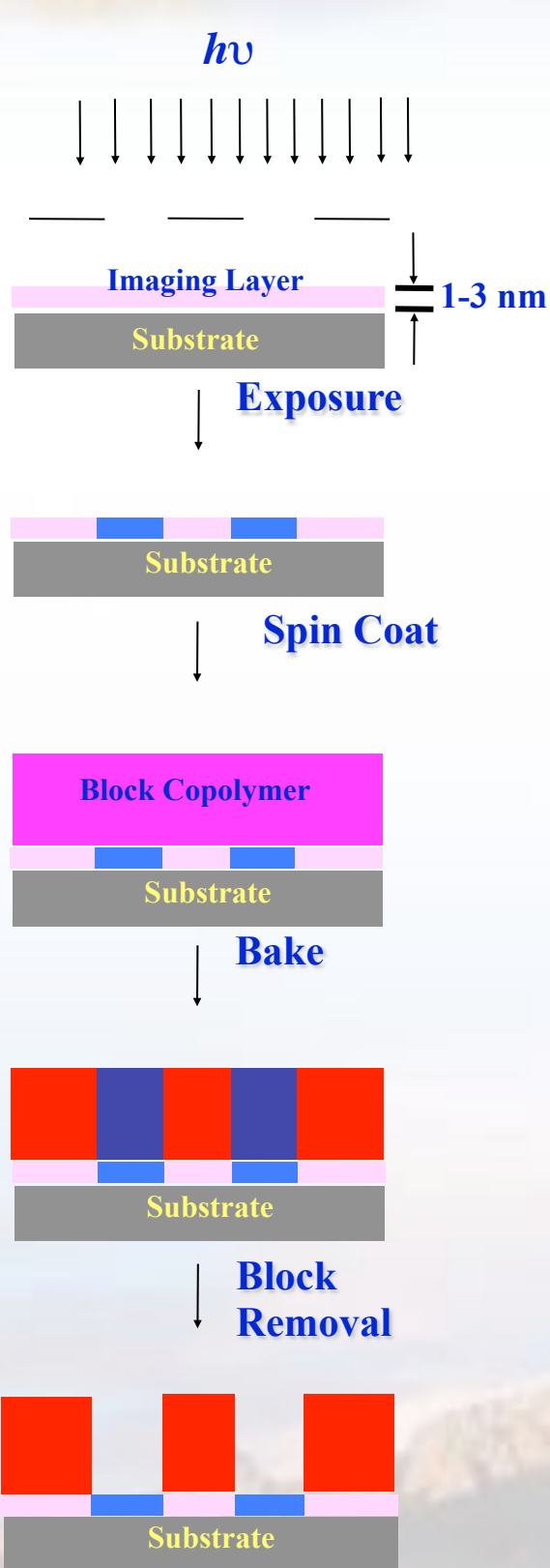


Remove Mask

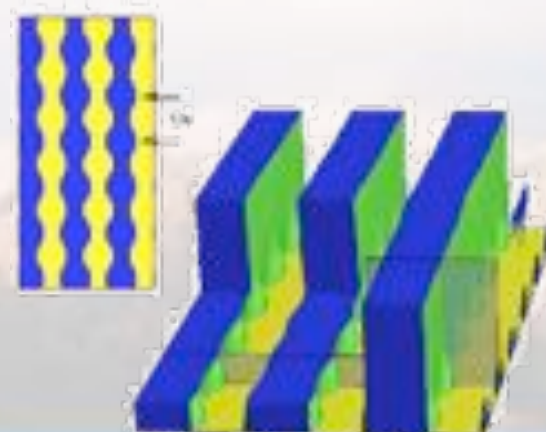


Block-Copolymer Directed Self Assembly

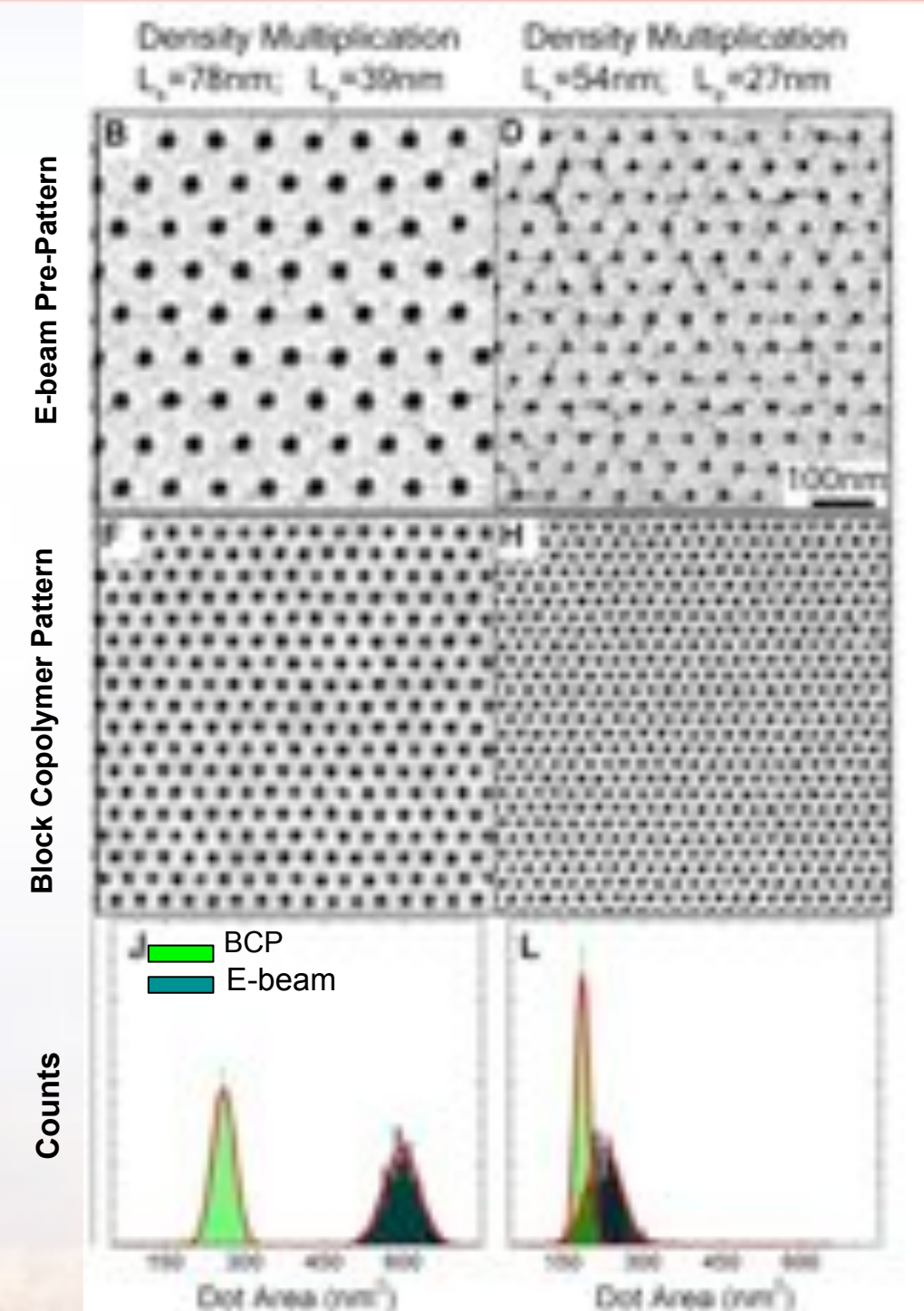
with Prof.
Paul Nealey



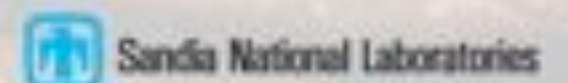
Stoykovich et al. *ACS Nano*, 2007, *Science* 2005



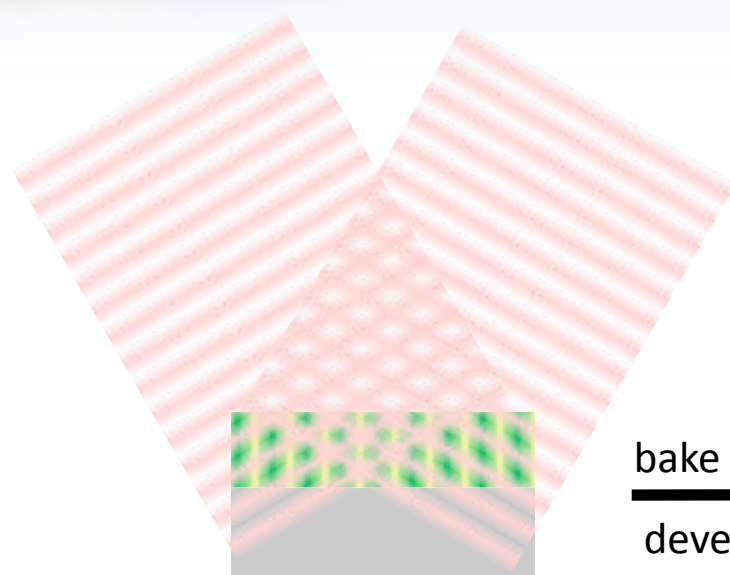
Daoulas et al.,
Langmuir, 2008



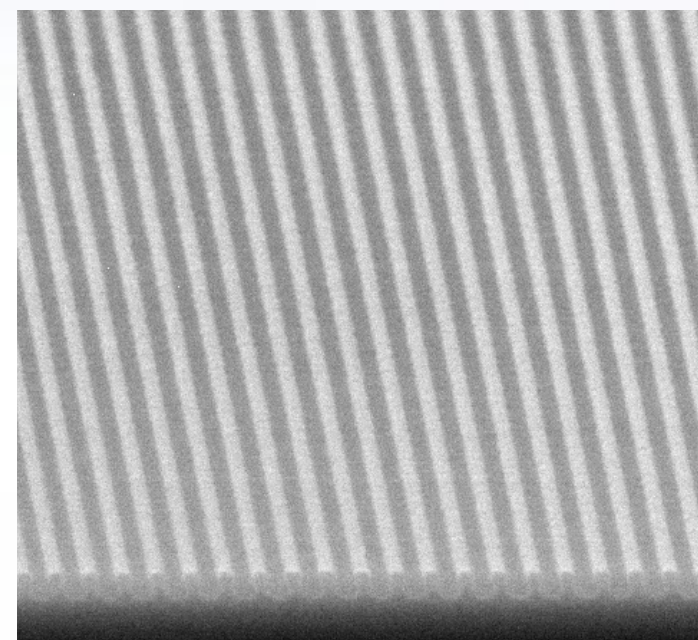
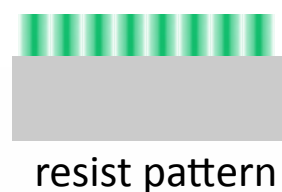
Ruiz, Nealey, de Pablo
et al. *Science*, 2008



Optical Interference Lithography



bake and
develop



Critical dimensions ~ 70 nm
Patterned areas $\sim 4\text{cm}^2$



dielectric
mirror

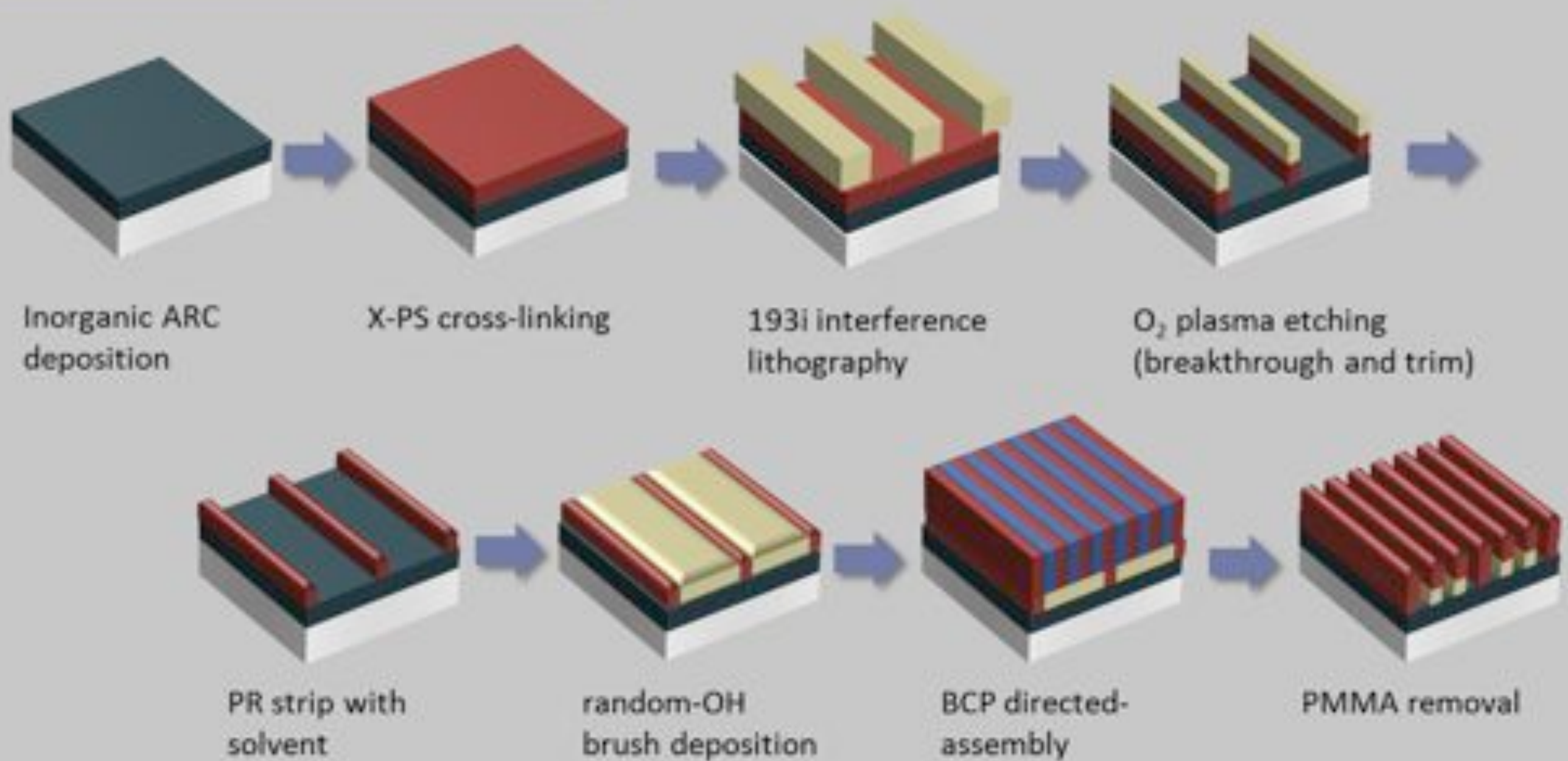
BS = beam splitter



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Density Multiplication

Process flow with ARC and 193i



3x density multiplication
30nm features in 90nm IL pattern
over mm² areas

Density Multiplication

22-22k on 100nm

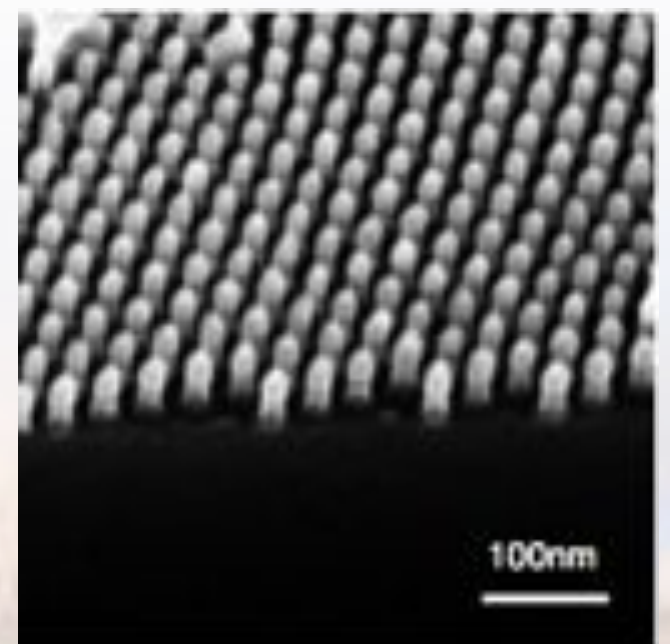
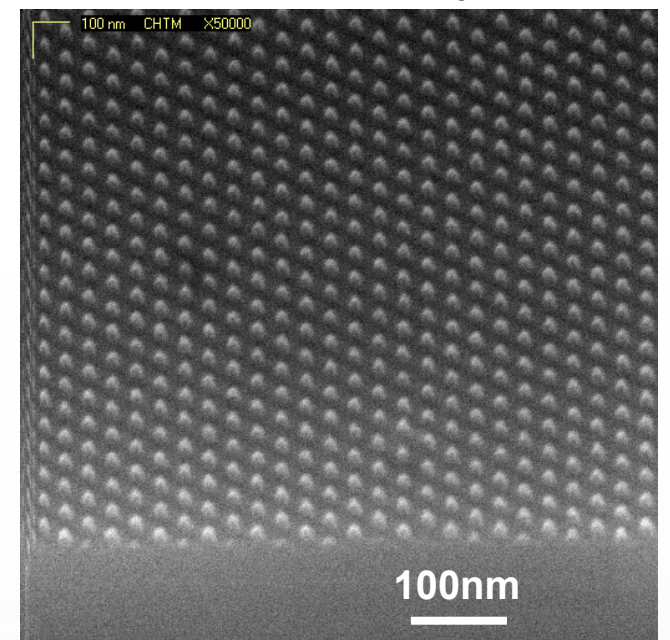
300nm

18-18k on 110nm

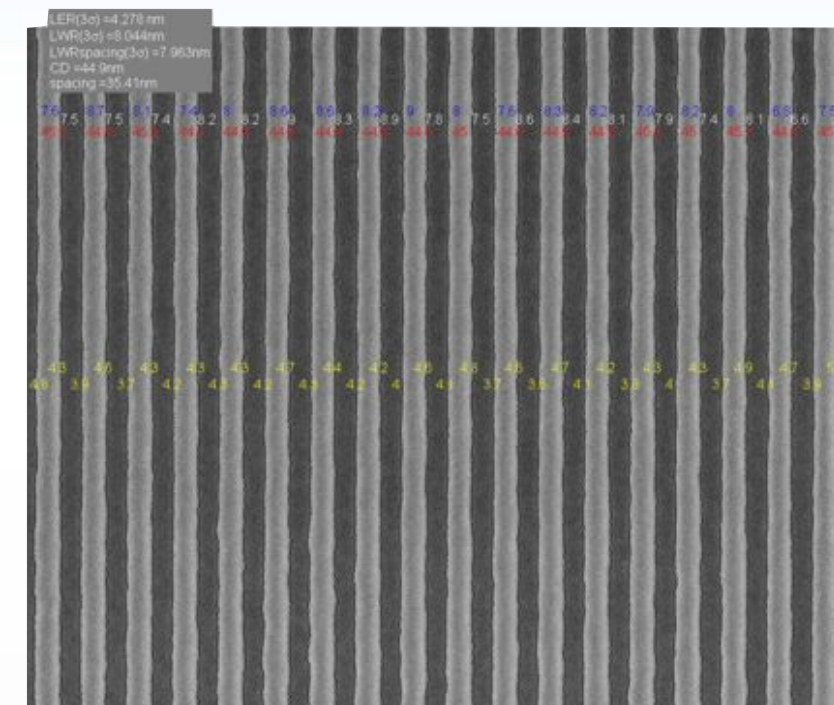
300nm

4X Multiplication

Cylinders

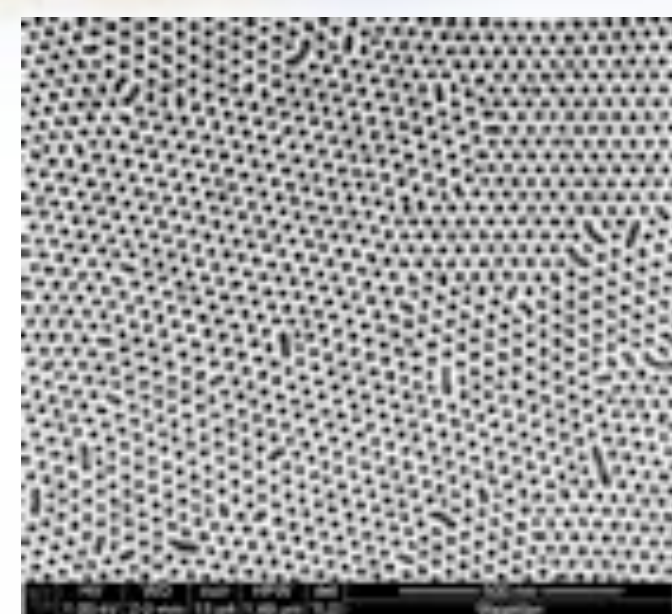


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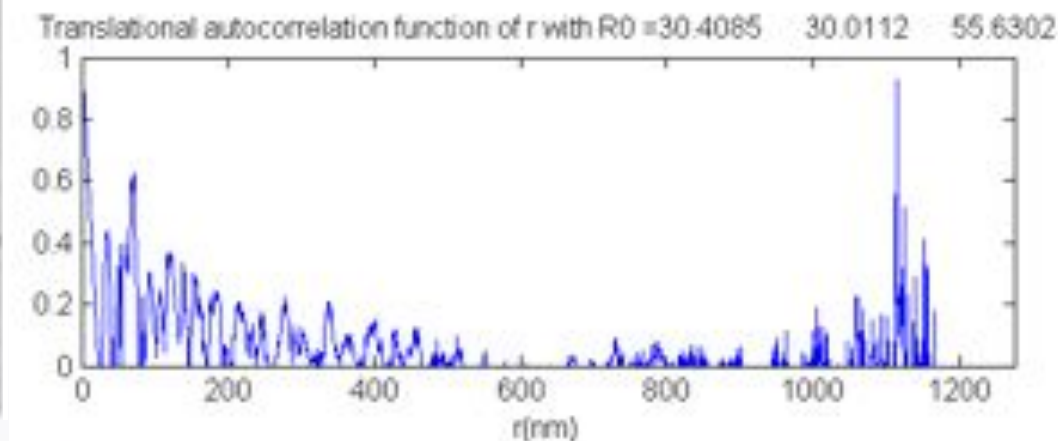
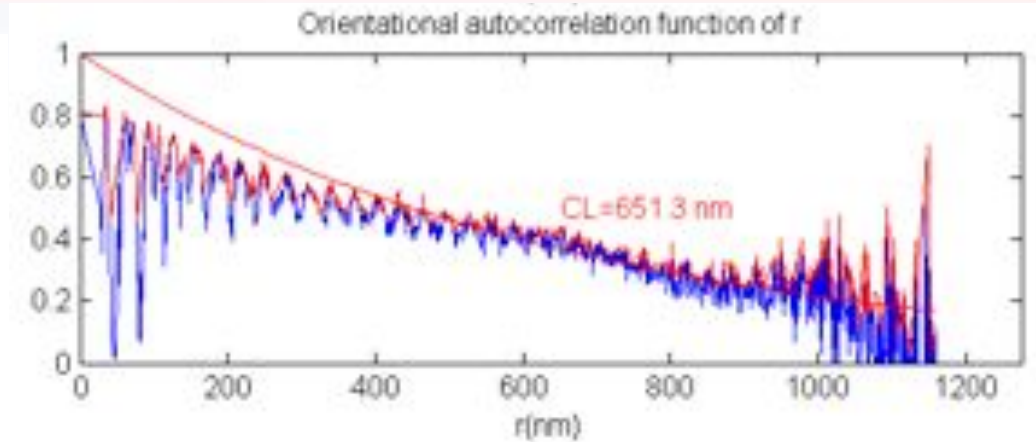
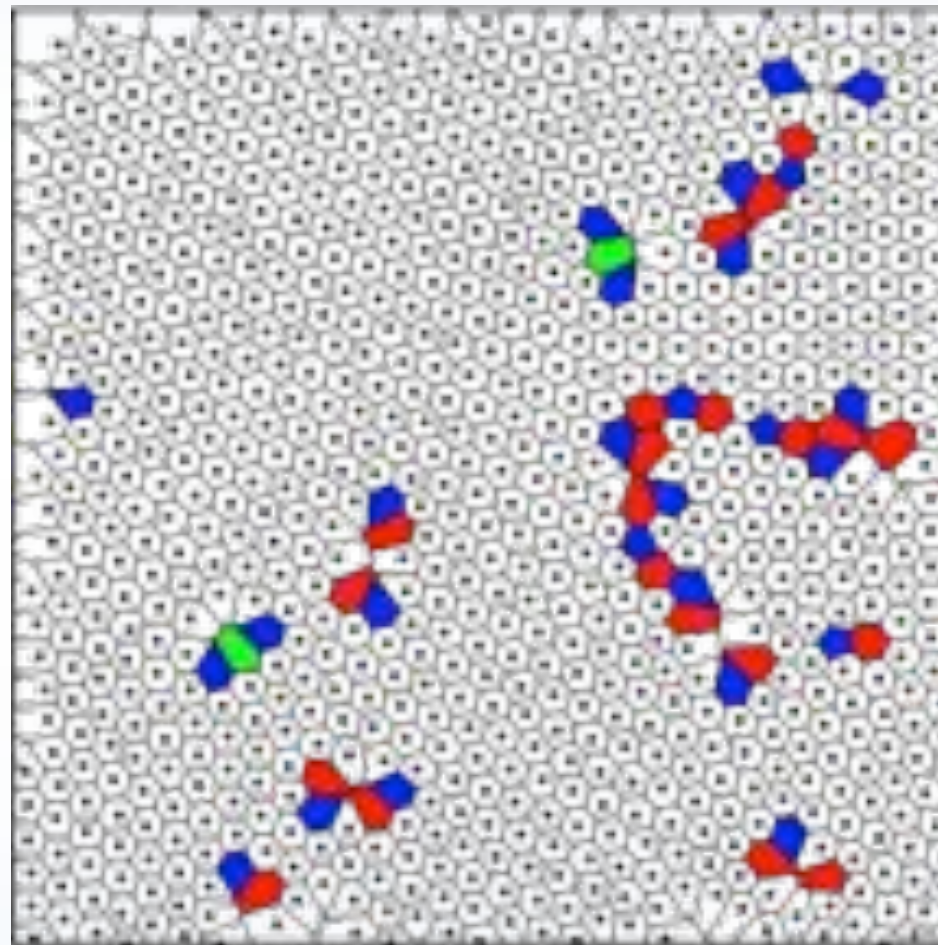
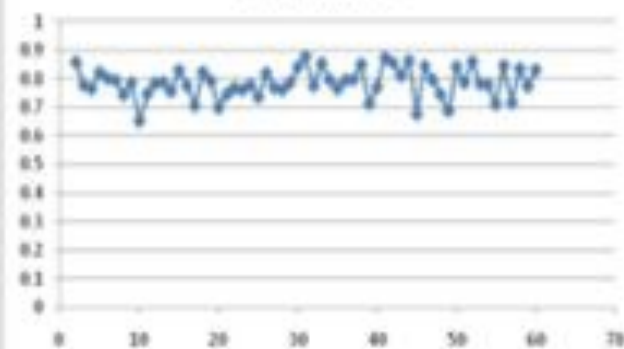


Intel-blessed standard, quantitative, non-destructive feature/defect analysis at each stage of process

Metrology



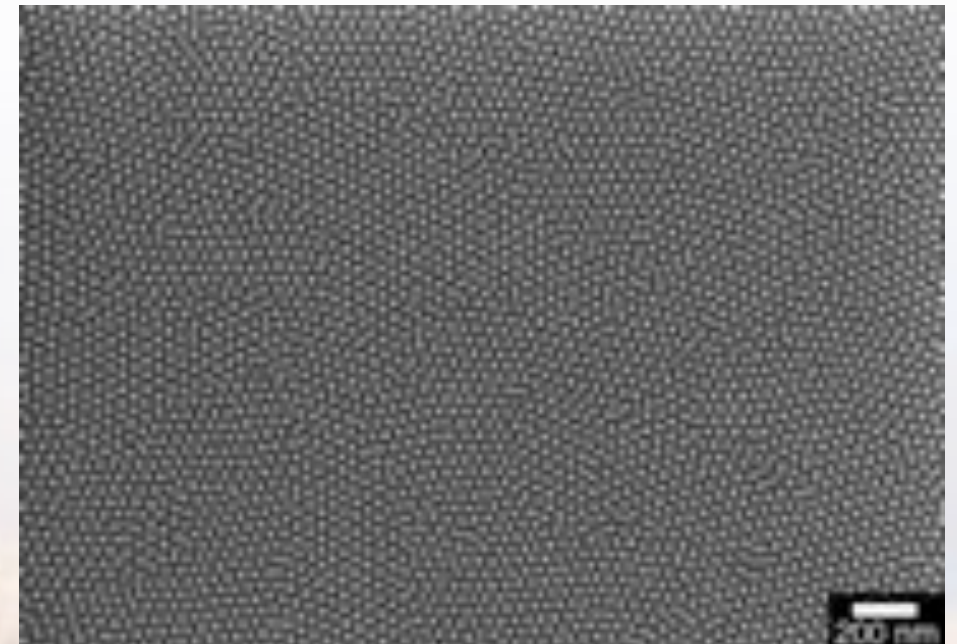
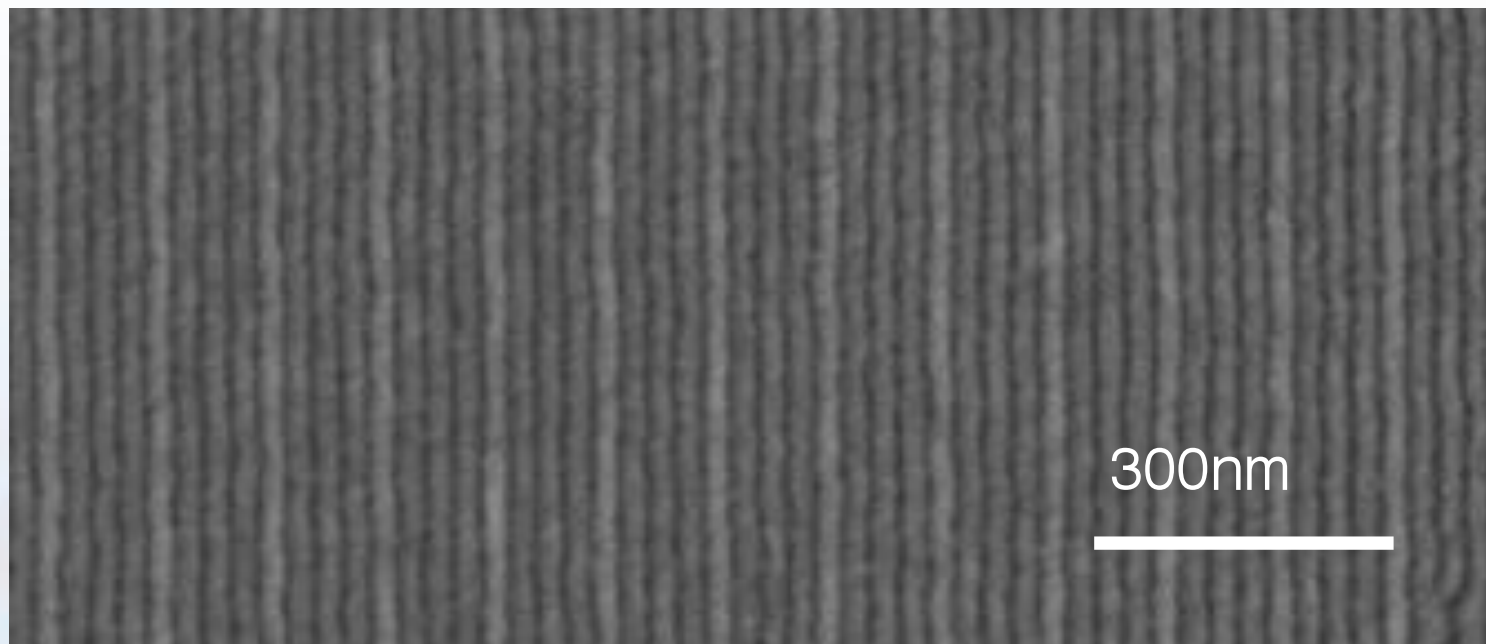
Roundness



All made possible by FEI Magellan SEM:
quantitative sub-nm measurements from
uncoated samples

Summary

- Extended BCP-based patterning to wide variety of materials (substrates and solution-derived features)
- Up to 4x density multiplication with DSA-BCP over mm² areas
- Near-arbitrary control over position and (to some extent) size of nanoscale features



Acknowledgments

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