GATE-ALL-ARROUND SINGLE-CRYSTALLINE SILICON NANOWIRE OPTICAL SENSOR

SAND2011-2835C

M. Ziaei-Moayyed, B. Draper, and M. Okandan
Department of Advanced MEMS, Sandia National Laboratories, Albuquerque, NM, USA

ABSTRACT

In this paper, we demonstrate gate-all-around (GAA) single crystalline nanowires (SiNWs) that are fabricated using top-down standard CMOS front-end processes. The GAA silicon nanowires are fabricated in well-defined locations with high-quality electrical contacts, and controlled geometry and alignment. Individual SiNWs are good candidates for high resolution optical sensing and allow for tuning of optical absorption by precise control of the nanowire geometry and orientation. The *p-i-n* silicon nanowires are highly sensitive to the intensity and polarization of the incident light. These top-down fabricated SiNWs can be easily integrated in high density arrays for enhanced light absorption, resulting in imaging sensors with nanoscale spatial resolution.

KEYWORDS

Silicon nanowire, gate-all-around nanowire FET, photodetector, *p-i-n* photodiode, optical sensor.

INTRODUCTION

Semiconductor nanowires have gained much attention recently due to their potential as the next building blocks in microelectronics, sensors, solar cells, photovoltaics, and optical systems [1-5]. Nanowires due to their one-dimensional nature exhibit unique electrical, mechanical, thermal, and optical properties not found in bulk materials and thin films. Downscaling of the active sensing material and large surface-to-volume ratio allows for enhanced sensitivity in chemical, biological, and optical nanowire sensors [3-5]. Silicon nanowires, with diameters on the order of the wavelength of light, show strong resonant field enhancement of the incident light, so they are good candidates as highly sensitive photodetectors for integrated nanophotonic systems, as well as optical biosensor systems, CMOS image sensor arrays, optical modulators, switches, and interconnects.

Efficient implementation of nanowire sensors requires on-chip integration with transistors for accurate and automated signal processing. Many fabrication efforts have involved bottom-up grown nanowires that are deposited on pre-fabricated contact electrodes and control electronics by suspension in liquid or transferred using micro-contact printing [3,5]. However, the mechanical and electrical contacts in these devices are not well controlled and not reproducible. An alternative solution is to define nanowires lithographically by a top-down approach [8-9]. Many top-down fabricated nanowires use electron-beam lithography or focused ion beams (FIB) to define SiNWs. This paper demonstrates individual gate-all-around (GAA) single-crystalline silicon nanowires (SiNWs) as optical intensity and polarization sensors. These nanowires are fabricated in a top-down CMOS front-end process. The GAA silicon nanowires are fabricated in well-defined locations with high-quality electrical contacts, and controlled geometry and alignment. The results in this work demonstrate that individual SiNWs are good candidates for high resolution optical sensing and allow for tuning of the optical properties of the nanoscale devices by precise control of the nanowire geometry and orientation of the incident light.

SILICON NANOWIRE OPTICAL SENSORS

Semiconductor nanowire photodetectors have attracted increased attention due to their potential for very high sensitivity detection for optical communication systems, medical, imaging, and defense applications. Nanowire photodetectors can be realized using both hetero- and homo- p-n junctions. Many of the current nanowire photodetectors involve cross-nanowire assemblies configured as a p-n junction photodiodes [5-6]. Individual silicon nanowire photodetectors are particularly interesting for detection in the visible and near infrared (IR) spectrum, because of their smaller size and the possibility of integration with CMOS technology. The large surface-to-volume ratio of nanowires gives rise to new physical properties that allow for novel physical effects to play a key role in the device behavior.

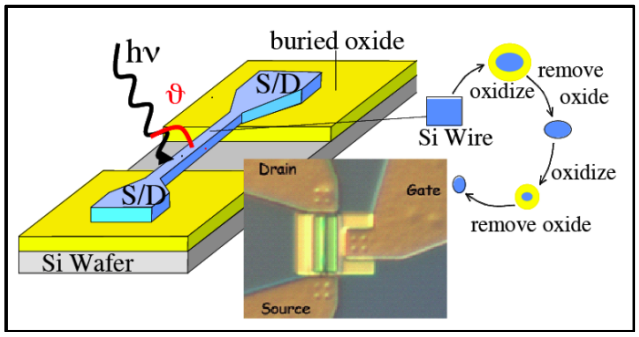

Figure 1: Schematic of single crystalline silicon nanowire optical sensor. The inset shows a top view the fabricated silicon nanowire field effect transistor.

As the incident light strikes the surface of a nanowire photodetector, the absorbed photons create free electron and hole pairs. If the absorption occurs in the junction's depletion region (or one diffusion length away from it), these carriers are swept away from the junction by the built-in field, resulting in a photocurrent. This photocurrent is sum of the dark current and the light current. The dark current includes a thermally-generated portion, and defect-mediated generation current in the semiconductor junction. The dark current must be

accounted for by calibration since it is a source of noise in optical systems. Photo conductance involves several mechanisms, namely the absorption of the incident light, carrier photo-generation, and carrier transport. The steady state photocurrent density is defined as [4]:

$$I_{Ph} = \frac{\eta^* P_{OPT}}{\hbar\omega} \frac{eF\mu_n\tau}{l} \quad (1)$$

where, P_{OPT} is the incident optical power, η^* is the photo-generation quantum efficiency, $\hbar$ is the reduced Planck constant, ω is the frequency of the incident light, F is the applied (or internal) electric field ($F=V/l$) across the nanowire length, l, and μ and τ are the carrier mobility and lifetimes. Because of the large surface-to-volume ratio, nanowires have an extremely high density of surface states. Therefore, due to the pinning of the Fermi energy at the surface, NWs exhibit a depletion space-charge layer, which provides physical separation of electrons and holes and leads to potentially enhanced carrier lifetime.

The sensitivity of a photodetector can be defined in terms of the number of charge carriers which pass between the electrodes (drain and source) per second for each photon absorbed per second that creates an electron-hole pair. The responsivity is then defined as the ratio of the generated photocurrent to the incident light power (A/W). Even though silicon is an indirect semiconductor, high absorption efficiencies are possible because of the resonant enhancement effects occurring in SiNWs [6]. Unlike nanowire ensembles where the scattering response dominates, individual SiNWs are good candidates for sensitive sensing and tuning of optical absorption properties by precise control of the nanowire geometry and orientation. The absorption coefficients of individual silicon nanowires depend on diameter of SiNWs, on the wavelength of the illuminating light, the angle of incidence, and the polarization of the incident light. In the case of thin NWs ($r<\lambda$, $r<100$nm), the major mechanism that leads to polarization dependence of photoconductivity is the dielectric confinement of the optical electric field due to the difference between the dielectric constants of the nanowire, ε, and the environment, ε_o. The ratio of absorption coefficient for light polarization parallel and perpendicular to the NW axis is given by [4]:

$$\frac{\alpha_{\parallel}}{\alpha_{\perp}} = \left|\frac{\varepsilon+\varepsilon_o}{2\varepsilon_o}\right|^2 \quad (2)$$

The anisotropy of the optical absorption results in photocurrent amplitude varying as:

$$I_{Ph} = I_{Ph}^0 cos^2\vartheta \quad (3)$$

where ϑ is the light polarization angle with respect to the principal nanowire axis (See Fig.1). Light polarization dependence of photoconductivity has been observed in single nanowires of a variety of material systems [6].

Figure 2 shows a schematic of vertical and lateral *p-i-n* nanowires, as well as a large area photodiode, used as optical polarization and intensity sensors. A *p-i-n* photodetector functions similar to a *p-n* junction photodiode, expect that the depletion region is wider and almost entirely confined to the intrinsic area of the detector. The wider depletion region results in a larger volume, where the electron-hole pairs can be generated with an incident photon, resulting in higher sensitivity and also faster response time due to the reduced junction capacitance. As a photodetector, the *p-i-n* diode is reverse biased; the source (p) is grounded, a positive voltage is applied to the drain (n), and a voltage is applied to the gate. Gate allows the electric field and therefore the carrier concentration in the nanowire to be controlled in the conjunction with the source/drain bias. With this structure, it is possible to accumulate, deplete, and invert the silicon nanowires while controlling the field across the length of nanowire with the source/drain bias.

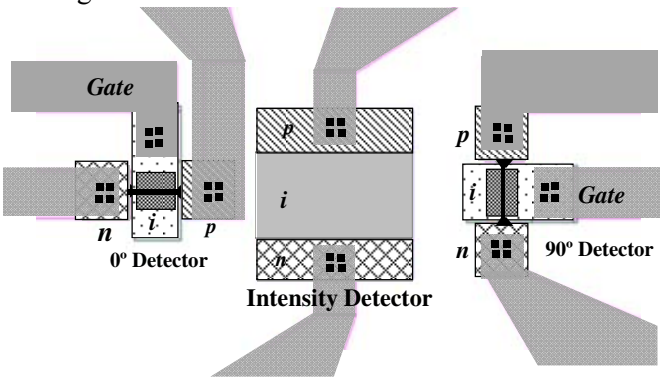

Figure 2: Schematic of the area intensity detector and gated p-i-n silicon nanowire as 0° and 90° polarization sensors.

FABRICATION PROCESS

The gate-all-around single-crystalline silicon nanowires were fabricated in a top-down CMOS-compatible front-end process. The gated *p-i-n* silicon nanowires along with the intensity photodetector area shown in Fig.2 were fabricated using the process flow summarized in Fig.3. Starting with 150mm silicon-on-insulator (SOI) substrates, the silicon nanowires, contact pads, and area detectors are defined in the silicon device layer using a single photolithography and reactive ion etch (RIE) step (Fig.3(a)). Using a nitride hard mask, the source and drain areas are doped using ion implantation steps, the remaining nitride is removed, and the dopants are activated using rapid temperature anneal steps. Another nitride hard mask layer is deposited on the SiNW and pads and removed on top of the nanowire to define the trench area ((Fig.3(b)). The buried oxide layer is then etched away in hydrofluoric acid (HF) to suspend the nanowire above the substrate in the trench area. The lithographically defined nanowires have starting dimensions of 300-500nm. To reduce the diameter of the SiNW to nanoscale, a repeated series of oxidation and etch steps are used resulting in nanowires as small as 50nm (Fig.3(c)). A gate oxide with thicknesses varying 75-125Å is then grown on the SiNWs (Fig.3(d)). A polysilicon layer is then deposited and patterned, which defines the surrounding gate (Fig.3(e)). A standard interlayer dielectric (ILD) is deposited and planarized using a chemical mechanical polish (CMP) step. Next contact vias are patterned and etched (Fig.3(f))

followed by tungsten deposition to contact the source/drain areas. This is followed by sputtering and definition of Al contact pads (Fig.3(g)). A nitride layer is then deposited and patterned as the release etch mask. Finally the silicon nanowires are released in a vapor HF process resulting in the final cross section in Fig.3(h). This process allows for large metal–silicon contact areas through standard W plugs that are connected seamlessly to SiNWs, resulting in small contact resistance and good ohmic contact.

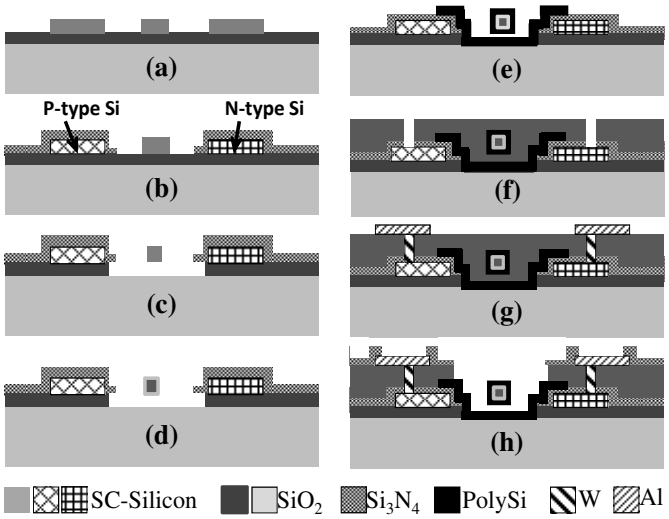

Figure 3: Process flow for the silicon nanowire optical sensors shown in Fig.1.

Figures 4(a) and (b) show top-view scanning electron microscope (SEM) images of the fabricated bare and gated silicon nanowires. Figure 4(c) shows the cross-sectional SEM of a gated SiNW suspended above substrate. Figure 4(d) shows a transmission electron microscope (TEM) image of a gated single-crystalline silicon nanowire. The trapezoidal shape of the nanowire in Fig.4 (c) is due to the silicon RIE etch profile and the orientation-dependent oxidation of the 3D nanowire structures. A subsequent high-temperature annealing step would allow for symmetric nanowire cross-sections.

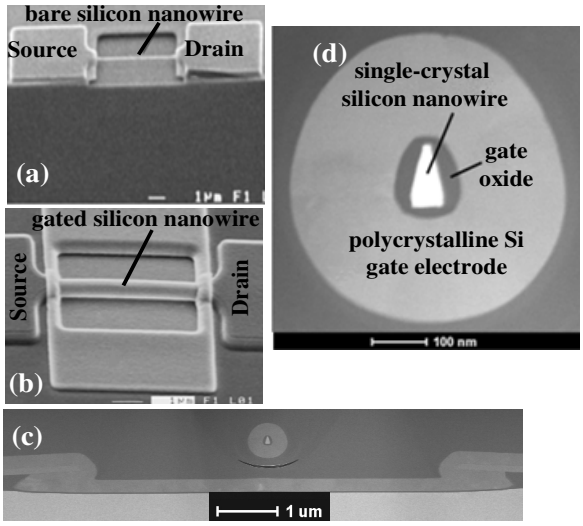

Figure 4: SEMs of (a) bare single crystalline silicon nanowire (b) gated single crystalline silicon nanowire (c) Cross-sectional SEM of gated silicon nanowire (d) TEM showing single crystalline silicon nanowire with wrap-around polysilicon gate.

RESULTS AND DISCUSSION

The silicon nanowires were wire-bonded to a standard ceramic package for electrical and optical characterization. Figure 5 shows the performance of the silicon nanowire field effect transistors (FETs) fabricated using the process in Fig. 3. The SiNWs have a diameter of ~75nm, and length of 5µm. These SiNW FETs have demonstrated repeatable performance with threshold voltages of ~0.2V and subthreshold slopes of ~80mV/dec [7,9]. Gate-All-Around Si NWs allow for ultimate electrostatic control of the FET channel to reduce short channel effects, making them ideal candidates for new integration approaches and novel multi-domain (optical/mechanical/electrical) sensors.

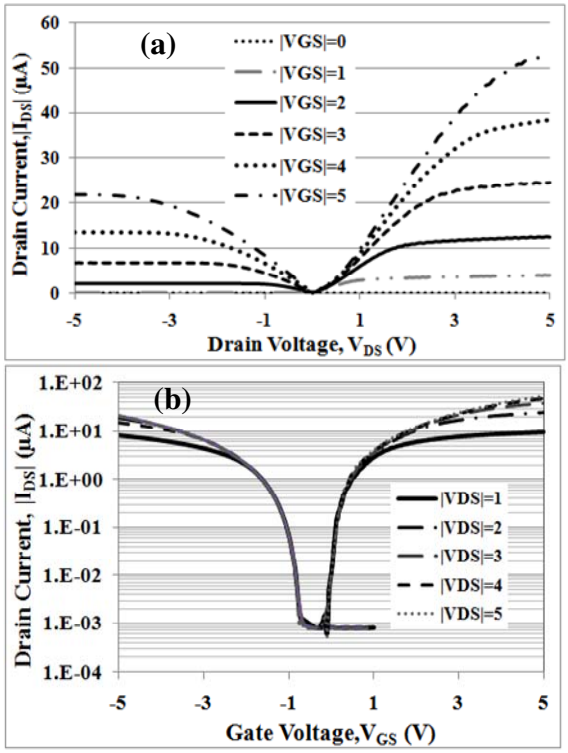

Figure 5: Electric characterization of n-type and p-type GAA SiNW FETs. (a) I_{DS}-V_{DS} measurements for V_{GS} varying from 0 to 5 V (b) I_{DS}-V_{GS} measurements for V_{DS} varying from 1 to 5 V. The source was grounded for all these measurements.

The photocurrent response of the SiNWs was measured using a HP4155B precision semiconductor analyzer, with a stabilized Helium-Neon laser beam (λ=633nm) focused on the sample through a polarization rotation setup. Figure 6 shows the response of the SiNWs increases from <1pA to 1.2nA as the intensity of the laser is increased from 0.15µW to 2.27µW. Figure 7 demonstrates the silicon nanowire response is highly sensitive to the orientation of the nanowire. The photocurrent depends on the whether the illumination is perpendicular or parallel to the SiNW. In the case of lateral nanowire, the reduced illumination area and non-uniform absorption across the junctions result in a much lower photocurrent and responsivity. Figure 8 demonstrates that the silicon nanowire response is sensitive to the polarization angle of the incident light; the responses of the nanowires were normalized by the

response of the intensity area detector. In these devices, alignment is essential for consistent response to both the intensity and polarization of the incident light.

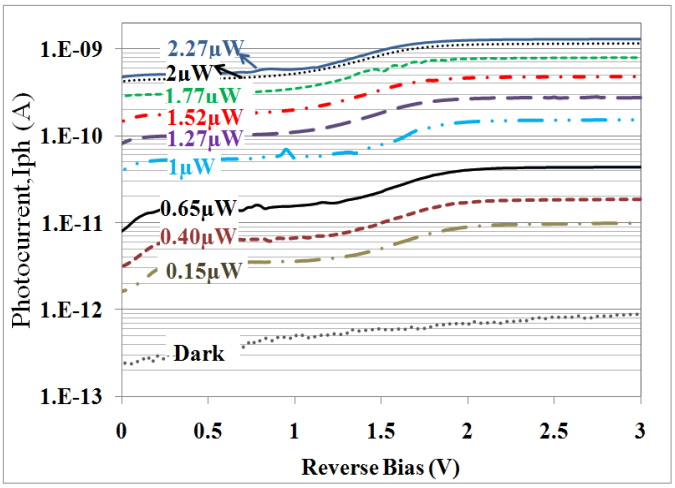

Figure 6: I-V response of a SiNW showing the photocurrent versus reverse bias voltage for laser intensity varying from 0.15mW to 2.27mW.

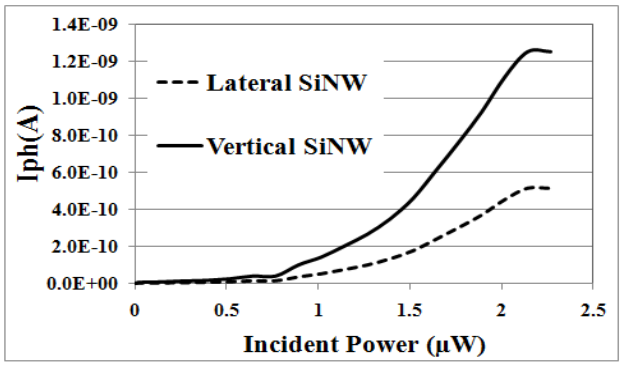

Figure 7: Reponsivity of vertical and silicon nanowires showing the photocurrent vs. incident laser power.

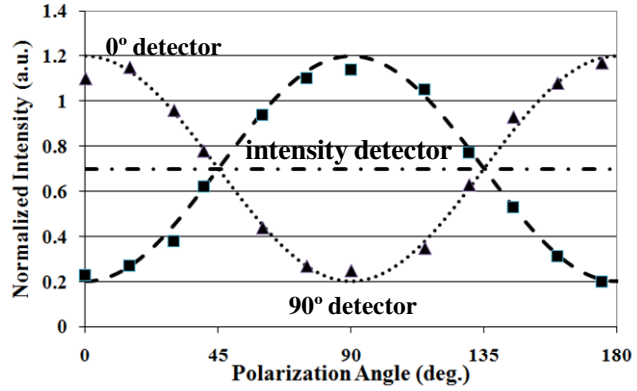

Figure 8: Polarization response of the GAA SiNWs and intensity detector.

CONCLUSIONS

We have demonstrated gate-all-around single crystalline silicon nanowires fabricated using a top-down CMOS-compatible process. We have demonstrated *p-i-n* silicon nanowires as highly sensitive intensity and polarization optical sensors. The size, uniformity, and placement of these top-down fabricated SiNWs can be precisely controlled, making them attractive for high density arrays with enhanced light absorption for imaging sensors with nanoscale spatial resolution. The sensitivity of these nanowires can be drastically increased using these *p-i-n* photodetectors in the avalanche mode, which enables large photocurrent gain [6,10] and ultimately nanoscale photodetectors capable of single photon detection.

ACKNOWLEDGEMENTS

The authors would like to thank the staff at the Microelectronics Development Laboratory at Sandia National Labs for fabrication of the devices. Sandia is a multi-program laboratory operated by the Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's Nuclear National Security Administration under contract DE-AC04-94AL85000.

REFERENCES

[1] Y. Cui, Z. Zhong, D. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," Nano Lett., vol.3, 2003, pp.149-52.

[2] E. C. Garnett and P. Yang, "Silicon nanowire radial p-n junction solar cells," *J. Am. Chem. Soc.*, vol. 130, 2008, pp. 9224-5.

[3] Y. Cui, Q. Wei, H. Park, C. M. Lieber, "Nanowire nanosensors for highly sensitive and selective detection of biological and chemical species," *Science* 293:1289-92.

[4] C. Soci, A. Zhang, X.-Y. Bao, H. Kim, Y. Lo, and D. Wang, "Nanowire Photodetectors," *J. of Nanosci. Nanotech.*, Vol.10, 2010, pp.1-20.

[5] Z. Fan, J. C. Ho, Z. A. Jacobson, H. Razavi, and A. Javey, "Large-Scale, heterogeneous integration of nanowire arrays for image sensor circuitry," PNAS, vol.105, 2008, pp.11066-70.

[6] O. Hayden, R. Agarwal, and C. M. Lieber, "Nanoscale avalanche photodiodes for highly sensitive and spatially resolved photon detection." Nature Mat., vol.5, 2006, pp. 352-356.

[7] B. Draper, M. Okandan, and M. Shaneyfelt, "Radiation response of a gate-all-around silicon nanowire transistor," IEEE Trans. Nuclear Sci., vol.56, 2009, pp.3274-9.

[8] I. Park, Z. Li, A. P. Pisano, and R. S. Williams, "Top-down fabricated silicon nanowire sensors for real-time chemical detection," Nanotechnology, vol. 21, 2010, 015501-9.

[9] S. Monfray, T. Skotnicki, Y. Morand, S. Descombes, P. Coronel , P. Mazoyer , et al, "50 nm-Gate all around silicon on nothing devices: a simple way to co-integration of GAA transistors within bulk MOSFET process," VLSI Technol Dig 2002, pp. 108–9.

[10] A. Zhang, S. You, C. Soci, Y. Liu, D. Wang, and Y. Lo, "Silicon Nanowire detectors showing phototransistive gain," *App. Phys. Lett.* **93**, 12110 (2008)

CONTACT

* Maryam Ziaei-Moayyed, tel: +1-510-541-1320; mziaeim@sandia.gov