Degradation Mechanisms and Characterization Techniques in SiC MOSFETs at High Temperature Operation

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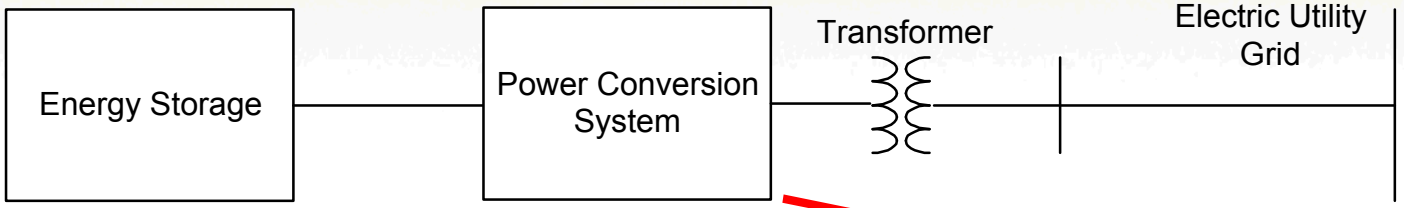
Power Conversion System



- Heart of the power conversion systems are semiconductor switches that determine overall cost, reliability, and performance (efficiency, power quality)
- Most systems today utilize silicon-based semiconductor switches (IGBTs, thyristors)
- Recent advances in semiconductor materials include wide-bandgap devices that offer high-voltage breakdown and high-temperature operation (less cooling required); examples are Silicon Carbide (SiC) and Gallium Nitride (GaN) based devices

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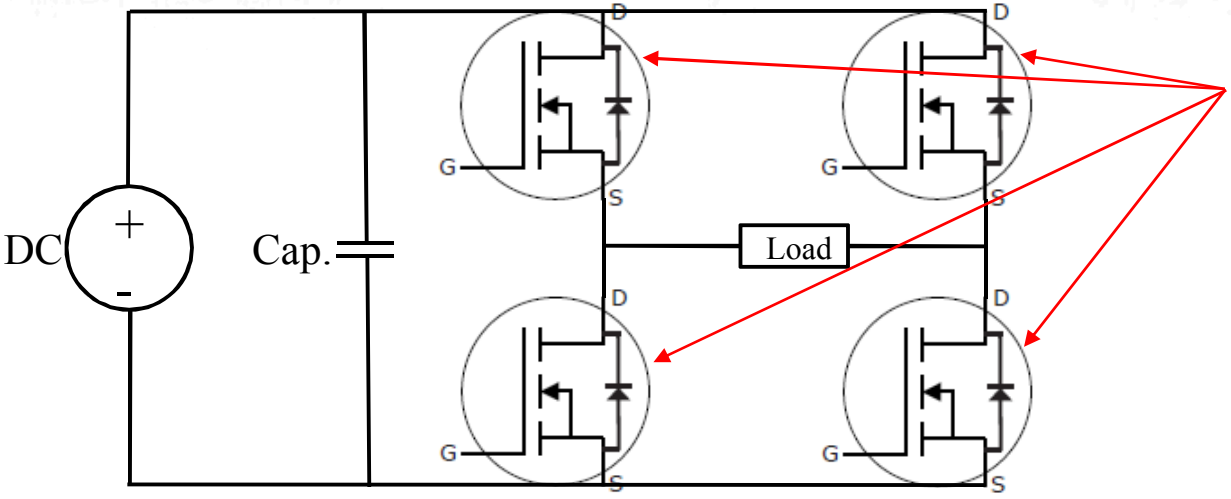
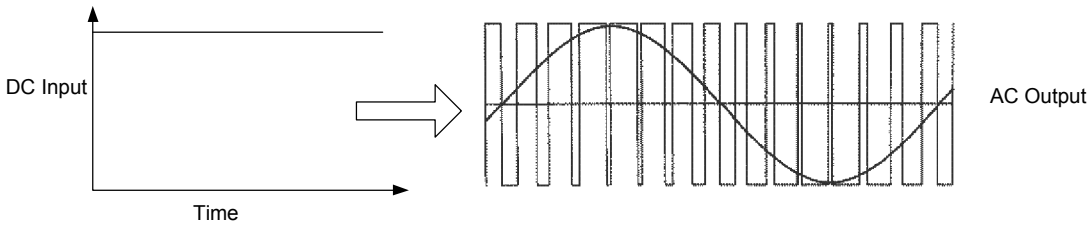
Power Electronics and Power Conversion

- Example power conversion system (H-bridge inverter):



TO-247-3



- Pulse-Width Modulation (PWM) switching @ ~10 kHz
- Components are subject to multiple stresses: high temperatures, high voltages and currents, high power transients

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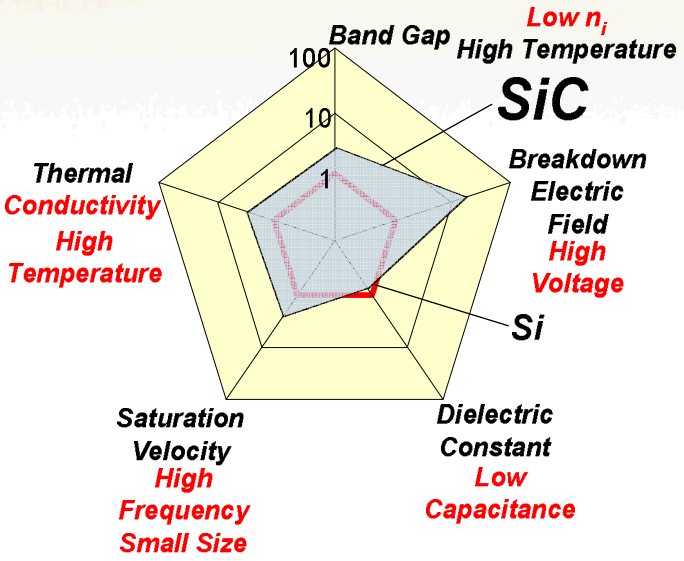
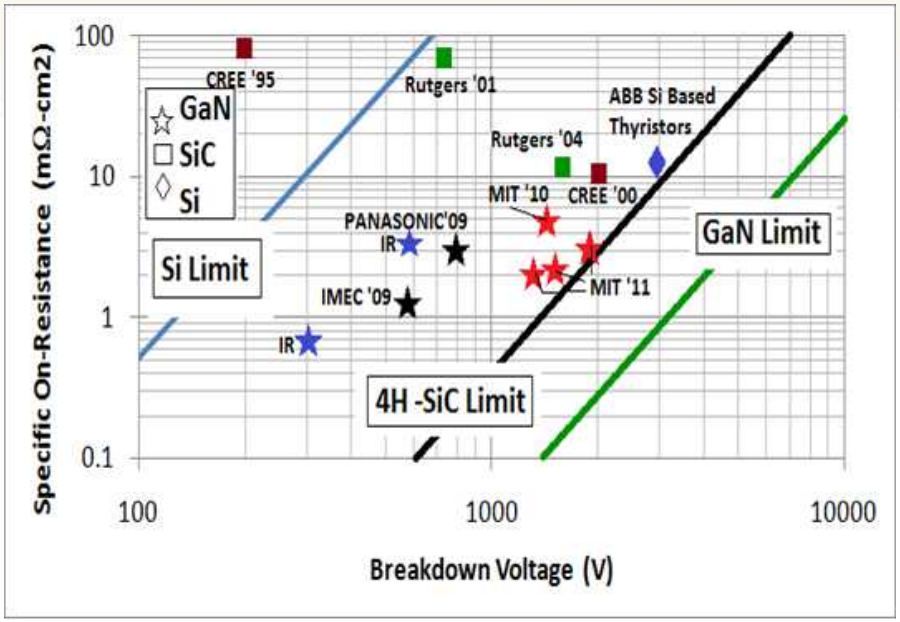
Advantages of SiC Compared to Si



Courtesy of Prof. D. K. Schroder, ASU



Superior properties of SiC translate to better power electronics performance:

- Lower switching and conduction losses (higher efficiency)
- Higher voltage operation (fewer power stages)
- Higher temperature and thermal conductivity (reduced thermal management)
- Smaller system size, reduced weight, lower cost

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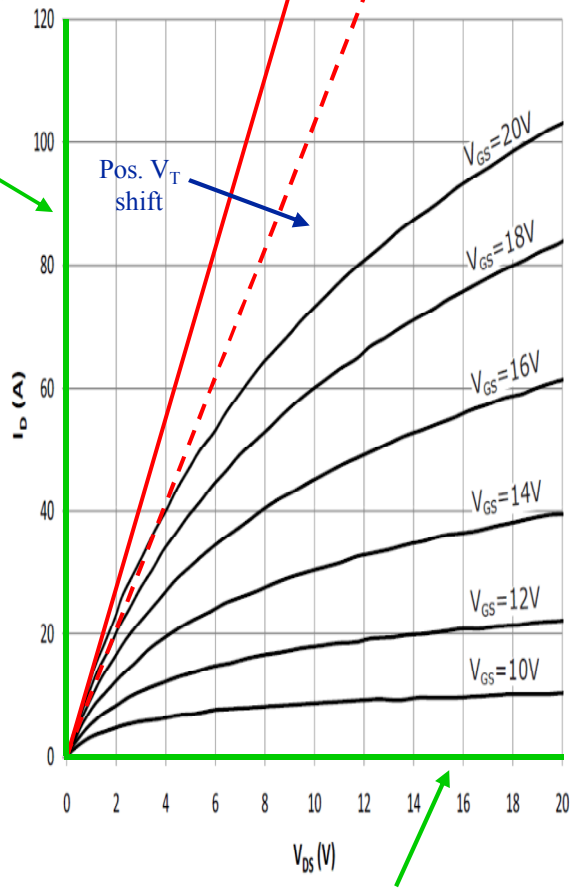
MOSFET Current-Voltage Characteristics

1/slope = On-state resistance

Ideal switch on-state



Ideal switch off-state

Positive threshold voltage shift reduces gate drive (equivalent to smaller applied gate voltage) and results in increased on-state resistance (higher conduction loss)

Non-ideal switch model:

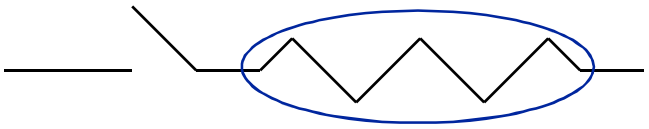


Diagram source: Cree, CMF2012D data sheet

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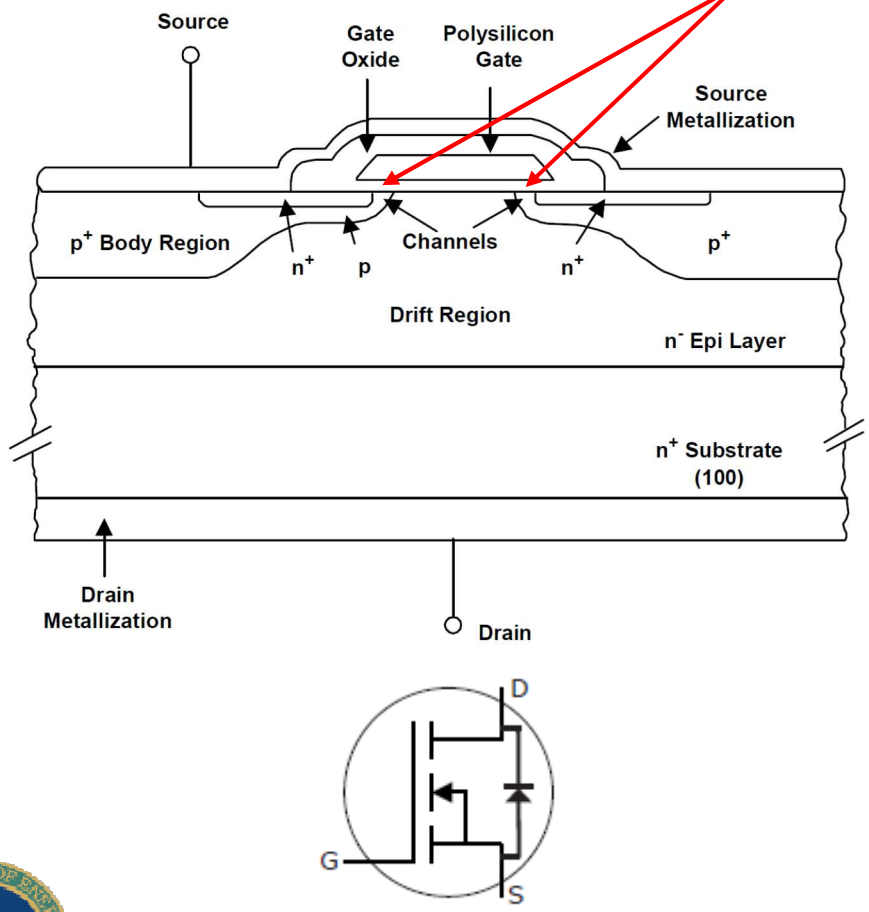
Schematic of Power D-MOSFET

Critical gate oxide interfacial region



Charge injection due to small band offset at SiO_2/SiC interface enhances V_T shift

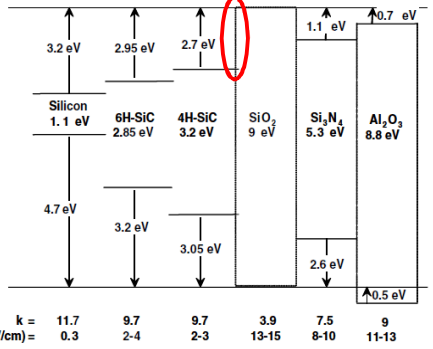


Fig. 1. Dielectric constants, and critical electric fields of various semiconductors (Si, 6H-SiC, 4H-SiC) and dielectrics (SiO_2, Si_3N_4 and Al_2O_3). Conduction and valence band offsets of these are also shown with respect to SiO_2.

Microelectronics Reliability, v. 46, p. 713 (2006).

Diagram source: International Rectifier, "Power MOSFET Basics"

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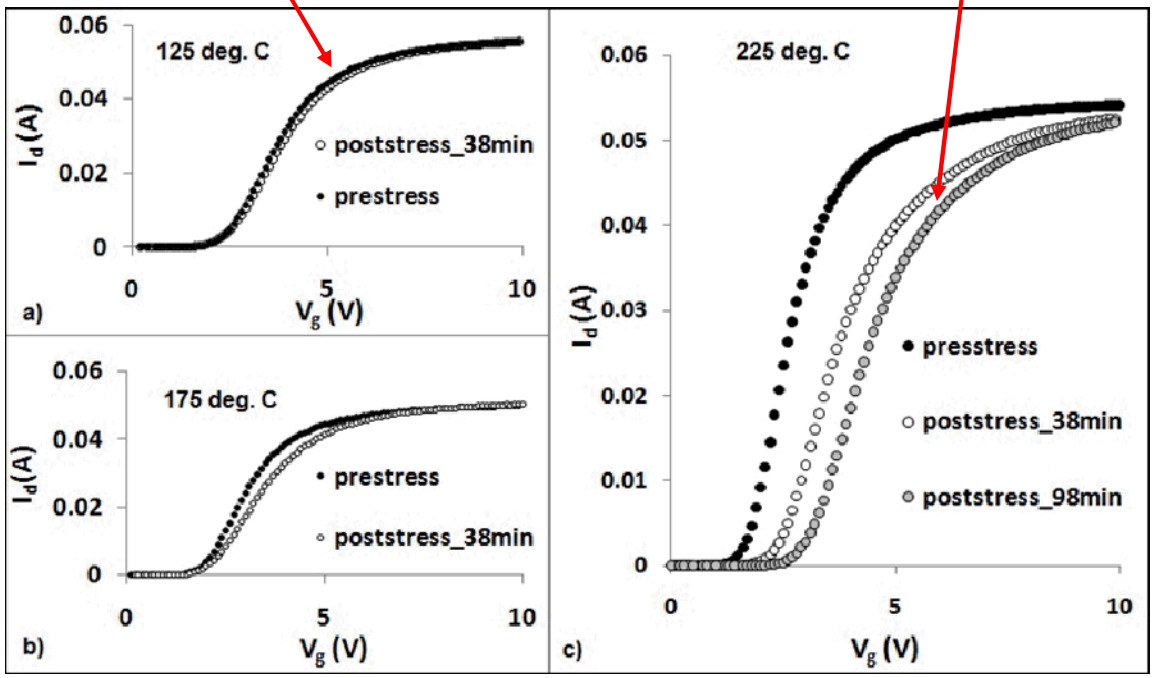
On-State Gate Voltage Stress at High T

Minimal degradation at rated T; severe degradation at high T

TO-247-3

Commercial SiC MOSFET in TO-247 package:

- 1200 V blocking
- 33 A DC @ 25 C
- $T_{case,max}$ = 125 C



Stress: V_{GS} = +20 V, V_{DS} = 0.1 V

S. DasGupta, R. Brock, R. J. Kaplar, M. J. Marinella, M. A. Smith, and S. Atcitty, Appl. Phys. Lett. **99**, 023503 (2011).

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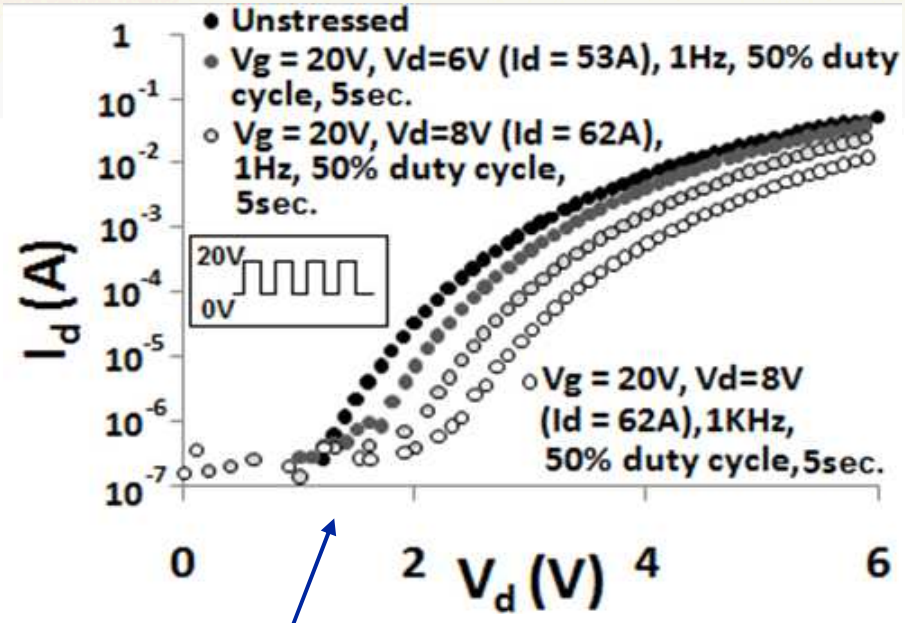
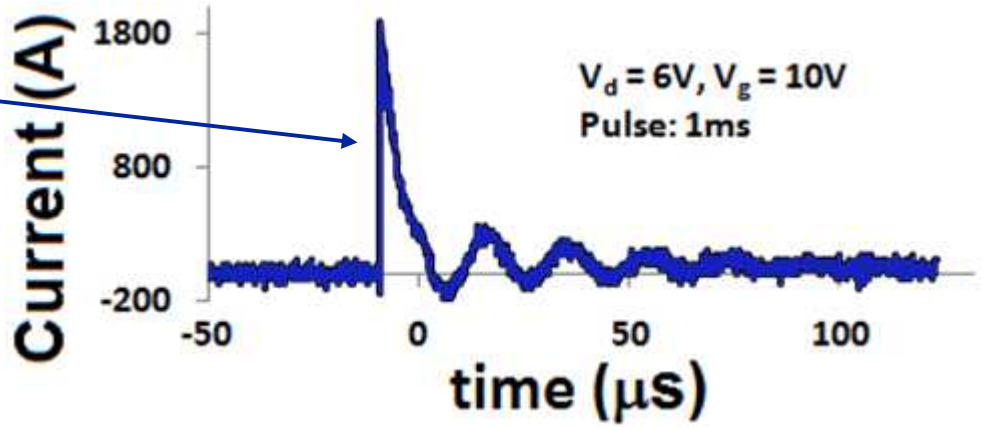
Pulsed Over-Current Operation



High switching transient over-current raises junction temperature (mimics high-T DC operation); transient minimization is therefore critical in system applications

Room T stress and measure



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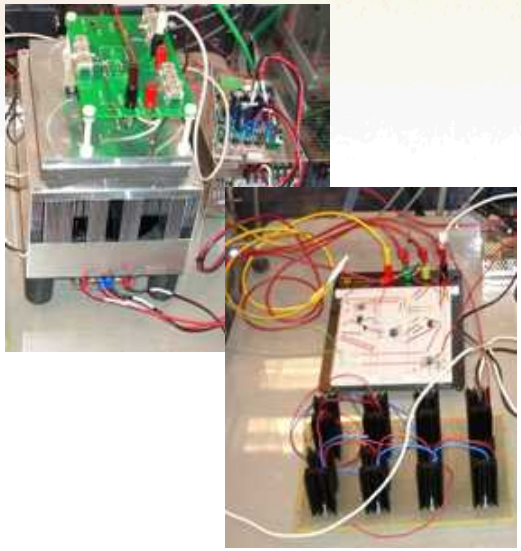
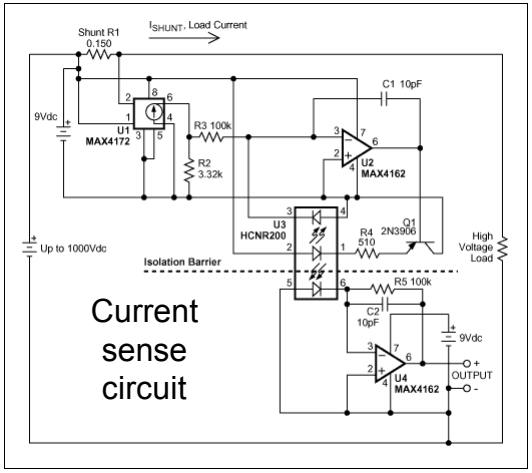
Condition Monitoring (CM) and Prognostics and Health Management (PHM)

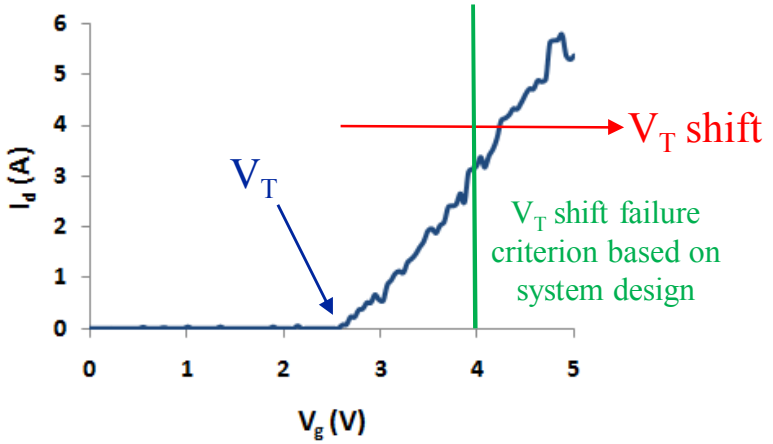
- CM: Monitor component / system health
  - Detect anomalies
  - Flag maintenance needs
- PHM: Includes CM, also predicts time-to-failure
  - Compare data to pre-existing reliability models
  - Optimize premature replacement vs. catastrophic failure
  - Maximizes system availability when unreliable components are utilized

Condition Monitoring (CM) Implementation



- Microcontroller-based stress-measure system
- Breadboard-based prototype is working
- Made using < $25 of COTS components
- Currently integrating components onto single PC board





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Summary/Conclusions to Date

• SiC enables superior semiconductor power switches for enhanced system efficiency; higher voltage; reduced thermal management, size, and weight

• Reliability studies on SiC devices undertaken (e.g. commercially available 1200 V, 33 A, 125 C MOSFET)

• Dissemination of information:
  - Six publications / presentations accepted
  - One submission under review

• Device instability at high temperature and pulsed operation leads to higher on-state resistance and higher conduction losses

• Prototype CM/PHM system has been designed and built to monitor device degradation; working to reduce size and complexity of module

Future Work

- Continue SiC MOSFET device physics studies and refine degradation models; examine other SiC-based devices

- Basic studies of SiO_2/SiC interface using MOS capacitors grown under different process conditions to alleviate V_T shift (collaboration with Auburn University and Arizona State University)

- Integrate CM module onto single PC board; implement PHM using hardware and device physics models

- Investigate competing GaN-based power HEMTs (collaboration with MIT; measurement and design feedback)

- *We gratefully acknowledge the support of Dr. Imre Gyuk of the DOE Office of Electricity Energy Storage Program*