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Sandia National Laboratories

A High Speed, High Temperature Datalink for Geothermal Applications

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Sandia National Laboratories

U.S. DEPARTMENT OF ENERGY | NNSA

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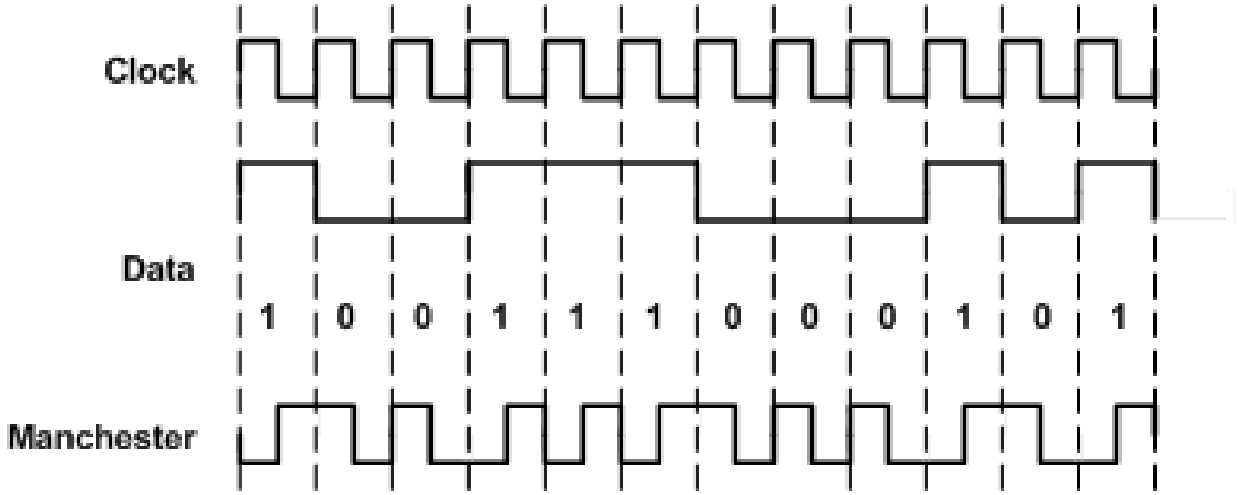
Project Motivation

- A key technical goal of Sandia's Geothermal Research Department is to develop high speed communication links utilizing only high temperature electronics in downhole tool
  - Phase 1*: The goal of this phase was to design an uphole receiver capable of optimizing communications interfacing with Sandia's existing high temperature tools – *complete*
  - Phase 2: The goal of this phase is to design new high temperature downhole transmitter using advanced digital modulation - *ongoing*
  - Separate project: Design and test a high temperature fiber optic transceiver system - *ongoing*
- High speed datalinks are a critical component of logging tools such as televiewers and seismic tools

**Much of the Phase 1 work was completed by an Engineering Clinic team at Harvey Mudd College during the 2010-2011 school year*

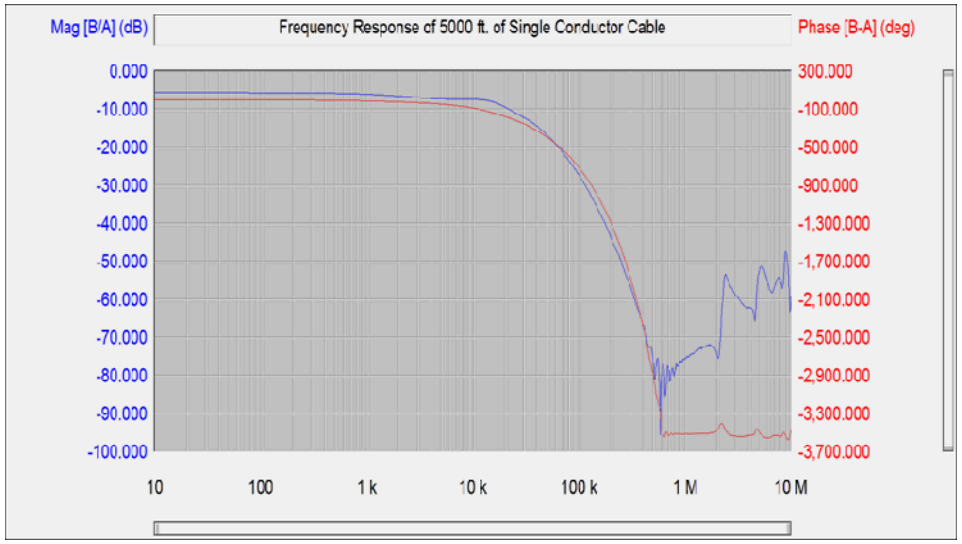
Existing Downhole System

- Sandia's current high temperature tools utilize a Manchester encoded signal to transmit data to the surface
  - Manchester encoding is very simple to implement with high temperature components and the signal can be interfaced to either single or multi-conductor cable

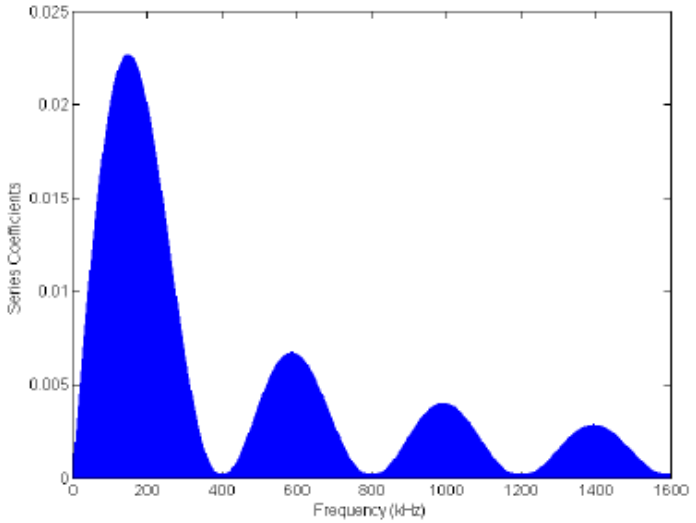


Cable Response – Frequency Domain

- Standard logging cable significantly distorts high data rate signals
- Example below shows the frequency response of 5000 ft. of single conductor cable
  - -3 dB frequency ~ 11 kHz
  - ~ -80dB attenuation at 500 kHz



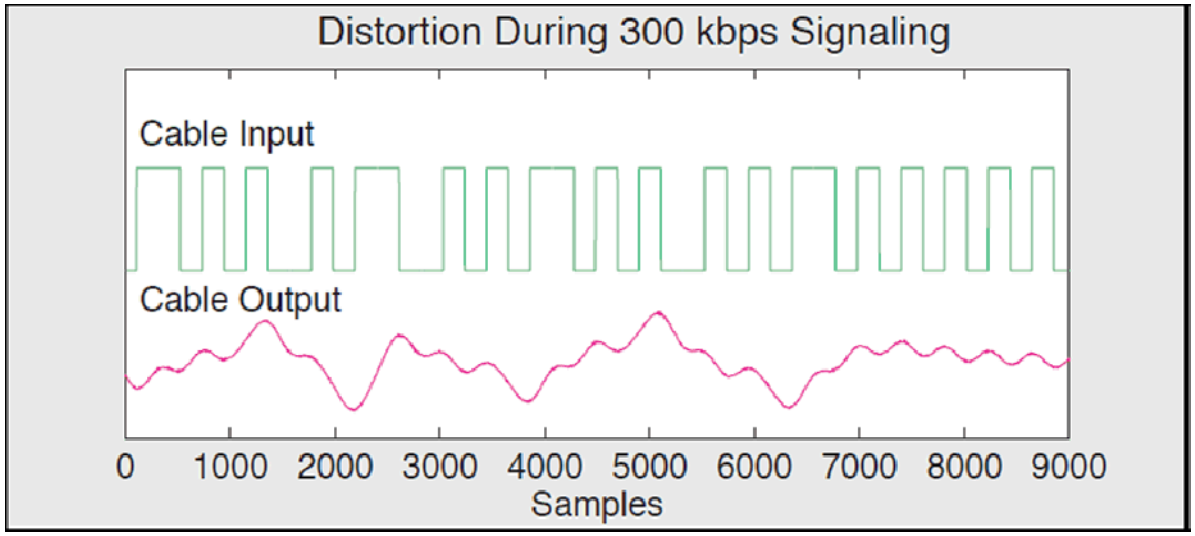
Cable Frequency Response



200 kbps Manchester Signal Magnitude

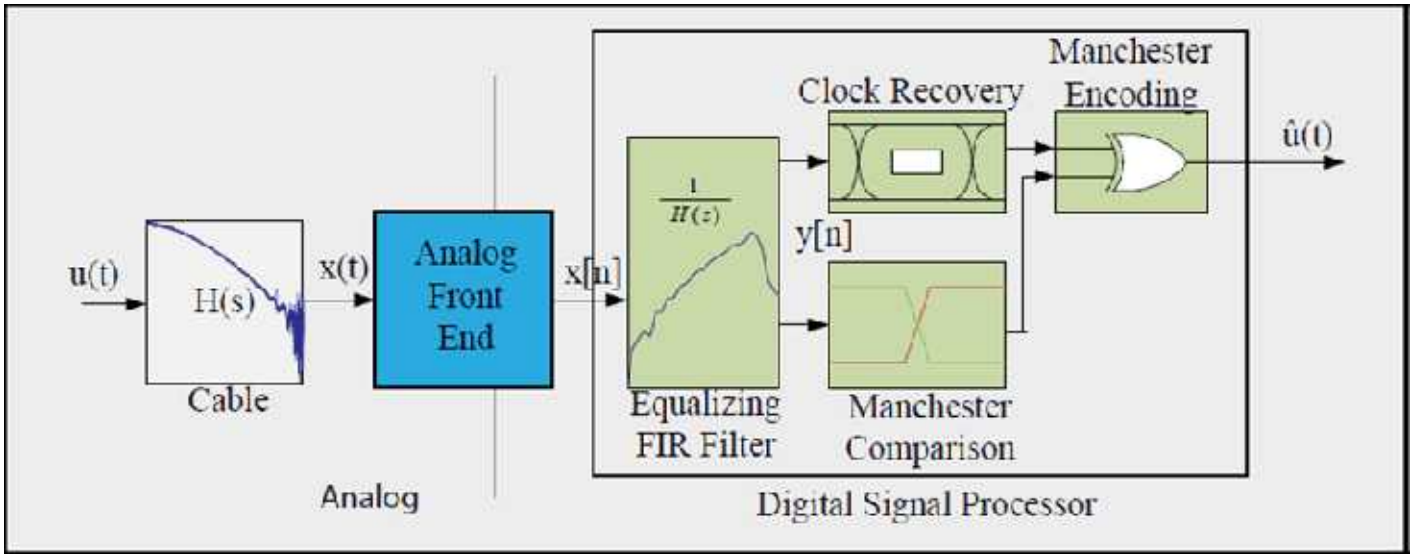
Cable Response – Time Domain

- The time domain manifestation of high frequency attenuation is severe signal distortion
- Typical Manchester receiver circuits rely on sharp signal edges to recover the clock and data
  - Other techniques must be employed to recover distorted signals as shown below



New Receiver Overview

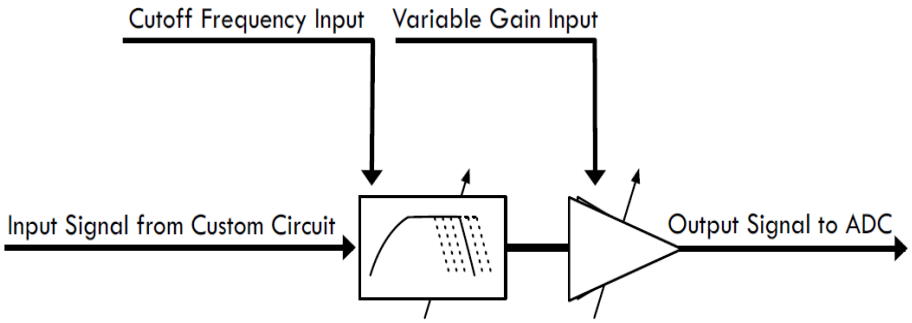
- The design requirements for the new uphole receiver were as follows
  - Achieve ≥ 400 kbps data rate over 5000 ft of single conductor logging cable
  - Minimize the bit error rate (BER)



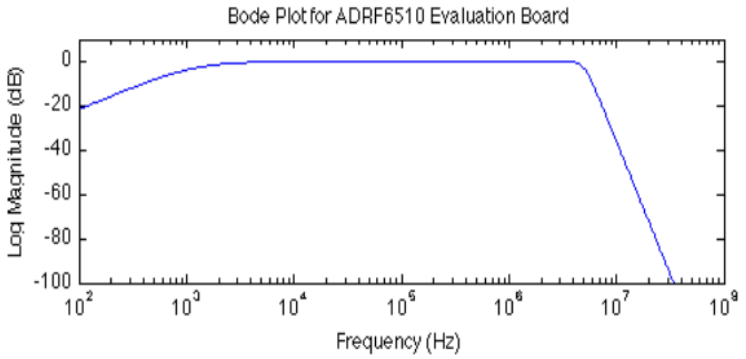
Receiver Block Diagram

Analog Front End

- The analog front end provides power to the downhole electronics and conditions the received signal prior to conversion to the digital domain
- The signal conditioning circuit is implemented using an Analog Devices ADRF6510 amplifier



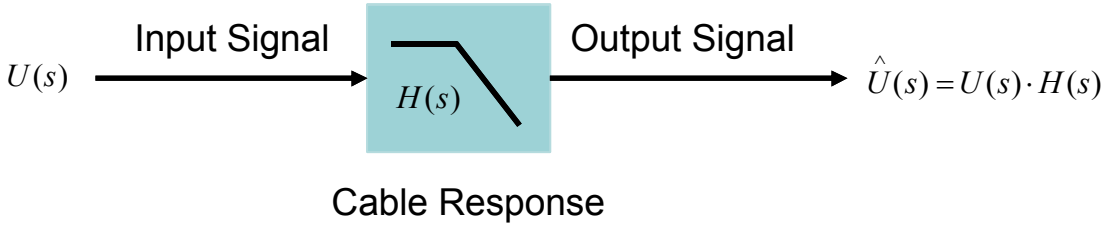
Signal Conditioning Block Diagram



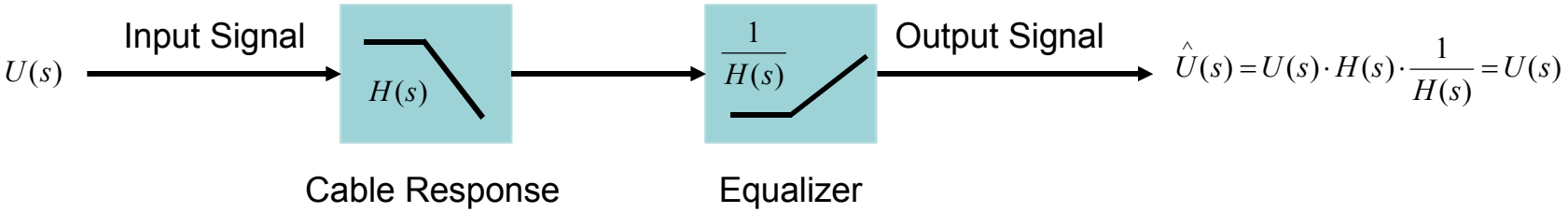
Analog Front End Frequency Response

Cable Equalization

Not Equalized

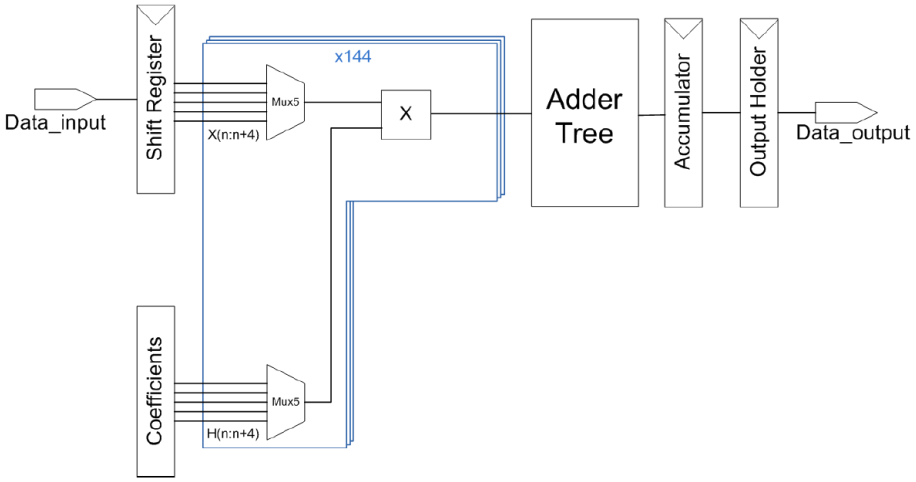


Equalized

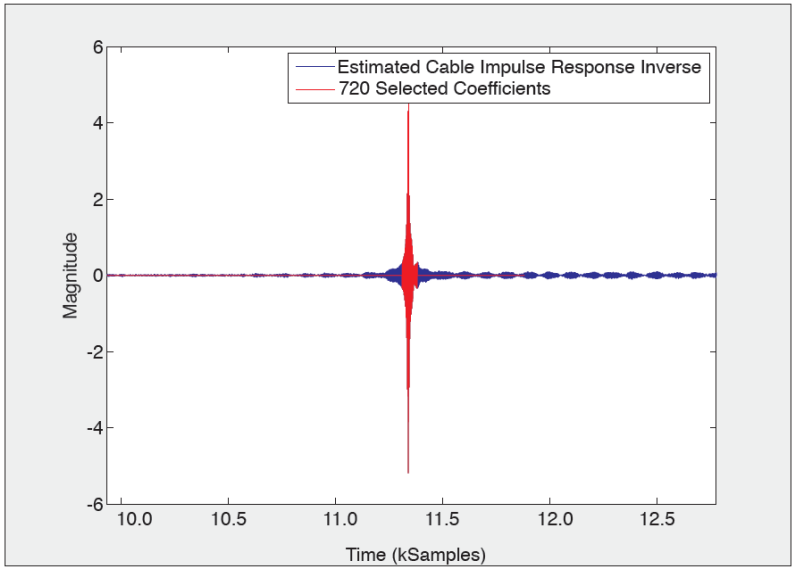


Equalizer Implementation

- The equalizer was implemented on a Altera Cyclone III Field Programmable Gate Array (FPGA) using a 720 tap finite impulse response (FIR) filter
  - 720 coefficients cover a majority of the energy in the cable's inverse impulse response
  - The equalizer clock runs at 25 MHz



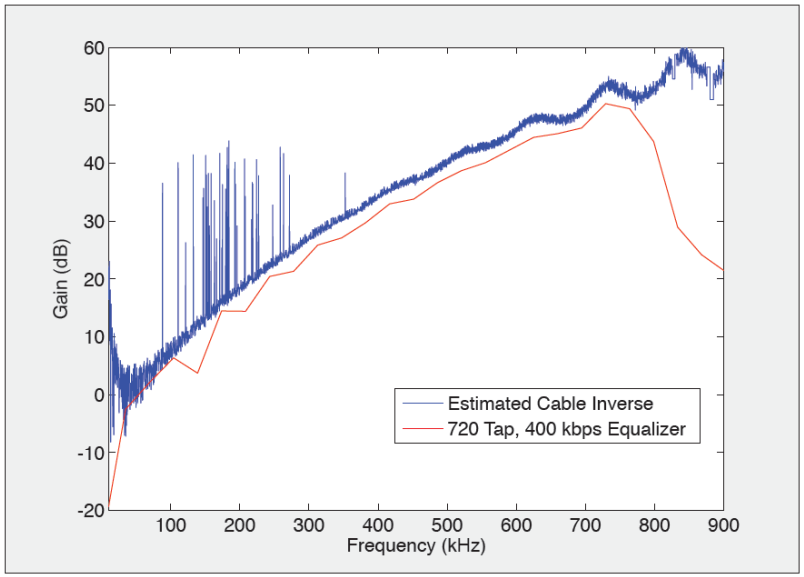
FIR Filter Implementation



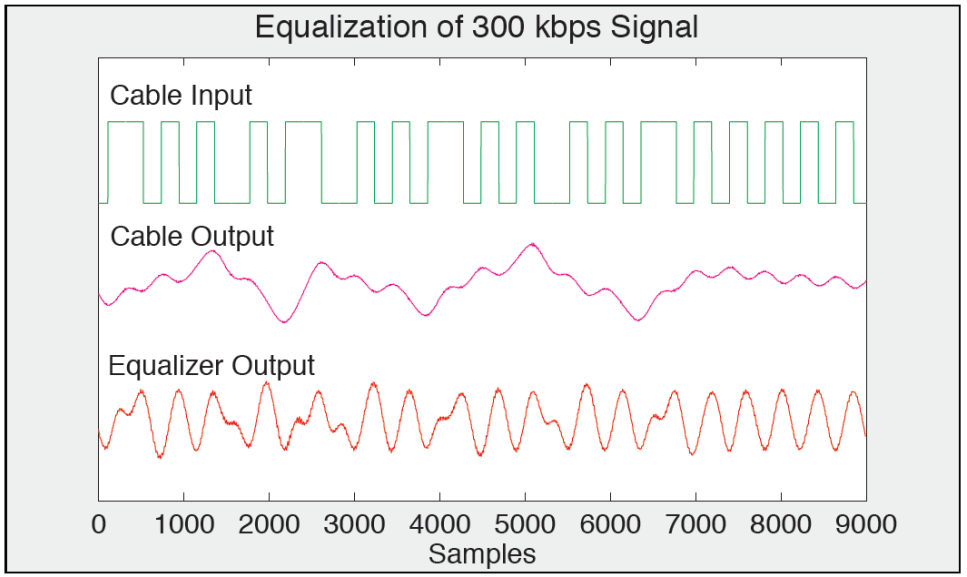
FIR Filter Coefficients

Equalizer Results

- Testing of the equalizer shows it is able to cancel out a large portion of the cable's high frequency attenuation effects



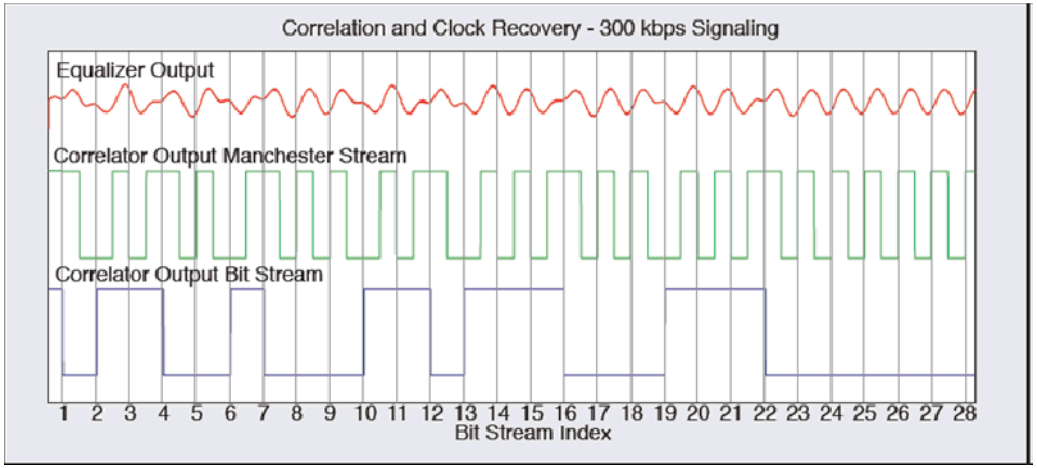
Equalizer Frequency Response



Equalizer Time Domain Results

Clock and Data Recovery

- The clock and data recovery block, which is also implemented in the Cyclone III FPGA, works to take the equalizer output and convert it back into digital clock and data signals
- The system uses a correlator to recovery the data signal and a first order PLL to recover the clock
  - Clock skew is detected by the correlator and fed to the PLL for clock timing adjustment

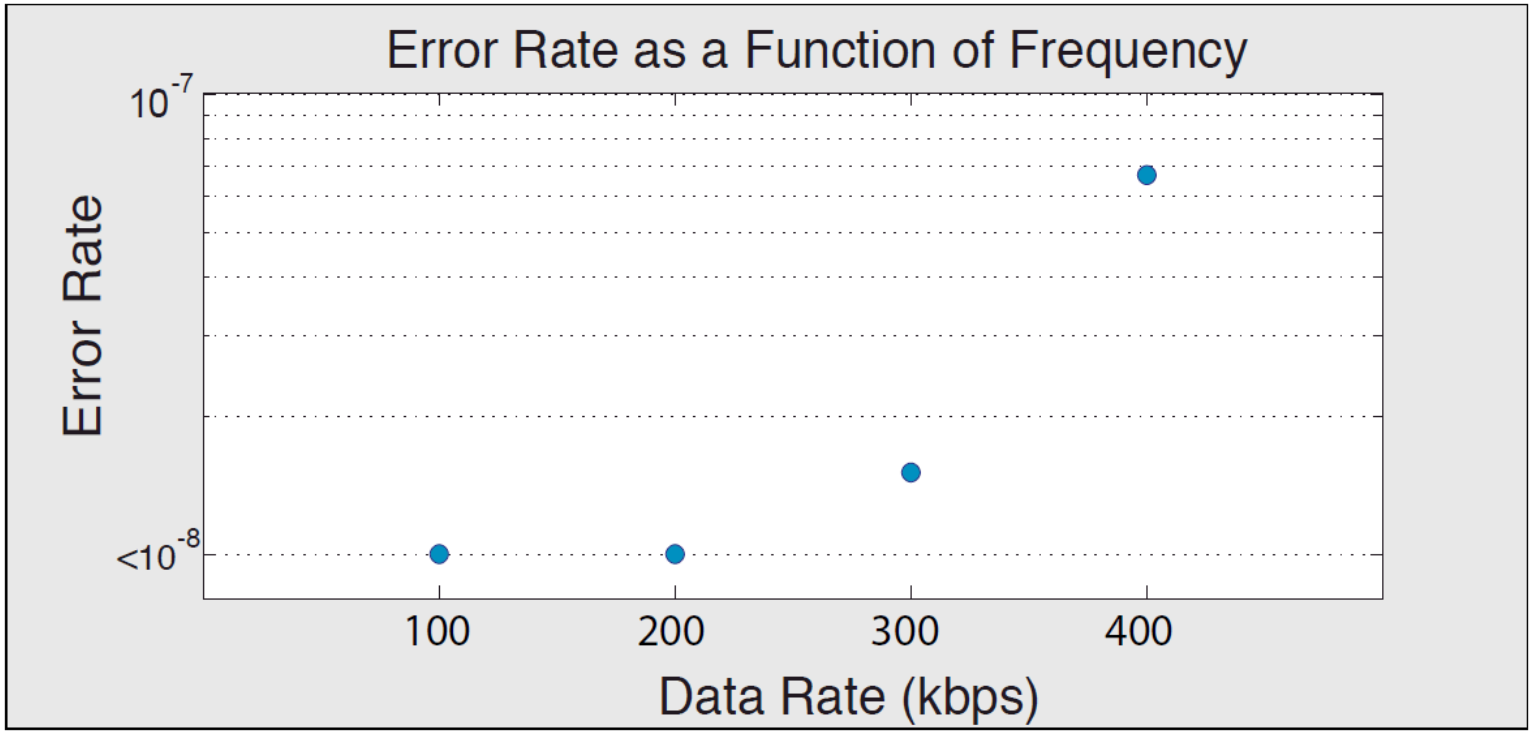


Correlator Output

Bit Error Rate Testing

- Bit error rate testing was performed with a 2^{10} bit pseudorandom bit sequence transmitted over the test cable
- A bit error checker was implemented in the receiver FPGA module
- Approximately 1 billion bits were run through the system at 100 kbps, 200 kbps, and 300 kbps
- Test system was also tested with 30 billion bits at 400 kbps
- All bit errors were recorded in order to calculate bit error rate

Bit Error Rate Results



Conclusions/Future Work

- We have demonstrated a functional uphole receiver capable of operating at 400 kpbs using Sandia's existing downhole high temperature electronics
- Work is underway to explore modifications to the downhole electronics to increase data rate
  - Pre-filtering
  - Digital modulation
  - Error correction
- Since the equalizer and clock and data recovery circuits are implemented in an FPGA their functionality can be easily modified to accommodate changes to the downhole transmitter