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Progress in SiC MOSFET Reliability

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Bias-temperature stress experiments performed on two generations of SiC power MOSFETs from the same manufacturer show reductions in threshold voltage (V_T) shift at elevated temperatures from first- to second-generation. The negative V_T shift is reduced from a range of -1 V to -1.6 V to a range of -100 mV to -300 mV for temperatures from 125°C to 175°C. Plastic-packaged parts show a gate-bias-independent junction leakage current at temperatures above the rated temperature, suggesting that the plastic packaging introduces an extrinsic leakage path. Junction leakage in metal-packaged parts can be significantly reduced by applying a small negative gate bias at elevated temperatures. Switching gate bias temperature stresses show V_T shifts dependent on duty cycle, with a higher duty cycle resulting in a higher rate of V_T shift. Cumulative damage effects may be observed between switching gate bias stresses.

Introduction

SiC is a unique wide-bandgap material in that its native oxide is SiO_2 – an excellent insulator that is particularly useful in creating a field-effect transistor. SiC MOSFETs have been commercially available for over two years with blocking voltages of 1200 V and excellent on-state resistances ($R_{DS\text{-}on}$) as low as 80 mΩ. In addition, SiC devices can *in theory* operate at higher temperatures than competing Si devices. SiC MOS technology could offer major system-level improvements due to reduced size and weight for motor drives, hybrid electric vehicles, photovoltaic inverters, and even grid-level applications such as flexible AC transmission systems (FACTS) (1)-(2). Currently, the most significant hurdles to market penetration are reliability and cost, the latter of which is improving rapidly as the SiC technology becomes more widespread.

SiC MOSFET reliability challenges stem mainly from SiC/SiO_2 interface quality as well as interactions between devices and packaging. When operated under high gate electric fields and high temperatures, threshold voltage instabilities are often observed both in SiC MOSFET (3)-(4), and MOS capacitor (5)-(6) structures. Our constant-bias stress measurements comparing first- and second-generation commercially available SiC MOSFETs indicate significant progress on this front. Switching bias measurements performed on second generation parts simulate a more realistic operating condition and show that V_T degradation depends on duty cycle.

Junction leakage current at elevated temperatures is also a significant reliability concern. Comparisons of leakage measurements for first-generation SiC MOSFETs in plastic and metal packaging show increasing leakage current at high blocking voltages as temperature increases. However, the leakage current is worse for plastic packaging.

Applying a negative voltage on the gate can significantly reduce the leakage current for metal-packaged parts, but has no effect on plastic-packaged parts.

Experimental Details

First- and second-generation power MOSFETs from the same manufacturer were subjected to a variety of temperature and bias stresses. The first-generation devices that were tested had both plastic and metal packaging. The temperature rating for the first-generation devices is 125°C for the plastic-packaged parts and 225°C for the metal-packaged parts. The second-generation devices that were tested only had plastic packaging, and their temperature rating is 225°C (testing of metal-packaged devices is planned for future experiments). Current-voltage measurements were performed using a Keithley 2651A high-current sourcemeter coupled with a Keithley 2601A for gate control. For forward-blocking leakage measurements a Keithley 2410 high-voltage sourcemeter was used. First-generation parts were heated using a Corning ceramic hotplate for leakage measurements and a hot chuck for all other tests. Second-generation parts were heated using a VWR aluminum hot plate. Hot plate temperatures were verified using a temperature probe. Each part was allowed to stabilize at a given temperature for thirty to forty minutes after the desired temperature was reached, or until the gate sweep curve stopped shifting. After the gate bias stress at a given temperature, gate-sweep characterization curves were measured to ascertain changes in the MOSFET's V_T. Following this, in order to revert the device to its original condition, a gate bias of opposite polarity to the stress gate bias was applied in small time increments until the characterization gate sweep curve matched the initial gate sweep curve at that temperature. V_T is taken to be the voltage resulting in I_D = 10 mA, with the drain voltage at 100 mV. For leakage current measurements, the drain voltage was swept from 0 V to 900 V for gate biases of 0 V, -2 V, and -5 V at various temperatures.

Results

Threshold Voltage Shift

V_T decreases significantly for SiC MOSFETs compared to Si MOSFETs simply as a function of temperature, without considering gate bias stress. This is due to the higher interface trap density of the gate oxide for SiC devices, since at elevated temperature the surface potential under strong inversion is reduced along with the concentration of interface traps that must be charged or discharged to achieve that potential (7). This is demonstrated by the first-generation parts in Fig. 1. The low V_T at elevated temperatures makes further V_T shifts due to bias stress more concerning. This is particularly true for negative shifts.

In order to assess the V_T shift due to electron and hole injection in the oxide, SiC MOSFETs are stressed with positive and negative gate biases for thirty minutes at varying temperatures. Devices from both generations show varying amounts of V_T shift, depending on the magnitude and polarity of the bias, as well as temperature. Constant bias stress results using gate biases of 20 V and -20 V for plastic- and metal-packaged first-generation devices are shown in Fig. 2(a). ΔV_T is relative to the initial V_T at the stress temperature, not room temperature. Positive shifts are likely due to electron injection from the inverted SiC into the oxide (Fig. 2(b)) and negative shifts are likely

due to hole injection from the accumulated p-type SiC into the oxide (Fig. 2(c)). Each type of packaging shows larger negative V_T shifts than positive V_T shifts, indicating that hole injection is a significant issue, similar to concerns in SiO_2 on Si where holes are trapped at oxygen vacancies (E' centers) (8) with analogous models being developed for SiO_2 on SiC (9). Negative V_T shifts appear to be slightly worse for plastic-packaged parts, but the differences are so small it is likely that packaging has no significant effect on ΔV_T. The negative V_T shift at 125°C (the rated temperature for plastic-packaged parts) is -1 V and increases to -4 V at 225°C. The positive V_T shift is below 100 mV at temperatures up to 150°C and reaches 1 V at 225°C.

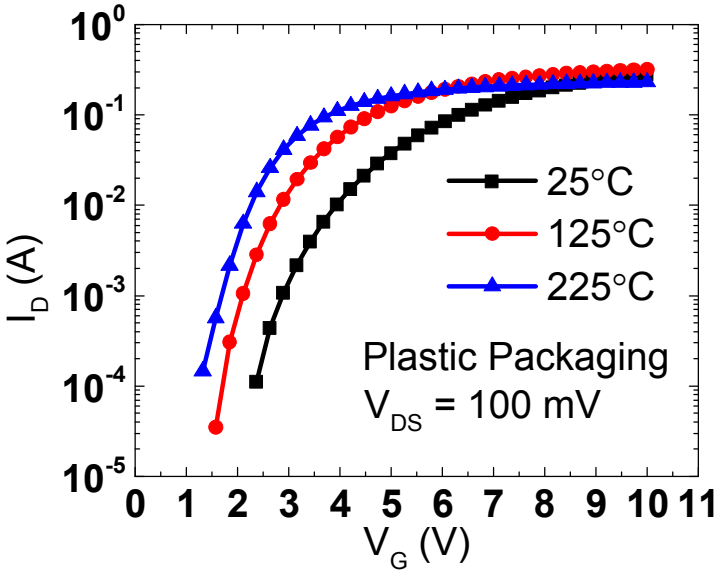

Figure 1. Drain current vs. gate voltage curves for first-generation 1200 V SiC MOSFETs in plastic packages, measured at various temperatures.

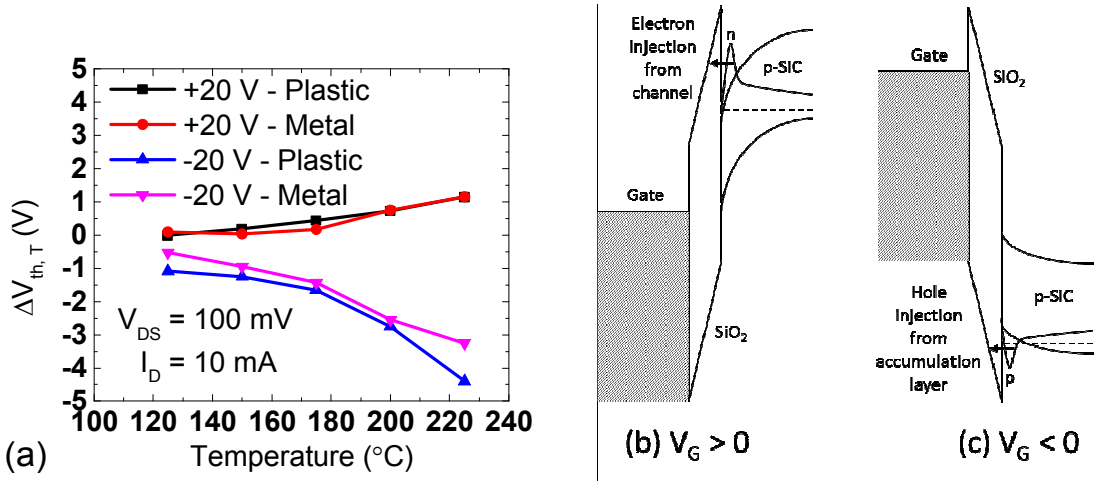

Figure 2. (a) ΔV_T for first-generation plastic- and metal-packaged parts stressed at ±20 V as a function of temperature. Schematic band diagrams illustrating (b) electron injection for $V_G > 0$ and (c) hole injection for $V_G < 0$.

The recommended off-state gate voltage is -5 V, so the devices are stressed with a gate bias of -5 V to evaluate them using more realistic operating voltages. Fig. 3 plots the results for plastic- and metal-packaged first-generation devices. No significant degradation is observed until a temperature of 250°C when the plastic-packaged parts show a V_T shift of -0.85 V. This degradation occurs at double the rated temperature of 125°C, demonstrating high resilience to bias and temperature stress at recommended operating voltages and temperatures.

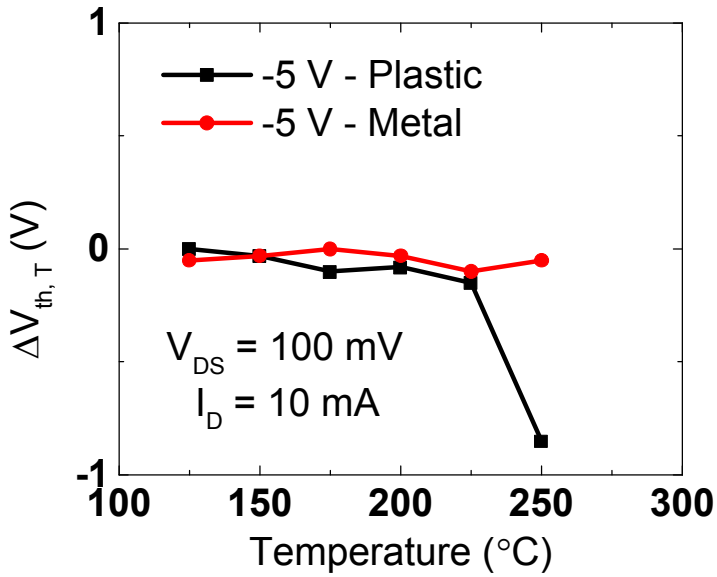

Figure 3. ΔV_T plotted vs. temperature for -5 V gate bias stress on plastic- and metal-packaged first-generation SiC MOSFETs.

Constant-bias-temperature stress experiments were repeated on second-generation plastic-packaged SiC MOSFETs. Gate biases of 20 V, -20 V, and -5 V were applied at temperatures of 125°C, 150°C, and 175°C. Fig. 4(a) plots the results and Fig. 4(b) compares the V_T shifts of first- and second-generation parts. Negative V_T shifts for a gate bias of -20 V were reduced significantly. Second-generation parts shifted by -300 mV at 175°C, compared to a shift of -1.5 V for first-generation devices. Positive V_T shifts due to a gate bias of 20 V were reduced as well, decreasing from 500 mV to 100 mV. The smaller V_T shifts indicate an improvement in the quality of the gate oxide from first-generation to second-generation devices.

In real-world applications, the power MOSFET will have a rapidly switching gate bias applied to it, which may result in different V_T shifts compared to constant bias stresses. Previous data using a switching gate bias stress have shown smaller V_T shifts compared to constant bias stress, even when tested for months (10). A second-generation SiC MOSFET stressed at 150°C with switching gate bias of +20 V / -5 V at a frequency of 100 Hz shows varying amounts of degradation depending on duty cycle. The part was stressed at a 50% duty cycle (50% of the time with 20 V on the gate, 50% of the time with -5 V on the gate) and 90% duty cycle (90% of the time with 20 V on the gate, 10% of the time with -5 V on the gate). Every half-hour the stress was stopped to perform a gate sweep. The device was recovered to its initial state using short stresses of positive bias after the first stress at 50% duty cycle. V_T rapidly drops for each stress, and then

continues to shift negatively, but at a slower rate (Fig. 5). For a 50% duty cycle, after a fast initial shift of roughly -150 mV, the V_T shift recovers slightly and then gradually shifts at a rate of -2.5 mV/hr, with a cumulative V_T shift of -370 mV after 120 hours. For a 90% duty cycle, the fast initial shift is roughly -335 mV and after a slight recovery, V_T continues to shift negatively at a rate of -0.26 mV/hr, resulting in a final shift of -364 mV at 165 hours.

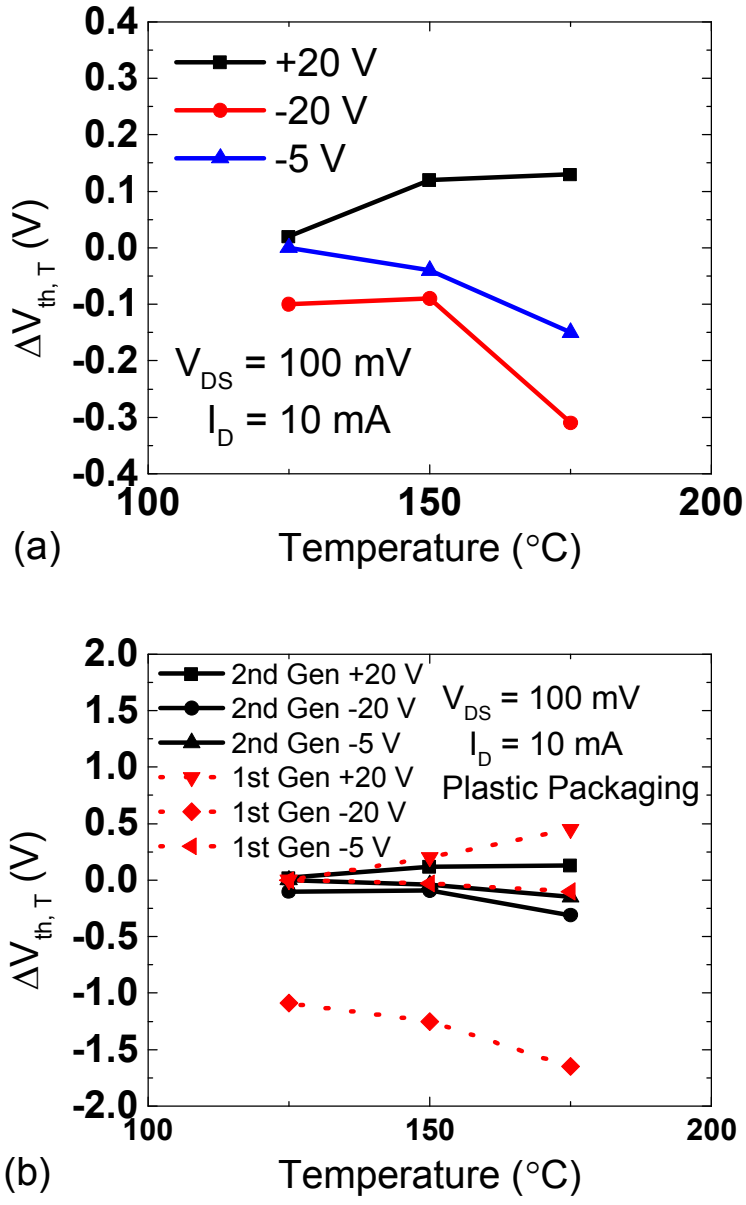

Figure 4. (a) ΔV_T for plastic-packaged second-generation SiC MOSFETs plotted vs. stress temperature, for ±20 V and -5 V gate bias stress conditions. (b) Direct comparison of first- and second-generation plastic-packaged parts for ±20 V and -5 V gate bias stress conditions.

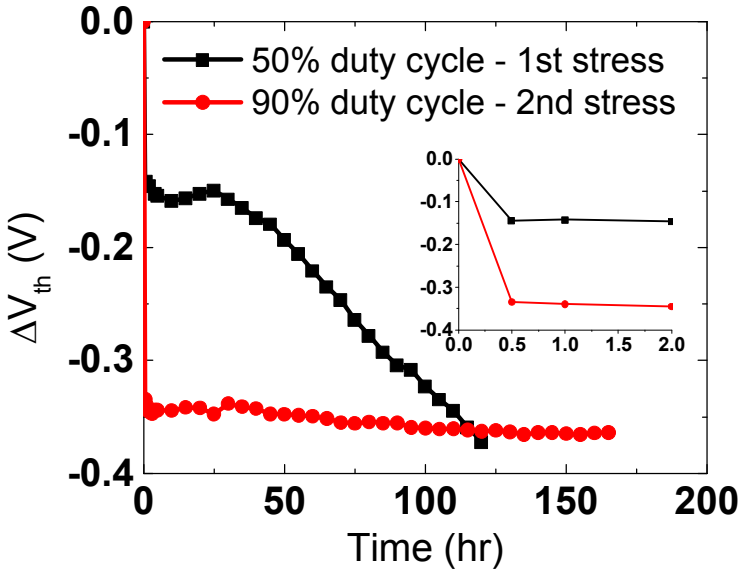

Figure 5. ΔV_T for a second-generation SiC MOSFET subjected to 50% and 90% duty cycle, +20 V / -5 V gate switching stress at 150°C. Inset shows expanded view of first two hours of stress (axis units same as main figure).

Leakage Current

Another key reliability concern is junction leakage current. This can be a significant concern at elevated temperatures, due to the negative V_T shifts observed at elevated temperatures that may prevent the device from being shut completely off with a gate bias of 0 V applied. Leakage current for a variety of temperatures was measured for first-generation SiC MOSFETs. Leakage current versus drain bias for a metal-packaged device is plotted in Fig. 6(a) and for a plastic-packaged device in Fig. 6(b). Both packages show increases in leakage current with increasing temperature, as expected. Note that the rated temperature for the plastic-packaged part is 125°C, so the temperatures at which these experiments were performed are above the rated temperature, indicating robust device performance within the recommended operating temperature range. For a drain bias up to 900 V, leakage remains below 1 μA for the metal-packaged part at 180°C and for the plastic-packaged part at 140°C. For temperatures of 140°C and 180°C, the leakage for the plastic-packaged part is roughly three times the leakage for the metal-packaged part, but at temperatures of 215°C and 250°C the leakage for the plastic-packaged part is larger by an order of magnitude.

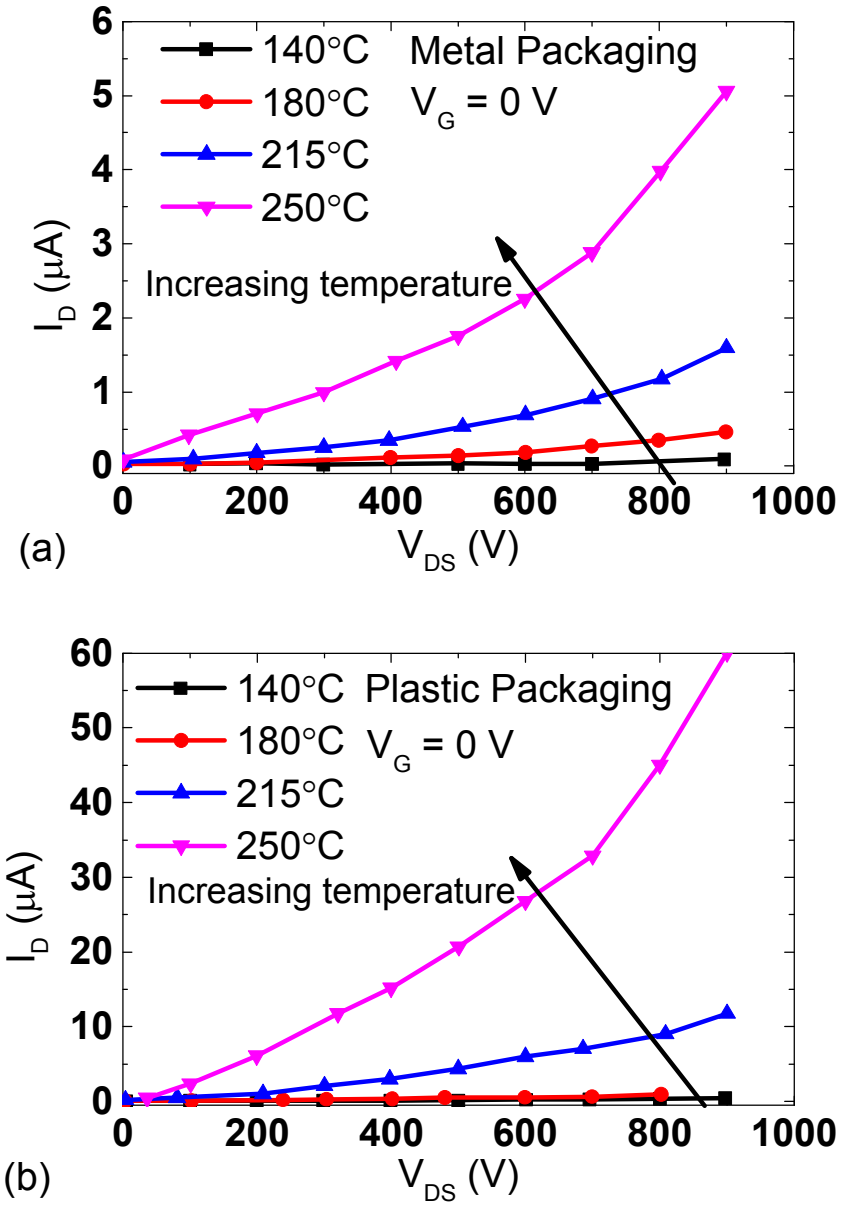

Figure 6. Drain current vs. drain voltage in the forward-blocking state (V_G = 0 V) for first-generation 1200 V SiC MOSFETs for the indicated temperatures, shown for (a) metal-packaged parts and (b) plastic-packaged parts.

Since V_T can be reduced at elevated temperatures, the experiments were repeated using gate biases of -2 V and -5 V. The results at 250°C, the highest temperature used in these experiments, are plotted for a metal-packaged part in Fig. 7(a) and for a plastic-packaged part in Fig. 7(b). A negative gate bias significantly reduced the leakage in the metal-packaged part, with a gate bias of -2 V resulting in less than 10 nA for a drain bias up to 900 V, compared to 5 μA with a gate bias of 0 V. However, there appeared to be virtually no effect of negative gate bias on leakage current for the plastic-packaged part. This result was obtained for multiple plastic-packaged parts. This suggests that the dominating leakage mechanism at these temperatures (which are above the rated temperature for this part) is related to the plastic packaging.

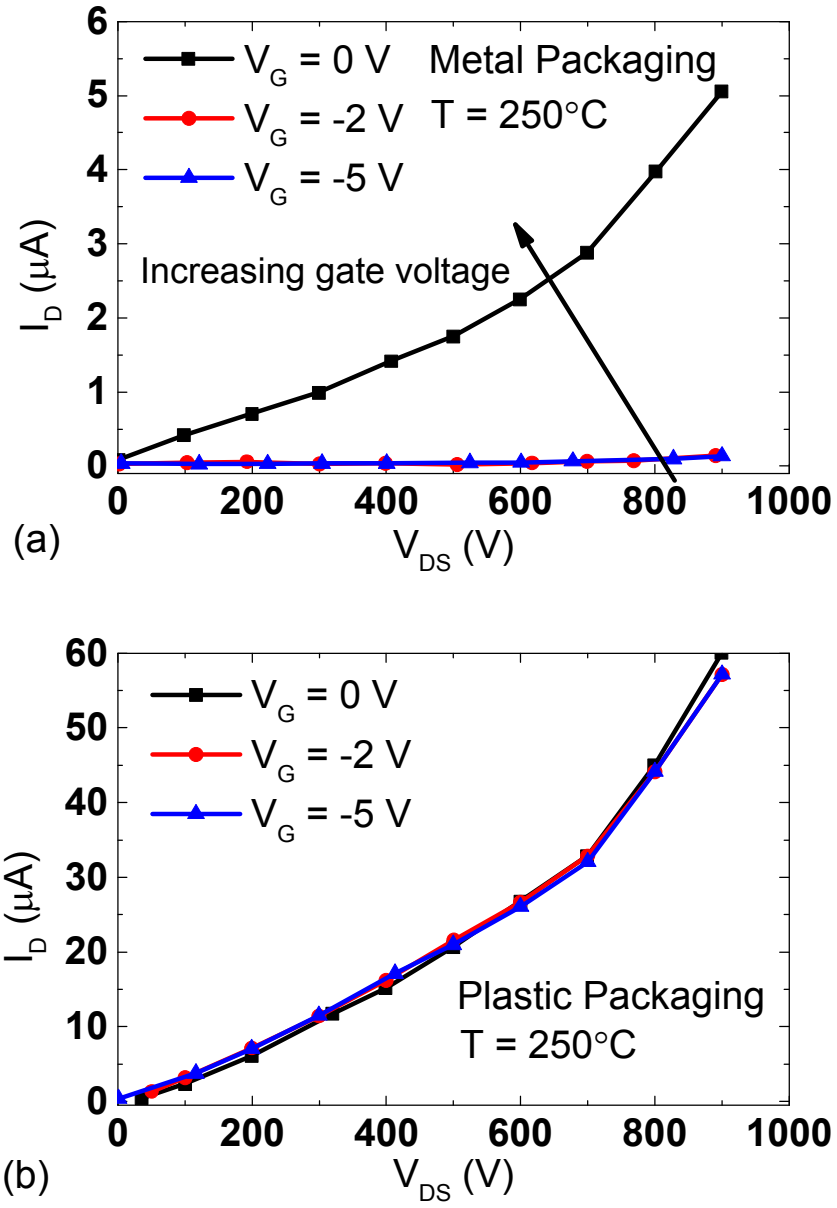

Figure 7. Drain current vs. drain voltage in the forward-blocking state for first-generation 1200 V SiC MOSFETs at 250°C and V_G = 0 V, -2 V, and -5 V for (a) metal-packaged parts and (b) plastic-packaged parts.

Discussion and Conclusions

SiC power MOSFETs are expected to endure high voltages and currents at elevated temperatures. The devices tested in this paper were assessed using two key reliability metrics, V_T shifts and junction leakage. V_T issues are likely a result of the quality of the oxide, with significant concentrations of interface traps contributing to larger V_T shifts with temperature, as well as additional V_T shifts with gate bias and stress due to charge trapping (more of an issue in this material system due to reduced band offsets compared to SiO_2/Si). However, packaging issues can also limit reliability (11), demonstrated in this experiment by the plastic-packaged parts having larger V_T shifts than metal-packaged parts after elevated temperature bias stresses and increased leakage current at elevated

temperatures. Additionally, the plastic-packaged parts appear to have an extrinsic leakage path, since using negative gate bias does not reduce the leakage current. In contrast, metal-packaged devices show almost three orders of magnitude lower leakage current when using a gate bias of -2 V instead of 0 V. Constant bias temperature stress shows little effect of using a gate bias of -5 V up to at least 250°C (Fig. 3). The result for the metal-packaged part suggests that when not limited by packaging, applying small negative gate biases can reduce leakage current without a major impact on V_T.

However, initial switching gate bias experiments indicate that using a gate bias of -5 V can cause significant negative shifts in V_T. The V_T shift appears to be composed of a rapid change and slight recovery, followed by gradual degradation. The rate of degradation seen after the initial drop and recovery appears to decrease with increasing duty cycle, which corresponds to less time with a negative bias applied to the gate. Yet, even at 90% duty cycle the V_T shift is negative, indicating that hole injection is a greater concern than electron injection. This is especially surprising considering that second-generation parts did not show a significantly larger shift for -20 V compared to 20 V until 175°C. Some self-heating may occur (similar to (12)) during the switching stress that raises the temperature of the junction above the applied temperature of 150°C. This temperature increase may be significant, since even at an applied temperature of 175°C, when comparing the shift using 20 V on the gate with the shift using -5 V on the gate, they are nearly the same. Self-heating may also explain why the shift after half an hour of switching stress results in a shift of ~150 mV compared to a shift of ~50 mV for a constant bias stress of -5 V at 150°C.

The rapid initial change in V_T is different for the two duty cycles, which may be due to the different stress conditions. However, the initial change at the start of the second stress is similar to the final V_T shift at the end of the first stress, suggesting the possibility of cumulative damage between stresses, despite the recovery of the gate sweep curve. If the damage caused by worst-case conditions cannot be easily recovered, damage would persist for the lifetime of the device, which is particularly concerning for parts with parameters that vary over the course of their lifetime. Cumulative damage may occur if there are additional defects created during the first stress that remain in the oxide. Another possibility is that the holes trapped during the first stress are not actually annealed during the recovery. Electrons may be trapped at defects and form a dipole without recombining, so when a negative bias is applied again the electrons would be emitted and the resulting V_T shift would be similar to previous values. This is similar to the situation described previously for E' centers in SiO_2 on Si (13).

A variety of other factors may also affect the V_T shift observed for these devices. Using a higher frequency should increase the temperature of the junction further, likely increasing the V_T shift. Using a gate bias of -2 V may reduce the V_T shift while still helping to suppress leakage current. The effects these factors have on the rapid V_T shift and the slope of the gradual V_T shift, as well as how they interact with possible cumulative damage effects, are topics for further study. While reliability experiments are ongoing, the present results demonstrate that first-generation plastic-packaged parts must be stressed above the rated operating temperature before significant degradation is observed, and there is a significant reduction in negative V_T shifts due to negative gate bias on plastic-packaged second-generation parts. The improved V_T stability under negative gate bias allows more flexibility in using negative gate biases to reduce junction

leakage at elevated temperatures and demonstrates the improving quality of gate oxides for SiC power MOSFETs.

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