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Asymmetric Voltage Pulse Simulation and Analysis in LTD Stages

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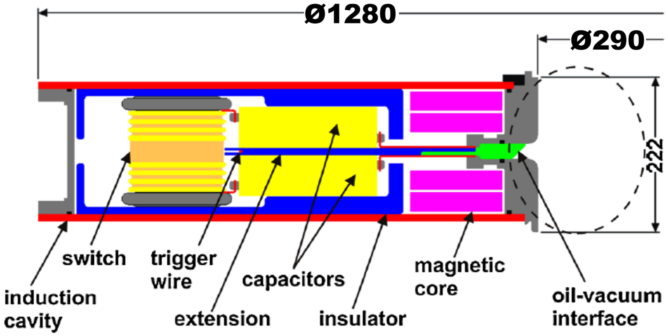
LTD Basic Operation

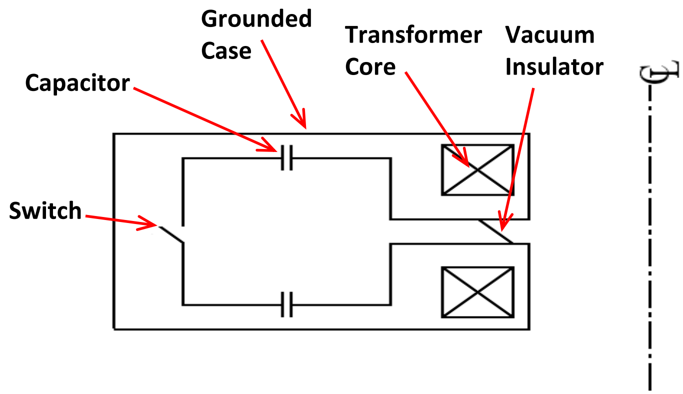
- **A linear transformer driver (LTD) is an inductive voltage adder (IVA), in which the pulse-forming components are entirely contained within individual LTD stages.**

- **Each stage is a parallel collection of "bricks", each functioning as a two-capacitor bank.**

- **Top and bottom of brick are practically identical.**



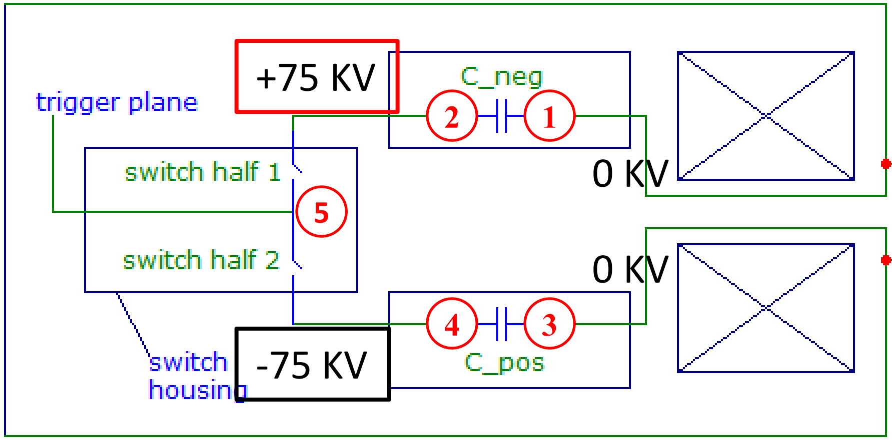
Section view of an LTD brick

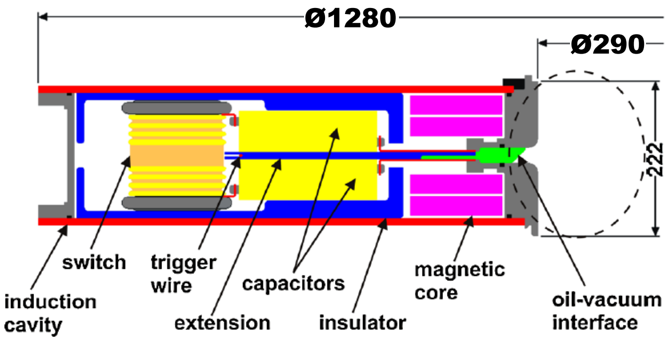


Idealized schematic of an LTD brick

Firing Process – Initial Conditions

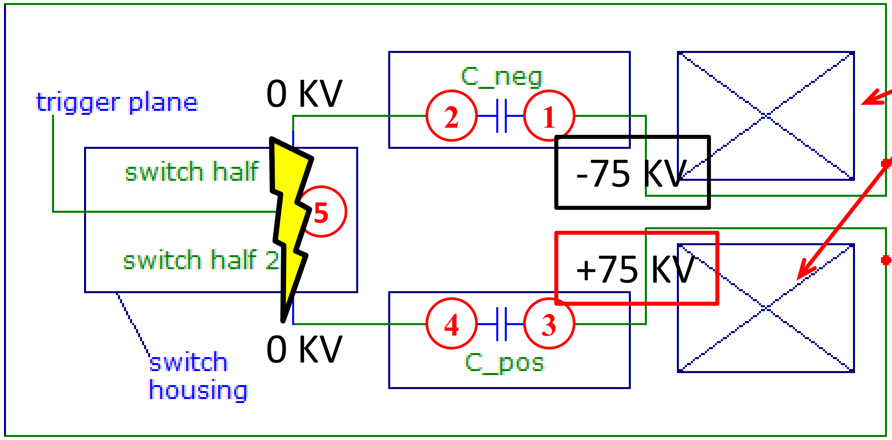
- V_2 and V_4 are charged to 75 KV and -75 KV, respectively.
  - Note that $V_2 - V_1 = 75$ KV, $V_4 - V_3 = -75$ KV.
- V_1 and V_3 are grounded (0 V) via the cavity wall.
- A spark gap switch (5) holds back the capacitors' voltages.





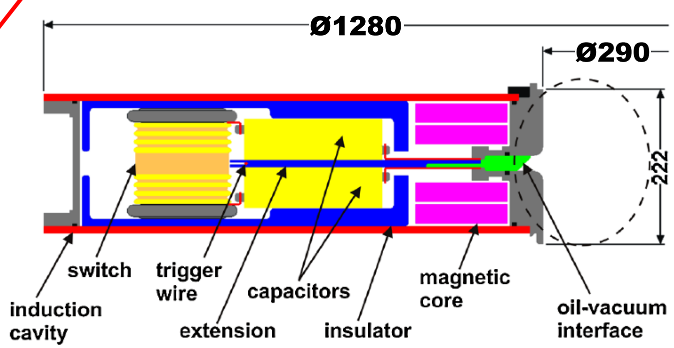
Firing Process – Circuit Discharge

- **Switch is triggered and closes, forcing nodes 2, 4, and 5 to ground (0 V).**
- **Capacitors maintain their initial conditions:** $V_2 - V_1 = 75\ KV$, $V_4 - V_3 = -75\ KV$.
- **To do this, V_1 becomes -75 KV and V_3 becomes 75 KV (capacitors invert their polarity).**
- **Load has a voltage across it, thus current flows and discharges capacitors.**



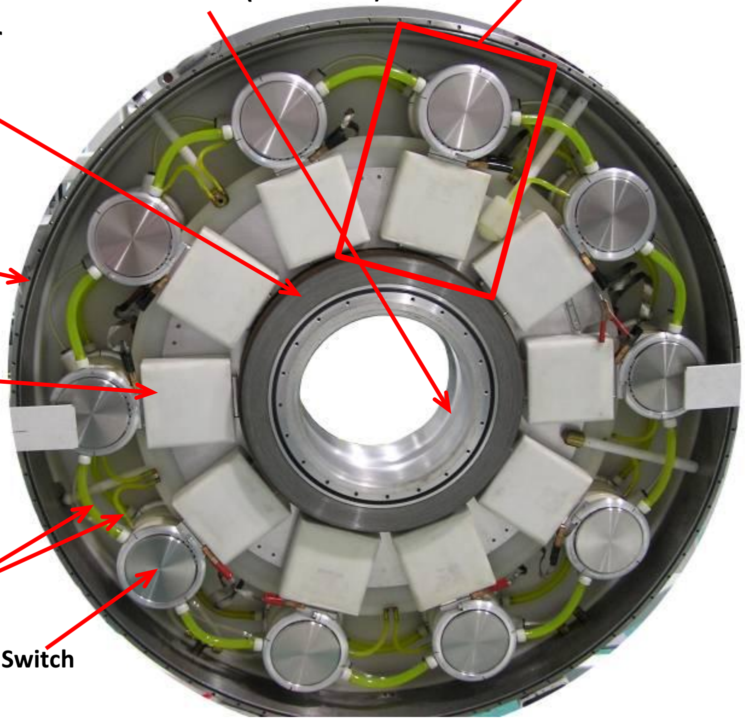
Cores (big inductance: L) prevent pulse from short circuiting via cavity wall.

$$\frac{dI}{dt} = \frac{V}{L}$$



LTD Stage Architecture

- Many bricks are arranged azimuthally within a toroidal, grounded metal cavity.
- Cavity is filled with insulating transformer oil to inhibit component arcing.
- Charge and trigger connections are routed through a network of water resistors.
- Pictured: a ten-brick LTD stage.

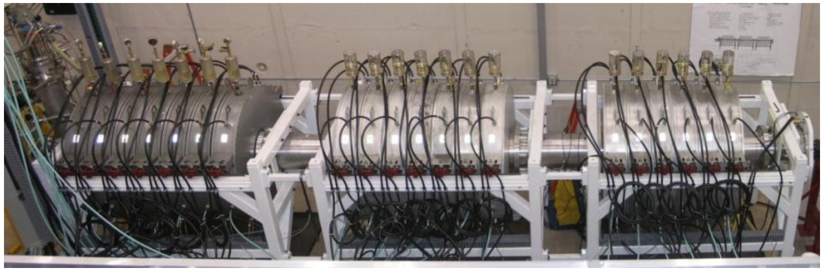


LTD Pulsed Power

- **Multiple stages can be arranged axially, forming a coaxial transmission line.**
  - **More stages stacked on axis → adds stage voltages**
- **Available voltage = 2 × (capacitor voltage) × (number of axially stacked stages) × (matching factor)**
  - **Matching factor: circuit characteristic, depends on load impedance**
    - *Exactly matched = .5*
    - *Critically damped = .7*

Seven-stage stack at the LTDR facility. Stacking cavities along their common axis adds voltages. This stack can deliver 1 MV to its load.

- **Available current = (brick current) × (# of bricks per stage) × (# of parallel stages)**



URSA Minor: a 21-stage linear stack, currently in verification phase. Rightmost cavity was under test when this picture was taken.

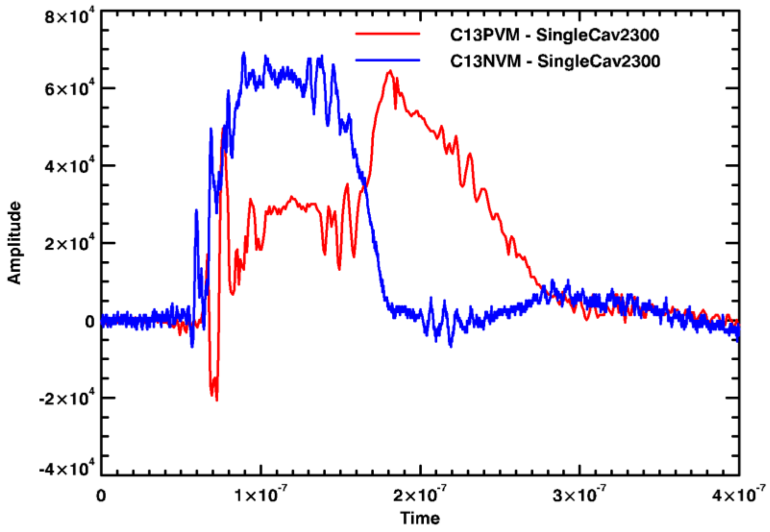
- **21-stage tests are now underway.**
  - **Expected to generate 2.5 MV pulse.**

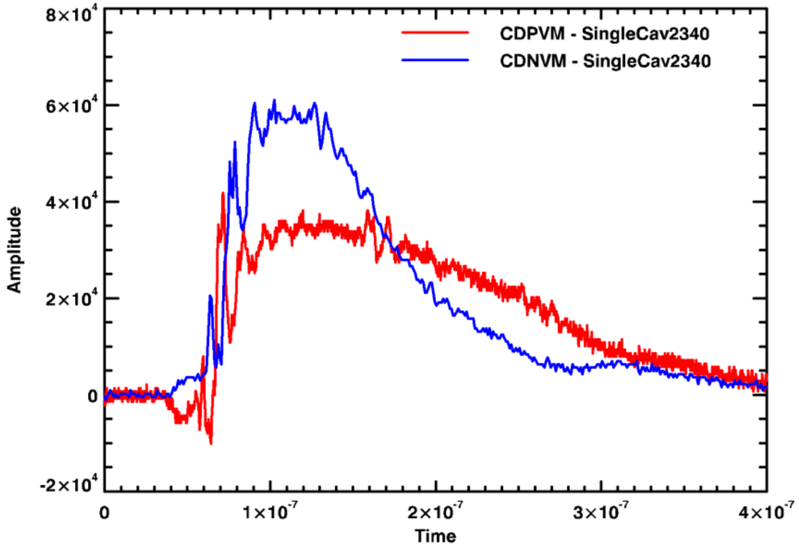
Previous Work – Asymmetric Voltage Pulses

- In March 2011, Josh Leckbee (1656) documented a voltage asymmetry between positive and negative output voltages.

- It was concluded this was due to differences in cores.

- Some imbalances were severe, while others showed only a 10-20% difference in voltage output.

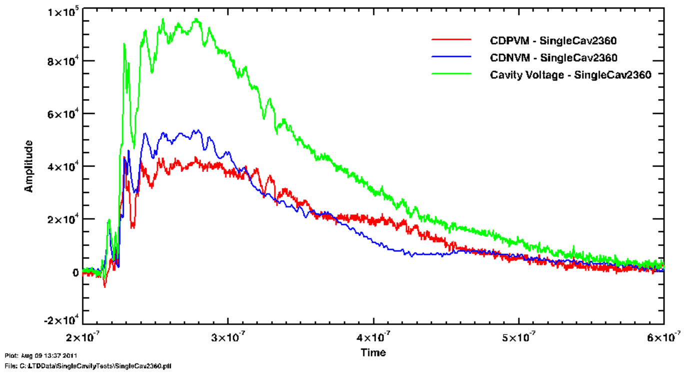




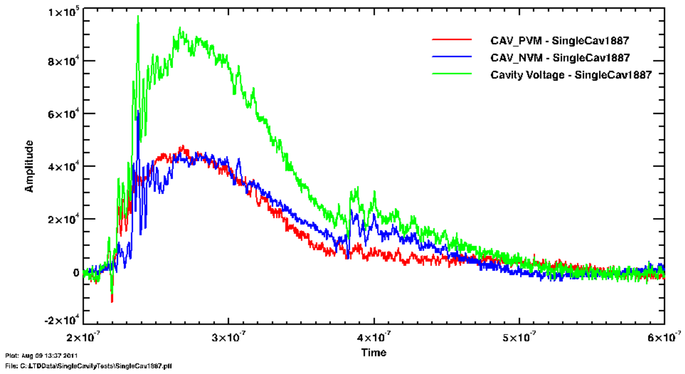
Output Pulses Not Affected by Asymmetric Components

- **Although component pulses are imbalanced, total output pulse of the stage appears normal, regardless of symmetry.**

- **If so, why worry about asymmetry? Because it may create system voltages exceeding design parameters, resulting in:**
  - **Core saturation**
  - **Core layer damage**
  - **Unequal wear / stray arcing**
  - **Less than optimal performance**



Asymmetric single cavity shot #2360



Symmetric single cavity shot # 1887

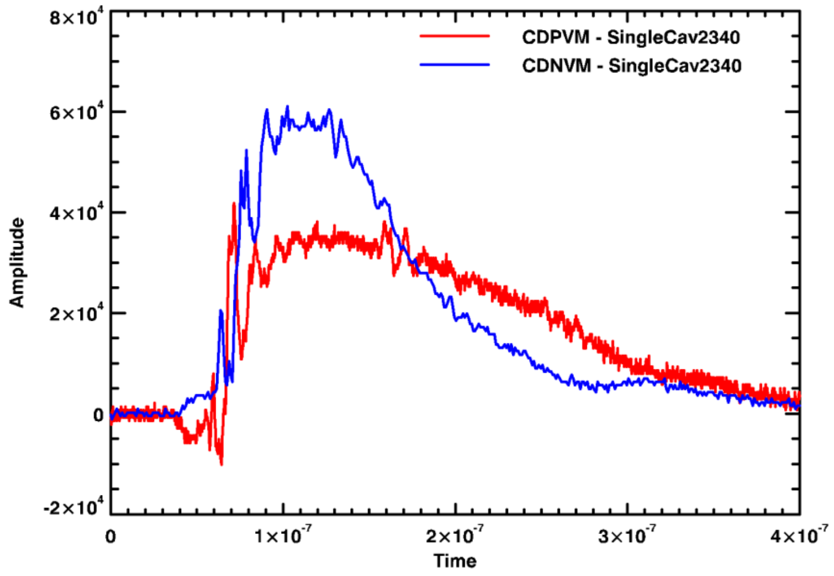
Previous Work – Why Blame the Cores?

- **Reversing charge polarity reversed asymmetry**
  - **Not a cavity geometry issue.**
- **Reversing trigger polarity reversed asymmetry.**
  - **Is the trigger interacting with the main discharge circuit?**
- **Reducing trigger amplitude reduced asymmetry.**
  - **Further evidence the trigger is the source of the imbalance.**
- **Pre-saturation of cores prevented asymmetry.**
  - **Saturation essentially removes the cores from the circuit.**
  - **Asymmetry appears to be related to the cores.**

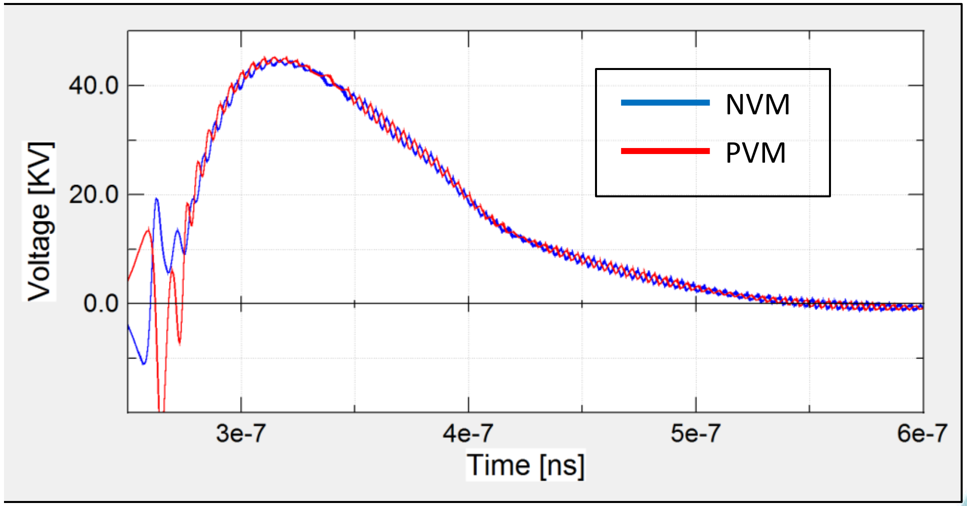
Simulation of Asymmetry

- **To aid in interpreting this asymmetry, Josh Leckbee created a BERTHA circuit simulation model of a single ten-brick cavity.**

- **Initially, the model did not predict voltage asymmetry as seen in data.**



Asymmetric single cavity shot #2340



Simulation of comparable cavity conditions, R_{trig} = 300 Ω.

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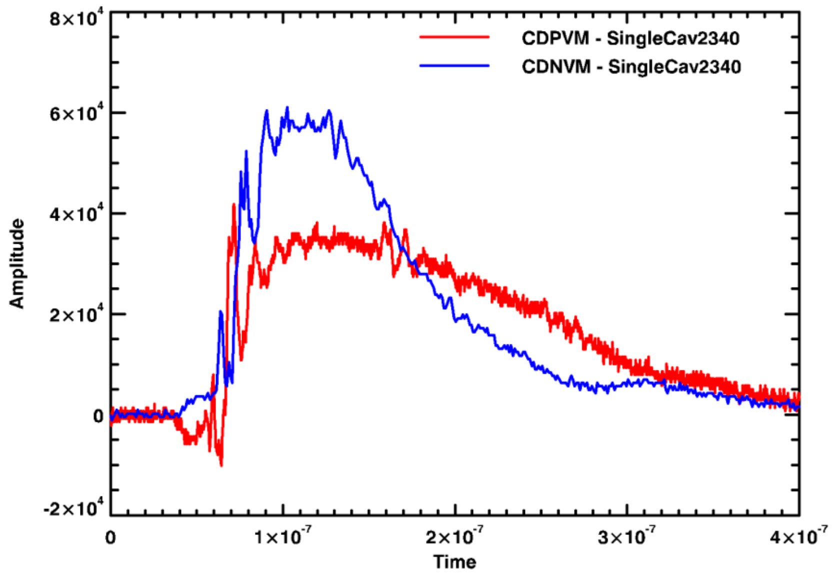
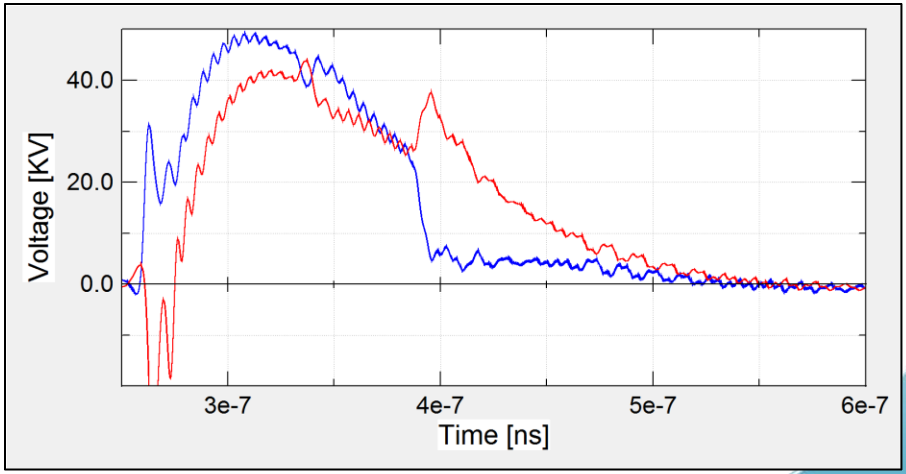
Simulation of Imbalance

- A 3 ns, 8 Ω transmission line was added to the trigger return path to represent the trigger pulse's return path through the cavity wall.
- These values were chosen based on cavity dimensions and voltage measurements in the experimental data.
- Resulting simulations indicated asymmetry, though not identical to data.
  - Larger prepulse in simulation, could be due to new voltage-triggered switch model.
  - Separation occurs earlier in simulation, possibly related to large prepulse.
  - Features not perfectly replicated, represents a non-ideal situation (experiment vs. theory!)





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Improved Simulation

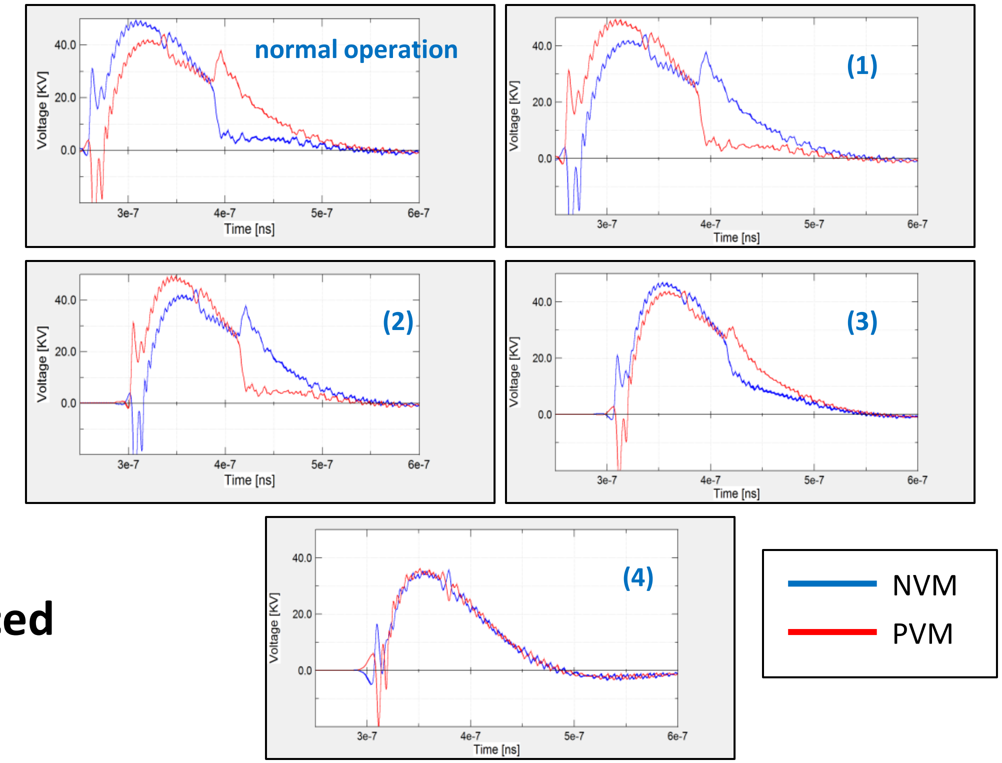
- **As with experimental shots, simulation shot conditions were varied:**

- **Polarity reversal**
  - Capacitor charge (1)
  - Trigger (2)

- **Trigger amplitude**
  - Half voltage (3)

- **Pre-saturation of cores (4)**
  - Cores no longer block the outputs from shorting via cavity wall.
  - Creates a secondary path to ground.

- **Variations in simulation produced similar results as seen in data.**
  - Successfully predicted what was observed in single cavity shots.



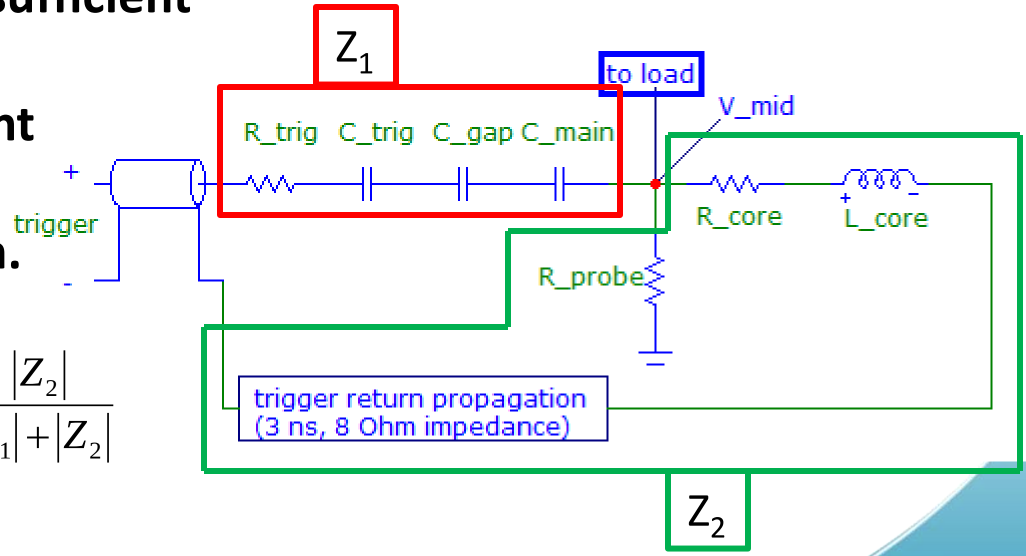
Possible Cause of Asymmetry

- **What led to our adding this trigger return path to the model?**

- **Trigger circuit appears to load the main circuit sufficiently to disrupt ideal behavior.**
  - **Trigger and main circuit are not isolated circuits.**
  - **Reactive elements do not block fast trigger pulse.**

- **If trigger return element is of sufficient impedance, it will, along with R_{core} and L_{core}, draw a significant portion of the trigger pulse voltage due to voltage division.**

$$V_{mid} \approx V_{trigger} \cdot \frac{|Z_2|}{|Z_1| + |Z_2|}$$



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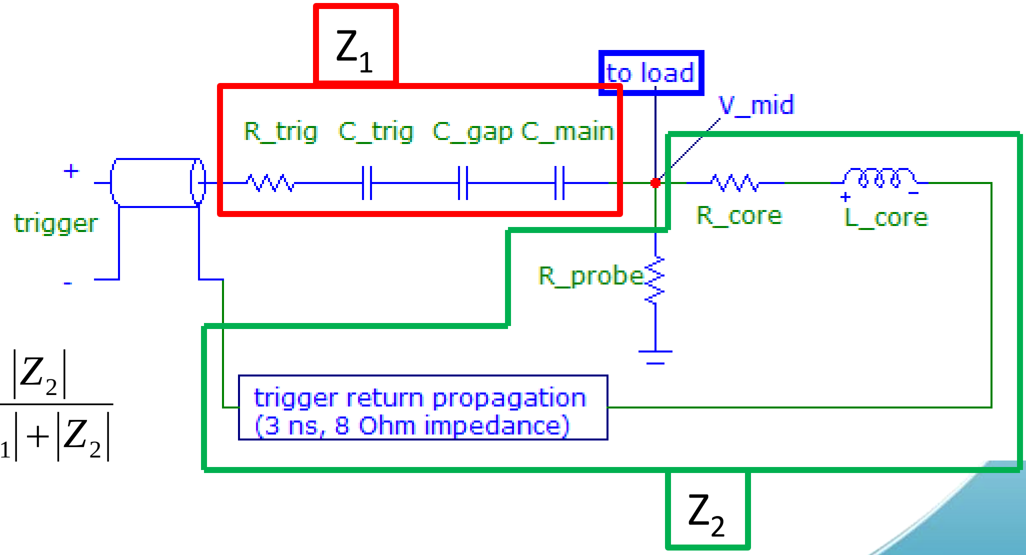
Mitigation of Asymmetry

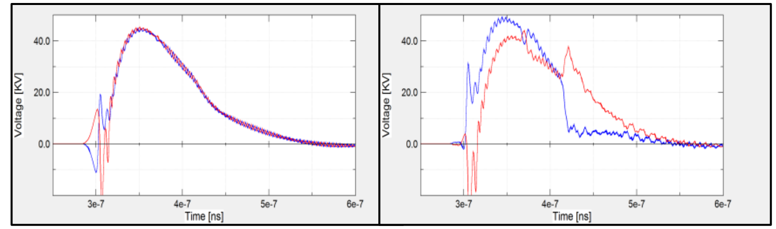
- To prevent this loading effect, Z_1 can be increased by increasing trigger resistance (R_{trig}).
- Corrects the asymmetry, but increases trigger rise time, which may increase switch jitter.
- R_{trig} went from 300 Ω to 2.5 KΩ, and this seems to mitigate asymmetry.



$$V_{mid} = V_{trigger} \cdot \frac{|Z_2|}{|Z_1| + |Z_2|}$$

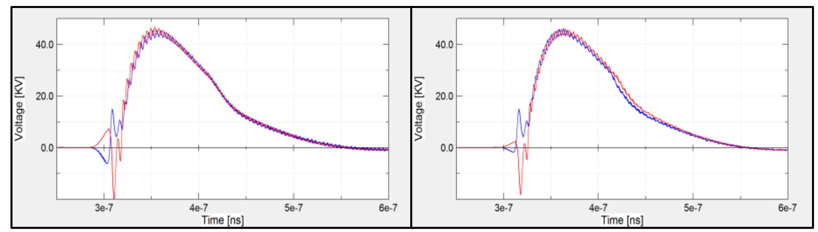
Mitigation of Asymmetry - Simulation

- **Without trigger return element: impedance of the return path is too low.**
  - **V_{mid} is low compared to full trigger pulse voltage.**
  - **Trigger does not influence the main circuit.**
  - **See plots on left.**



BERTHA simulations with **300 Ω trigger resistors**. Left: original model. Right: adjusted model including trigger return path. Asymmetry is clearly seen in the adjusted model.

- **With trigger return: return path draws enough of the trigger pulse voltage at V_{mid} to create potential significantly beyond 0 V.**
  - **V_{mid} side of C_{main} was originally at ground potential (0 V).**
  - **Displaced from ground when trigger pulse voltage-divides at V_{mid}.**
  - **C_{main} will charge or discharge, depending on its charge polarity vs. V_{mid}.**
  - **See plots on right.**



BERTHA simulations with **2.5 KΩ trigger resistors**. Left: original model. Right: adjusted model including trigger return path. A larger trigger resistor reduces asymmetry, as observed in experiments.

- <u>**Hypothesis: By increasing trigger resistance, voltage division due to trigger return is counteracted, V_{mid} remains low, and asymmetry is avoided. An experiment to test this is planned for August 2011.**</u>

Optimizing Trigger Resistance – Future Plans

- **Setting R_{trig} to 2.5 KΩ seems to give the desired result, but is that the best value? We need:**
  - Fast trigger rise time (gets slower with increasing R_{trig}).
  - Symmetric voltage pulses (gets more symmetric with increasing R_{trig}).

- **At this time, our understanding is that both parameters depend on R_{trig} on some level, but when one improves, the other gets worse!**

- **What's the best value for R_{trig}?**
  - Depends on jitter, which is not easily modeled.
  - Simulation indicates R_{trig} should optimize in the 1-10 KΩ range.
  - Jitter problems vs. asymmetry problems.

- **Try different conditions in single-cavity experiments.**
  - Vary R_{trig}, R_{load}, etc.
  - Measure jitter & asymmetry and optimize.
  - Further verify or update model.

References

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