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Silicon enhancement mode nanostructures for quantum computing

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Albuquerque, New Mexico, USA

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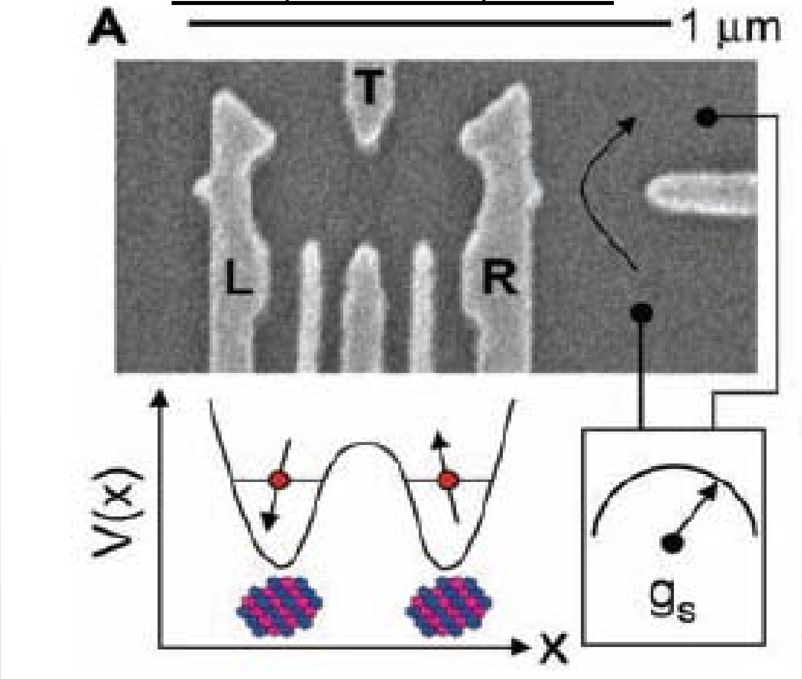
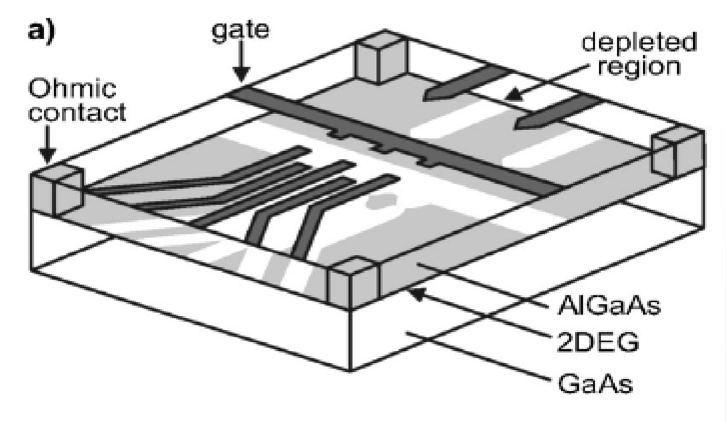
Inspiration for Semiconductor Based Quantum Computing

- Demonstration of GaAs qubits has spurred quantum do semiconductor qubit research (e.g., Petta et al. in 2005)

Petta, Science, 2005



Hanson, Rev. Mod. Phys. 2007

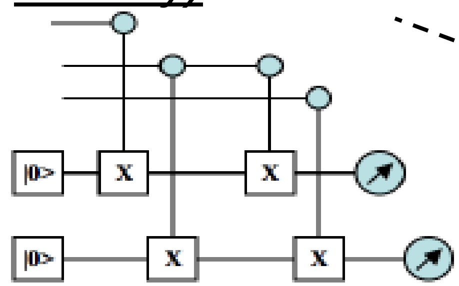


Need
- Isolate singlet triplet system
- Electrically tunable rotations
- Charge sense (fast is desirable)

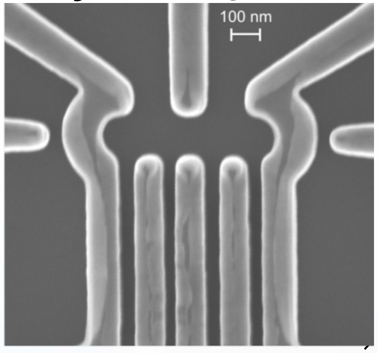
- Does T_2 need to be really long? ($p \sim 10^{-4}$?)

- <u>Conclusions from logical memory</u>
  - Scheduling conflicts lead to more idles (e.g., electronics & DD)
  - if T_2 error is non-negligible gates requirements are more strict
  - Circuit would shows benefit at $p \sim 5 \times 10^{-4}$ <u>assuming negligible idle error</u>

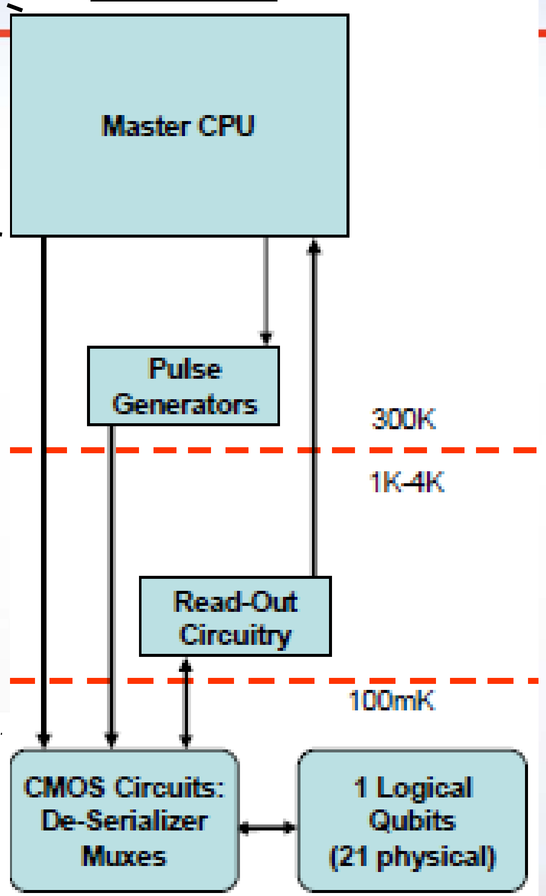
<u>Quantum Circuit (Logical Memory)</u>

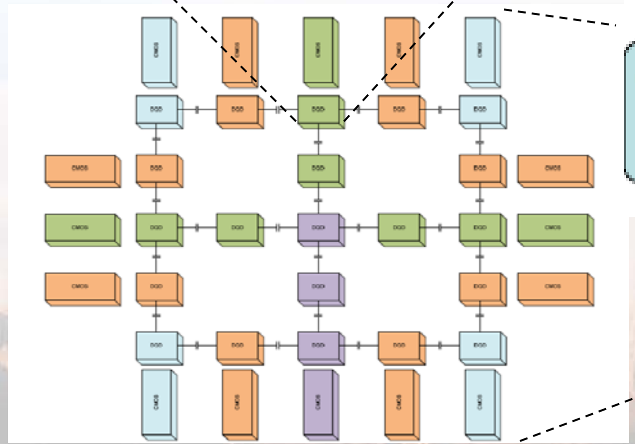


<u>Physical Qubit</u>



<u>Classical-Quantum Interface</u>

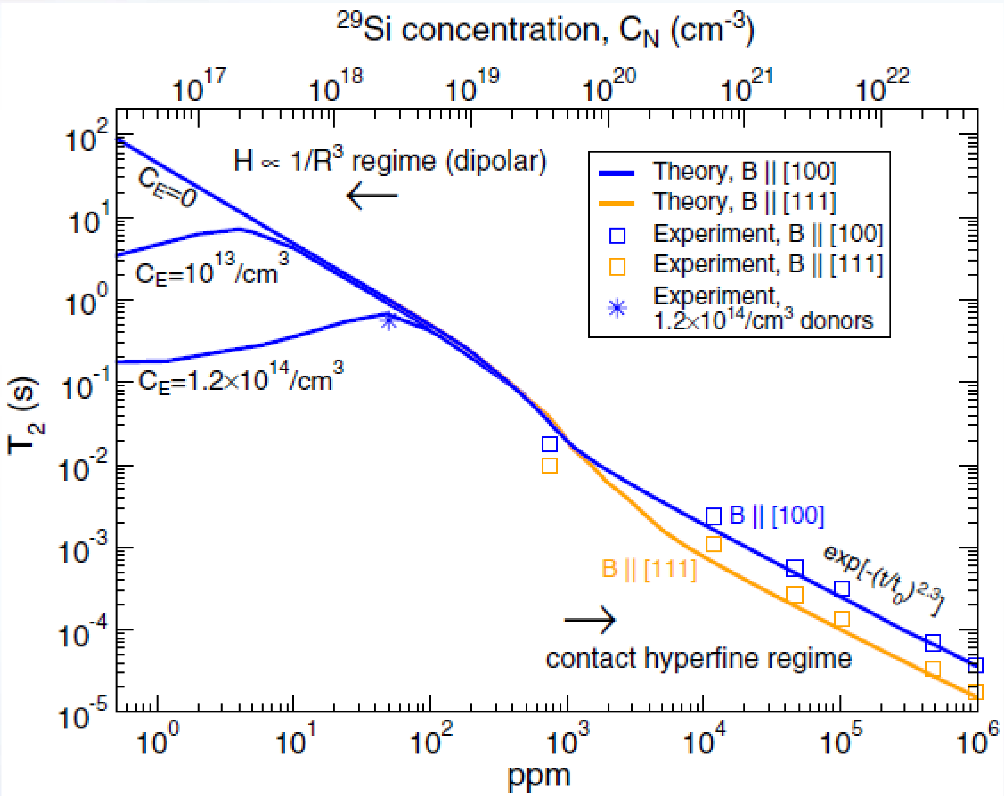




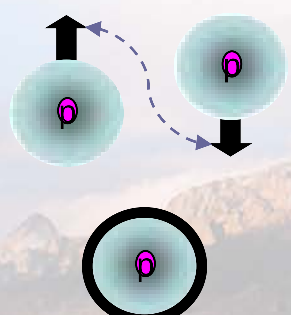
<u>Chip Level Circuit (21 qubits)</u>

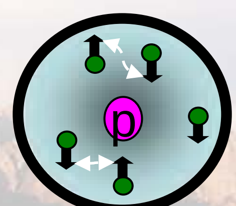
Levy et al. SPAA 2009
Levy et al. arXiv:1105.0682

Motivation for Silicon Qubits



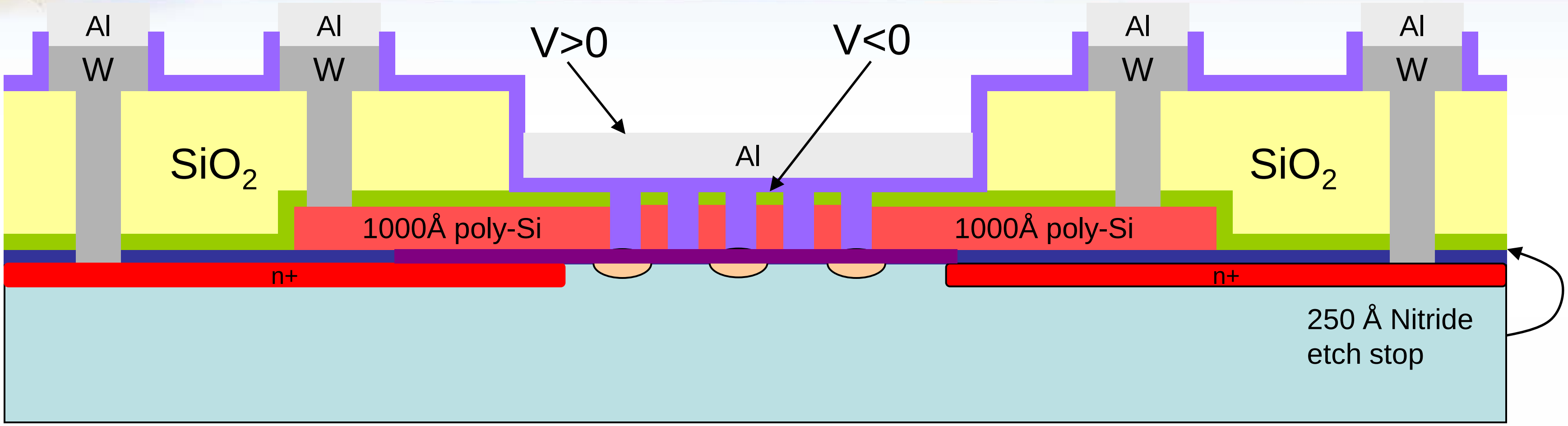
- Recent device progress in electron spin manipulation (spin read-out)
  - UNSW
  - UCLA
  - HRL
  - U. Wisconsin
- Si isotope enrichment removes nuclear spin, long electron spin T_2
- Long T_2 measured and longer predicted possible





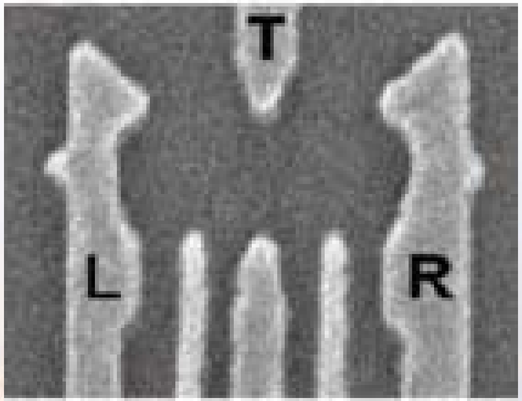
Witzel et al, PRL 105, 187602 (2010)

Enhancement Mode Si Quantum Dots



- Many silicon approaches
- SNL looking at enhancement mode Si foundry approach
  - start w/ MOS, now incorporating donors or SiGe/sSi

GaAs design to Si?

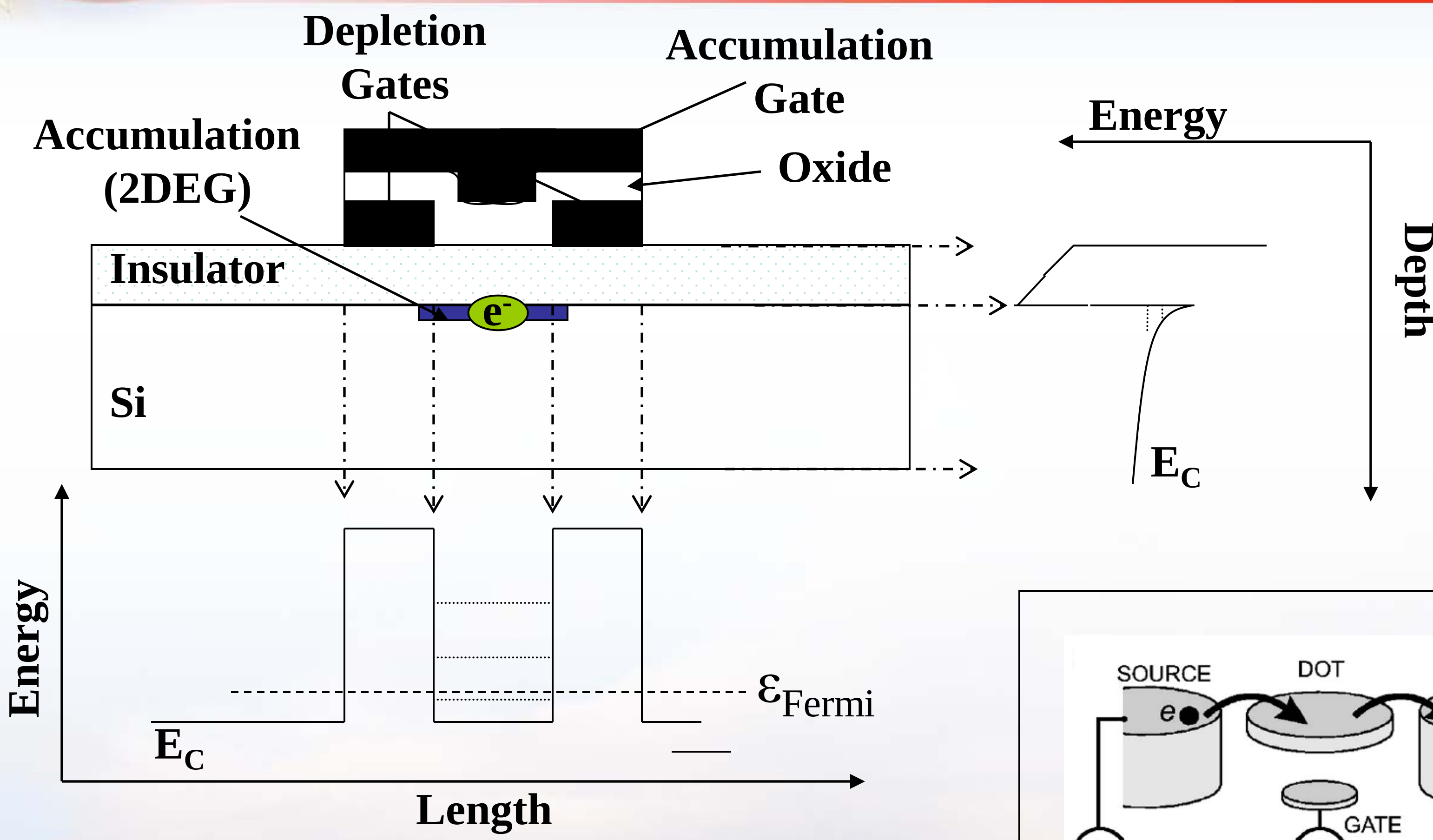


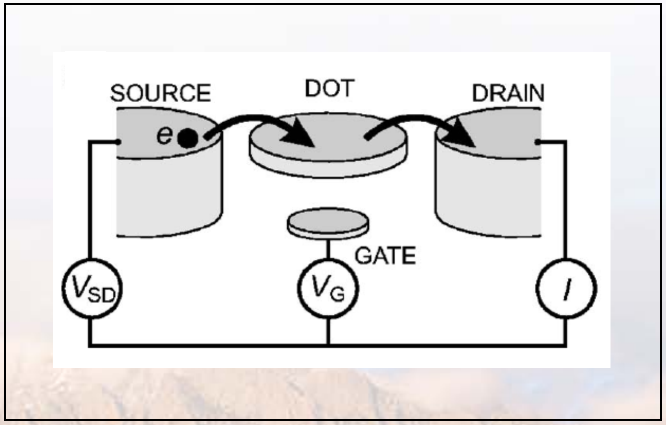
Petta et al. [2005]

Motivations

1. Platform is modular design for both donors and SiGe/sSi
2. Tunable parameters (density, valley splitting, g-factor?)
3. Start with MOS:
   - well understood material system
   - overlapped interests for other Si approaches
4. CMOS compatible (MOS)

Enhancement mode quantum dot concept

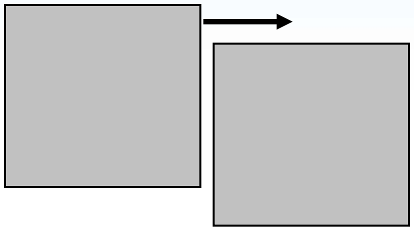




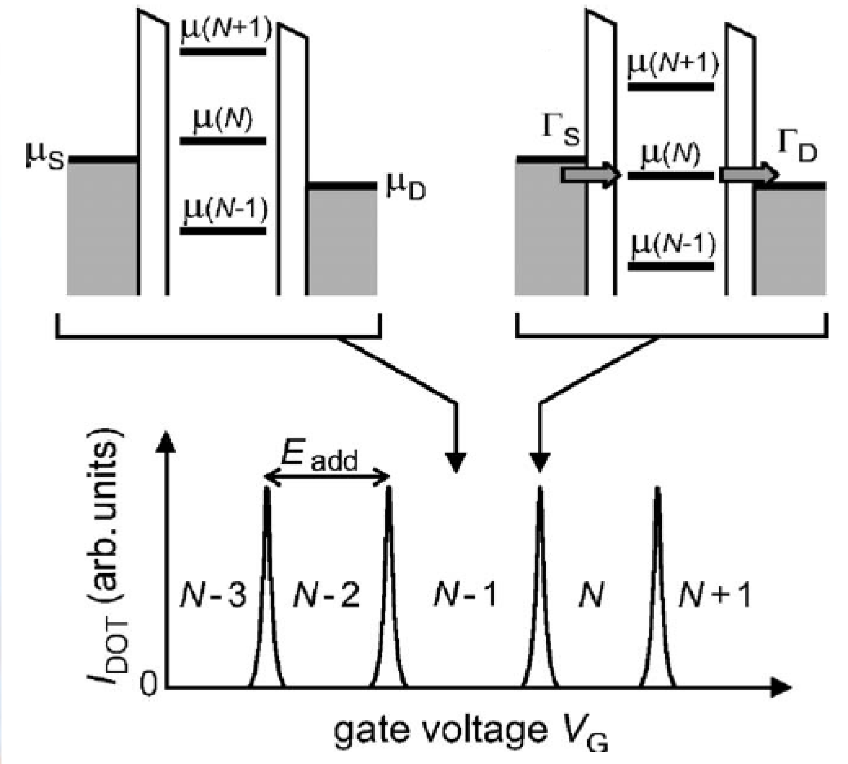
- Structure provides 3D confinement

Coulomb blockade

Imbalance in chemical potential produces current



Current goes through QD when levels lines up

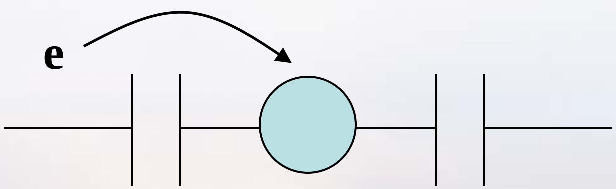


$V = \frac{q}{C}$

- Equally spaced energy levels related to charging energy of capacitance
- Periodic current resonances produces – “Coulomb blockade”
- Low temperatures required (T << 4K)

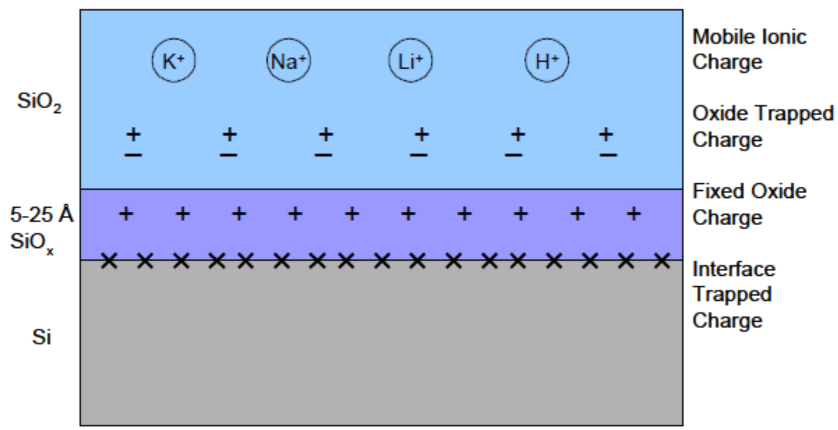
$$C_{sum} \sim 16 \text{ aF}$$

$$\Delta V = \frac{q}{C} \sim 1 \text{ mV}$$



Chemical potential levels are spaced by charging energy

Early challenge to MOS QDs

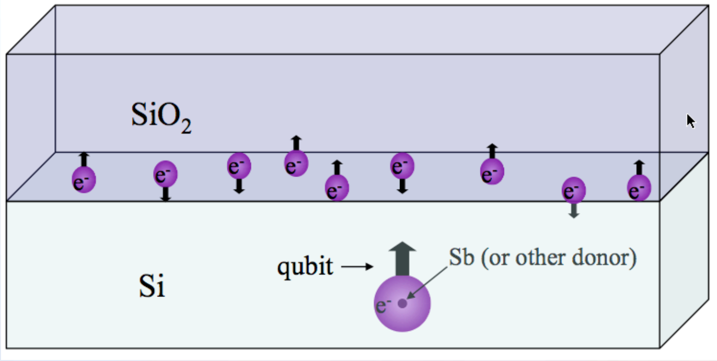


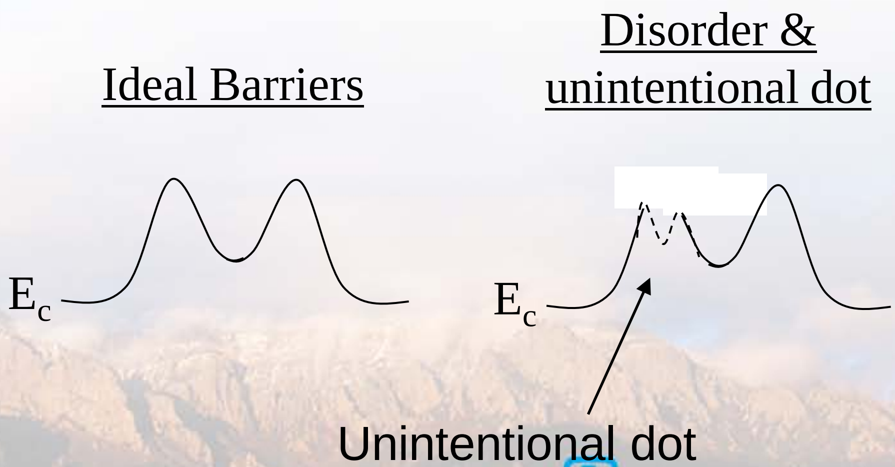
Charge defects & effective mass

1. **Uncertain confinement potential**
2. **Unintentional dots**
3. **Fluctuators (TLS)**

Magnetic defects

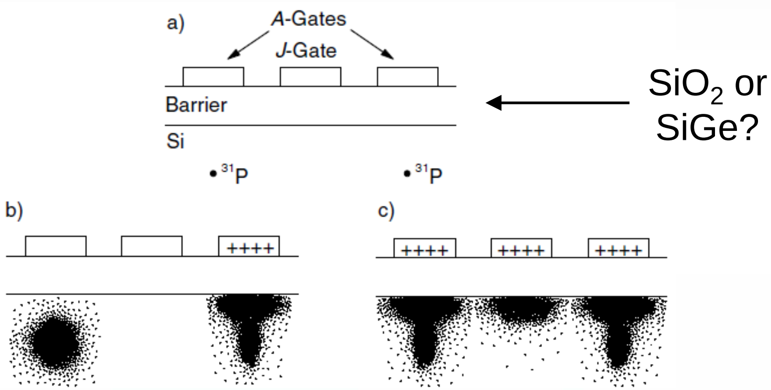
1. **Non-uniform magnetic field**
2. **Time varying magnetic field (if not polarizable)**

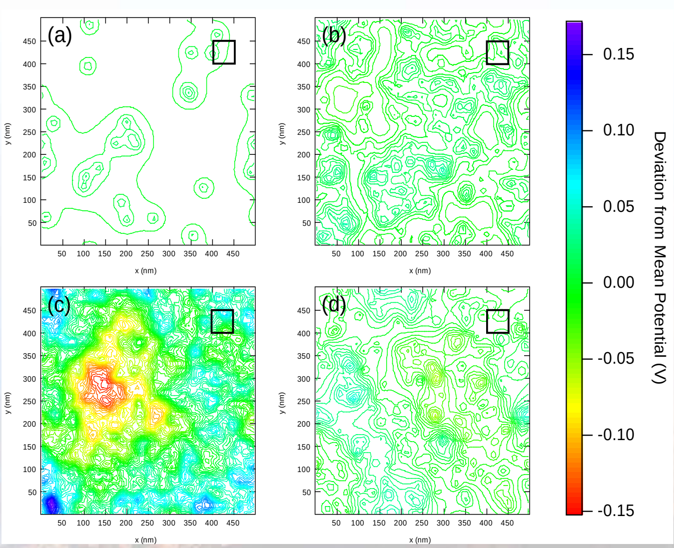




Shared Considerations (Donors)

Donor Device Architectures [e.g. Kane]

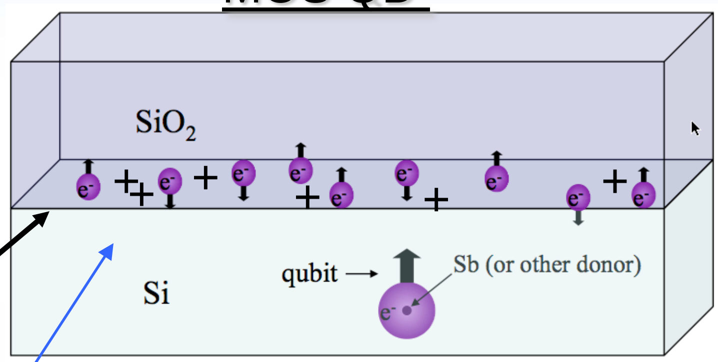




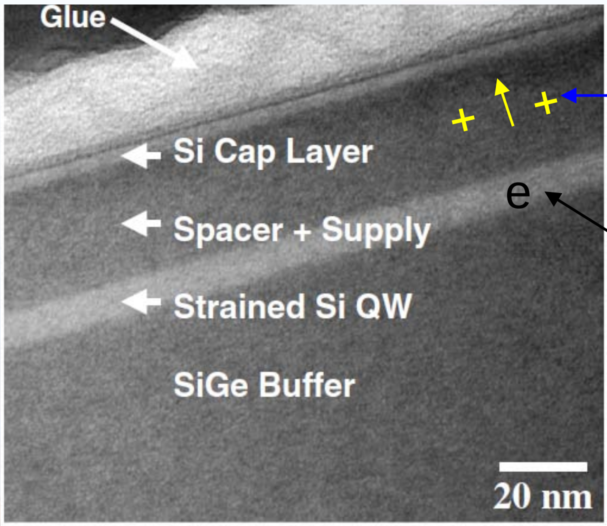
- ***Understanding MOS interface is a shared goal for donor architectures***
- ***Disorder potential***
- ***Interface traps***
- ***Effect of magnetic defects?***

Shared Considerations (SiGe/sSi)

MOS QD



sSi/SiGe Device Architectures



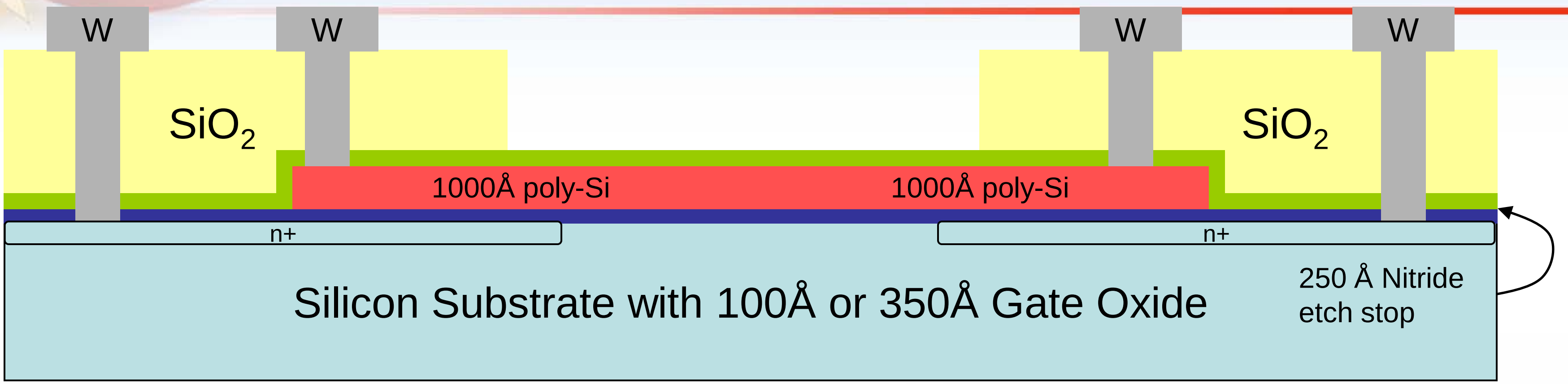
Ionized or unionized dopants

Qubit layer

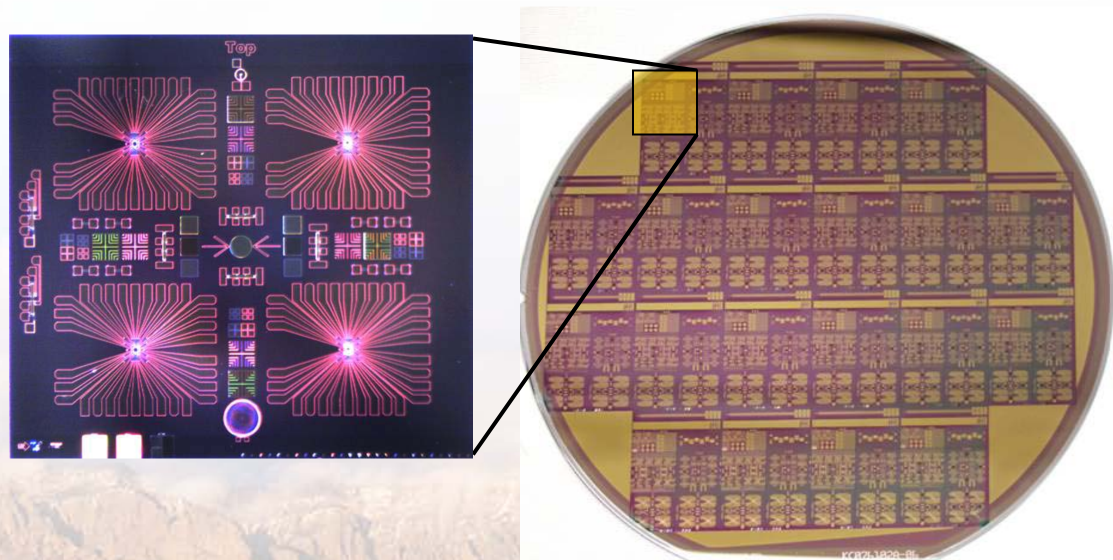
- *MOS interface may provide model system for SiGe/sSi*
- *SiGe distances defects further away… but more defects?!*
- *Modulation doping layer is source of unpaired spins and electrostatic disorder (similar magnitudes?)*
- *Valley splitting*

T. Pluym

How is device made: “Front-end”

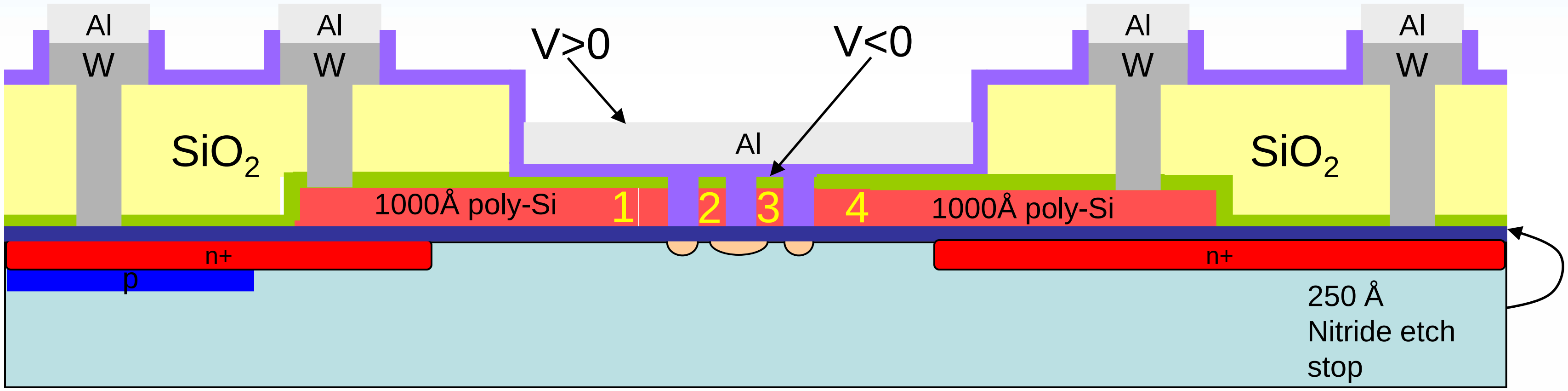


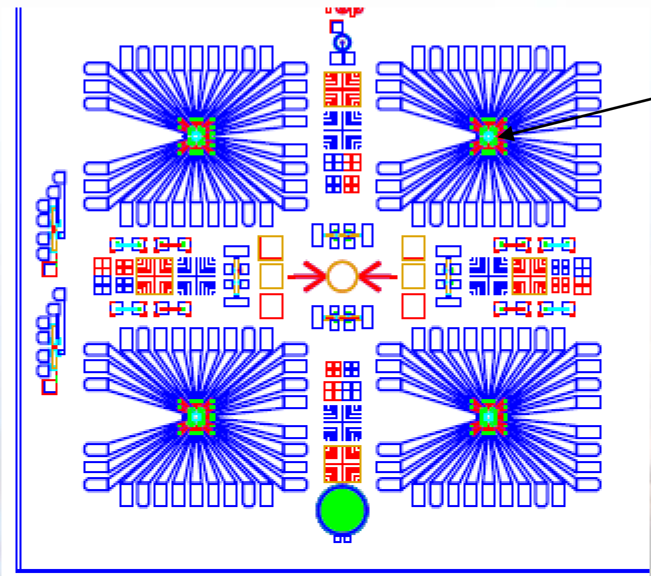
<u>MOS Stack from Si fab</u>
QDs possible with 0.18 ❍m litho
EDMR for external community
7,500 – 15,000 mobility, high resistivity substrates



- Built-in APD for single ion detection
- W metal for “back-end” donor implant & RTA

Back-end processing

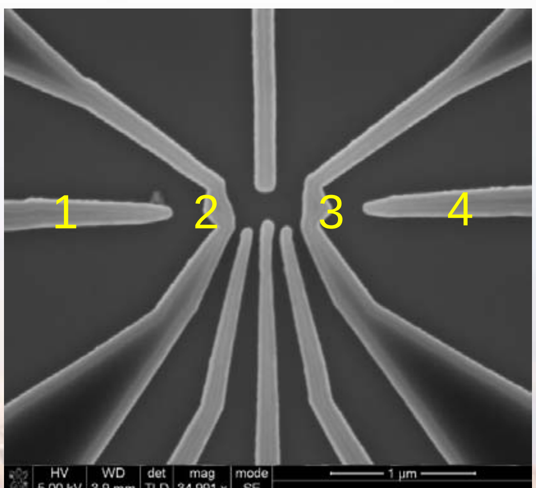




Micro-fab facility
E-beam lithography
Poly-silicon etch
Aluminum oxide
Top Al gate

Low parasitic RF die

GaAs design to Si



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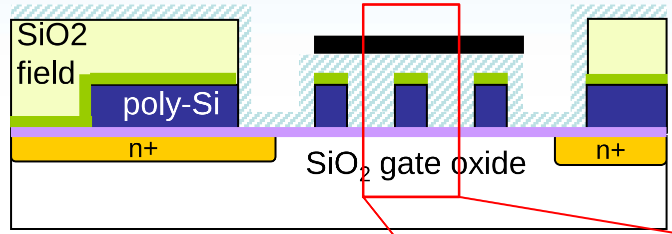
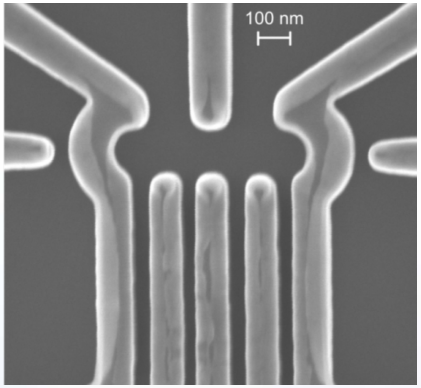
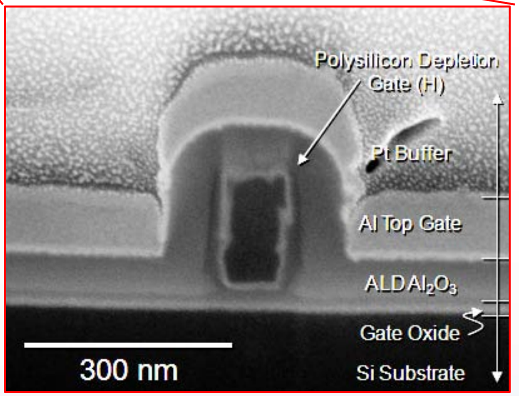
T. Pluym, B. Silva, J. Dominguez, N. Bishop, K. Childs

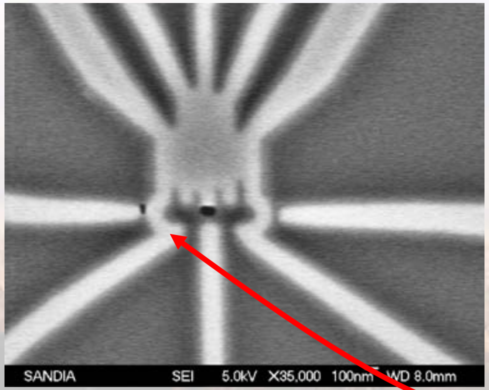
Process steps & modular drop-in

- MDL processing
- E-beam lithography
- Poly-Si etch
- EBL for implant window
- 40-100 kV implant
- Strip metal
- Poly-Si reoxidation
- Deposit ALD Al_2O_3
- Deposit Al gate
- Etch via holes
- Deposit Al pads
- Forming gas anneal





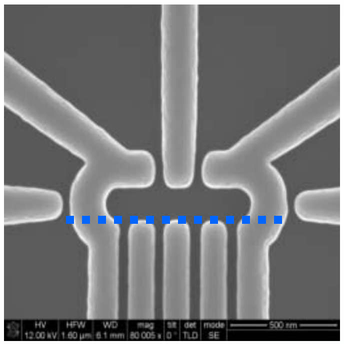


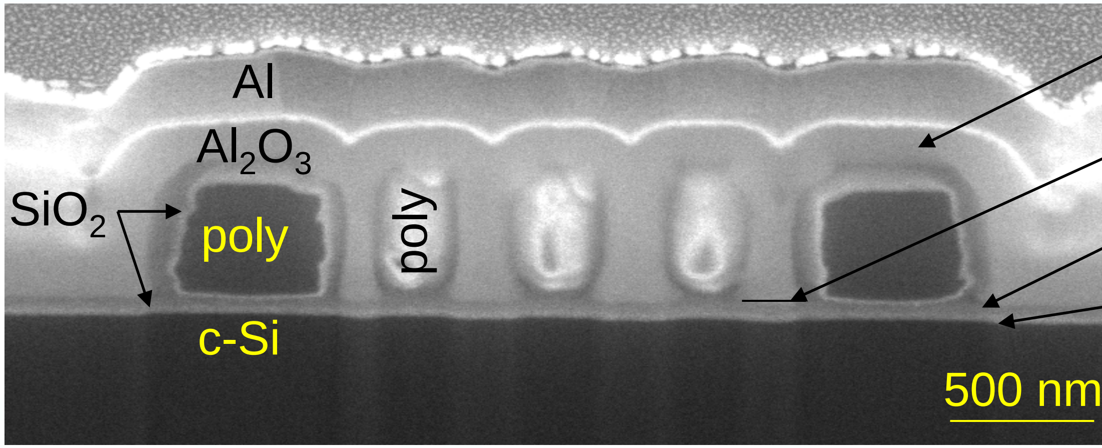


Implant here

Single ion detectors successfully integrated with polysilicon window

Immediate Challenge: Charge Defects

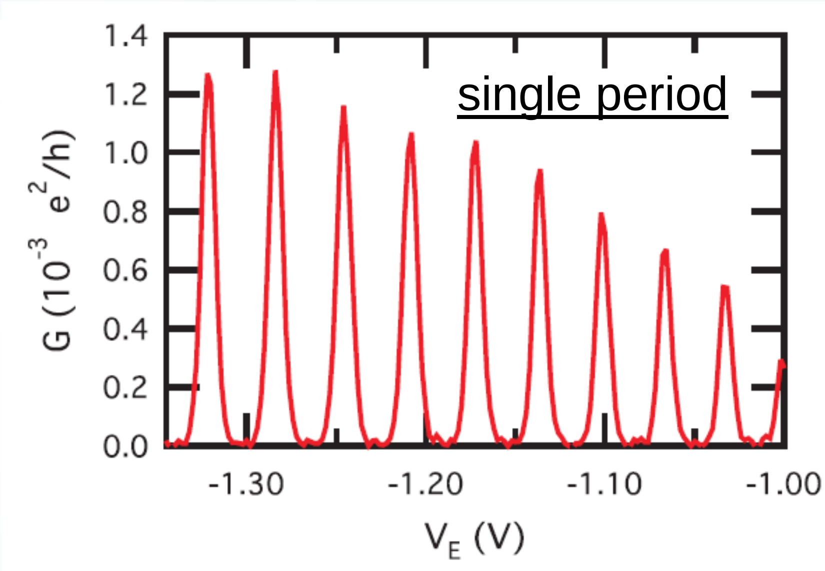




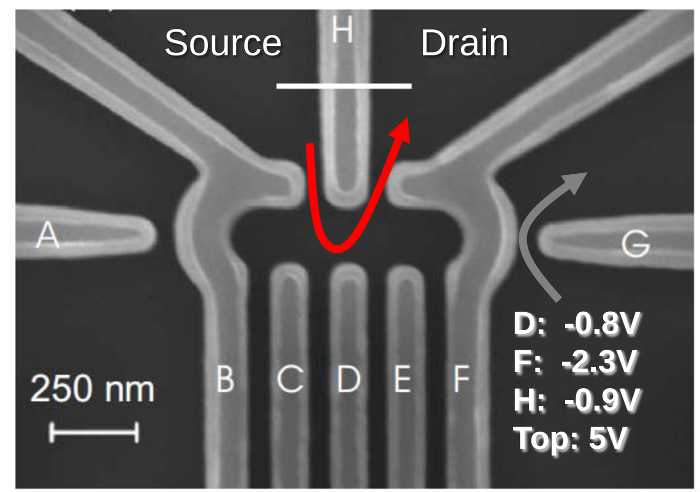
	Si Fab		QD Fab
mobility:	~15,000 ($cm^2V^{-1}s^{-1}$)	=>	~200
D_{it} :	~10^{10} $eV^{-1}cm^{-2}$	=>	~10^{12}
Q_{eff} :	~10^{11} cm^{-2}	=>	~10^{12}

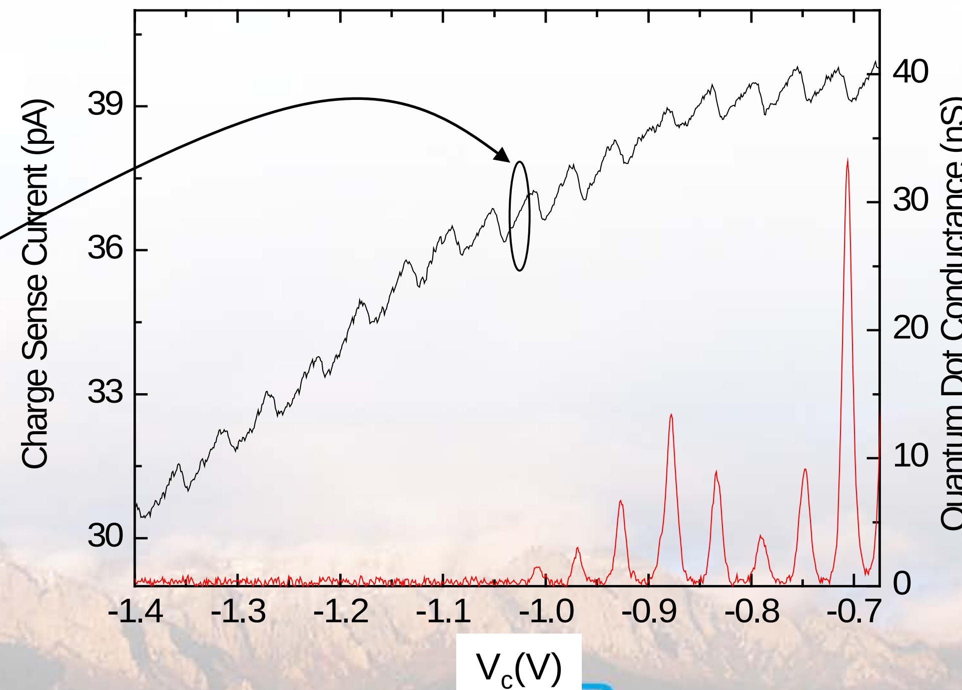
Quantified with C-V [G. Ten Eyck]

Sandia quantum dot platform



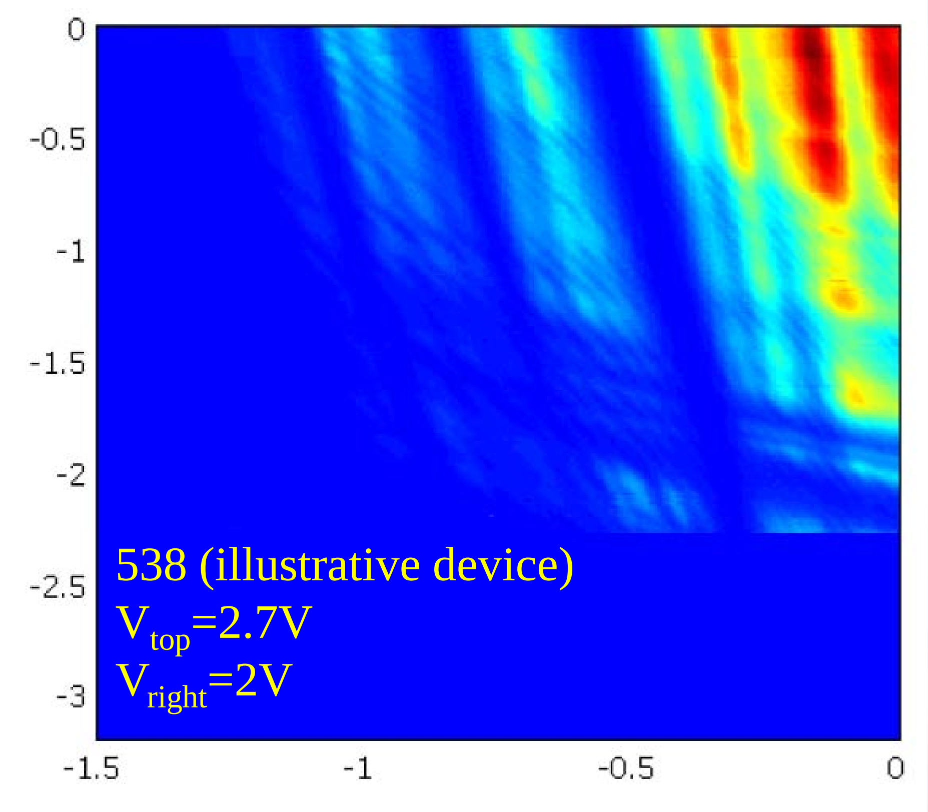
Improved processes (test stack):
Mobility: 8,000 ($cm^2V^{-1}s^{-1}$) [T ~ 4K]
D_{it} : 2.9 x 10^{10} $eV^{-1}cm^{-2}$
Q_{ox} : 1.1 x 10^{11} cm^{-2}
~ 2 charges per QD (r = 25 nm)



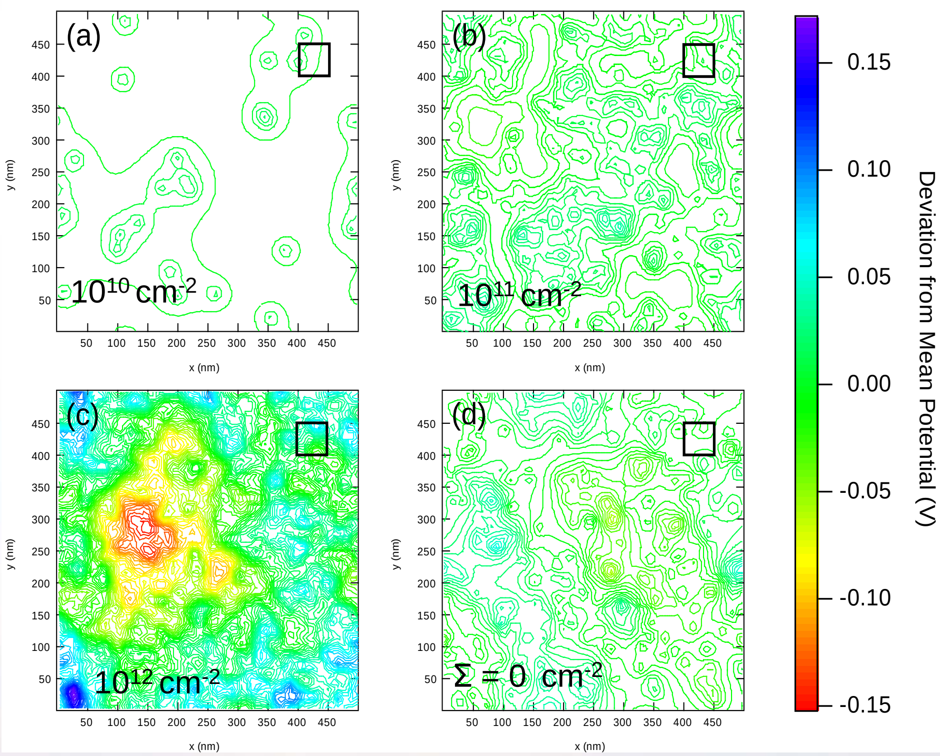


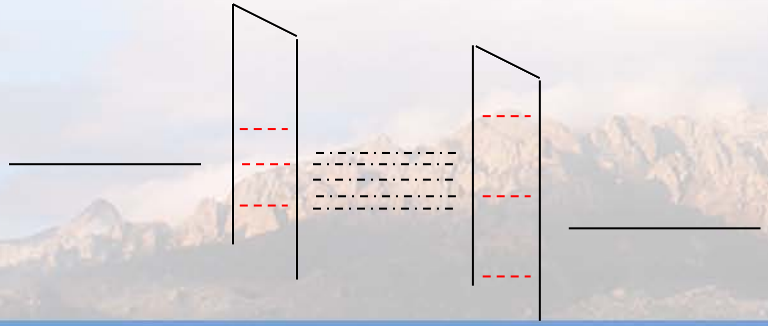
Nordberg et al., PRB (2009)

Disorder



RMS fluctuations approach GaAs at 10^{11} cm^{-2}





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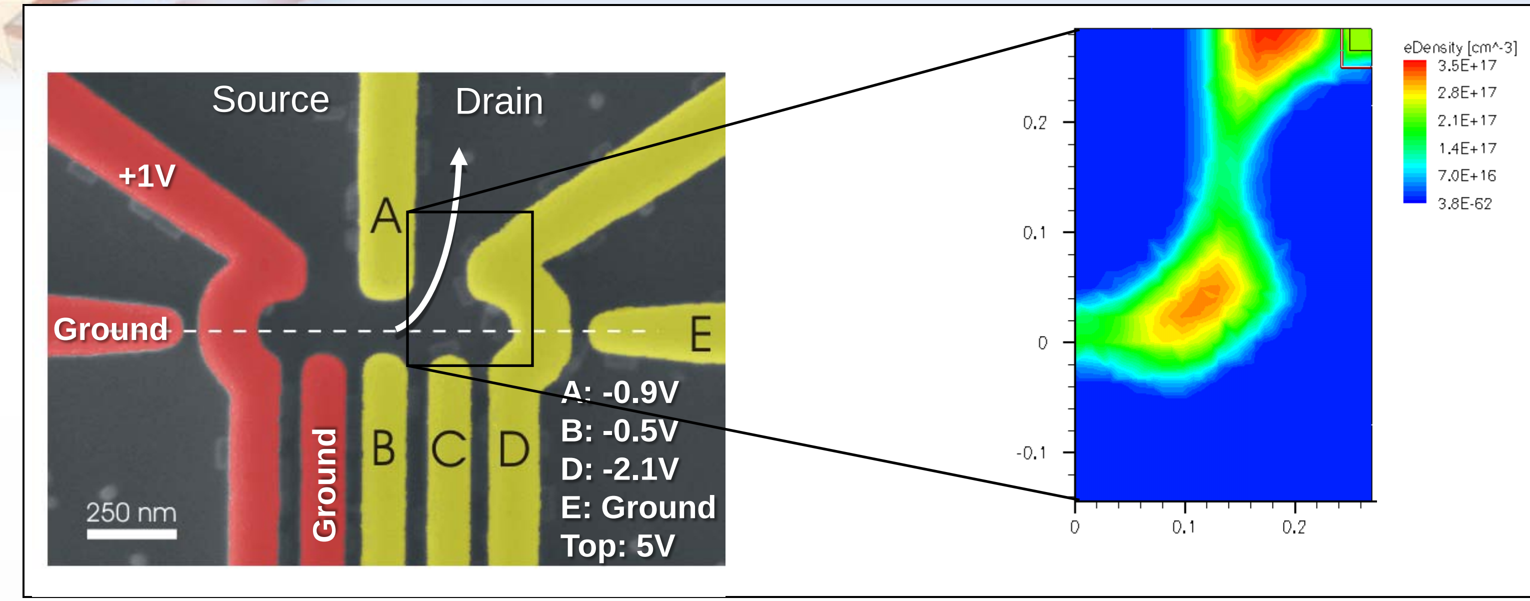
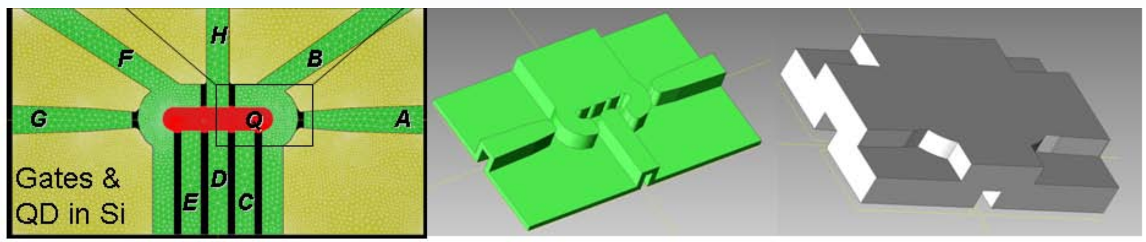
Lithographic dot verification



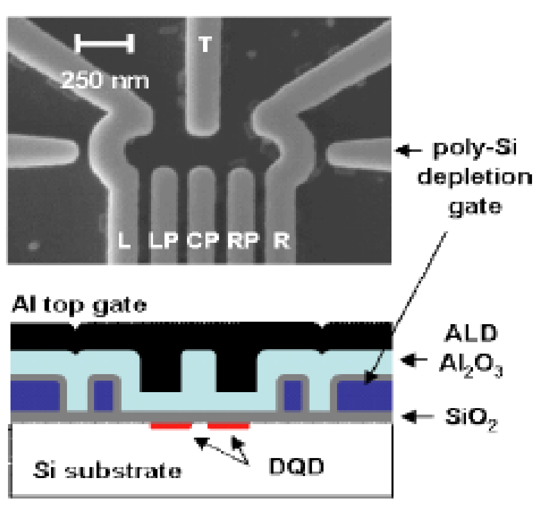
Gate	experiment [aF]	Model [aF]
A	6	6.2
B	3.2	3.3
C	3.3	3.4
D	7.2	7.3
Top	14.6	14.4

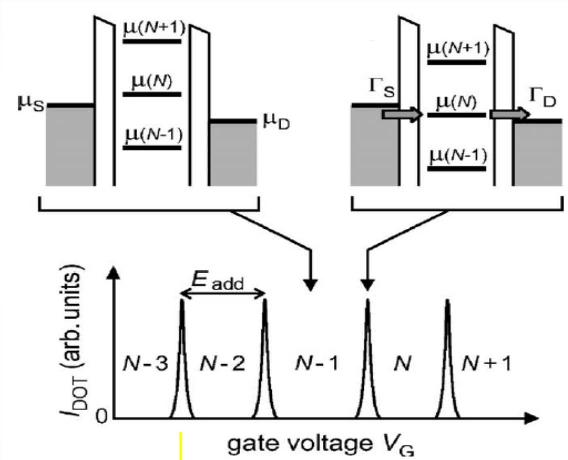


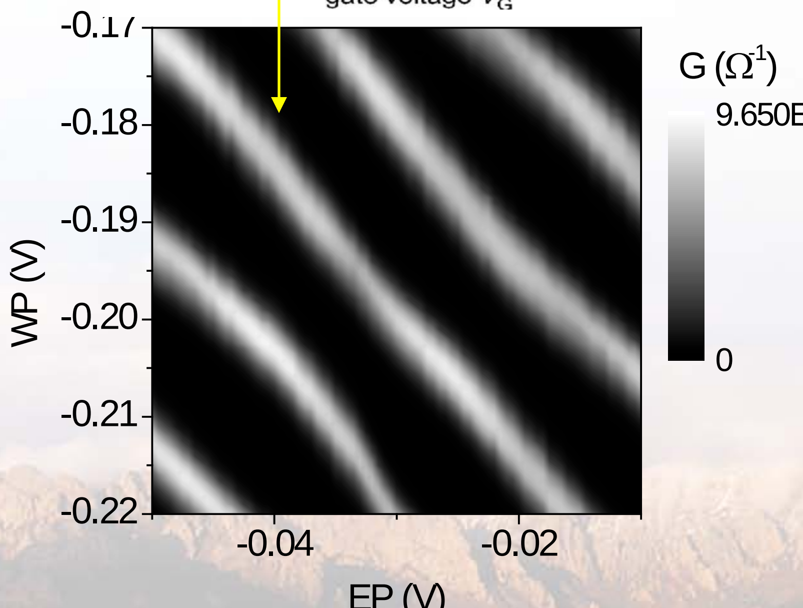
- Measured capacitances are consistent with lithographically formed dots
- Signal is consistent with 3D capacitance estimates for coupling

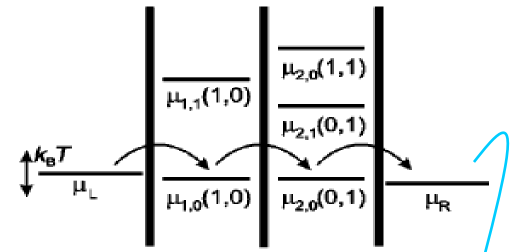
Stalford et al., IEEE T. Nanotechnology

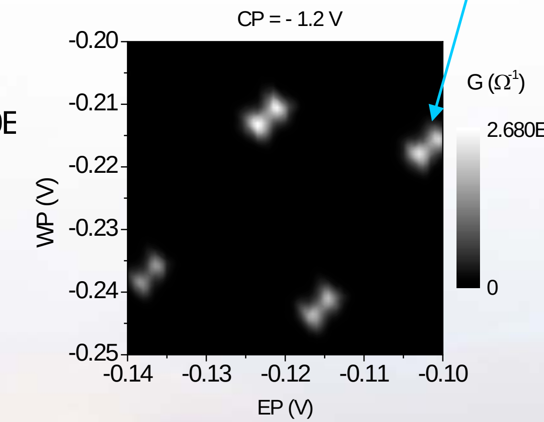
Reconfigurable Dot with Gates











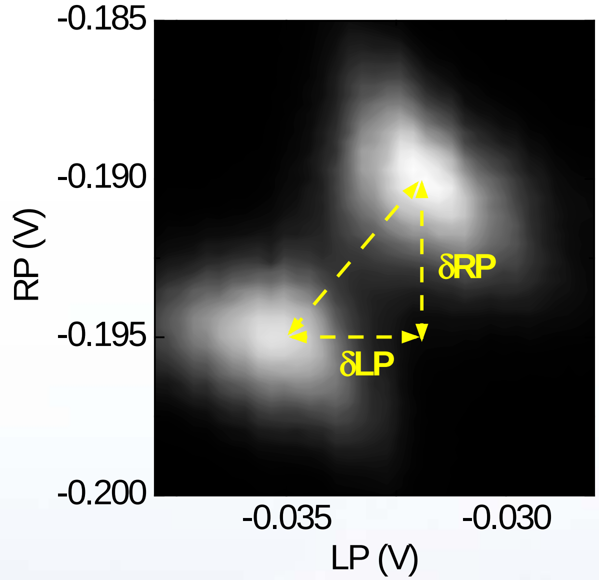
TG = 5.0V
T = -0.3V
CP = -1.2V
R = -2.0V

L. Tracy, et al.
APL 2010

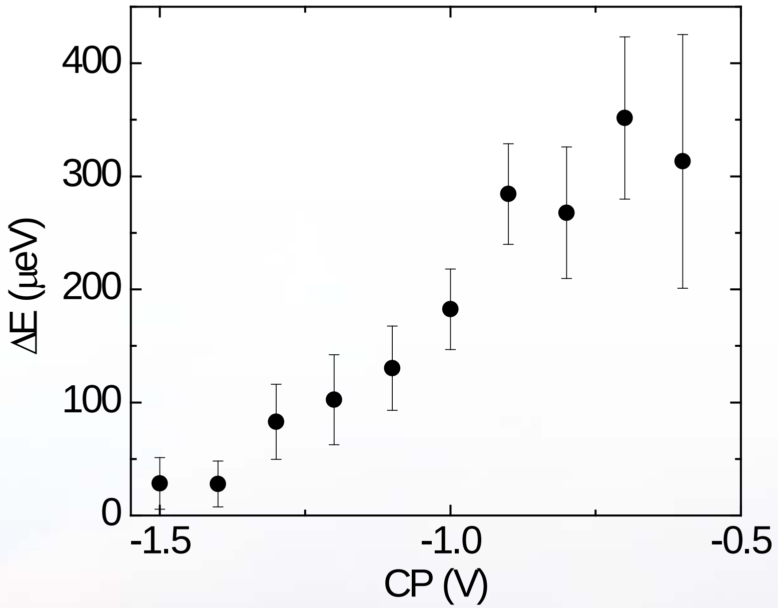
Double quantum dot tunneling strength

(L.Tracy)

Single triple point



Dot coupling

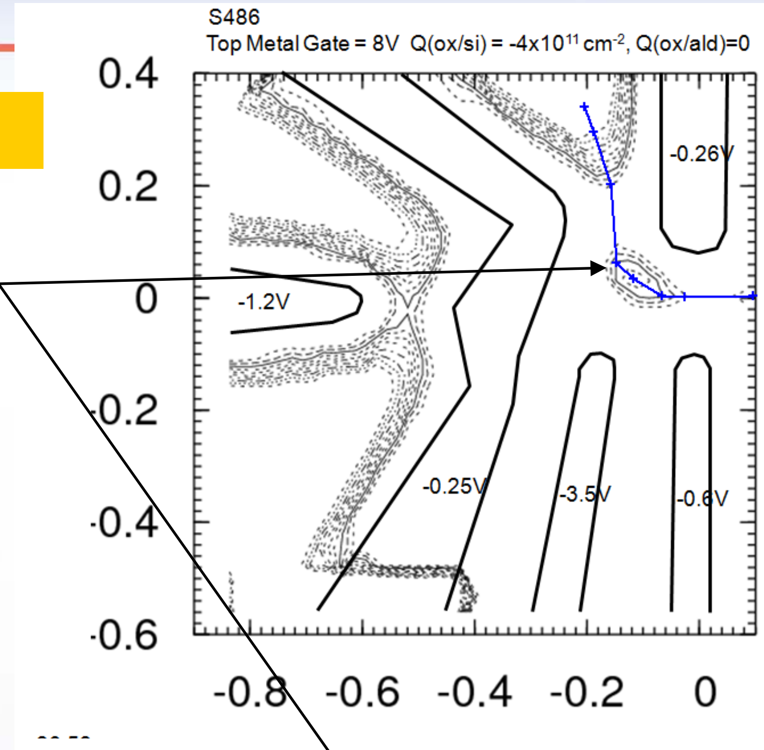


- $\Delta E = E_{cm} + 2t$, at lowest CP, $t = 0 \rightarrow C_m = 6$ aF
- Can tune t from < 14 ueV to possibly ~ 150 ueV
- All the basic functionality for the qubit demonstrated. <u>Need few electron S/T</u>

Challenges to achieving few electron

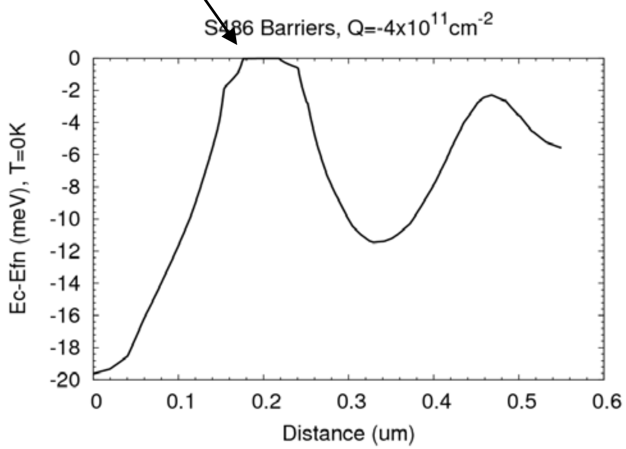
C_{top} agree with simulation (+/-20%) at 32 electrons

Challenge: More negative bias to reduce $N_{electron}$ ALSO results in wider tunnel barriers



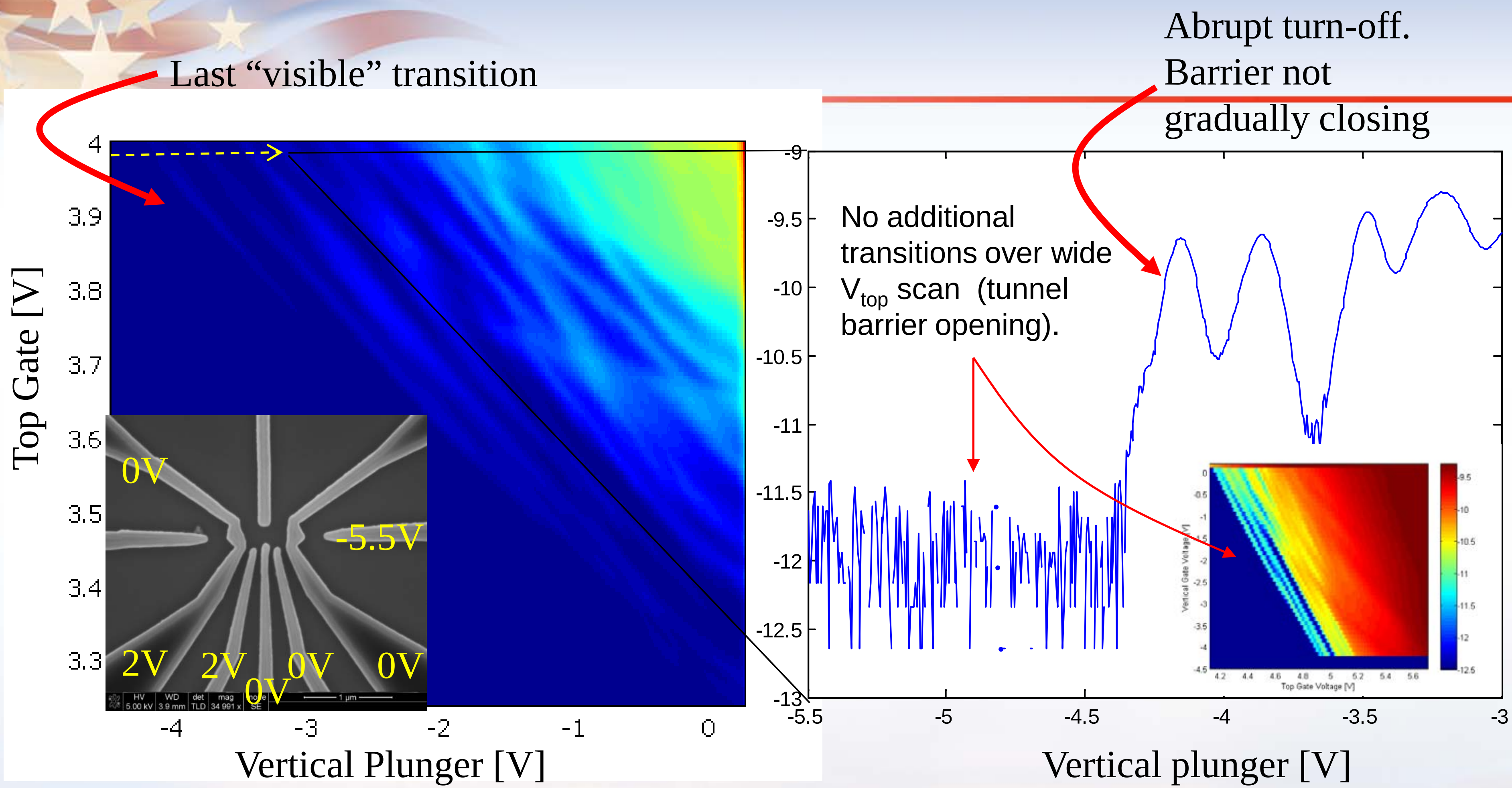
<u>Approach</u>

- Tunnel barrier
  - Design of gates as open as possible
  - Charge sensing technique
- Modeling: very good for analysis and qualitative design but not predictive
  - Trying to develop predictive deisgn
- Intelligent trial & error
  - Each scan ~ 1 day
  - Many scans to get tuned-up (large voltage space)
  - Can be order of 60 days to push a sample to limit & do all checks without success



R. Young

Wider tunnel barrier



- Edge of transport through dot observed
- Several possible reasons
  - tunnel barrier is gradually turning off (often the case)
  - Last electron
- <u>This case</u> is not gradual and no additional transitions are observed over reasonably large V_{top} scan

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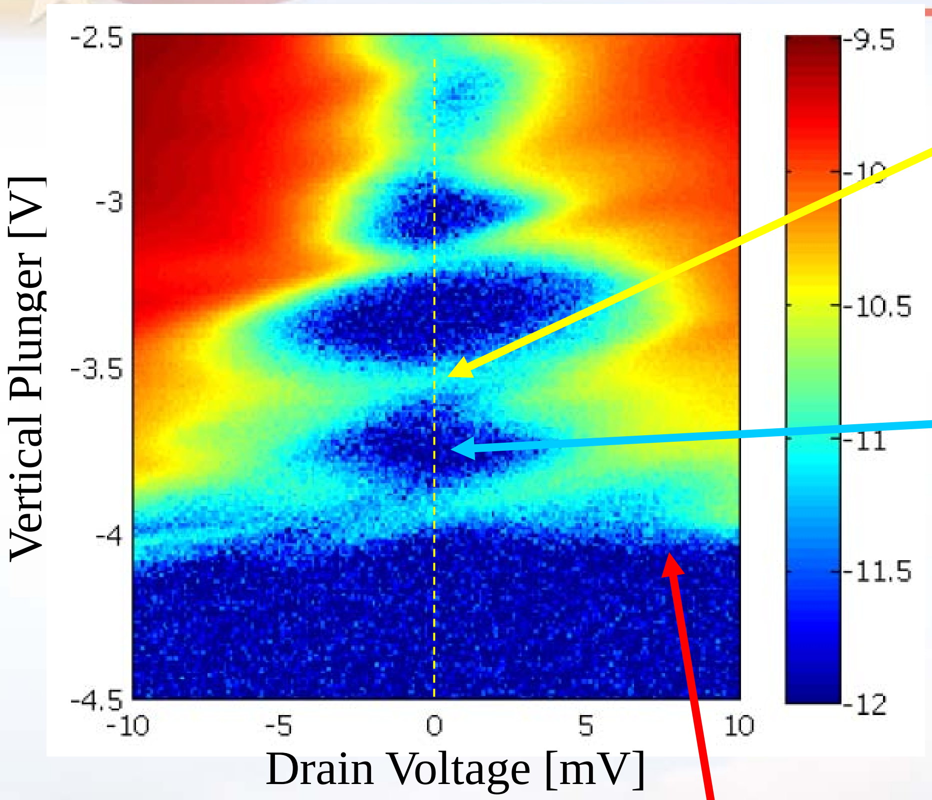
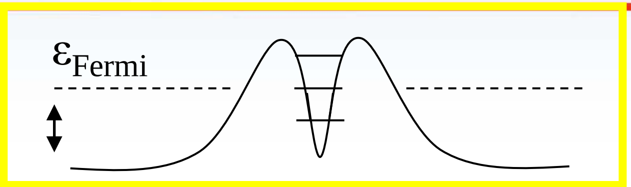
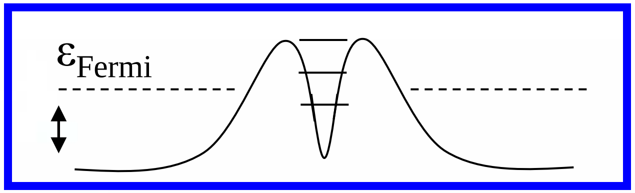
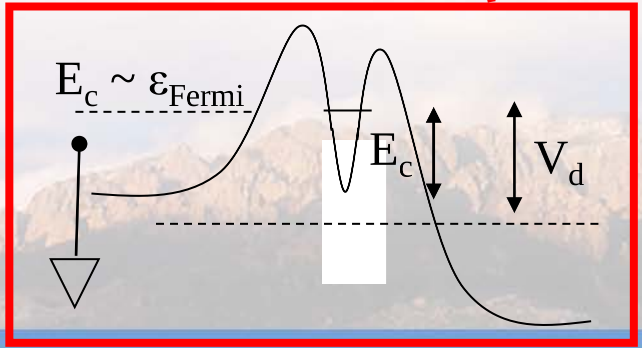
Charging energy and tunnel barrier probe







- No transitions observed at high V_{sd} beyond -4V on plunger
- V_{sd} can be set that all levels in dot can empty
- Edge of opening corresponds to line-up of energy level with Fermi energy
- Ideal case, well depth is no greater than Fermi energy
- Largest charging energy approximately equal to Fermi energy (5-6 meV)
- This sample examined up to ~2*Fermi energy
- $C_{top\text{-}meas}$ ~ 2.6 aF ($C_{top\text{-}sim\text{-}N=1}$ = 2.2 aF)
- Three measurements suggestive of N=1
  - Other groups have used this as a test of N=1



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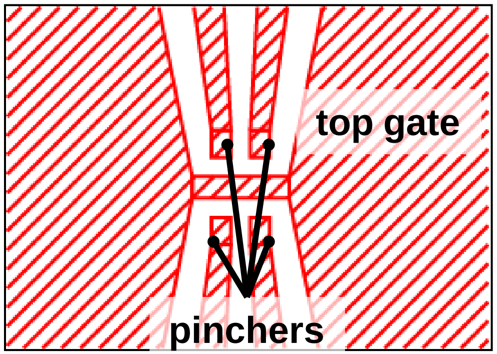
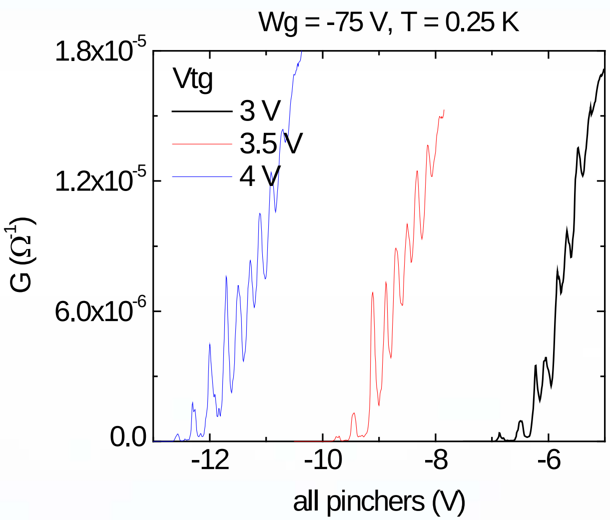
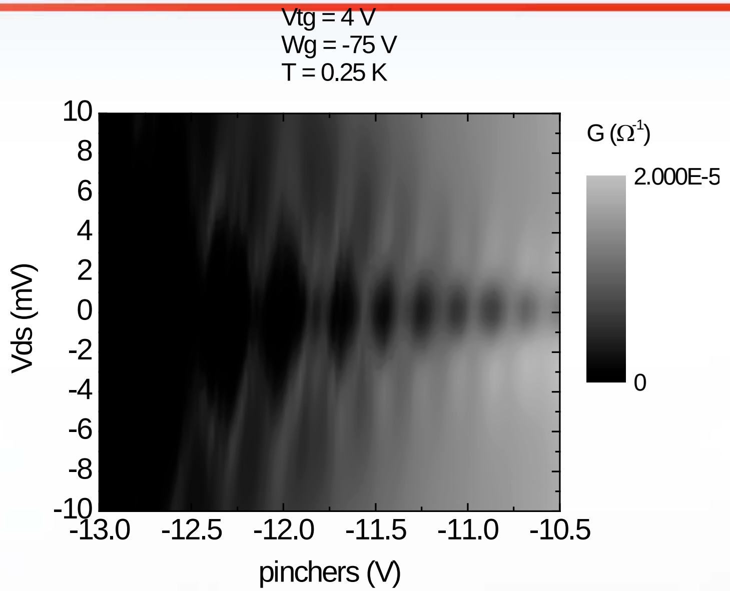
Last electron in MOS?

(K. Eng & L. Tracy)

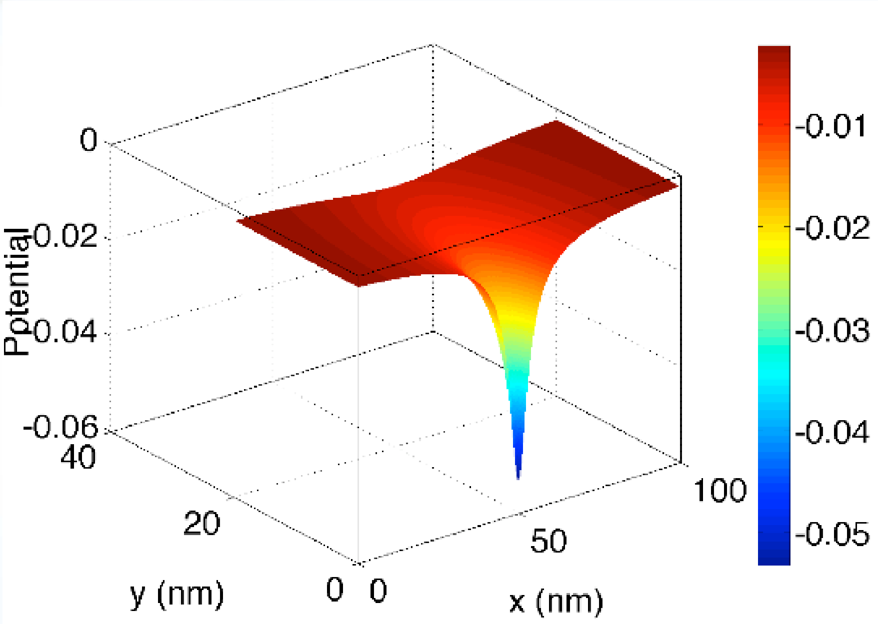


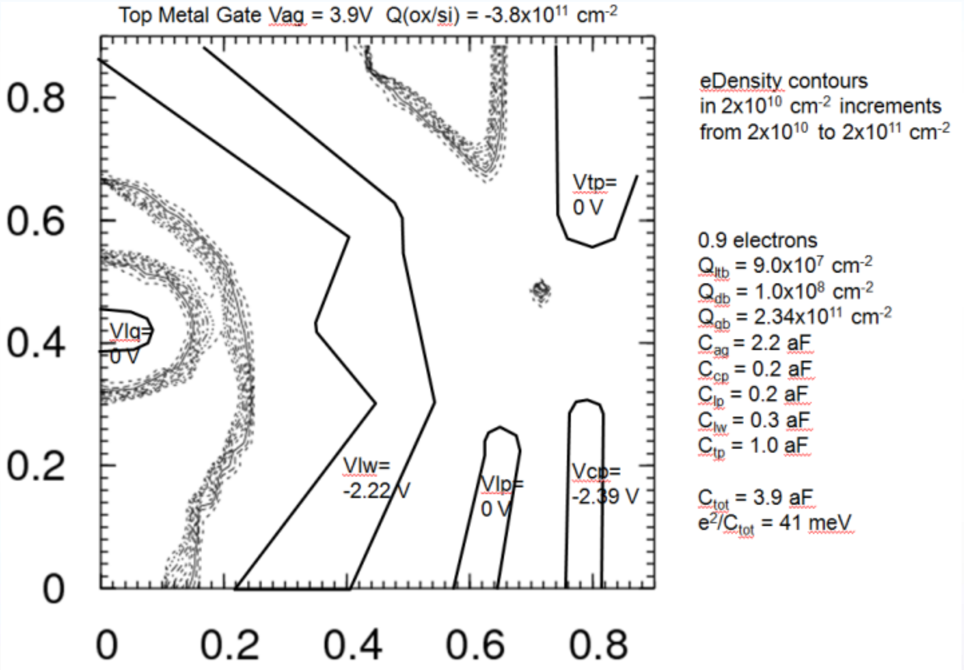




- Common in MOS for Ec to become very large as N is reduced
- This structure is 180 nm with negative top gate bias

Last electron modeling





D_{it} or Q_{ox} ($cm^{-2}eV^{-1}$) or (cm^{-2})

- 1×10^{10} → 0.04 per QD
- 1×10^{11} → 0.4 per QD
- 1×10^{12} → 4 per QD

CI modification to TCAD

- Single positive charge at SiO2 interface can strongly localize electron & large binding E
- Last transitions jump in charging energy? Operate in closed shell N>1?
- But electrostatic dot is also predicted to be very small!!
  - Similar sizes predicted (~20 nm x 20 nm)

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Other considerations: Decoherence near Oxide

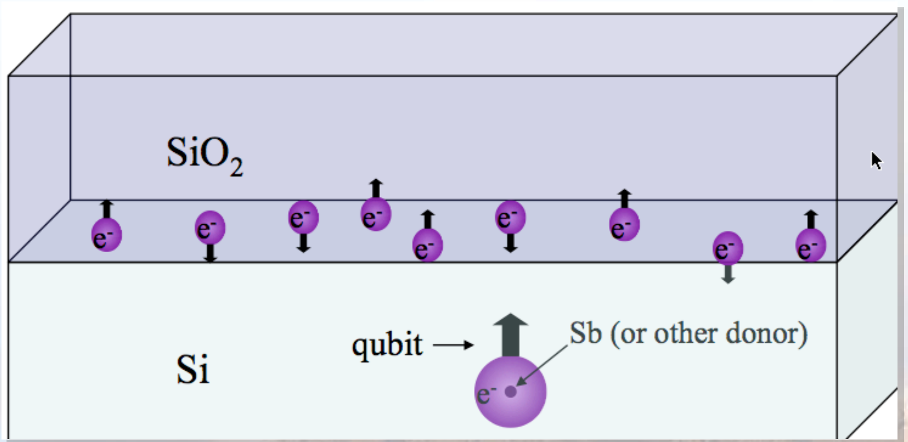
Schenkel et al. APL (2004)

Sample	Interface	Peak depth (nm)	T_1 (ms)	T_2 (ms)
120 keV	Si/SiO_2	50	15±2	0.30±0.03
120 keV	Si—H	50	16±2	0.75±0.04
400 keV	Si/SiO_2	150	16±1	1.5±0.1
400 keV	Si—H	150	14±1	2.1±0.1

SiO_2 from SNL **(2010)**

d (nm)	T_2 (SNL SiO_2)
25	490 μs
100	520 μs

99.95% ^{28}Si



- **T_2 not as long as bulk**
- **Some potential variation in T_2 oxide to oxide but problem persists**
  - **Preliminary result**
- **Resolvable with sufficient B-field and low enough temperature?**

Doubt: decoherence just not well understood
- **understand problem**
- **eliminate decoherence**

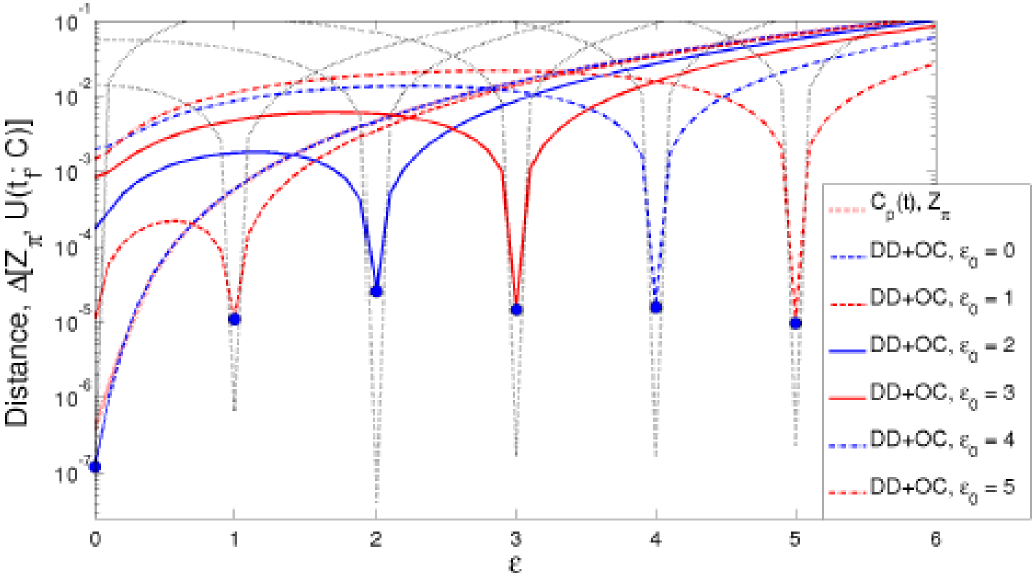
Optimal Control & Dynamical Decoupling for idle

Control

Uncontrolled rotation from spin bath

$$H = \sigma_z C_z(t) + \epsilon\sigma_x$$

$$\theta(t) = \int_0^t \vec{C}(\tau)\mathrm{d}\tau$$



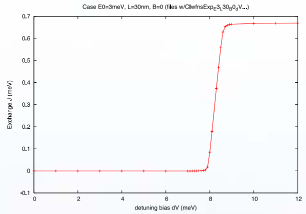
Passini et al => 1st and 2nd order (parameter independent)

Grace => DD+OC produces improved DD or more robust OC

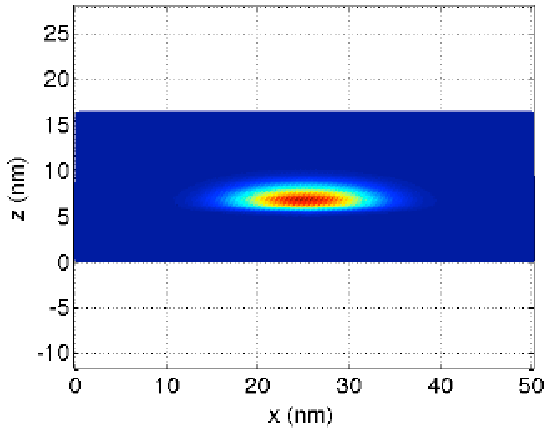
$$\mathcal{F}:\ 0.99 \ \rightarrow\ 0.9999$$

Grace et al., arXiv:1105.2358

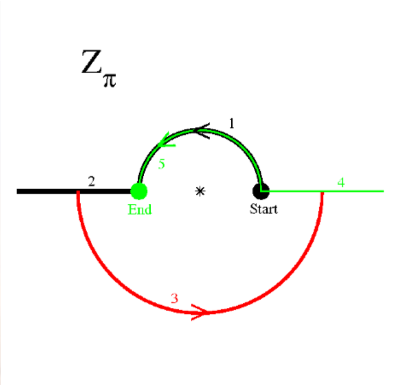
X-gate & dynamically corrected gates (DCG)



E=20 MV/m



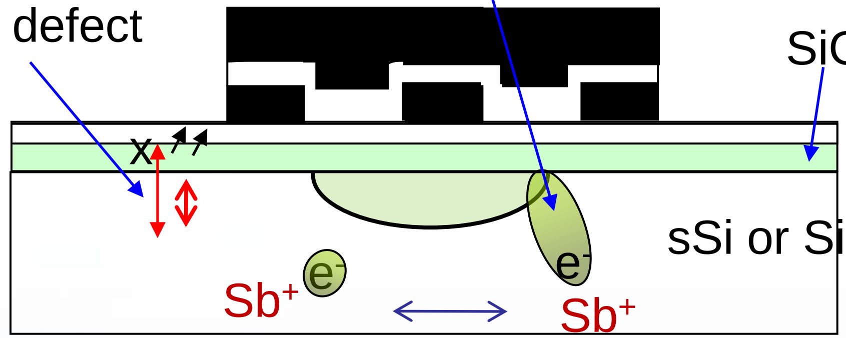
$$Z_\pi \;:=\; \tilde{Z}_\pi(\omega)\text{-}\tilde{I}[\tau]\text{-}\tilde{Z}_\pi(\omega/2)\text{-}\tilde{I}[\tau]\text{-}\tilde{Z}_\pi(\omega)$$



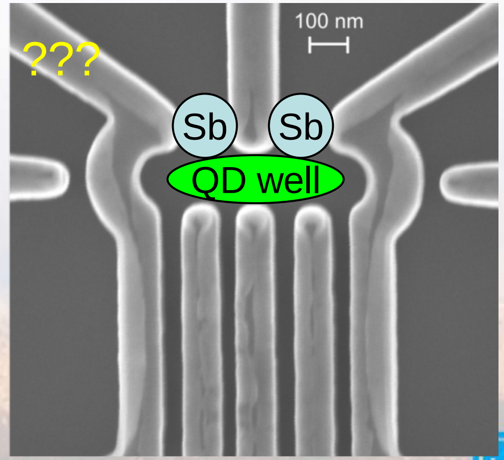
- Hahn-echo works because spin bath of first half is strongly correlated with second
  - Z-I-Z-I
- DCG sometimes leads to different configurations Z-I-Z-X

Alternate modes of SNL platrform for increased Distance from Surface (Donors & sSi/SiGe)

- sSi/SiGe Enhancement Mode Approach
  - Push defects away

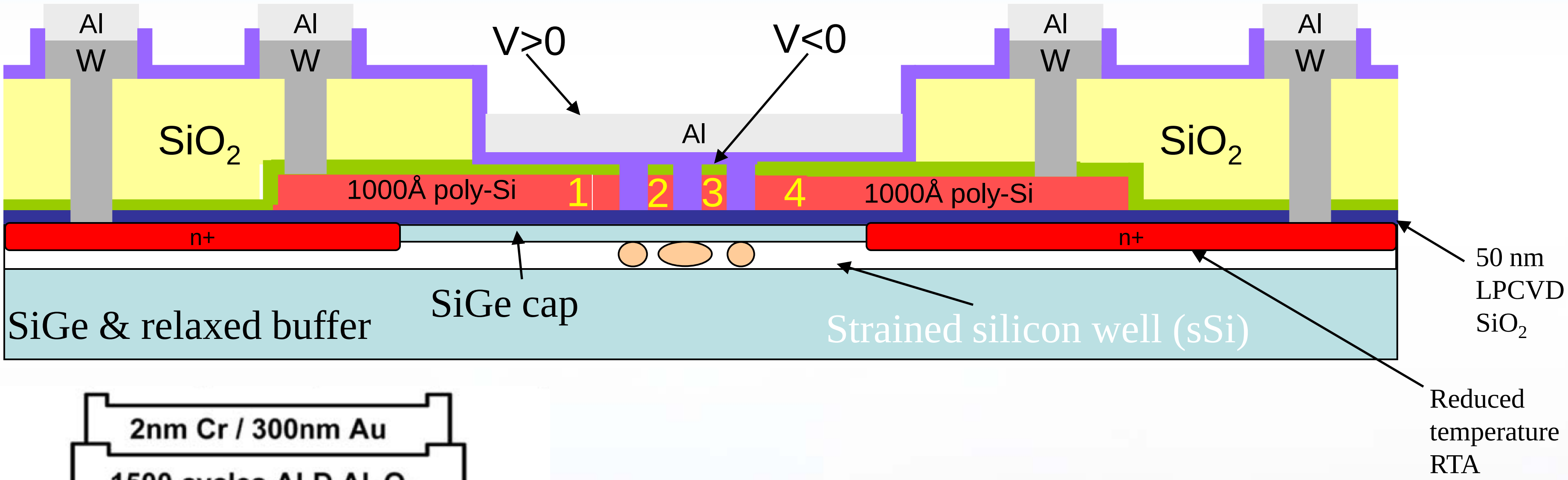


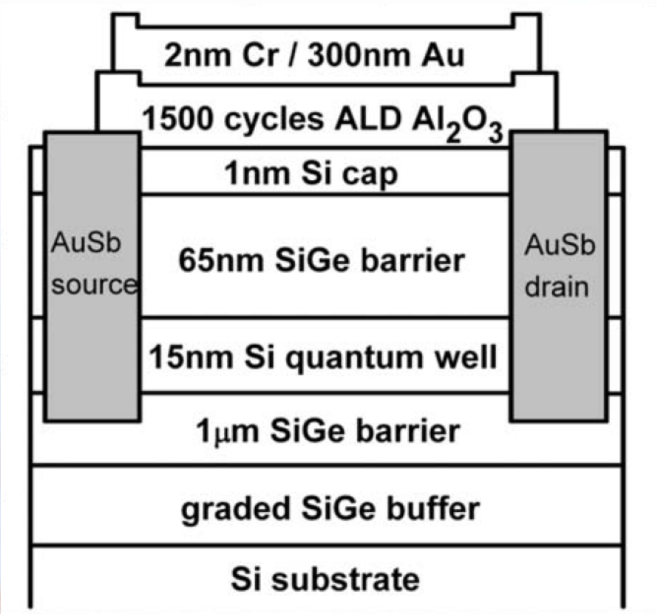
- Donors
  - Long T_2 at depth & large E_{vs}
  - How can we couple to donors?



Bishop et al (in preparation)

Enhancement Mode SiGe/sSi: High Mobility & Modular Change to MOS Flow



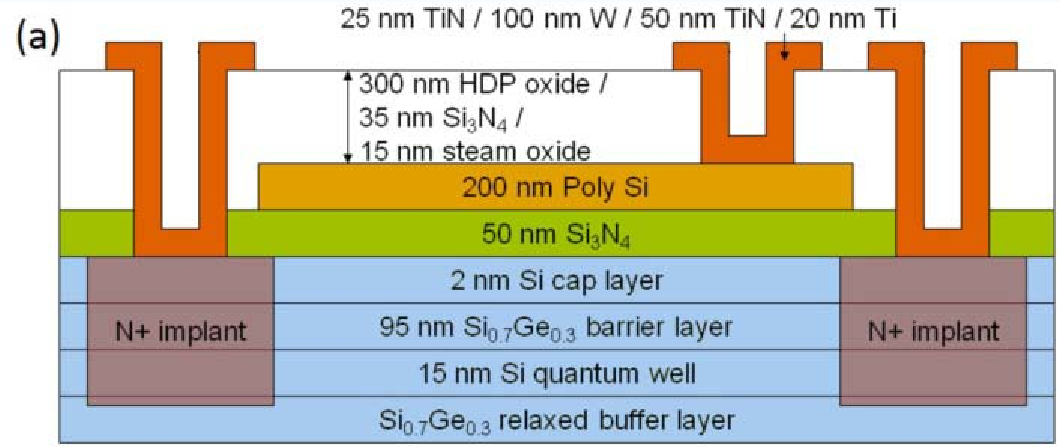


Undoped SiGe Heterostructure

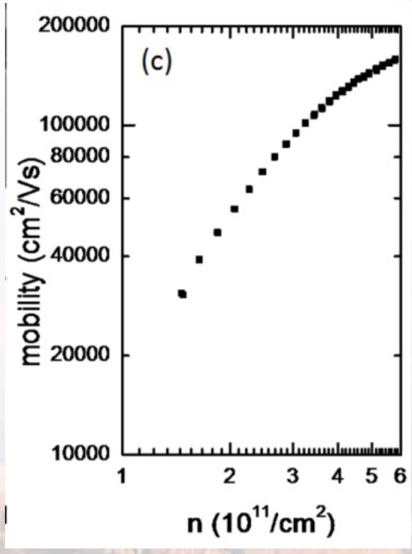
Lu et. al., APL **94**, 182102 (2009)

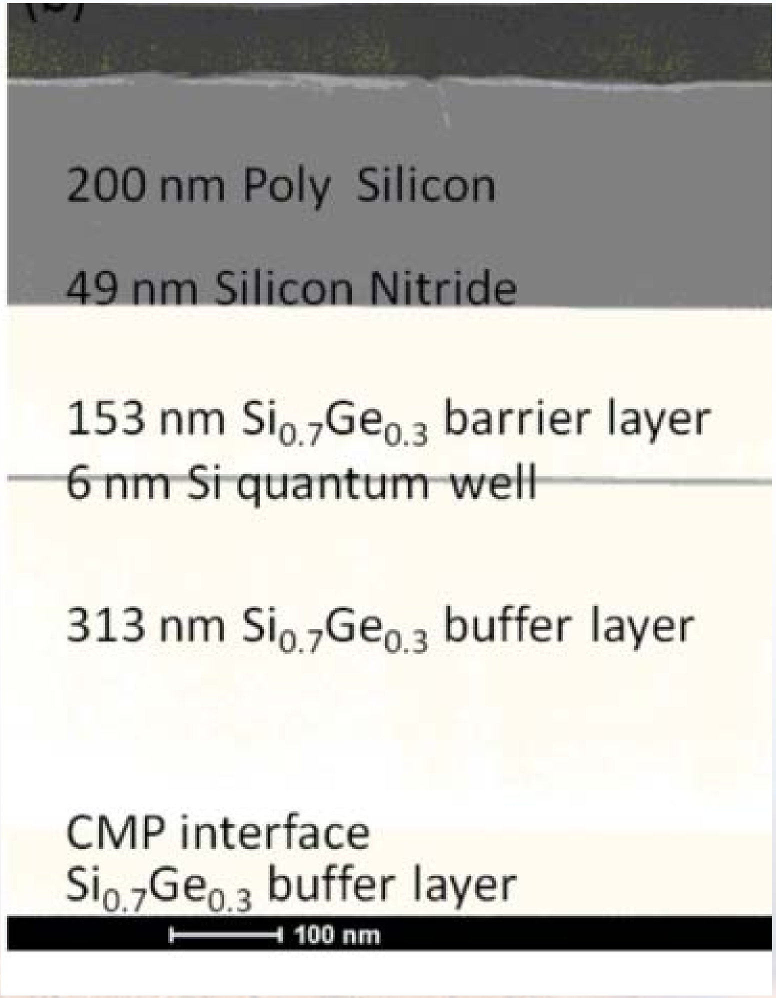
Mobility ~1.6×10^6 cm^2/Vs

Back to the fab: SiGe/sSi

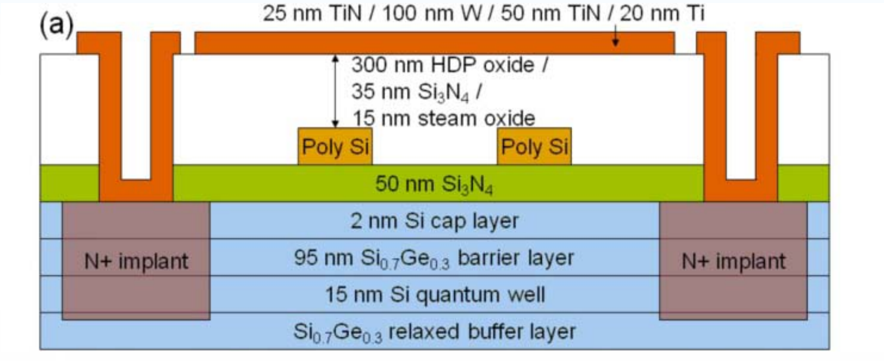


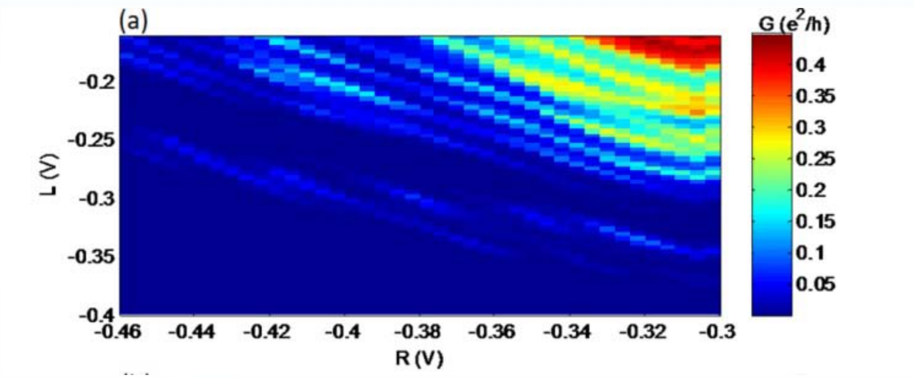
- Modifications:
  1. Substrate
  2. Gate dielectric
  3. Implant & anneals
- Questions:
  1. Ge/Si diffusion
  2. Surface pinning
  3. Mobilty

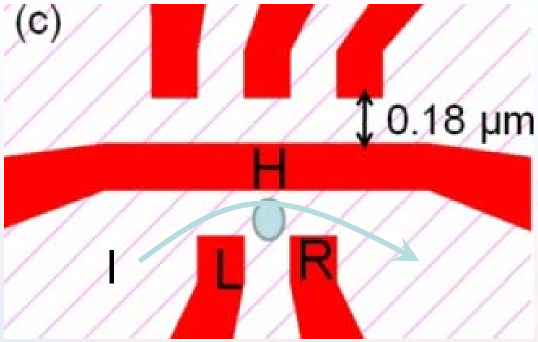


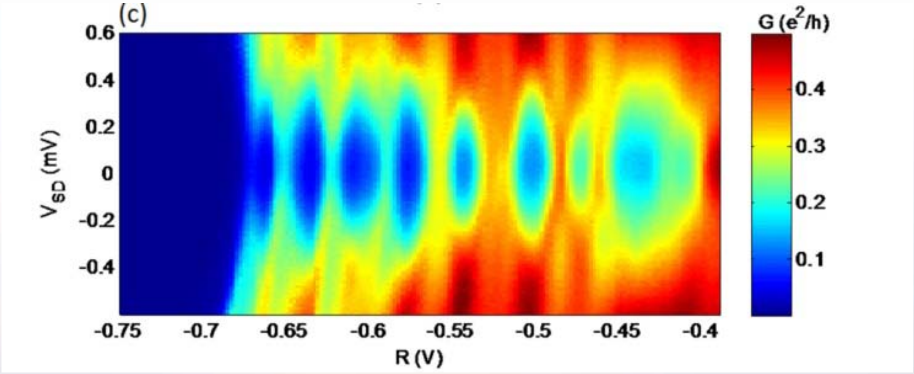


Transport through SiGe/sSi dot





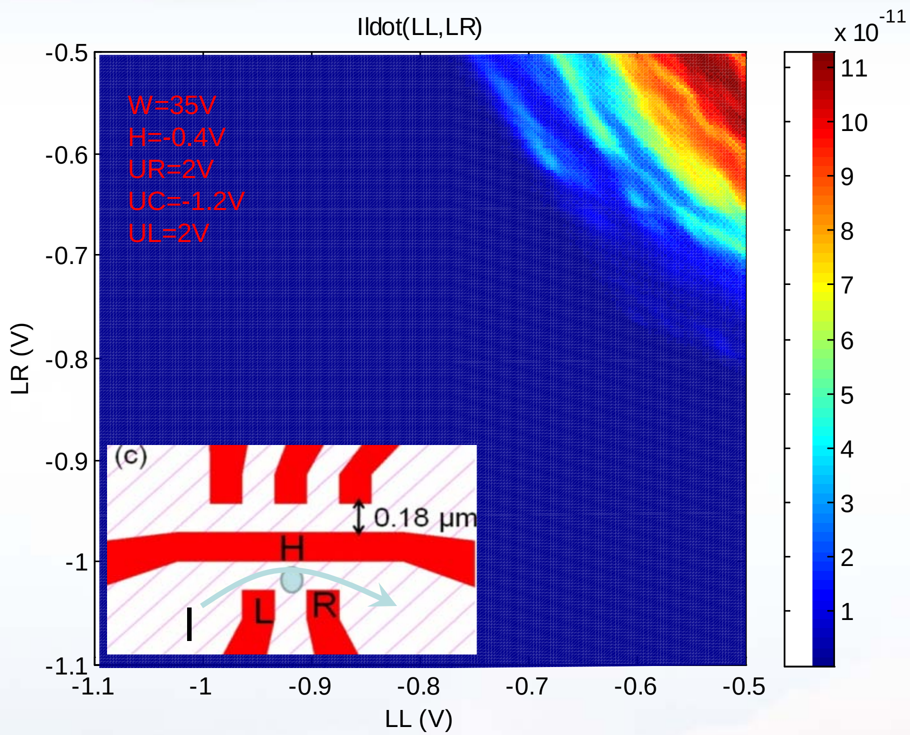


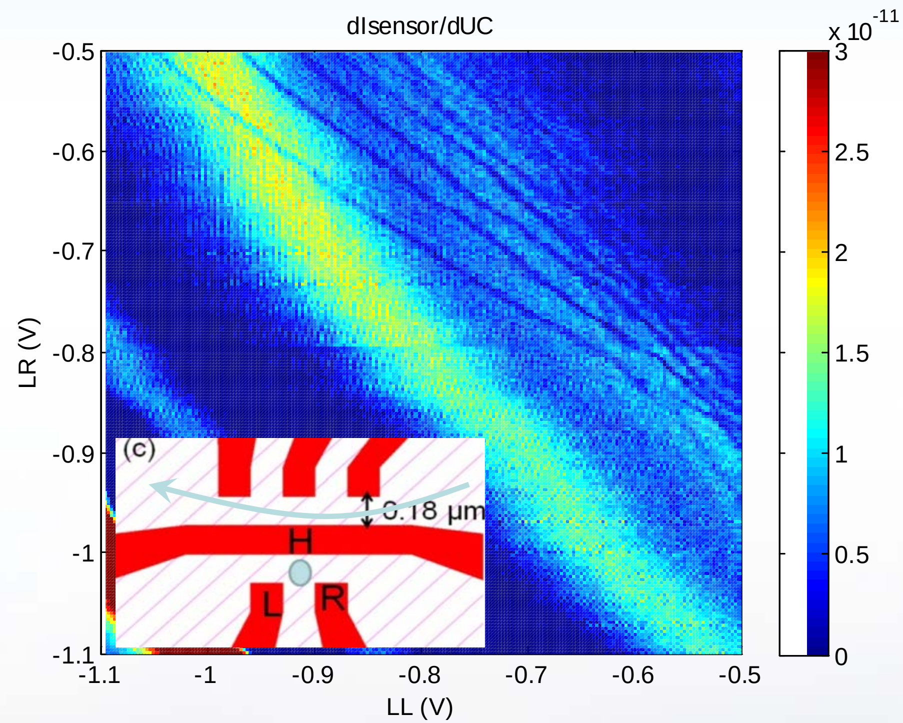


- Double top gated quantum dot w/ DUV lithography
- Relatively regular CB observed w/ small charging energy

Lu et al, (in preparation)

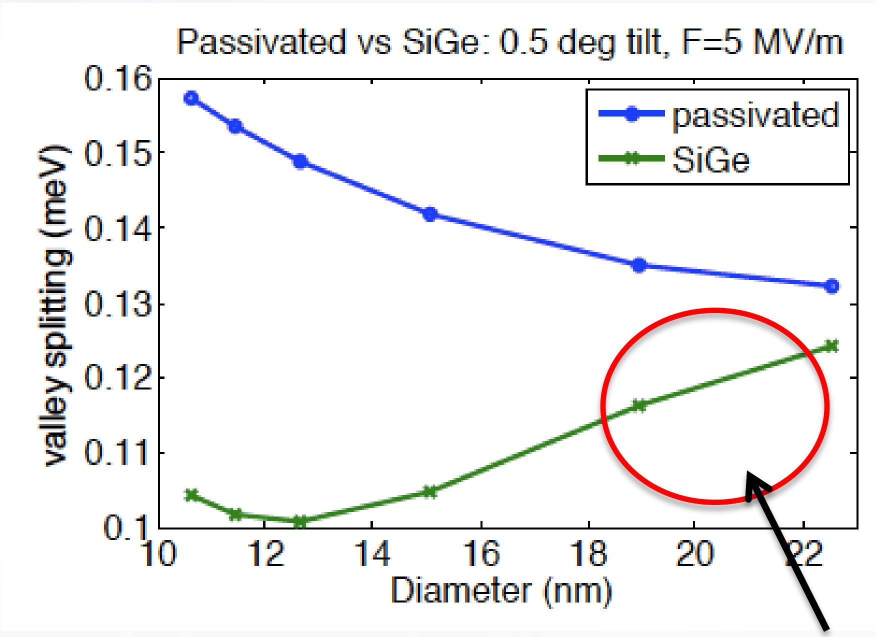
Charge sensing: last transition



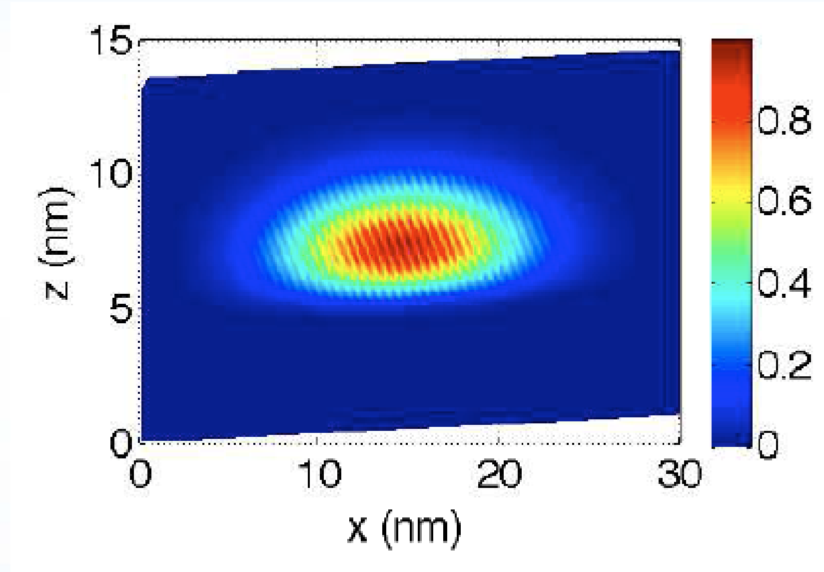


- Threshold shifts seen in these devices (tested ~5)
- New charge configuration looks different
- Opposite channel used as charge sensor
- Last transition in region of high sensitivity of sensor
  - looks like the last electron

Few electron energetics



Roughness



- Evidence suggests that VS can be big enough
- Ge and Ge profile dependence not well understood
- Atomistic modeling + CI : looking in to question
- Big phase space with E-field & processing
- Experimental tools: addition energy, spin filling, S/T sensing

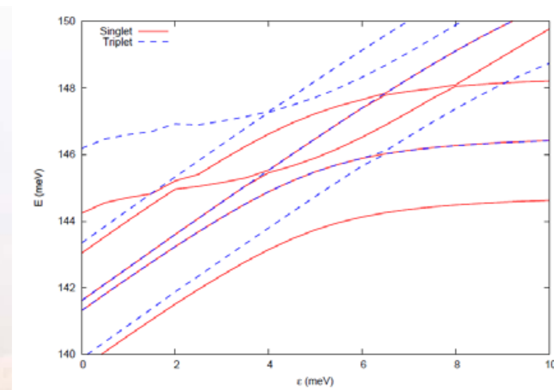
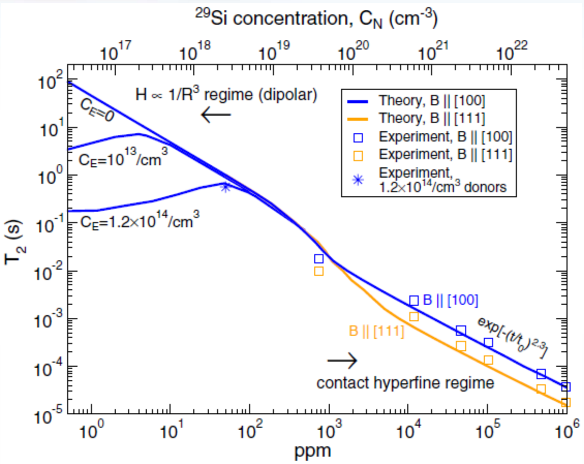


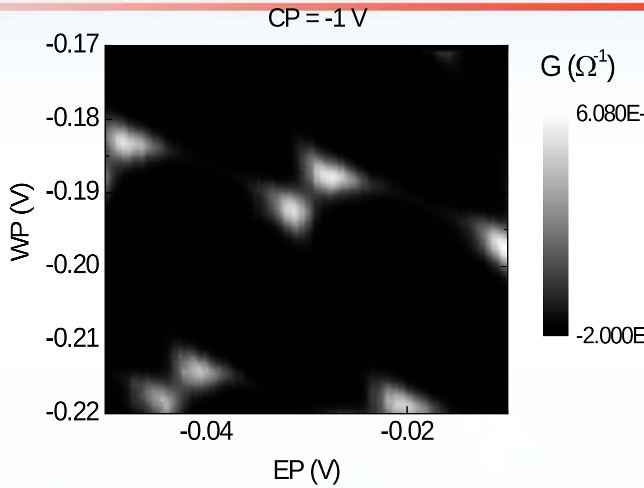
FIG. 2: Energy levels of a silicon (passivated-surface) DQD as a function of detuning parameter ϵ. $L = 20\,\mathrm{nm}$, $a = 0.0001\,\mathrm{eV/nm^2}$, and $E_z = 20\,\mathrm{meV/nm}$.

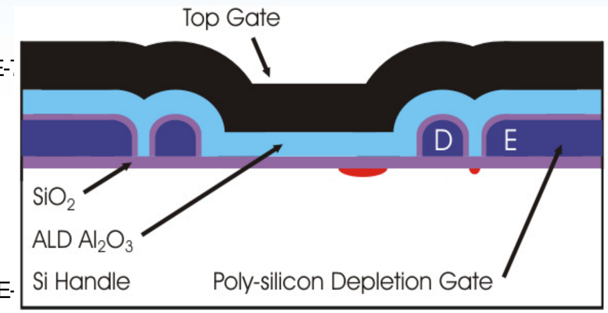
Where are things at?

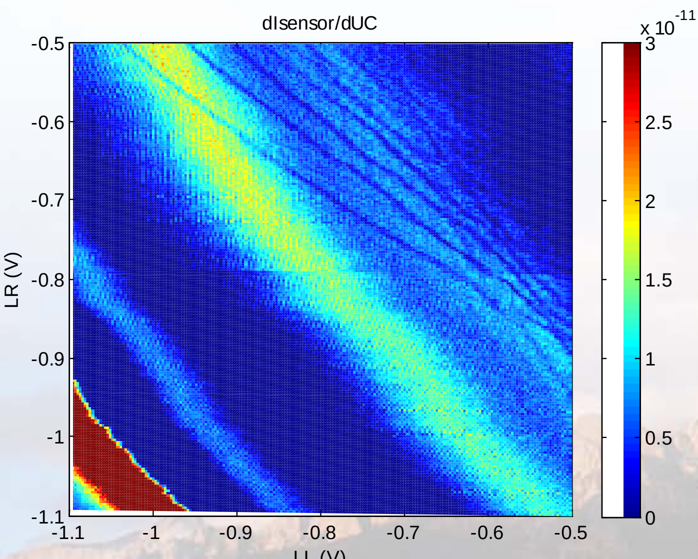
- Many Si groups showing single electron control
- Reports of coherent oscillations in both donors and SiGe/sSi
  - Last year it was spin read-out and T1
  - This year… T2* or T2?
- GaAs community has shown full control of qubit and are now working on two
- Moving fast and it's exciting
- At SNL:
  - Experiment and theory are geared at trying to understand device physics and what is needed for logical qubits
    - MOS DQD : jury is still out, lots of learning, good for donor technology
    - SiGe/sSi DQD : looks promising, perhaps less risk
    - Donors : really hard fab, big pay-off potential
  - Foundry fab:
    - learning on several paths
    - Extra devices: hand-shake with those interested in using foundry devices (joint learning!)

Summary









- Lateral, QD platform demonstrated
  - Low damage for MOS ($Q_f \sim 10^{11}$ cm^{-2} , $D_{it} \sim 10^{10}$ cm^{-2} eV^{-1}, mobility ~ 8000)
  - 150,000 mobility for SiGe/sSi
- Double quantum dot,charge sensing low electron number
  - Last electron charge sensed
- Decoherence times can be long in Si
  - Relationship to impurities and enrichment well understood
  - DD , DCG and OC show promise to reach logical circuit requirements
- Lots still to do:
  - Few electron charge sensed DQD (S/T)
  - Si QD physics (e.g., valleys)
  - Decoherence near oxide/Si interface??

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  Silicon quantum dot: M. Lilly, N. Bishop, S. Carr, T.-Z. Lu, L. Tracy, K. Nguyen, T. Pluym, J. Dominguez, J. Wendt, J. Stevens, B. Silva, E. Bower, R. Gillen

  Donor and donor-dot: E. Bielejec, E. Bussmann, D. Perry, B. McWatters, A. MacDonald

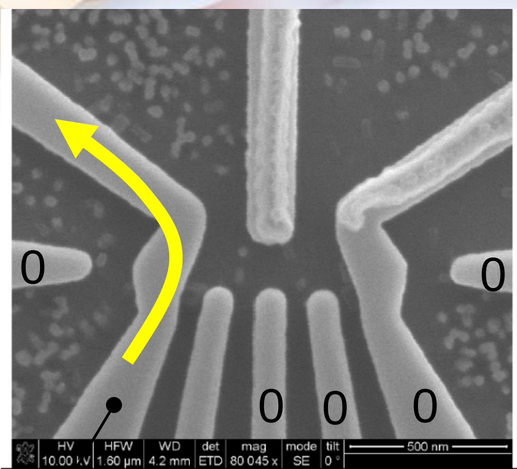
  Device modeling: R. Muller, R. Young, W. Witzel, E. Nielsen, R. Rahman, K. Young, J. Verley

  Cryogenic electronics: T. Gurrieri, J. Levy, R. Young, J. Hamlet, K. Barkley

  Architecture and quantum error correction: A. Ganti, M. Grace, W. Witzel, U. Onunkwo, A. Landahl, C. Phillips, R. Carr, T. Tarman

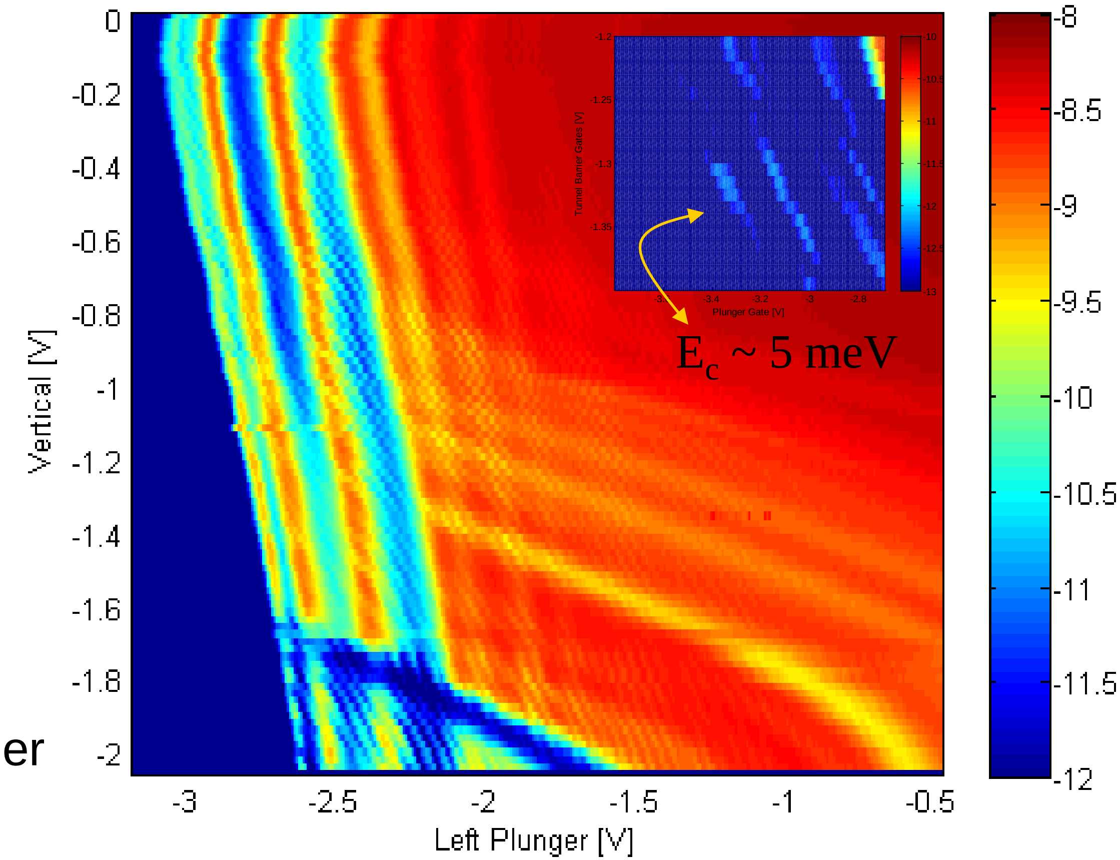
- Joint research efforts with external community:
  - U. Wisconsin (M. Eriksson, D. Savage, M. Friesen, R. Joynt)
  - Australian Centre for Quantum computing Technology (L. Hollenberg, D. Jamieson, M. Simmons, A. Dzurak, A. Morello)
  - Princeton University (S. Lyon)
  - U. Maryland (S. Das Sarma, M. Peckerar)
  - Lawrence Berkeley National Labs (T. Schenkel)
  - National Research Council (A. Sachrajda)
  - U. Sherbrooke (M. Pioro-Ladriere)

Disorder and ideal behavior



V=1.9V
V_{top}= -0.1

ow band diagram model of disorder



- Top gate capacitance measured to be ~27 aF in 35 nm SiO_2 structure (R ~ 90 nm)
- Threshold of dot region ~ 1.4V
- Very simplistic estimates with depletion from gates & $C_{measured}$: N_{elec} < 10 electrons
- Number of electrons is ambiguous because of uncertainties in values like V_{th} and C(V)
  - Charge sensing will be important to verify electron number

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