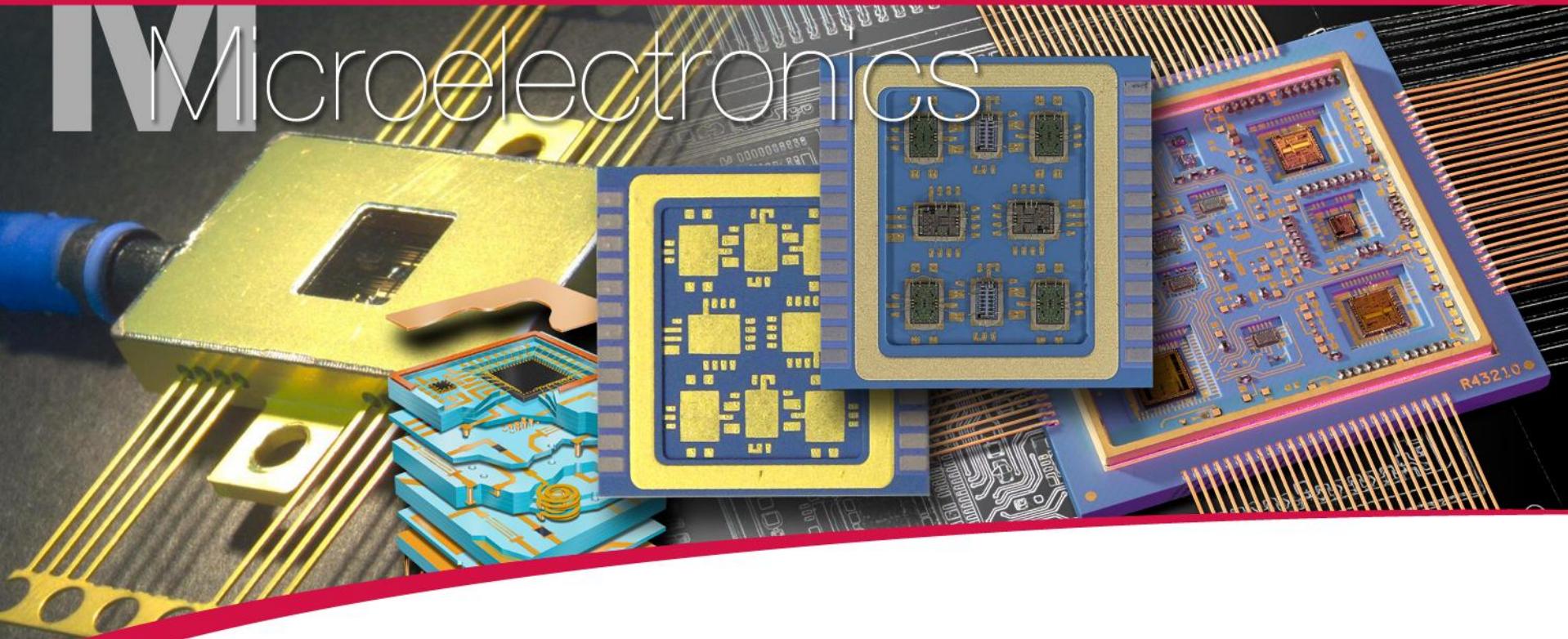




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Microelectronics



Electromagnetic Isolation Solutions in Low Temperature Cofired Ceramic

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Ken Peterson
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10/12/2011

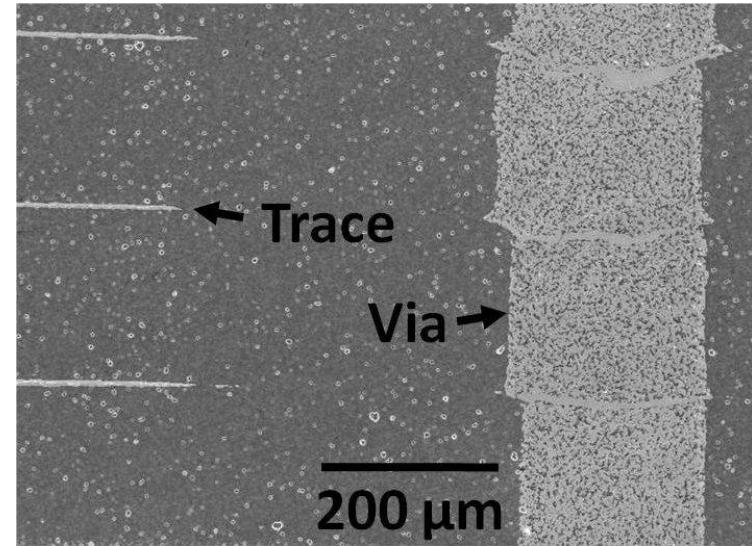
Overview

- Introduction
- Background
 - LTCC
 - EMI Isolation Approaches
- Results and Discussion
 - Processing
 - micromachining, thin film, via filling, soldering of seal frame, lid attach
 - Finite Element Modeling
- Summary



Introduction

- RF MCMs benefit from low dielectric losses and high metal conductivities
- Effects of EMI between individual sections require consideration
 - Metallic seal frame
 - Requires underlying structure in LTCC
 - Via fences and FTTFs
- LTCC consists of many discontinuities inherent to the technology
 - Discontinuities are 'healed' during sintering to allow for success

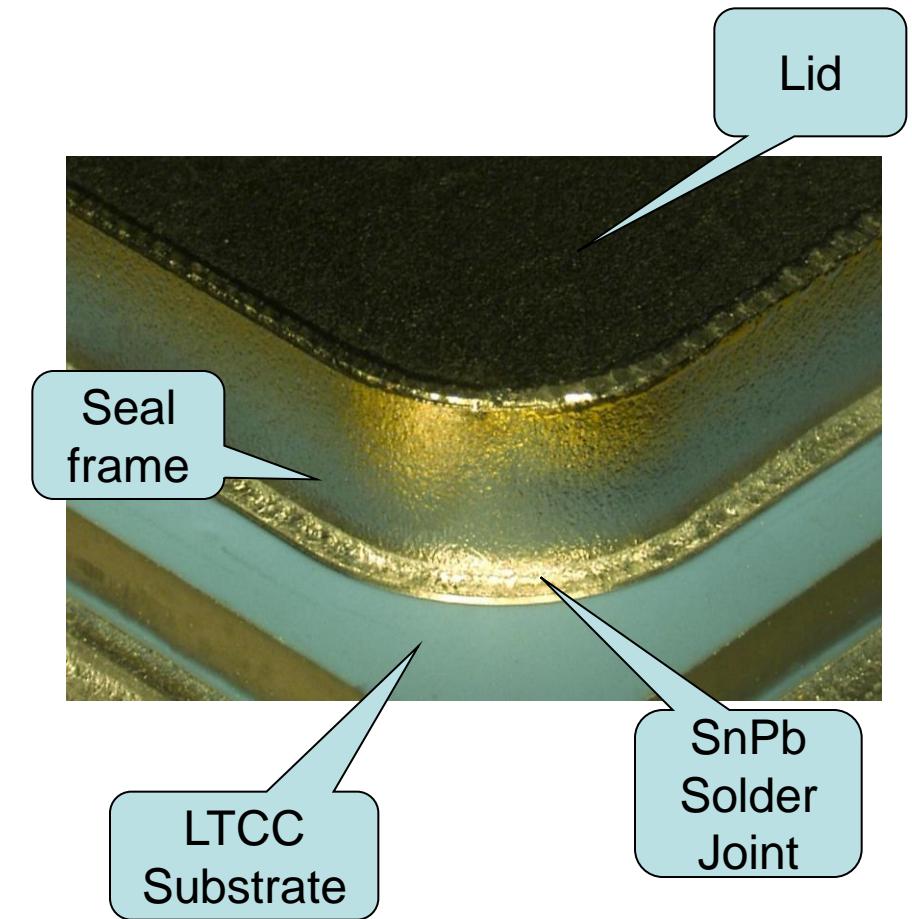


Discontinuities and potential stress concentration points that have healed by sintering.



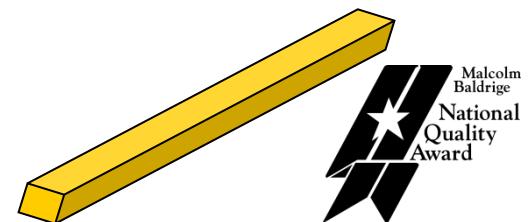
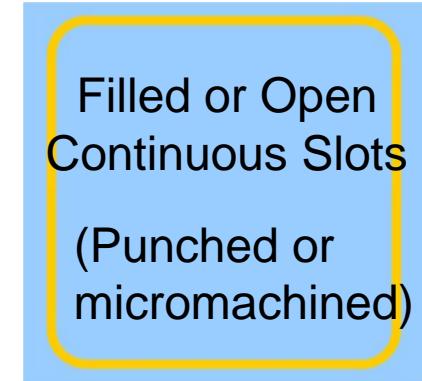
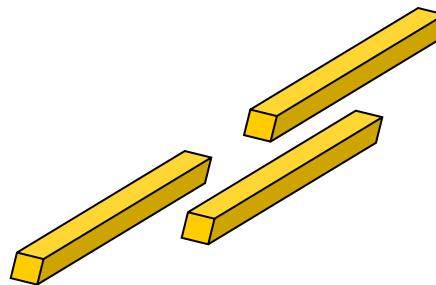
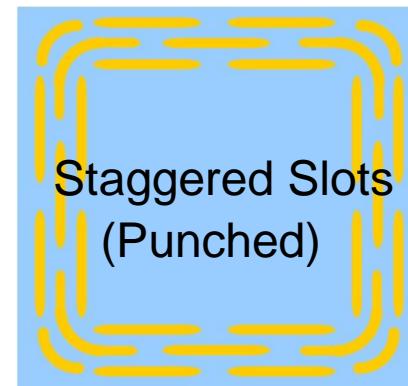
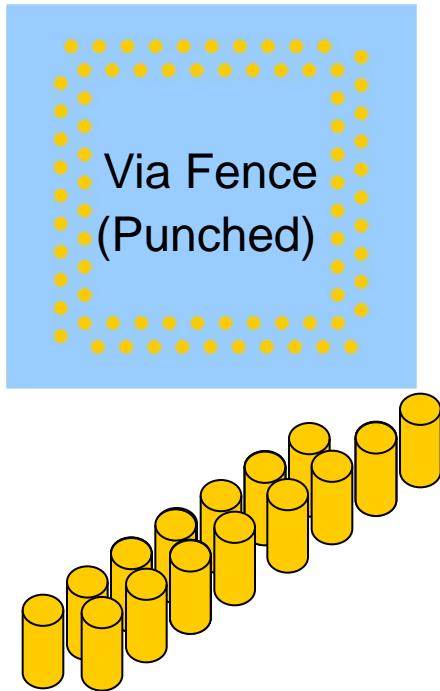
Background

- Conventional LTCC with commercial tapes, pastes, and processing except for EM isolation features
- Multiple approaches to EM isolation feature
 - Via fences
 - Elongated, discontinuous slots
 - Continuous slots (FTTF)
- High isolation achieved with FTTFs, structural challenges led to alternate approaches
- Open recesses that reach ground plane and metallized with thin film
 - Permits seal frame to form EMI isolation





EMI Feature Approaches





Processing

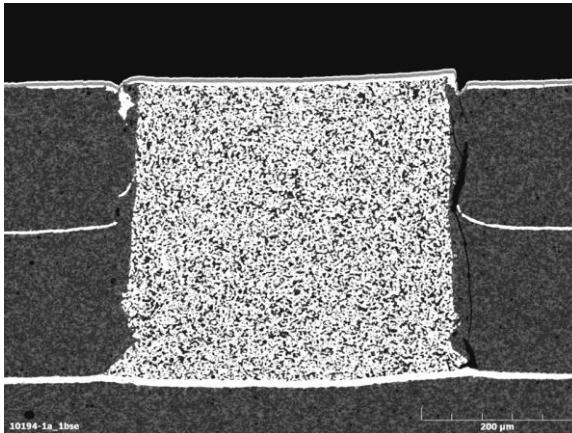
<u>Mechanical Punching Method</u>	<u>Green Machining Method</u>
CONDITION TAPE	CONDITION TAPE
PUNCH VIAS	PUNCH VIAS
PRINT/DRY VIA FILL	PRINT/DRY VIA FILL
PRINT/DRY CONDUCTORS	PRINT/DRY CONDUCTORS
PUNCH SLOT/WEBBING (TOP LAYER)	COLLATE & LAMINATE ALL LAYERS
-	GREEN MACHINE SLOTS
PROGRESSIVELY LAMINATE TOP 2 LAYERS	FILL SLOT/WEBBING LAYER
PUNCH PROGRESSIVELY LAMINATED SLOT LAYERS	-
FILL PROGRESSIVELY LAMINATED SLOT LAYERS	-
COLLATE & LAMINATE REMAINING LAYERS WITH SLOT LAYERS	-
BURNOUT & COFIRE	BURNOUT & COFIRE
PRINT/DRY/FIRE CONDUCTORS/DIELECTRIC/ PASSIVES	PRINT/DRY/FIRE CONDUCTORS/DIELECTRIC/ PASSIVES
SINGULATE	SINGULATE





Background

- Material properties of the system lead to undesirable stresses
 - Manageable when dimensions are small i.e. vias
 - Seal frames are common, however in some geometries the mismatches can be problematic
 - Cracking can be a problem, even when EMI structures are not present as recently published.
- Desire to understand the system interactions when considering placement, size, and material selection of EMI structures

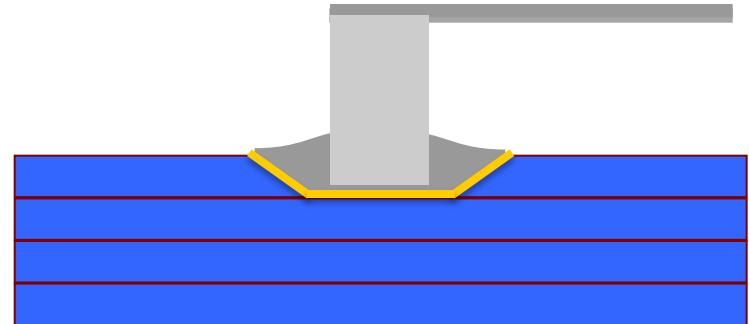


Crack accompanying FTTF structure.



Results and Discussion

- Role of MCM system components
 - Seal frame/lid warping
 - Seal frame geometry
 - Presence of filled slot
 - Location of seal frame
 - Solder composition
 - Fillet geometry
 - Seal frame composition
- Worst case
- Kovar vs. Titanium CTE for seal frame
- SnPb vs AuSn solder

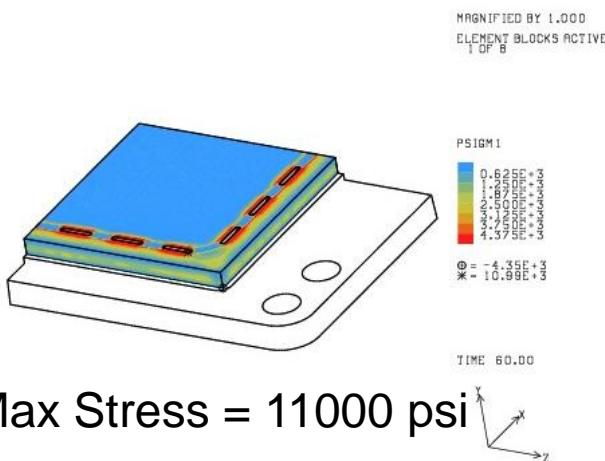
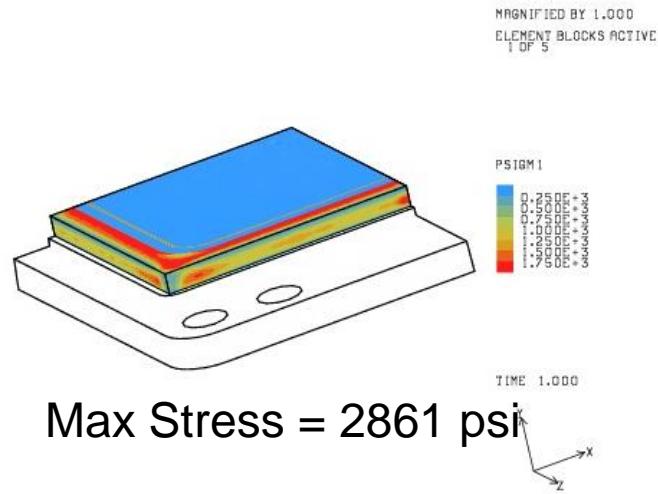
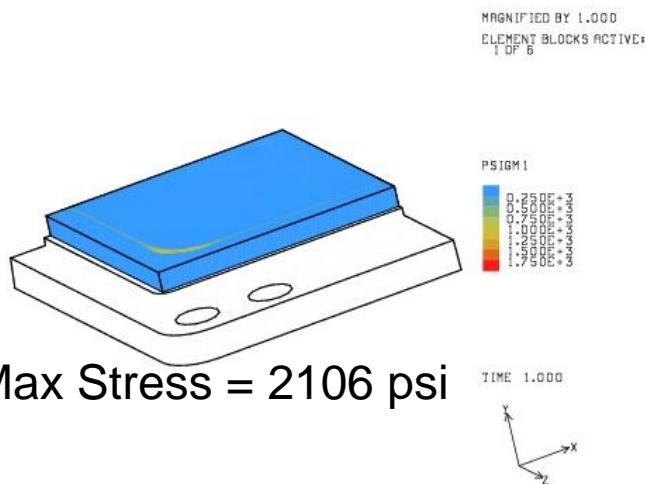


Representative cross section of preferred EMI isolation approach



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Lid Welding Load: LTCC Stress



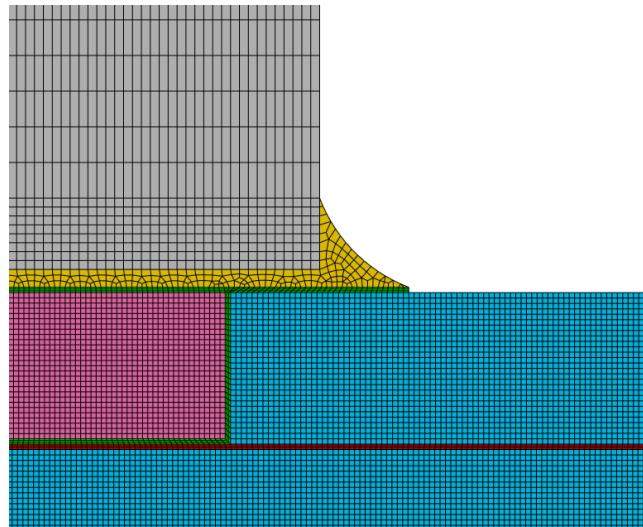
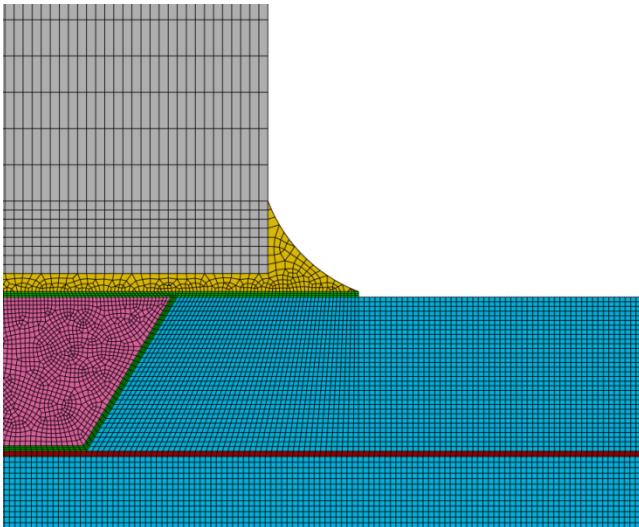
Location of max stress consistent with typical crack initiation point in temperature cycled products.

- Lid welding load without thermal cycle
- Thermal cycle (181 to -55 C)
- Take away:
 - Lid sealing stress not alarming, slot induced stress indicate need to evaluate further





Finite Element Model



- Plain strain
- Single temp cycle: 125C to -40C (high to low)
- Temperature dependent plasticity model for solder
- Parameters:
 - slot geometry
 - slot material

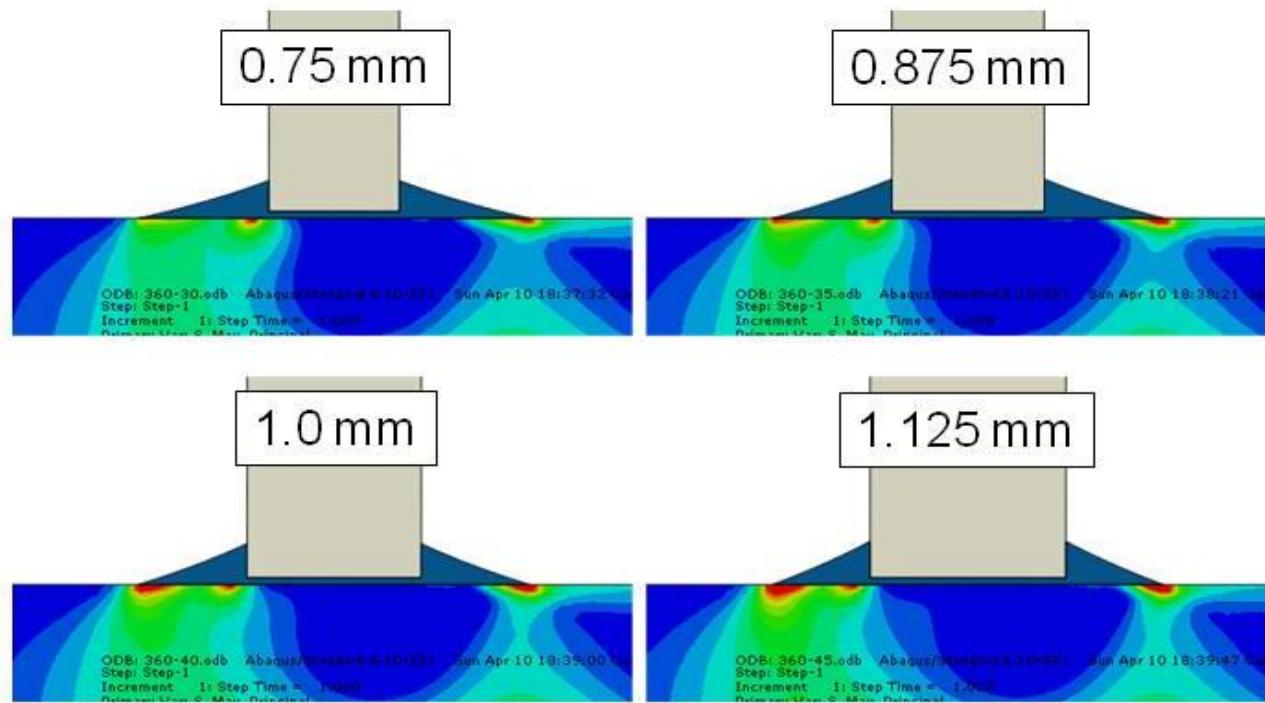
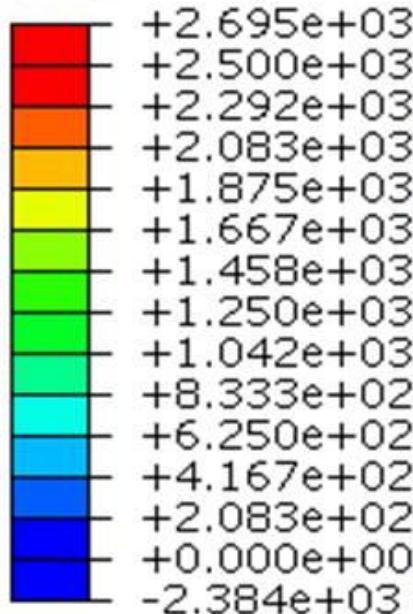
Because there is significant uncertainty of the gold fill material properties (for the slots), the problem was bounded by considering 2 scenarios: a pure gold filled slot and a slot filled with LTCC material.



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Seal Frame Width Study: LTCC Stress

S, Max. Principal
(Avg: 75%)



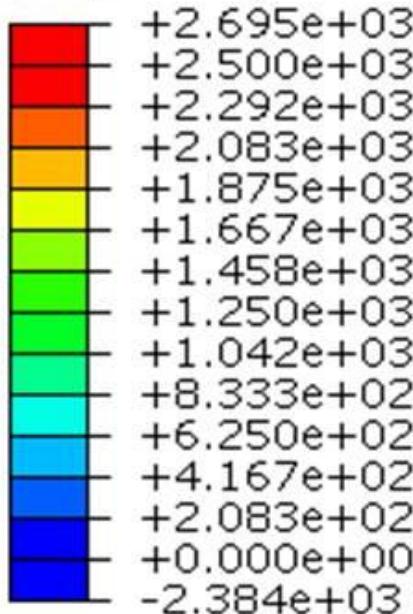
Sn-Pb Solder, Kovar Seal Frame 181C to -55C





Seal Frame Width Study: LTCC Stress

S, Max. Principal
(Avg: 75%)



0.75 mm

21,600psi

0.875 mm

24,230psi

1.0 mm

27,510psi

1.125 mm

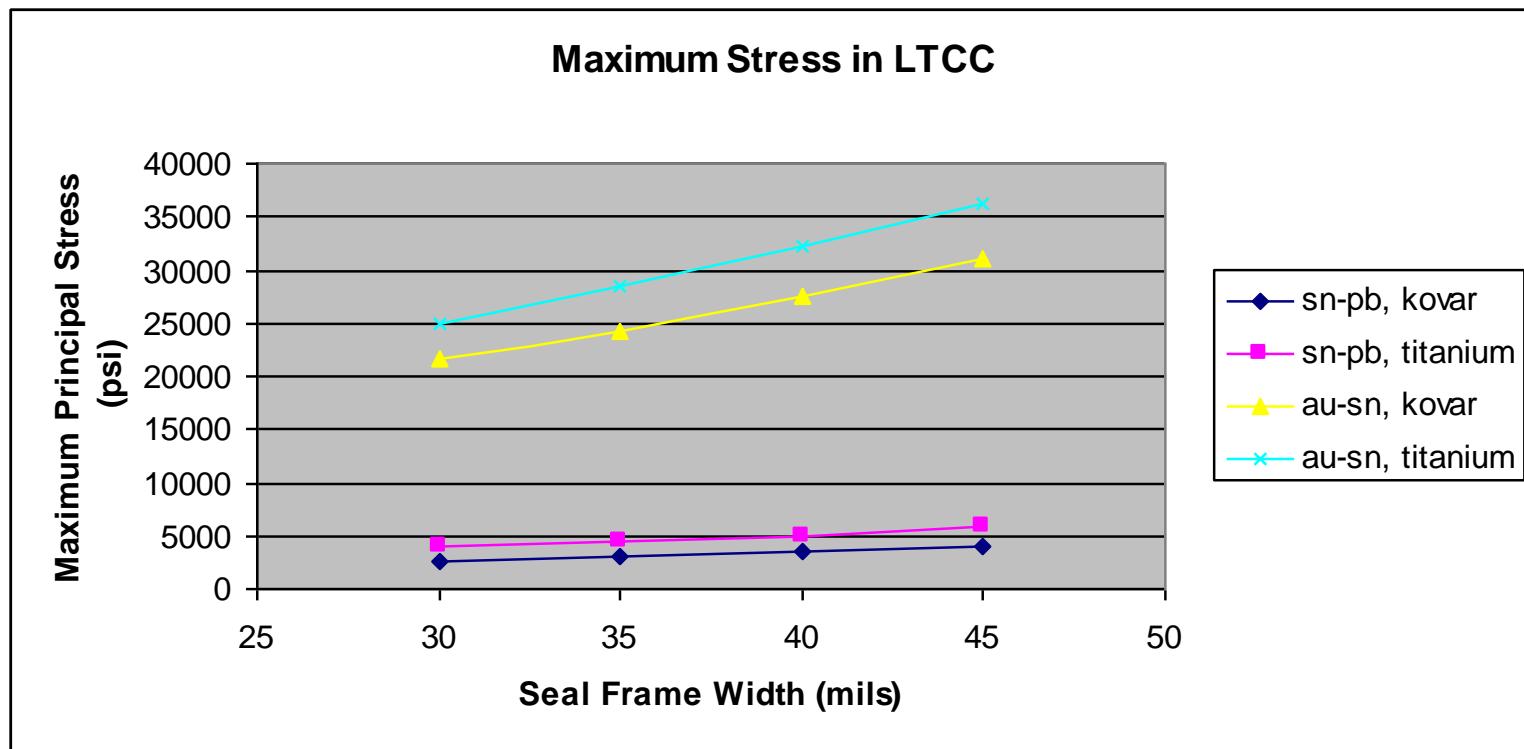
30,960psi

Au-Sn Solder, Kovar Seal Frame 281C to -55C





Seal Frame Width Study

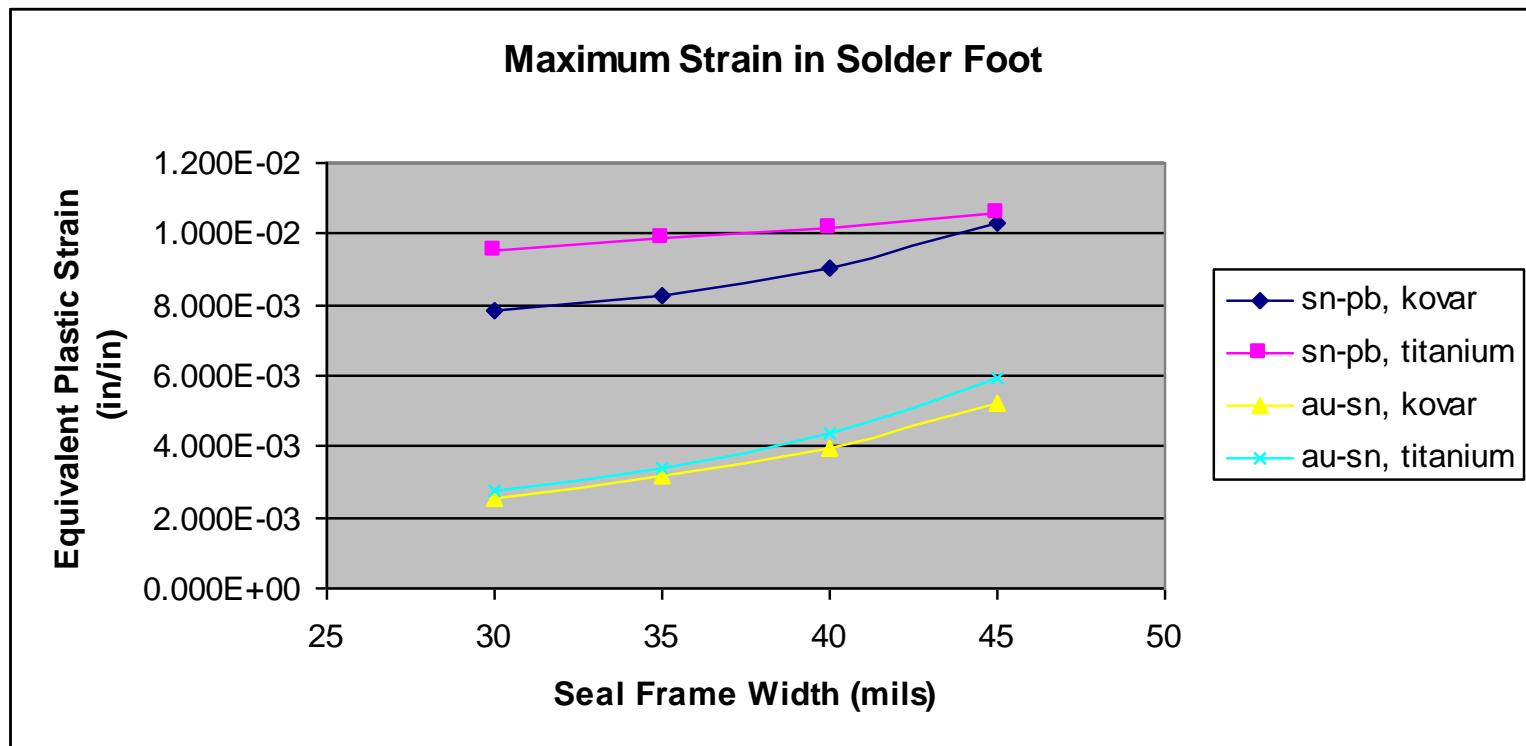


- Au-Sn solder increases LTCC stress significantly.
- For same solder volume, LTCC stress increases with increase in seal frame width.





Seal Frame Width Study



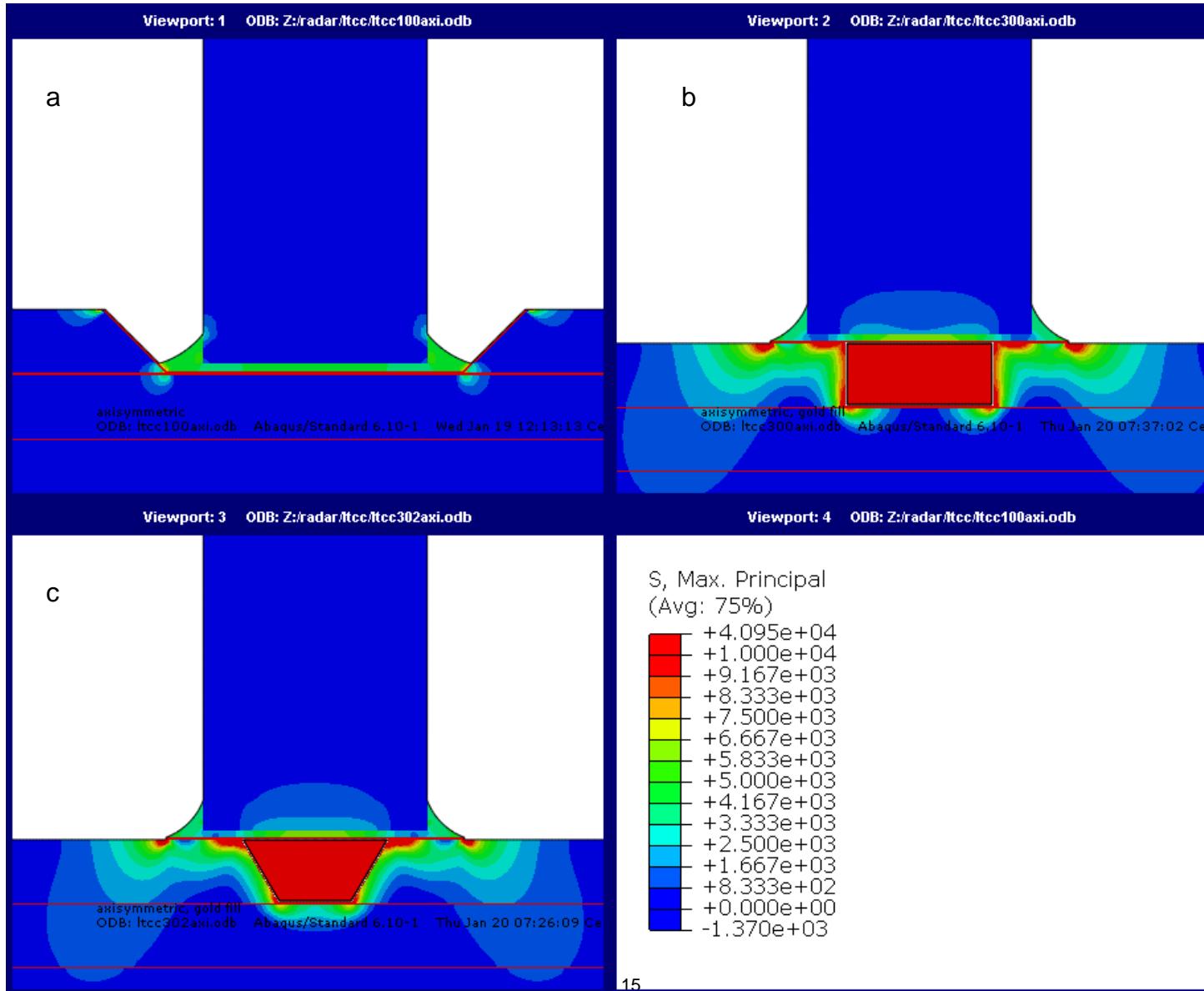
- Au-Sn solder decreases plastic strain in solder significantly.
- For same solder volume, plastic strain in solder increases with increase in seal frame width.





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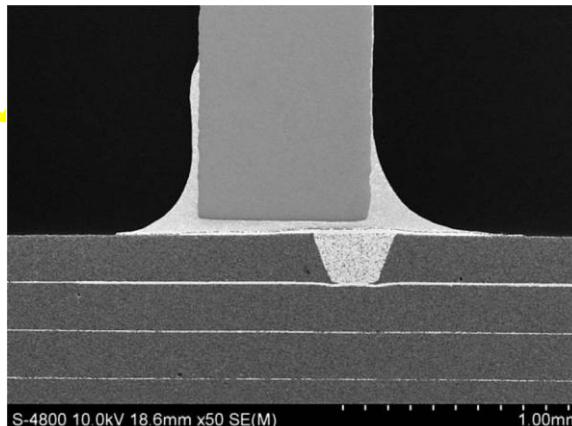
KCP Finite Element Analysis Slot Configurations



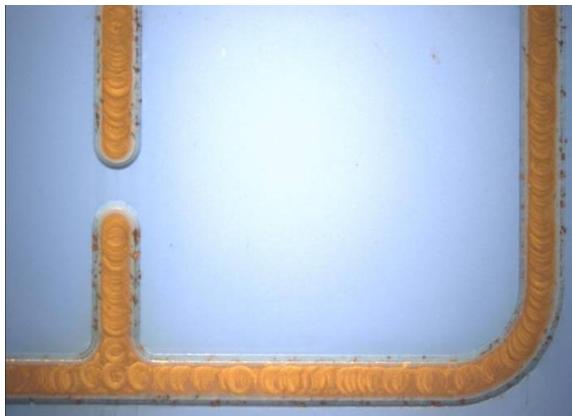


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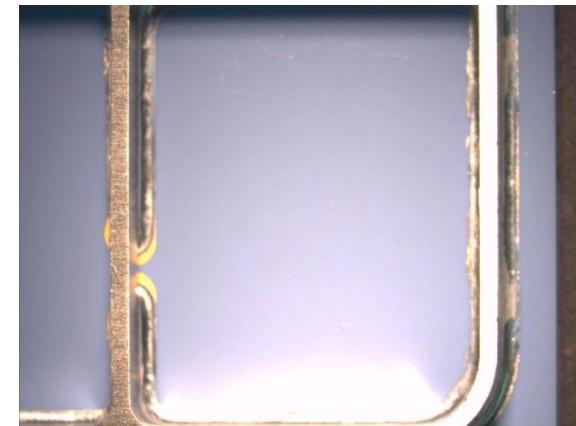
Cross Section Results



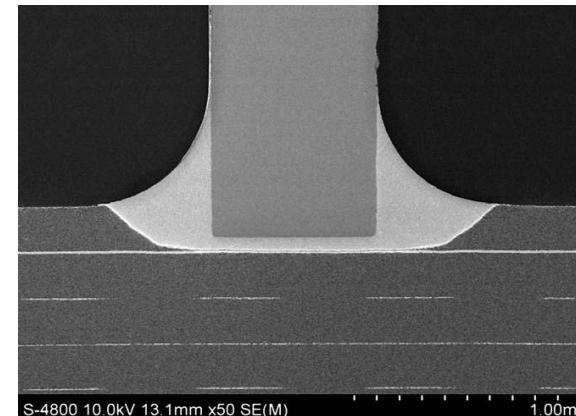
Cross sectional view of a seal frame soldered to a thin film covering a FTTF solid wall structure used in a prototype.



Milled slot, unfired, for TFN



Seal Frame soldered into slot after TFN deposition



SEM Micrograph of cross sectioned green machined, open recess with seal frame soldered into recess.



Conclusions

- Modeling showed the existence of the slot feature under the seal frame does increase the stress to a point that it needs to be addressed for reliability.
- Removing the slot material from the slot reduces the stress state in the substrate (LTCC)
- Shape of the slot is not major player (for the shapes analyzed here), volume of slot fill has impact
- Solder (geometry) is 2nd largest contributor to final stress
 - Steep solder fillet angles impart higher stress on LTCC at toe than lower angles
- Cross sections confirm
- Removal of slot would not necessarily resolve cracking due to solder/seal frame
- Au/Sn solder models much higher stress in the LTCC
 - Monti 2010 shows cracking with Au/Sn

Future Work and Acknowledgements

- Modulus and ductility of via fill material
- Vary solder volume in optimal solution
- Vary wall angle in optimal solution
- Depth of trench
- Dave Stockdale, Mike Girardi, Jim Mahoney, Brent Duncan
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