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SOI substrate removal for SEE characterization and recent results

M. R. Shaneyfelt, J. R. Schwank, P. E. Dodd, J. Stevens,

S. E. Swanson, and S. M. Dalton

Sandia National Laboratories

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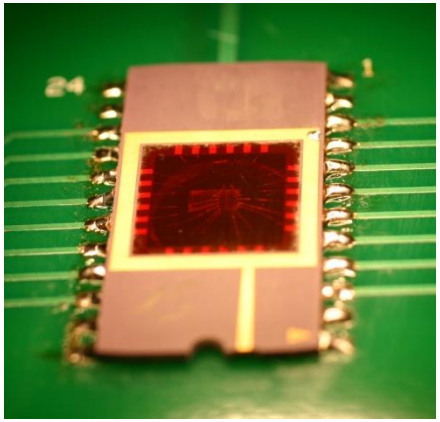
SEE characterization from the frontside can be problematic in some cases

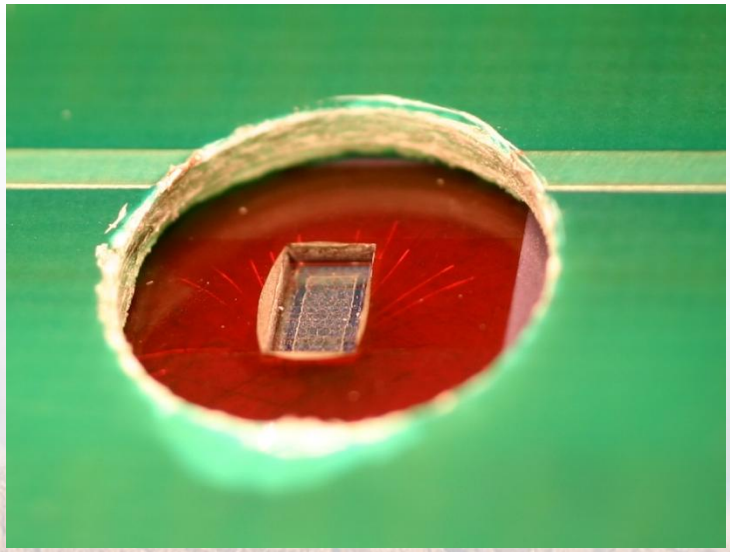
- For single-photon absorption (SPA) laser measurements, the density and opacity of the metal overlayers can be an issue
- The thick overlayers of today's IC technologies attenuate the low-energy ions incident on an IC
  - A problem for microbeam measurements
  - Even a problem for some low-energy broad beam facilities
- For flip chip die, access to the frontside of the die for SEE characterization may not be possible
- These problems can be overcome by characterizing ICs from the backside with the substrate removed
- *In this work we will explore techniques to remove the back substrate of SOI devices with and without traditional packaging*

Techniques to use for packaged devices

Sample preparation for packaged part

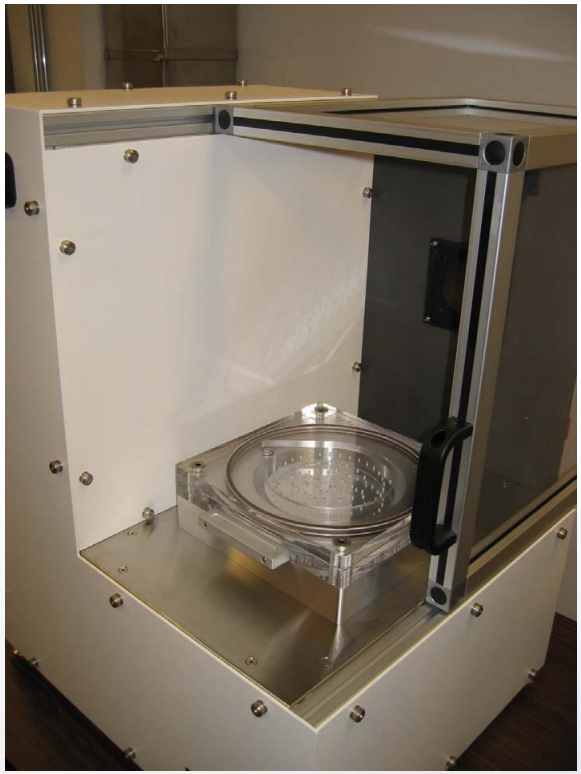
- Die mounted in 40-pin DIP packages with active circuitry facing up
  - Package cavity filled with non-conducting epoxy
- Backside of package ground and polished to expose back substrate
- Back substrates on some devices removed down to BOX using xenon difluoride (XeF_2)
  - N. Kanyogoro, et al., IEEE Trans. Nucl. Sci., 57, pp. 3414–3418, Dec. 2010.
  - J. R. Schwank, et al., IEEE Trans. Nucl. Sci., 58, pp. 820-826, June 2011.





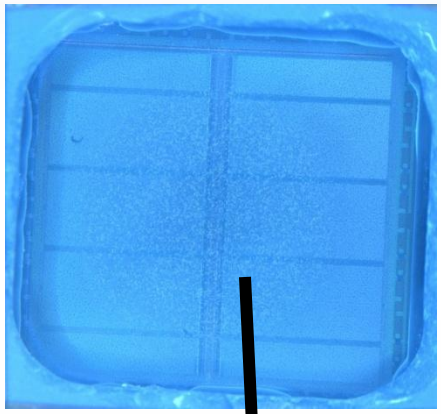
Substrate etch

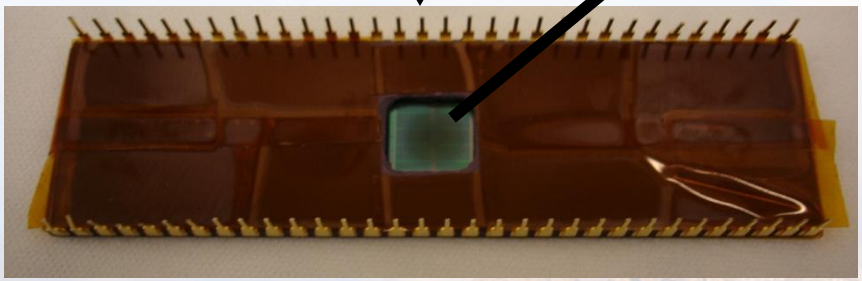
- IPA (isopropyl alcohol) clean
- RIE (reactive ion etch)
  - 60 second O_2 clean
  - 60 second oxide etch
- XeF_2 (xenon difluoride) etch

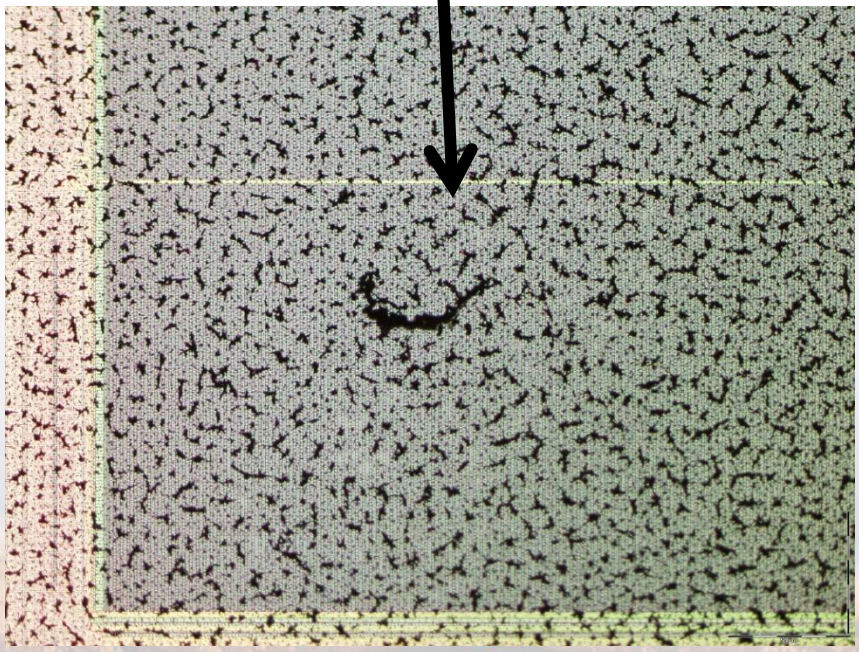


e1 Series™ *Xetch®*
Xenon Difluoride Etching Systems

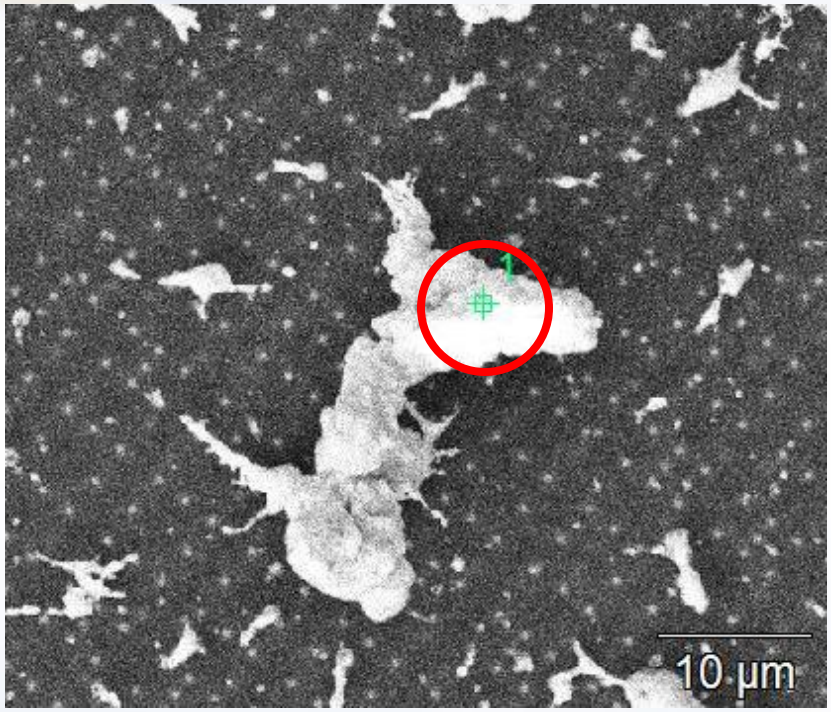
Chamber & die contamination found after test run

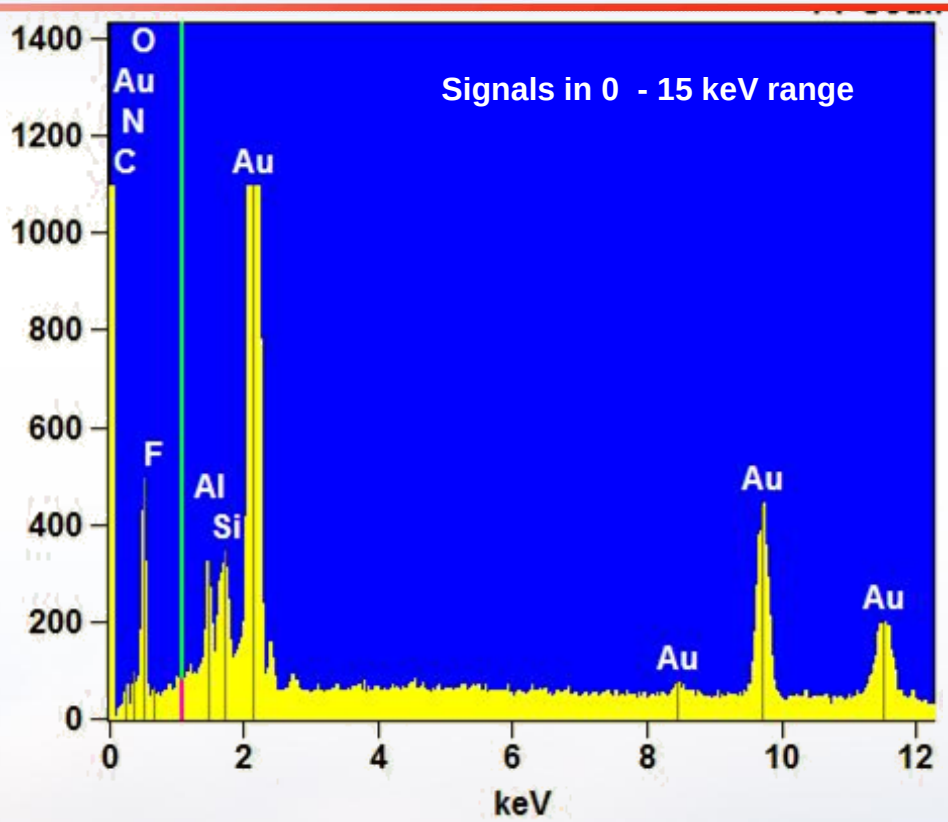






Energy-dispersive x-ray spectroscopy (EDS) analysis



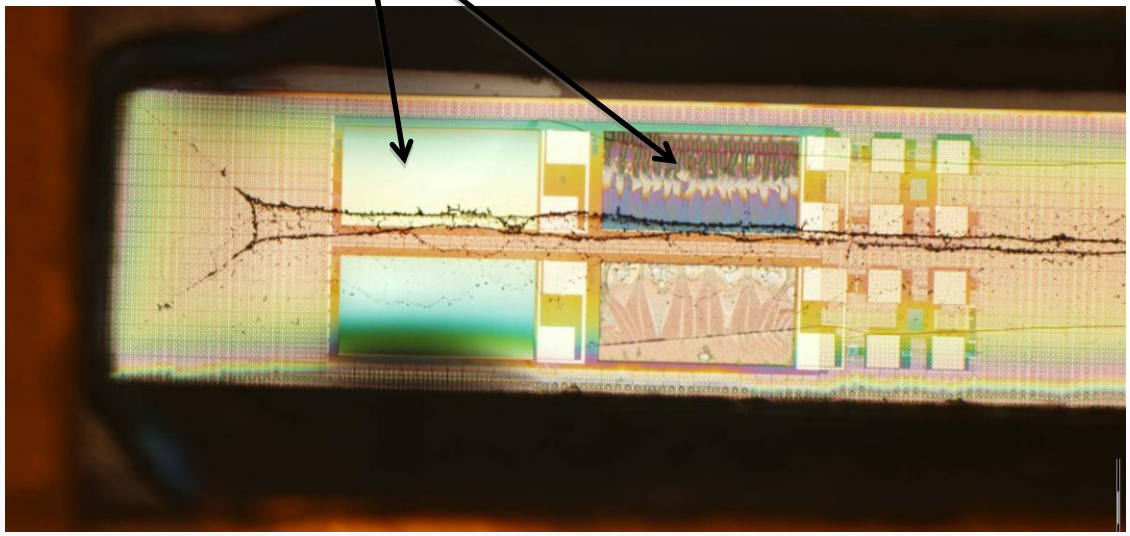


Analysis of “contaminated area” shows higher signals of gold and a trace signal of F

Must cover all gold areas with kapton tape to reduce or eliminate contamination

Diodes after grinding, polishing, and etching

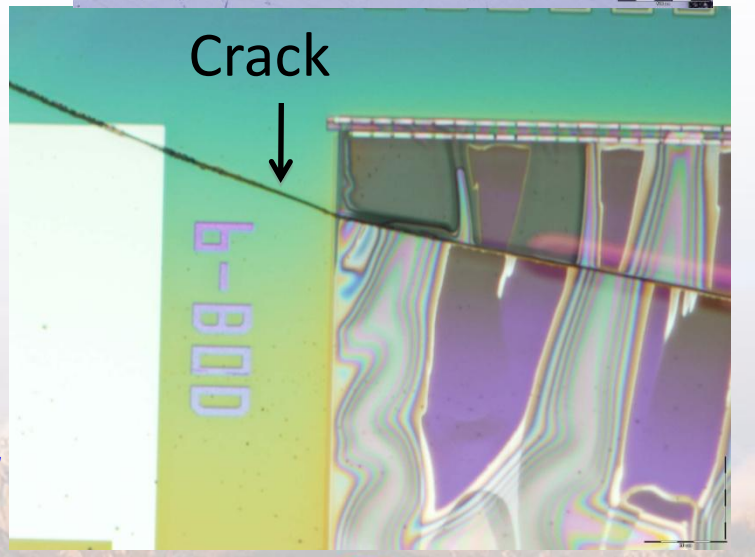
Diodes



From backside (silicon removed)

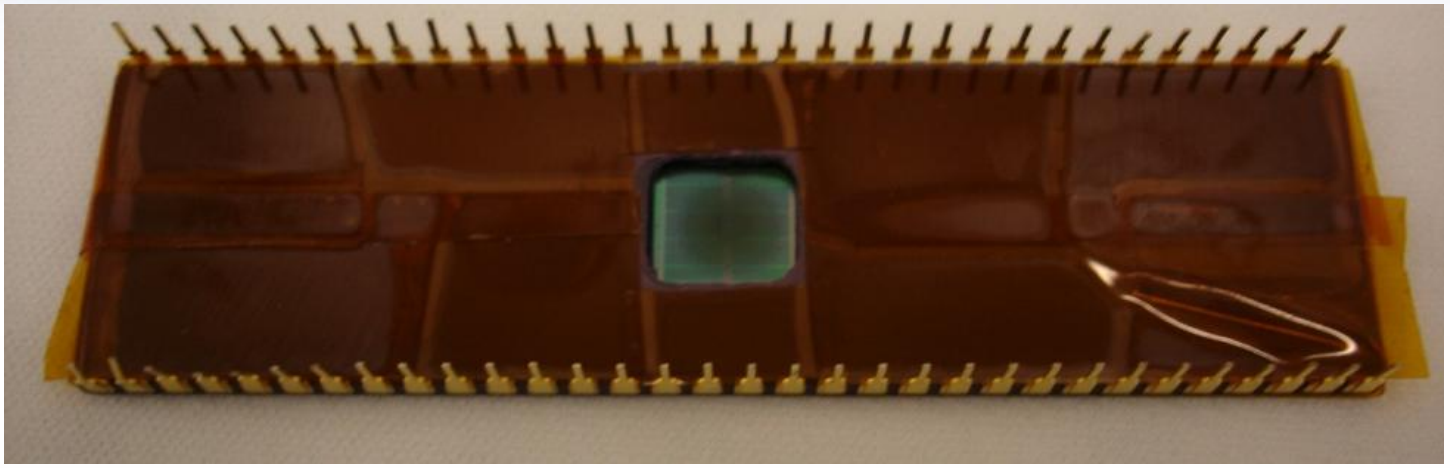
Believe grinding/polishing process induces microcracks in substrate causing over etching along crack (removing active silicon islands)

After grinding and polishing



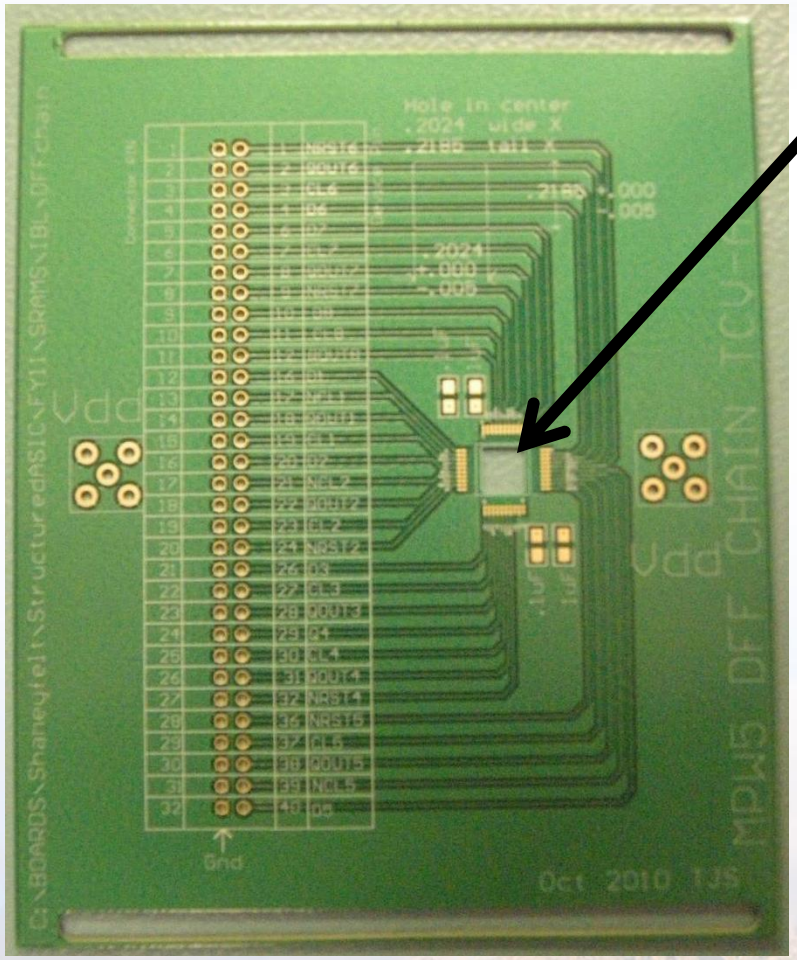
Techniques to use when die are available

One technique to use when die are available



- Laser mill out the package well (there needs to be enough of the package well remaining to attach die)
- Attach die and fill die cavity with non-conductive epoxy
- Kapton tape used to mask as much of the package (including gold) as possible
- Remove backside substrate with XeF_2 etch

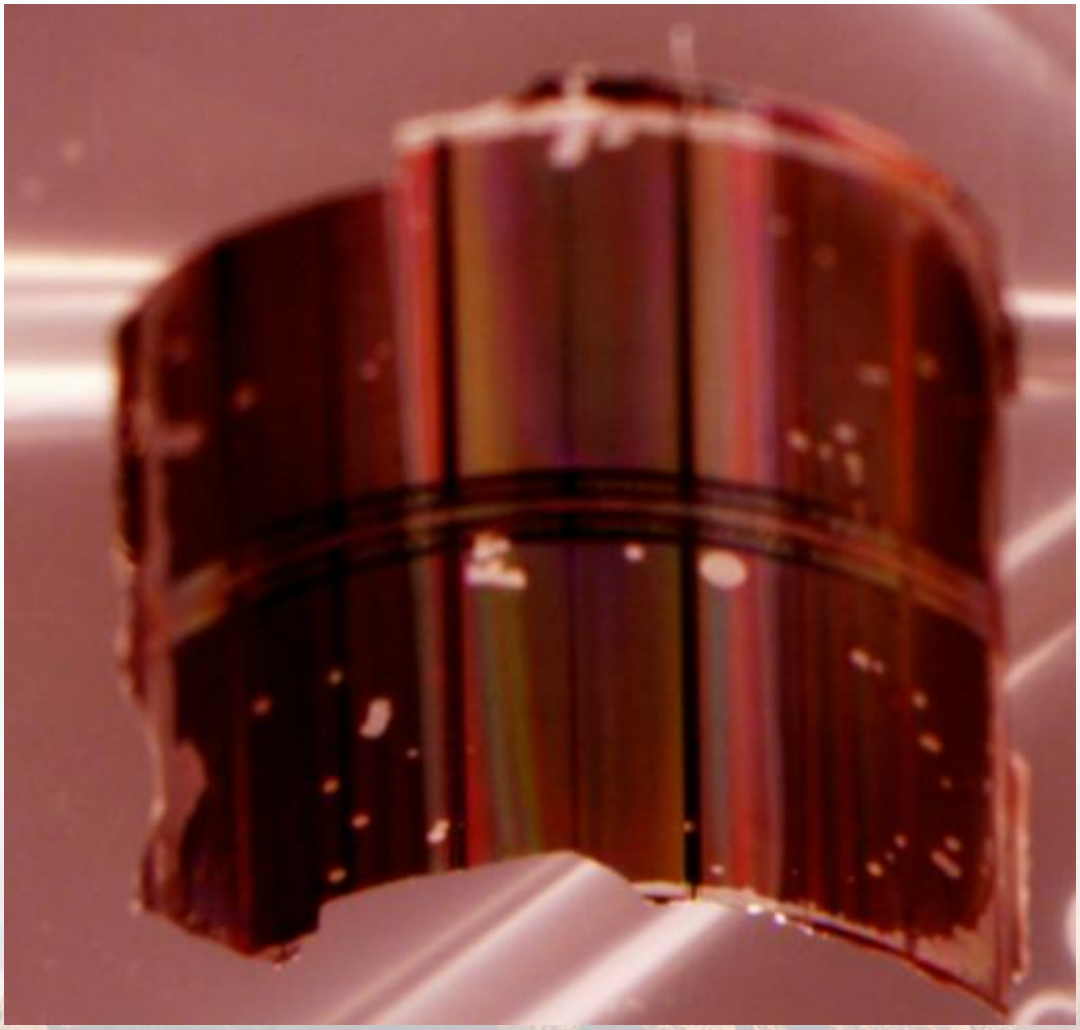
Another technique to use when die are available



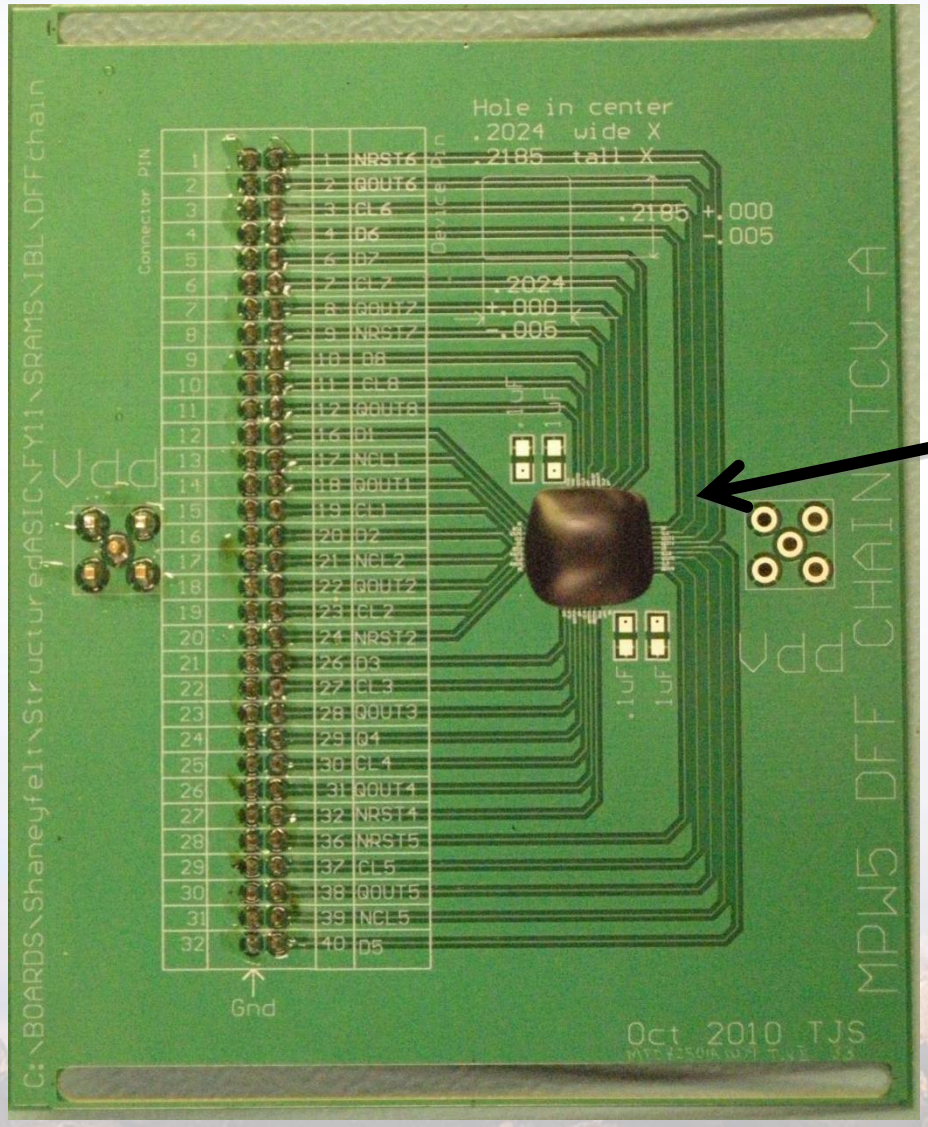
3” x 4.5” board

- PC board designed with a pre-cut hole that exposes the backside of the die
- Board designed to be compatible with laser testing, heavy ion testing, and microbeam testing (it must also fit in etch chamber)
- Attach die directly to PC board and attach bond wires
- Encapsulate front side of die with epoxy or plastic material
- Substrates removed down to BOX using XeF_2

Cannot etch die before mounting and encapsulation

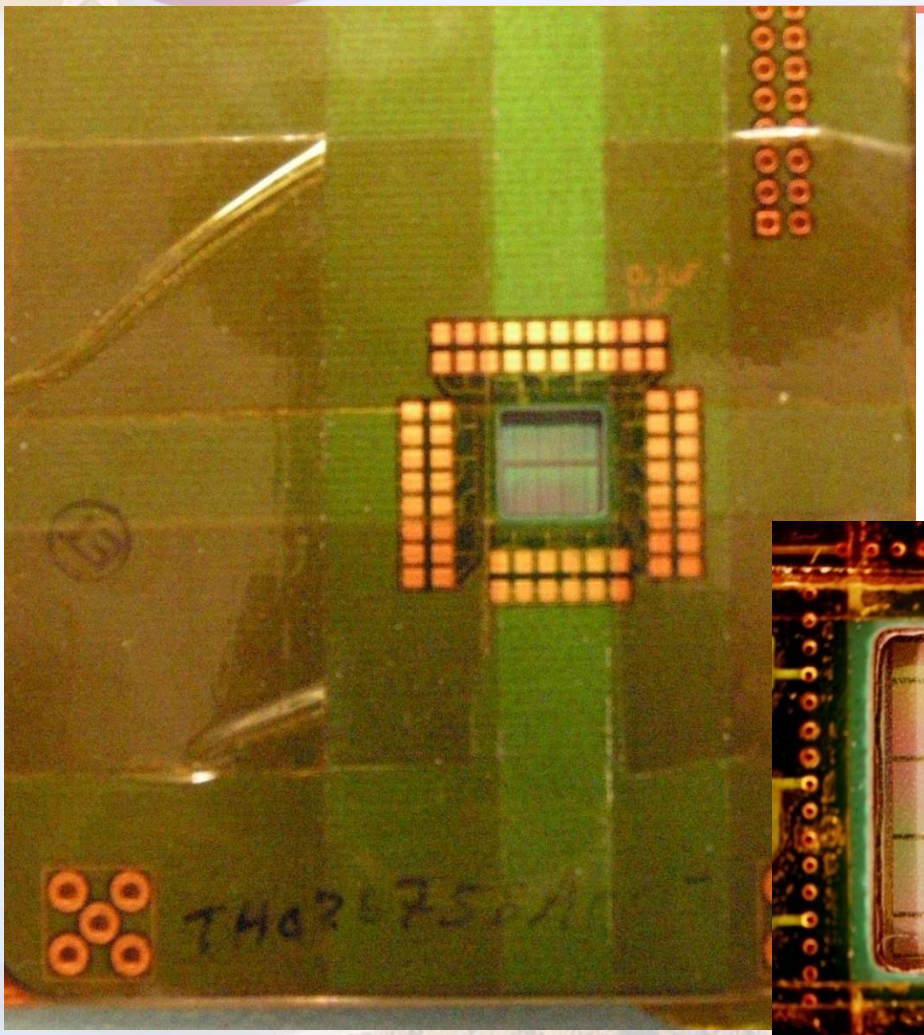


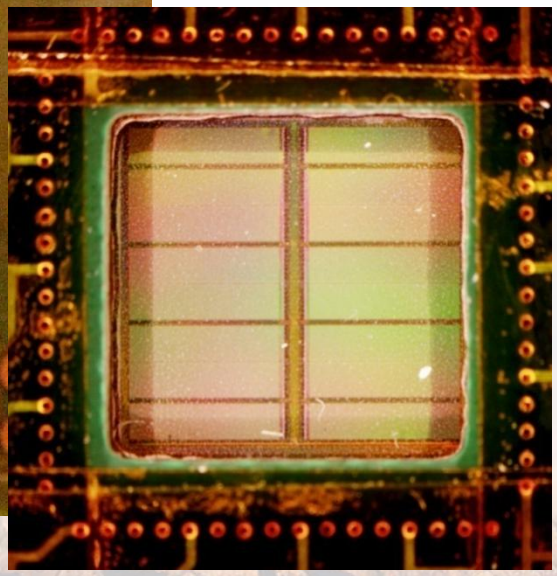
Encapsulate frontside of die with epoxy or plastic material



Die encapsulated with plastic material

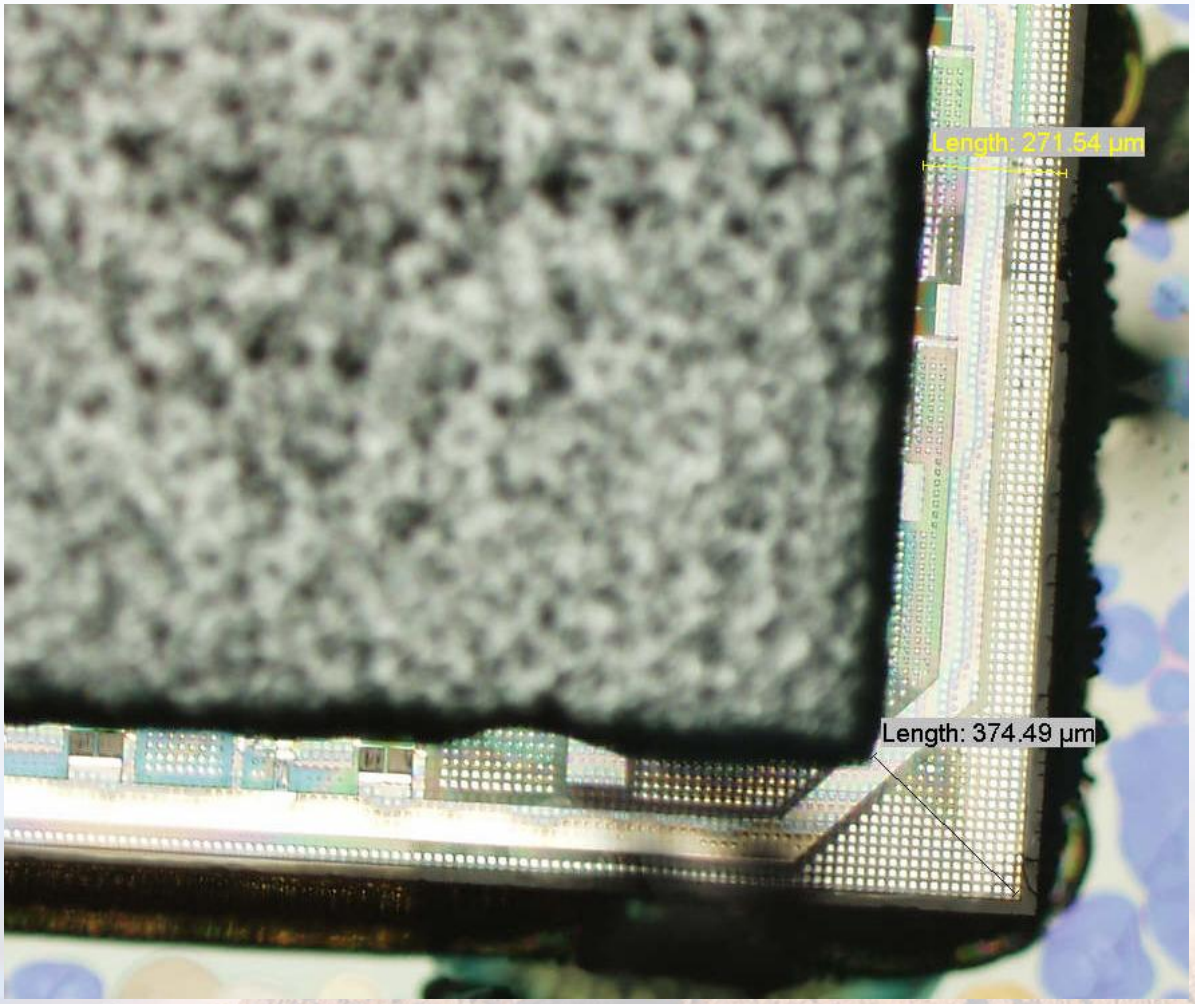
Cover front & backside of PC board with kapton tape to protect gold traces





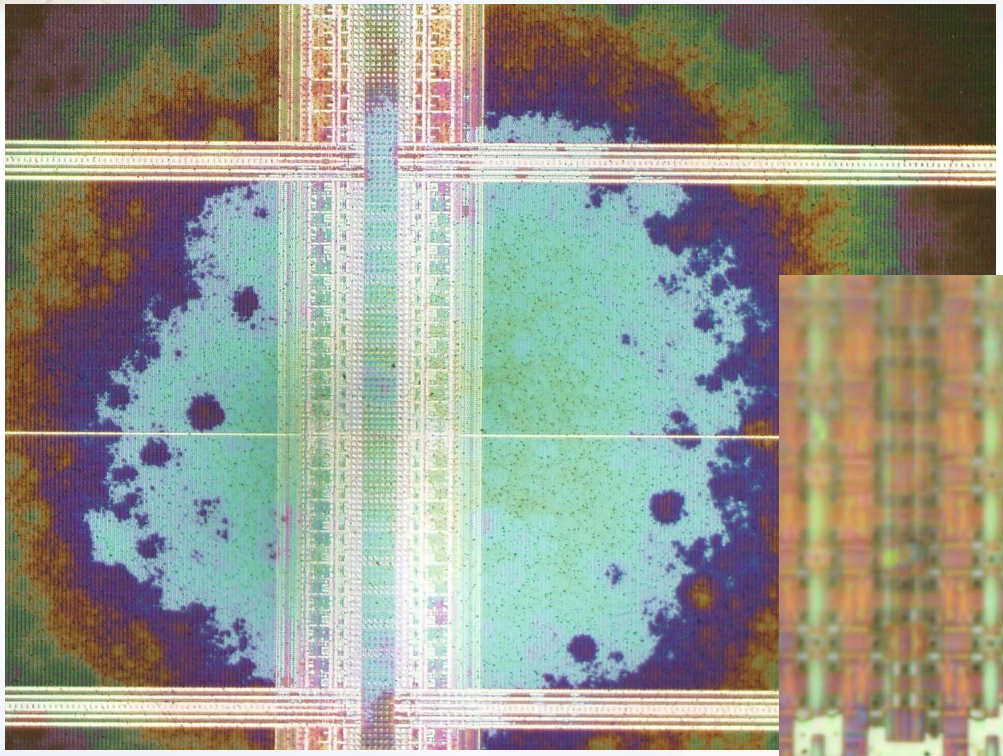
This is a critical step that also prevents gold from contaminating etch chamber

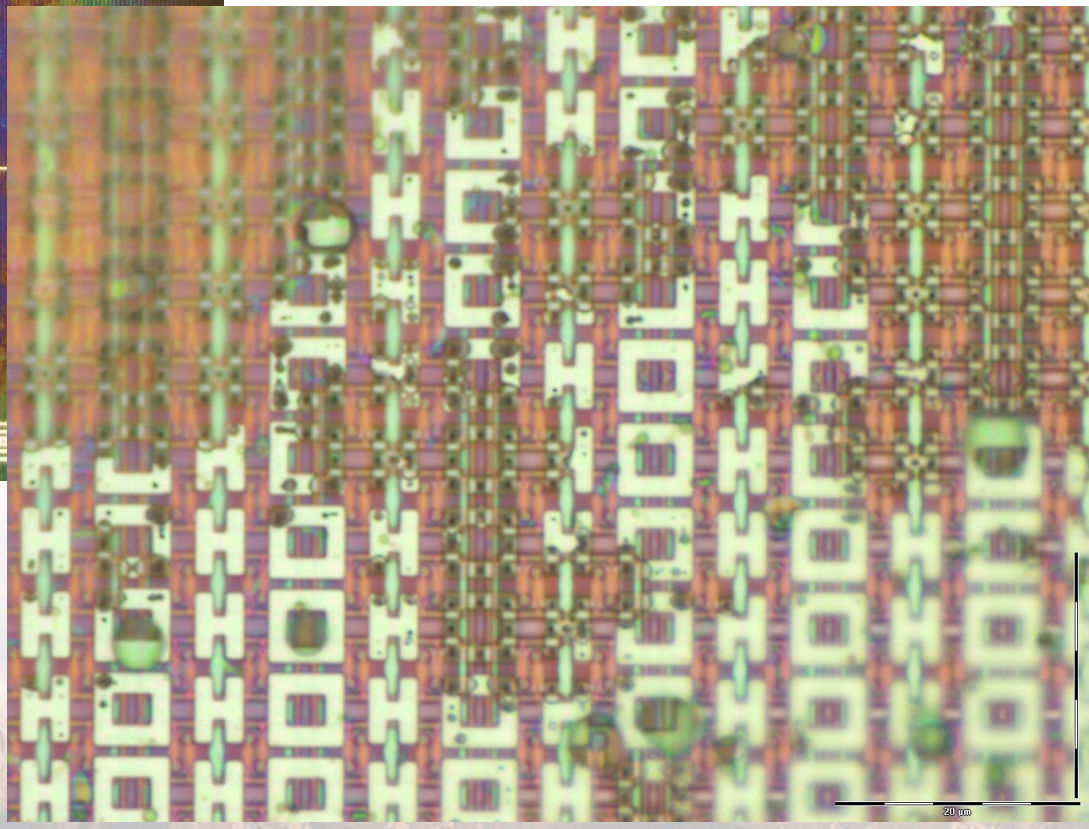
Si substrate generally etches from the outside of the die to the center



Care must be taken to develop an XeF_2 etch process with a high Si to SiO_2 selectivity to ensure the etch does not go through the oxide at the edges of the die before all the Si substrate on the die is removed

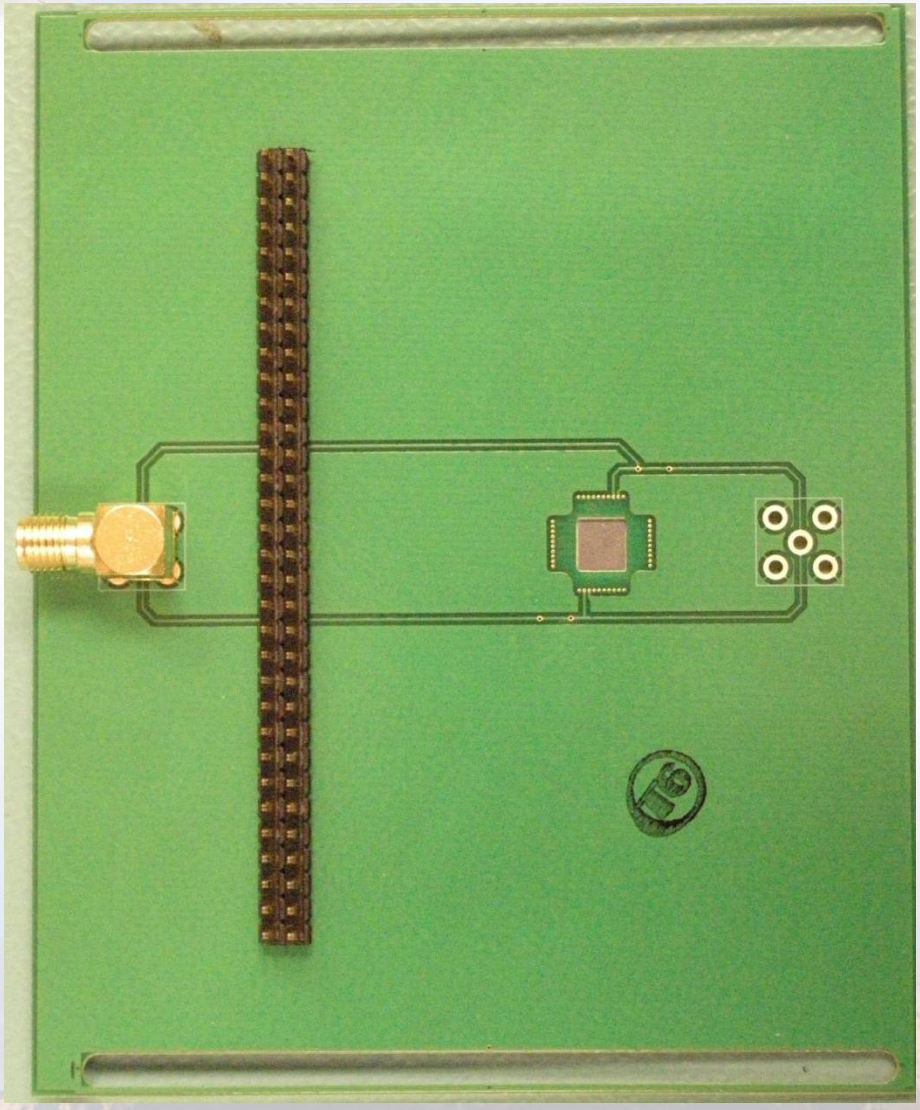
Care must be taken to prevent over etching samples





Etched through BOX and etched active SI regions

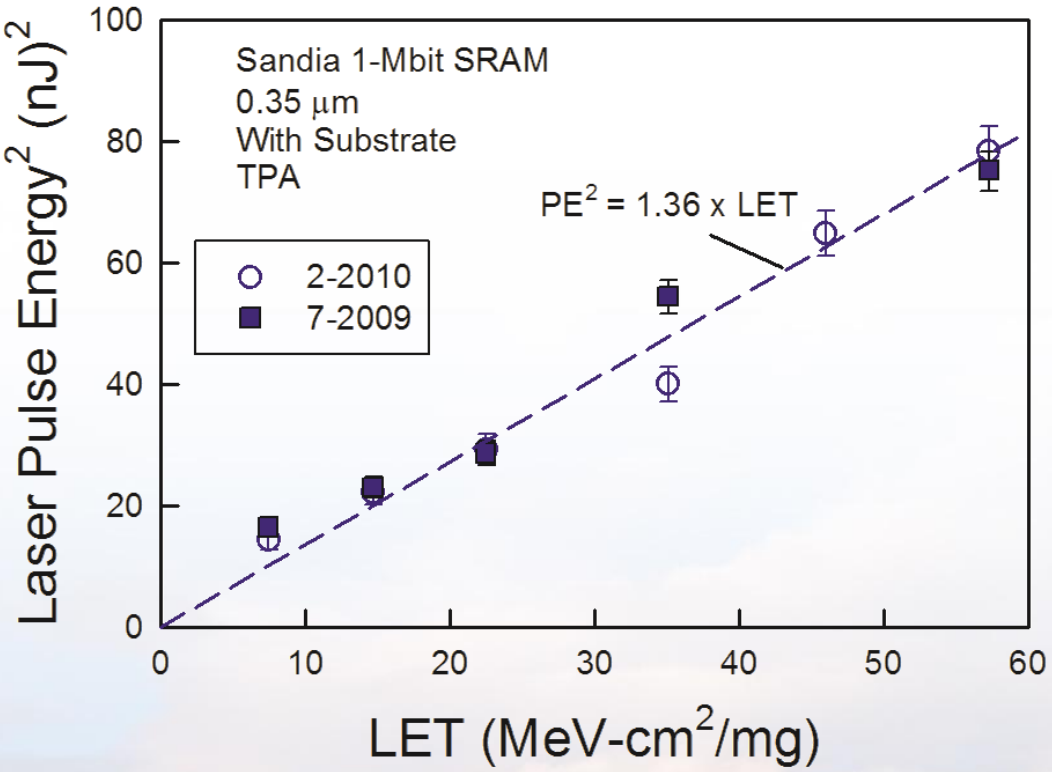
Once etch is completed, add connectors to board and you should be ready to test



Ready for backside laser, heavy ion, and microbeam testing!

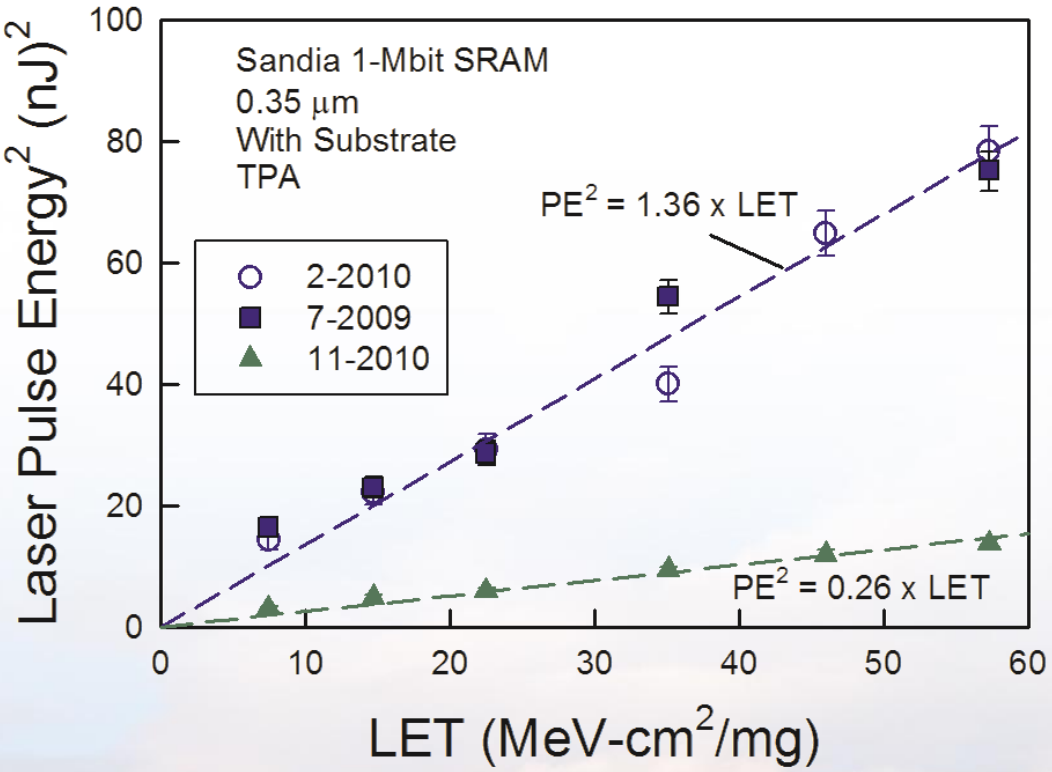
Recent results

Calibration of TPA system to heavy-ion SEU threshold LET for Sandia 1-Mbit SRAMs



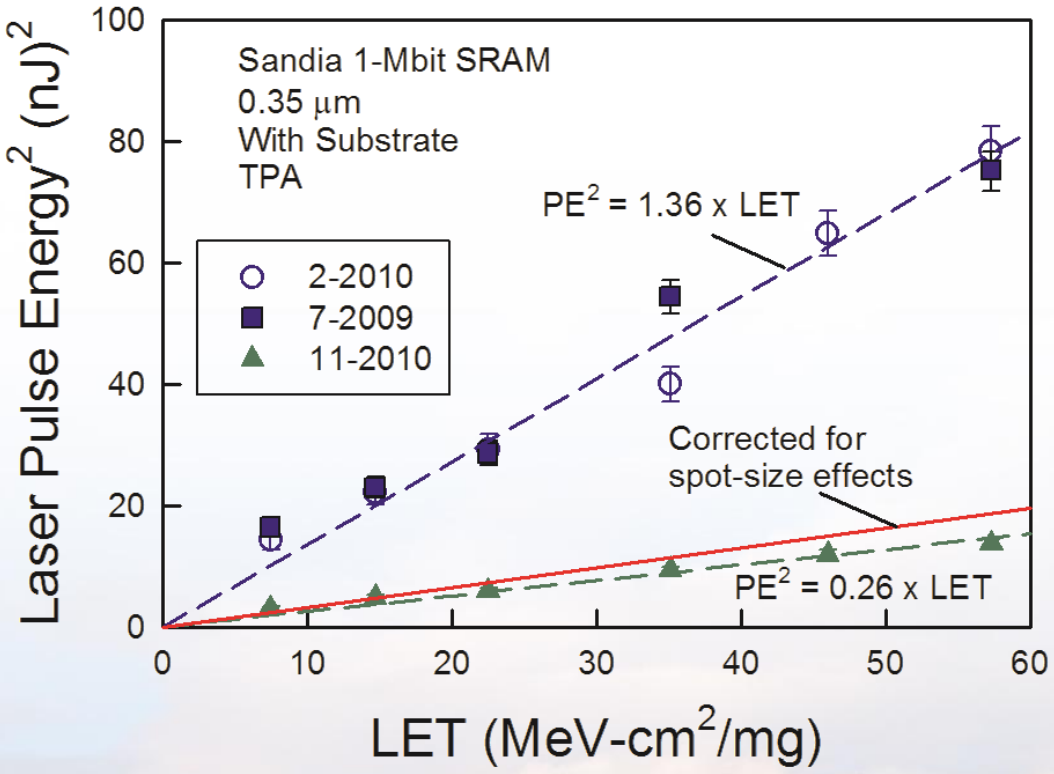
After calibrating laser energy, approximately the same correlation observed between laser pulse energy threshold and heavy-ion SEU threshold LET for the first two test campaigns

Calibration of TPA laser system has changed



- Major repairs and realignment of the laser system took place between the second and third test campaigns
- Laser pulse energy also calibrated for the third test campaign
- Differences may be due to nonlinear effects caused by changes in focused laser spot size
- Laser spot size found to have decreased from 1.7 to 1.35 µm during this time period

Calibration of TPA laser system has changed

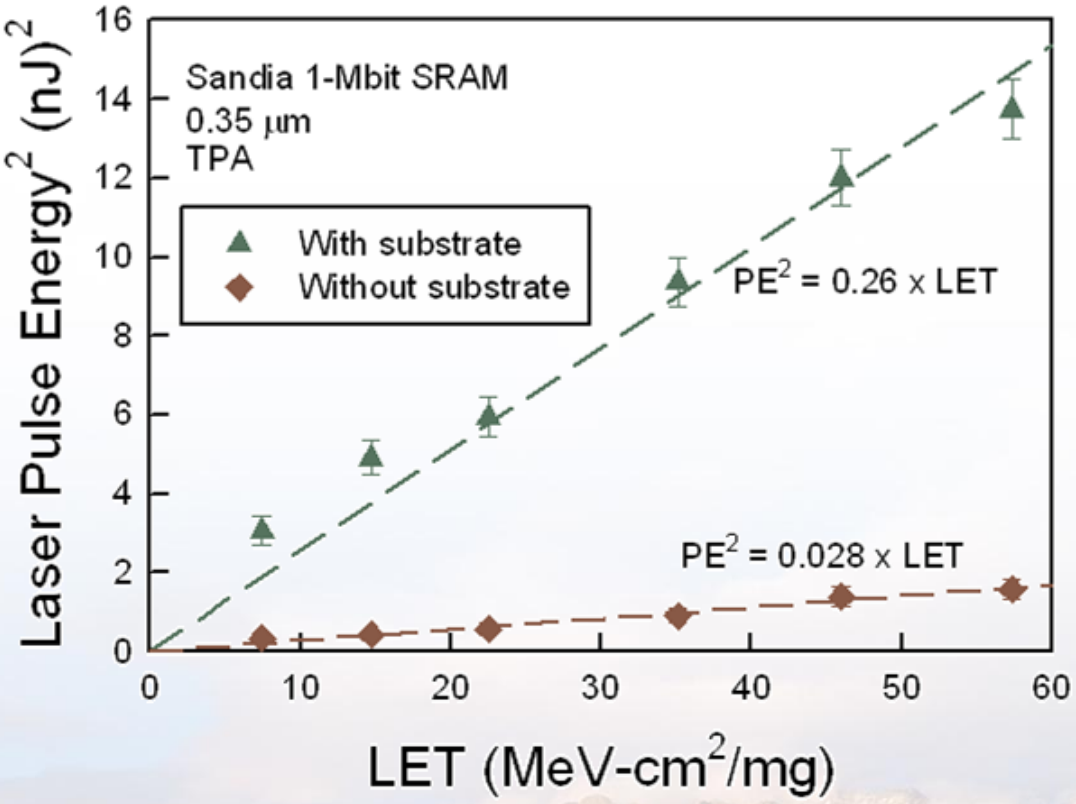


Change in spot size accounts for roughly 95% of the discrepancy between the data sets

- Variations in irradiance
- Geometric effects

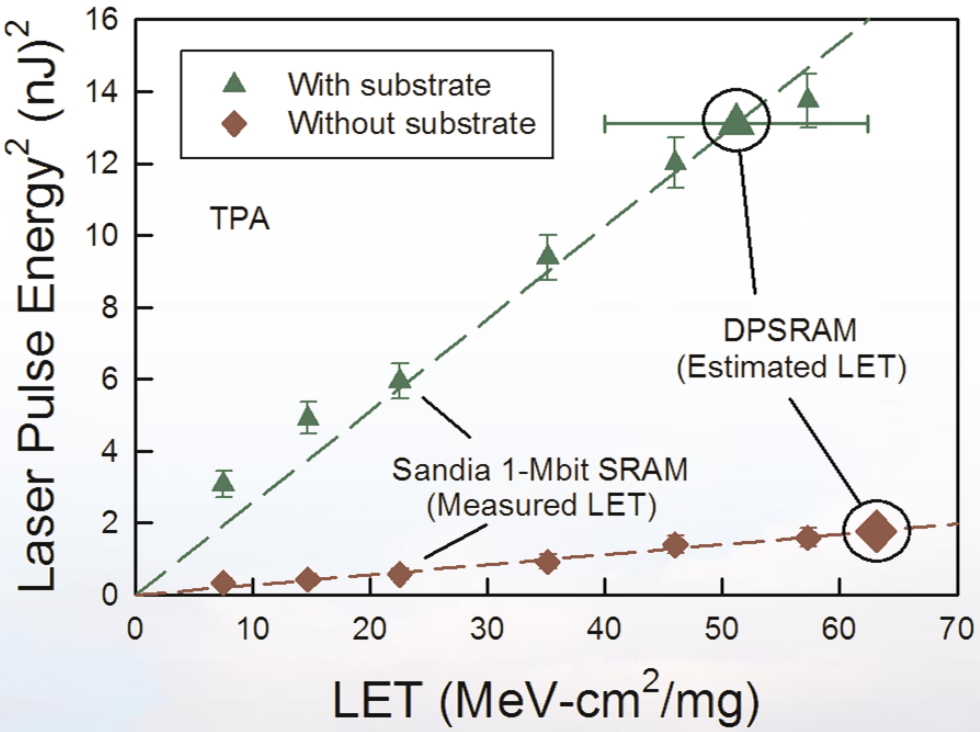
For TPA to be used as a routine quantitative tool, it is imperative that the laser pulse characteristics be monitored and assessed for possible changes

Removing the substrate reduces pulse energy SEU threshold by 10 times



- Differences in reflections cannot account for these large differences
- Charge generation in substrate by TPA may induce displacement currents
- Nonlinear processes also can contribute to a reduction in the pulse irradiance in the active region
  - "Pump depletion"
  - Nonlinear refraction and free-carrier absorption

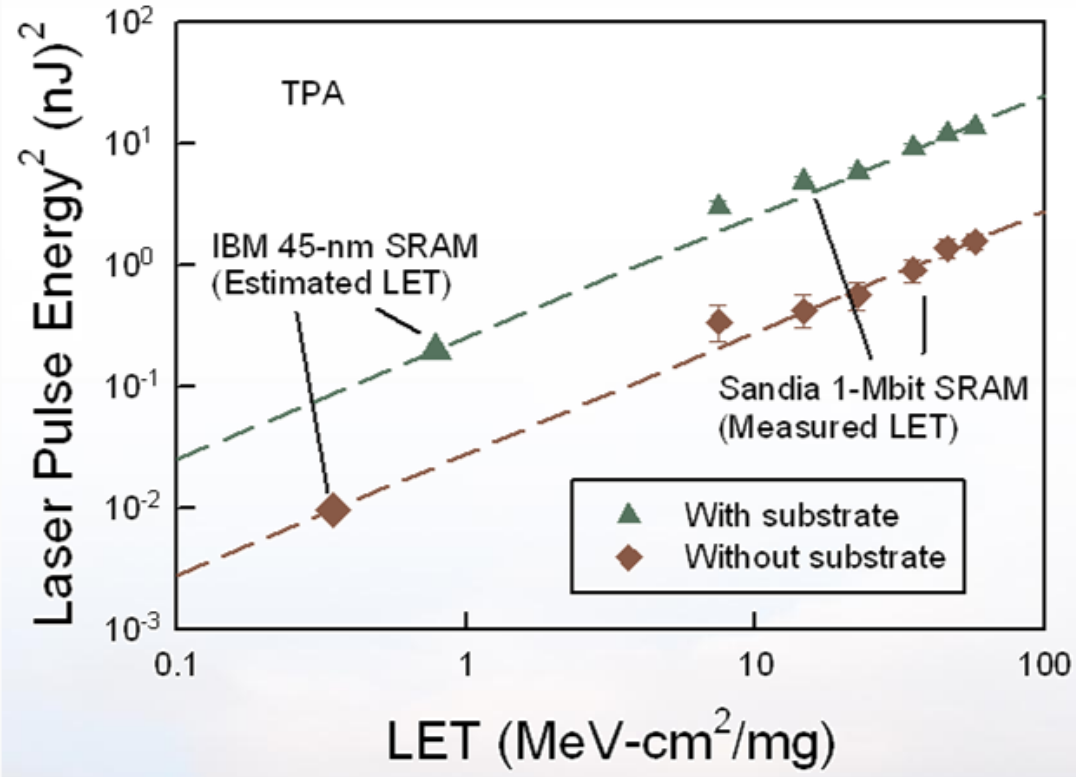
TPA laser measurements estimate Sandia DPSRAM threshold LET reasonably accurately



- Displacement currents do not qualitatively affect TPA results
- From heavy-ion measurements, threshold of DPSRAMs determined to be ~ 65 MeV-cm^2/mg (*Schwank et al. TNS 2009*)
- From laser measurements, estimated LET thresholds are 51 and 63 MeV-cm^2/mg with and without substrate, respectively

Results suggest that TPA laser measurements may be suitable for estimating threshold LET for circuits built in the same technology

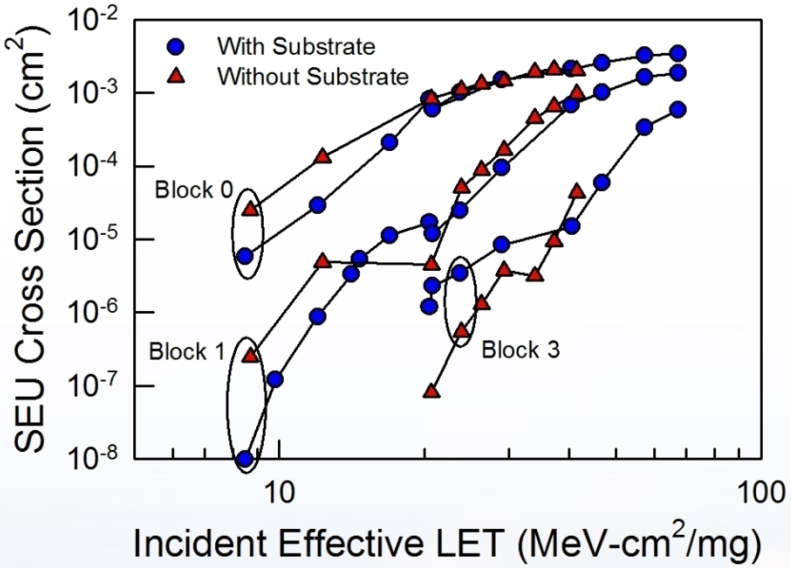
TPA laser measurements overestimate threshold LET for IBM SRAMs



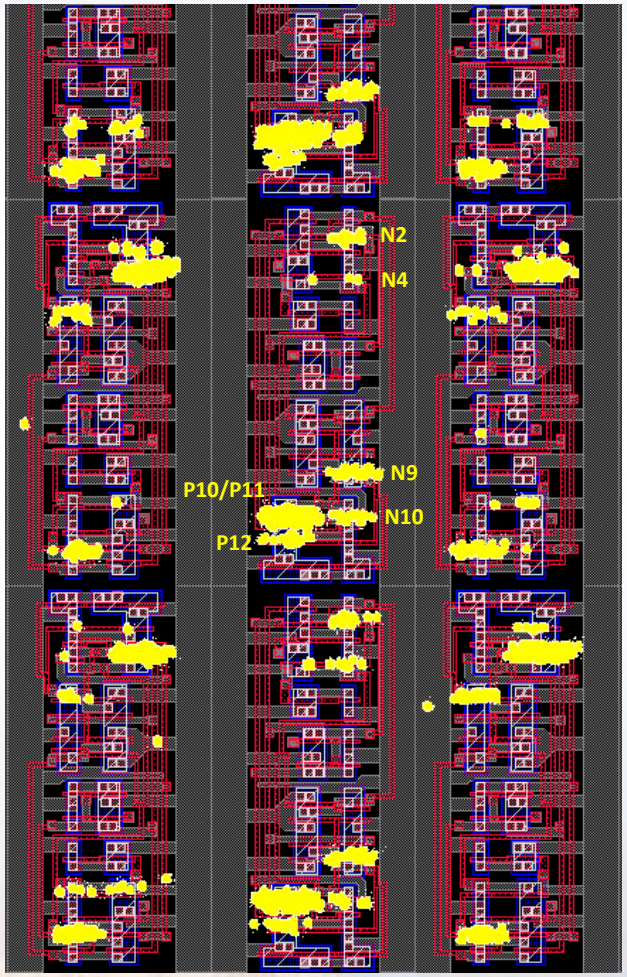
- From proton measurements, threshold of IBM SRAMs determined to be ~ 0.186 MeV-cm^2/mg (*Heidel et al. TNS 2008*)
- From laser measurements, estimated LET thresholds are 0.78 and 0.34 MeV-cm^2/mg with and without substrate, respectively

Likely cause for poor estimations due to large laser spot size compared to circuit dimensions

In addition to SPA and TPA, backside heavy ion and microbeam characterization being performed devices



Heavy ion results



Microbeam results

Summary

- We explored techniques to remove the back substrate for SOI devices with and without traditional packaging
- For packaged die, the backs of the packages were thinned down to the back substrate by a mechanical/polishing technique, and then the substrate was removed
  - Advantageous for removing the back substrates of commercially packaged devices
  - Microcracks can be induced in the die during the mechanical/polishing process, which led to overetching during substrate removal
- If die are available, die can be mounted directly onto a specially designed PC board or laser milled packages before removing substrate with XeF_2
  - Advantageous for flip chip bonded die
  - Microcracks are not an issue