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Analysis and Prediction of Stability in Commercial, 1200 V, 33A, 4H-SiC MOSFETs

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***Abstract*— State-of-the-art, commercially available, 4H-SiC MOSFETs are evaluated for stability under high-temperature over-voltage and pulsed over-current conditions. The devices show maximum vulnerability under high-temperature accumulation stress. The power MOSFET architecture coupled with a high interface trap density enables us to predict the stability of the device through a simple evaluation of the free-wheeling diode ideality factor (η) of the unstressed device.**

Keywords - Silicon Carbide; Power MOSFET; Free-Wheeling Diode, Hole Trapping.

I. INTRODUCTION

The Silicon Carbide (SiC) MOSFET is a leading candidate for next-generation power transistors due to the large bandgap, high thermal conductivity, high breakdown field strength, and high saturation electron drift velocity of SiC. The predominant degradation trends in state-of-the-art, commercially available, 4H-SiC MOSFETs [1] under high-temperature over-voltage and pulsed over-current stress are reported here. At a given temperature, the oxide shows greater vulnerability to hole trapping than to electron trapping. While different devices degrade uniformly under high-temperature inversion and pulsed over-current stress, D_{IT} near the valence band edge (E_v) strongly influences degradation rates and maximum degradation limits under accumulation stress. The free-wheeling diode ideality factor (η) for an unstressed device is found to be a strong predictor of the vulnerability of a given device to hole trapping.

II. DEVICE DEGRADATION UNDER HIGH-TEMPERATURE OVER-VOLTAGE:

Figs. 1 and 2 show the degradation in plastic packaged, 4H-SiC MOSFETs with t_{ox} = 70nm (rated at 1200V, 33A at T_j = 25°C; $T_{j,max}$ = 125°C) as a function of gate voltage (at 175°C, Fig. 1a) and ambient temperature (at ±20V, Fig. 1b), respectively. The devices showed no degradation within voltage limits of ±20 V up to 125°C. At a given temperature or bias, the oxide shows more vulnerability to hole trapping than to electron trapping. Heating the device at the stress temperature with a bias of opposite sign and equal magnitude completely recovers the trapped charge [2]. Either heating the device or applying the opposite bias alone does not recover the device significantly.

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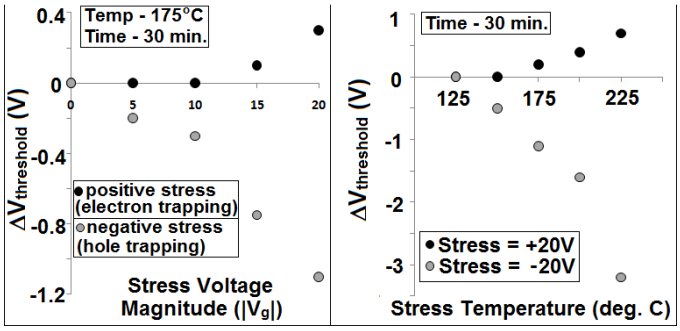

Figure 1. $V_{threshold}$ degradation due to charge trapping in the oxide at 175°C for 30 min. stress (left) and $V_{threshold}$ degradation due to charge trapping in the oxide at V_g = ±20 V for 30 min. stress (right). The device is recovered exactly to the initial state at the start of each bias step.

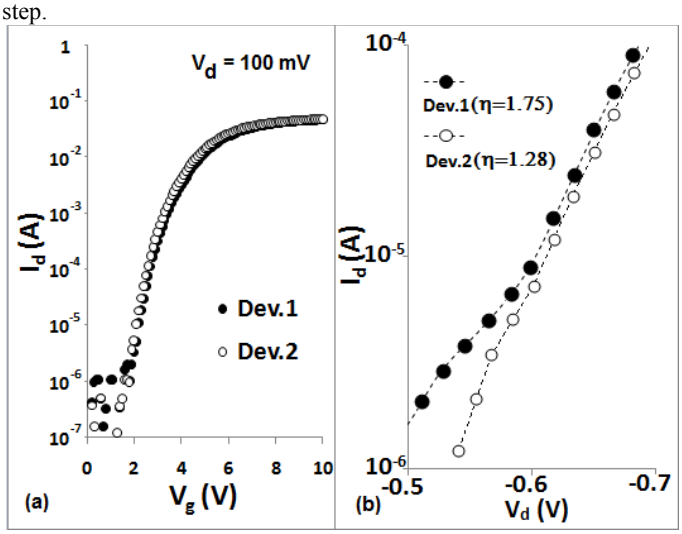

Figure 2. (a) Identical I_d–V_g characteristics of two devices (V_d = 100 mV. (b) Freewheeling diode characteristics of the same devices under zero gate bias.

The devices tested showed excellent uniformity of most electrical characteristics, including virtually identical sub-threshold I_d-V_g curves. However, the hole trapping rate and the maximum degradation at elevated temperature show considerable variation from device to device. Fig. 2a shows identical I_d–V_g characteristics in two devices. Contrary to conventional lateral MOSFETs, vertical power devices use an

integrated free-wheeling diode structure to protect against large transient currents in off-state bias due to inductive loads. The free-wheeling diode ideality factor (η) shows considerable variation from device to device, even for devices with similar I_d-V_g characteristics (Fig. 2b).

Fig. 3 shows post-stress (-20 V, 175°C, 150 min.) degradation in I_d–V_g characteristics of the two devices shown in Fig. 2. Device 2, having a smaller ideality factor, degrades more. This is a consistent trend with all tested devices (Fig.4). Both the degradation rate (degradation magnitude at different times) and the maximum degradation reached (the degradation saturates between 2.5 hrs and 3.5 hrs for all devices) increases with decreasing diode ideality factor η.

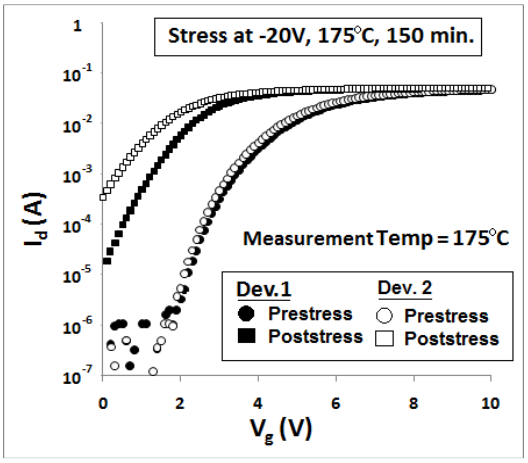

Figure 3. Post-stress (-20 V, 175°C, 150 min.) degradation in I_d–V_g characteristics (V_d = 100 mV) of the two devices in Fig. 2. Device 2, having smaller η (refer to Fig. 2b) degrades more.

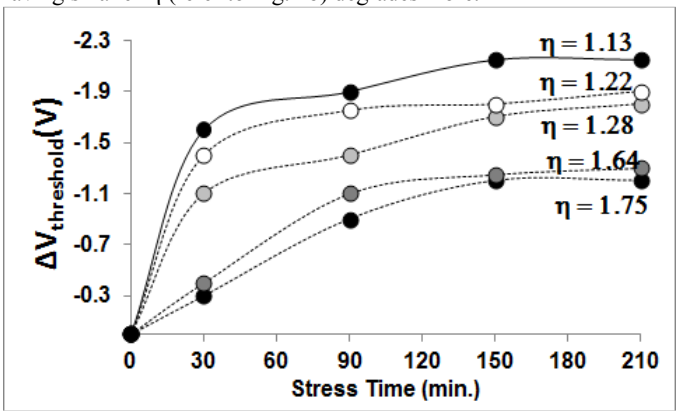

Figure 4. $V_{threshold}$ degradation due to accumulation stress (-20 V, 175°C) as a function of pre-stress free-wheeling diode ideality factor (η) for five different devices with nearly identical sub-threshold characteristics. Devices with low η show high rates of degradation as well as higher levels at which degradation saturates.

A. Free-wheeling diode turn-on path and D_{IT} near E_v

The correlation between η and hole trapping is better understood by studying the free-wheeling diode characteristics of the device as a function of V_g (Fig. 5). The explicit dependence of the diode turn-on voltage on V_g clearly shows that at V_g=0, the turn-on path of the diode is near the SiC/SiO_2 interface.

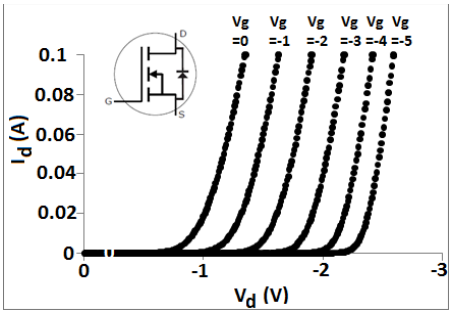

Figure 5. Free-wheeling diode characteristics of the 4H-SiC MOSFET as a function of V_g. Schematic of diode in the MOSFET structure is shown as inset. Biases less than the threshold voltage (V_g = 0 to -5V) ensure the MOSFET does not conduct.

At V_g = 0, the diode path having the smallest potential barrier is from the n-drift region, through the channel (which is depleted), to the source/p+ depletion region. This is clearly evidenced by the value of the turn-on voltage (~0.7 V), which is too small to represent the potential difference between quasi neutral p and quasi-neutral n-type 4H-SiC (E_g = 3.2 eV). In accumulation, the potential barrier between the n-drift region and the channel is raised to a much higher value, and the turn on-path is through the substrate. This will be demonstrated in detail through device simulations in the final paper. A difference in η is clearly visible in the low-current portion of the diode characteristics in Fig. 2b. A higher η for device 1 strongly suggests the presence of more defects at the SiC/SiO_2 interface, where the diode turns on. The sub-threshold characteristics of devices 1 and 2 are nearly identical and hence, the D_{IT} distribution near E_c must be nearly identical for the two devices. However, if the traps are neutral when filled, it is possible for D_{IT} near E_v to be much higher for device 1 than for device 2. This explains the lower hole trapping rate in device 1, since a higher D_{IT} near E_v would prevent the electric field at the interface from rising above the critical field required for hole tunneling into the oxide.

III. Device Degradation under Pulsed Over-current

The pulsed over-current operation (gate pulsed from 0 to 20 V) results in degradation similar to what is observed for electron trapping at high temperature, DC stress conditions. The primary mechanism appears to be electron trapping due to heating of the device beyond the T_j specification of 125°C. These experiments will be described in detail in the final paper. For a given duty cycle, the stressed devices showed more degradation for higher-frequency pulses. Increased junction heating due to very high current transients during device turn-off (which result in free-wheeling diode discharge near the interface at V_g = 0) is identified as a potential cause for this.

References

[1] http://www.cree.com/products/pdf/CMF20120D.pdf

[2] A. J. Lelis, IEEE Trans. Electron Devices **55**, 1835 (2008).