SAND2011-4813C

An Integrated MEMS Vacuum Diode

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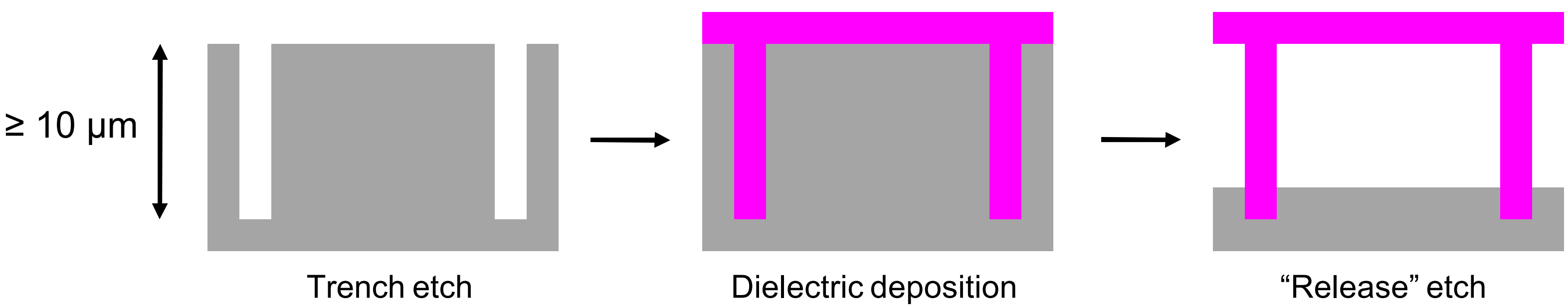
Fabrication methods

Adapt methods from microfluidics, photonic lattice, bulk micromachining to fabricated in situ vacuum encapsulated field emission diode

- Use deep Si reactive ion etching to create trench isolation.
- Dry SF_6/Ar silicon etching to form emitter tips.
- Low stress silicon nitride to create microcavities (similar to fluidic channels).
- Tungsten damascene used to fabricate anode.
- Selective CVD tungsten to clad Si emitter
- Deposit sputtered Al to seal cavities at the pressure of deposition.

Dielectric deposition

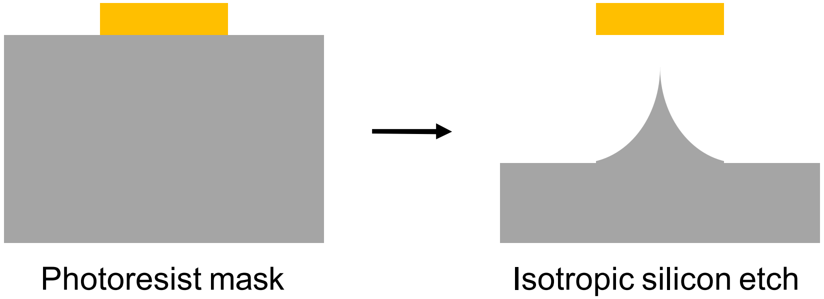
- To minimize capacitance, thick dielectrics are desired. This is incongruous with microfabrication because:
  - Thick dielectric films (many microns) are difficult to deposit & pattern.
  - Film stress of thick films may cause unacceptable wafer bow.
- CVD dielectric deposition, in combination with deep Si trench etch, can be used to create tall (>10 um) dielectric structures.
- Use low-stress (Si rich) silicon nitride for the dielectric (good mechanical properties, 200 mPa stress, can be > 1 um thick).



Generic, simplified structure

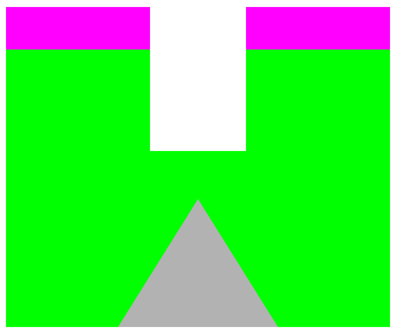
Tip formation

- Dry etch single-crystal silicon
  - May etch to completion, or use subsequent sharpening.
  - Can be readily incorporated into a tip-on-post geometry
- May use selective CVD tungsten deposition to clad tips with W.
  - Very thin (20 nm) self-limiting film; Si consumed in process; no apparent degradation of tip sharpness

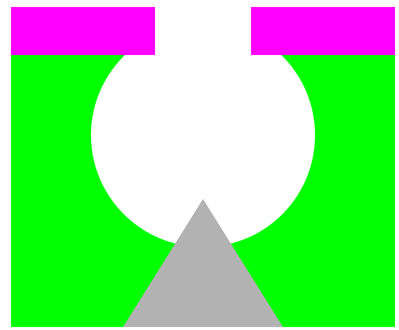


Anode formation

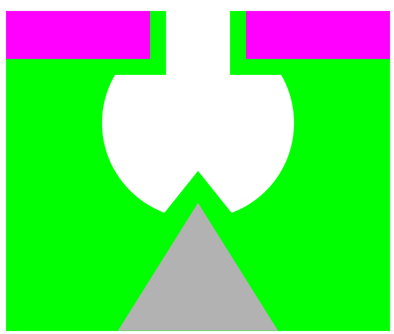
- Sacrificial spacer oxide used to create uniform anode/cathode spacing.
- Creates conformal anode shape above anode



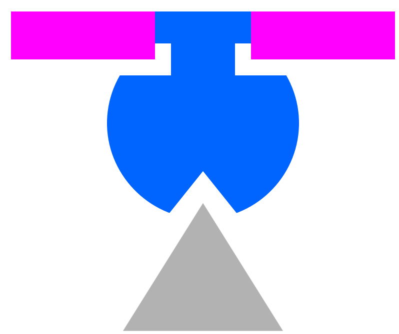
Etch hole in oxide



Wet etch to reveal tip



Deposit spacer oxide

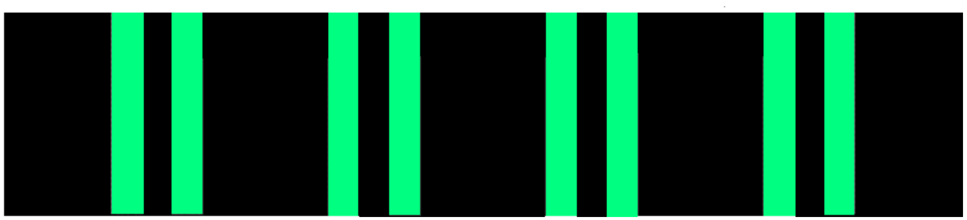


Deposit W anode; release

Integrated process

Etch isolation trench

Oxide overburden



Oxide CMP

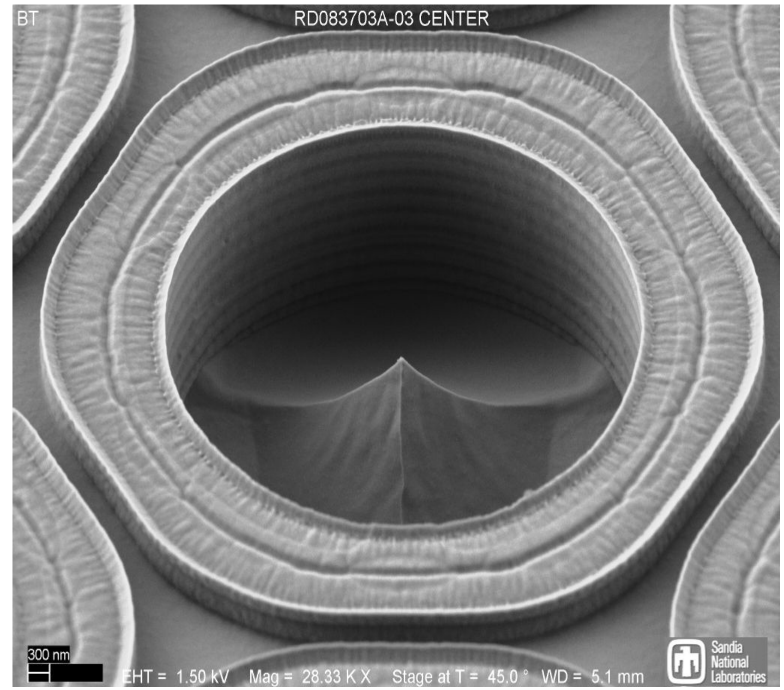
The oxide filling the trenches is sacrificial; will be etched away at the end of processing to create a vacuum moat

Integrated process

Pattern photoresist

Isotropic Si etch

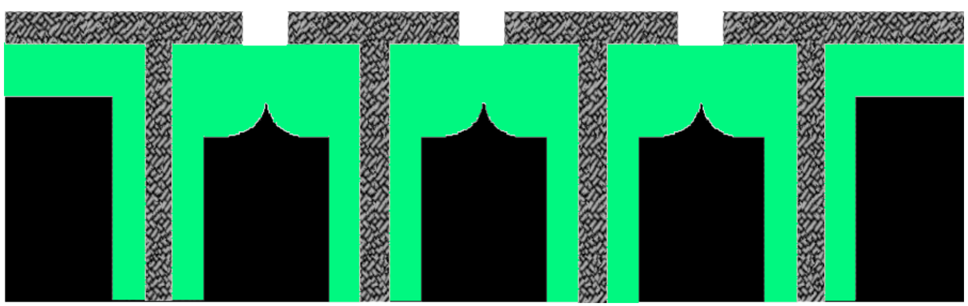
Strip photoresist



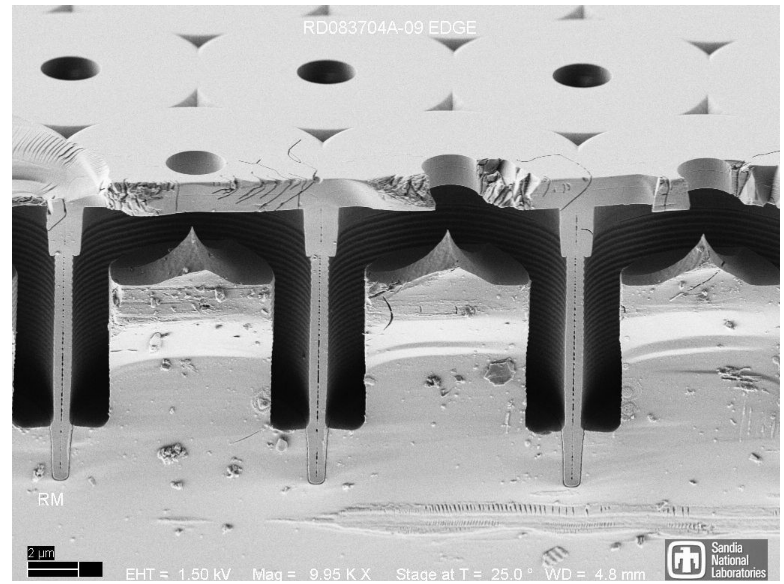
Integrated process

Oxide overburden; CMP

Trench etch

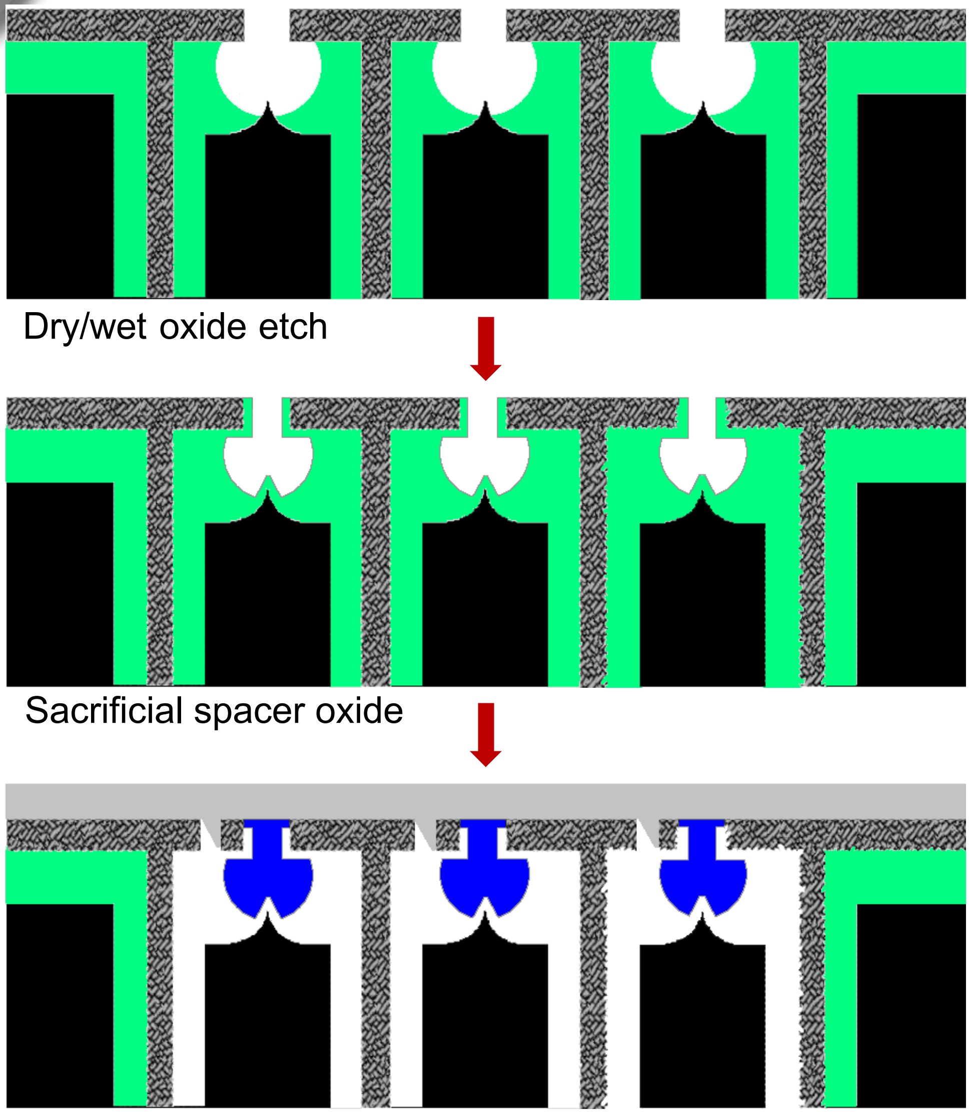


Low stress silicon nitride deposition; pattern anode



SEM micrograph after anode etch; sacrificial oxide has been stripped

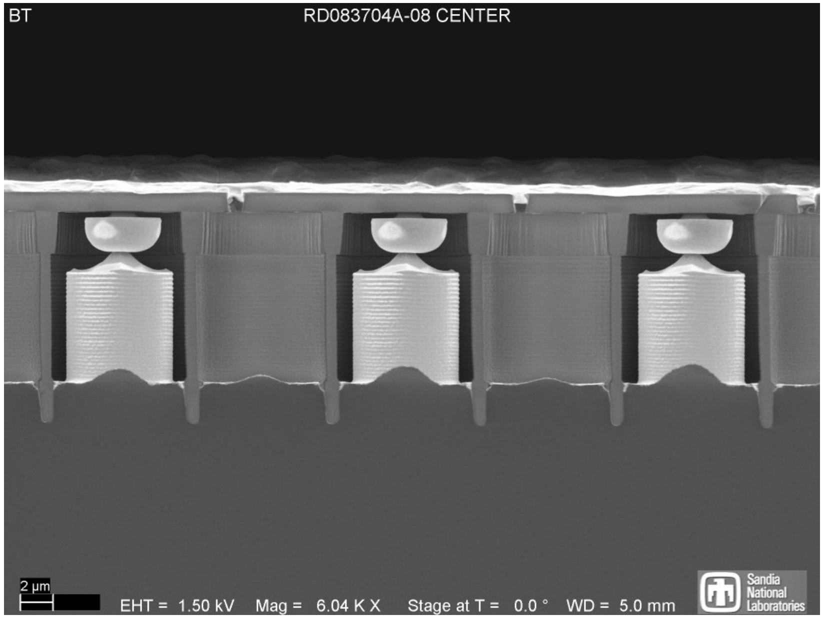
Integrated process



Dry/wet oxide etch

Sacrificial spacer oxide

Tungsten anode deposition; release etch; vacuum encapsulate



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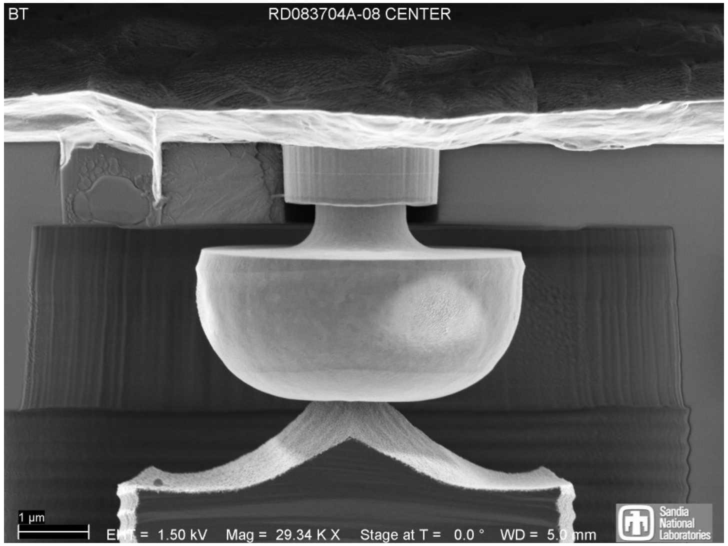
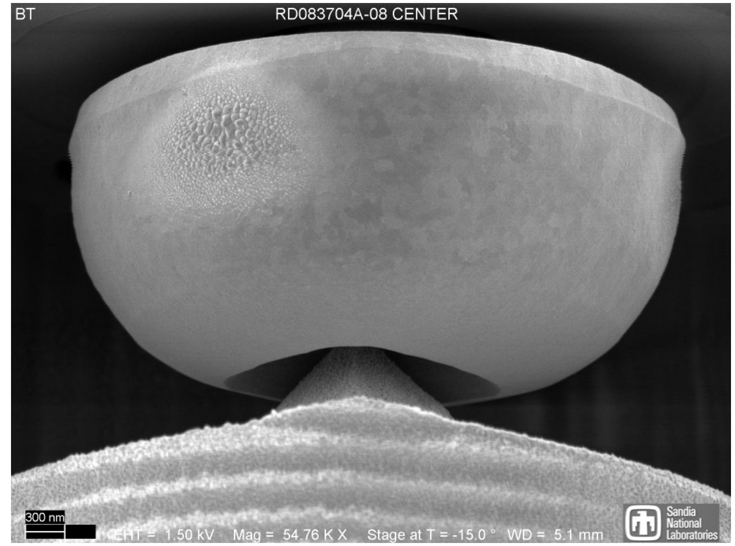
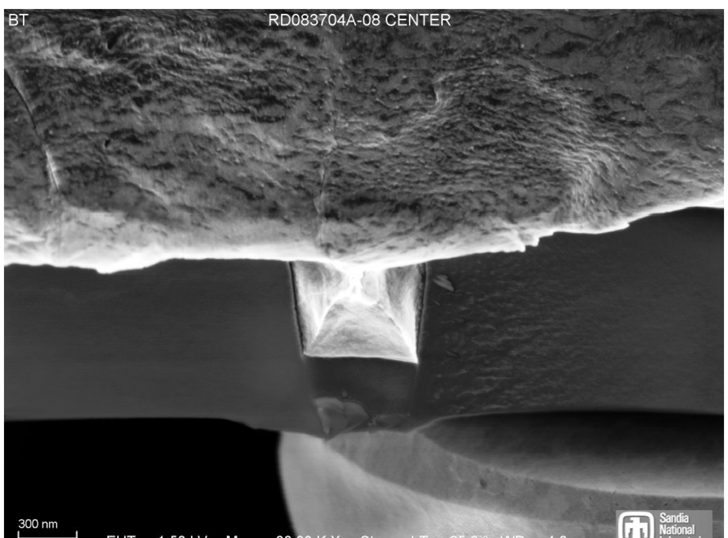
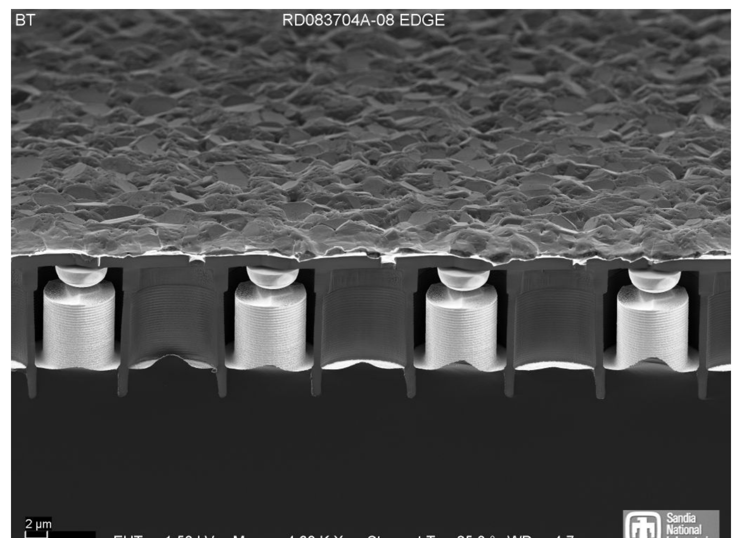
Conformal anode micrographs

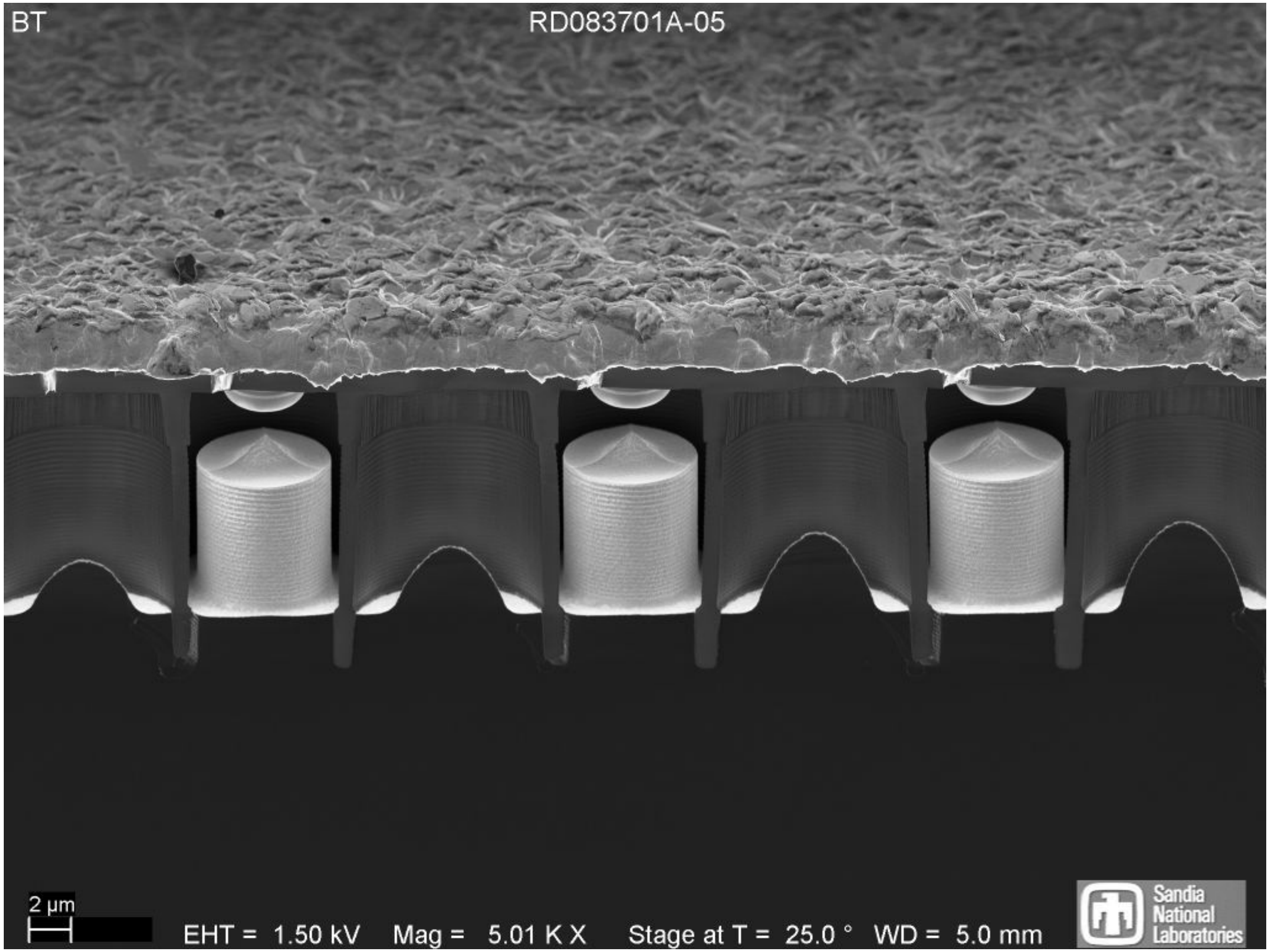




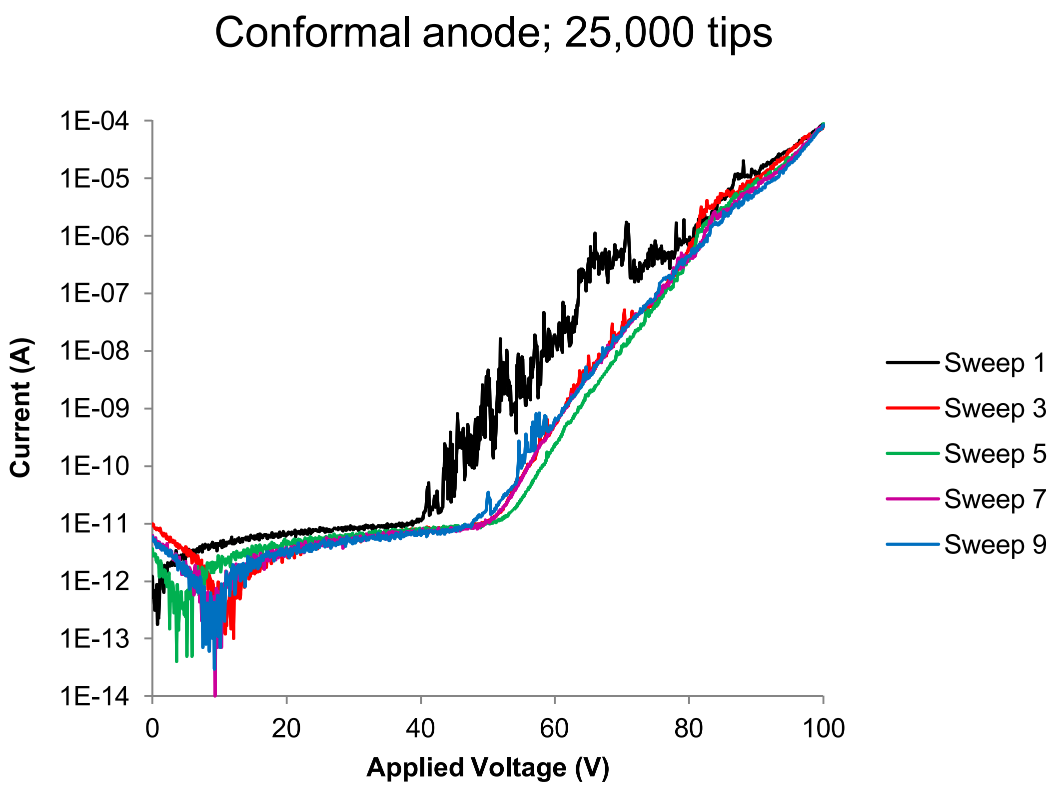




Non-conformal anodes



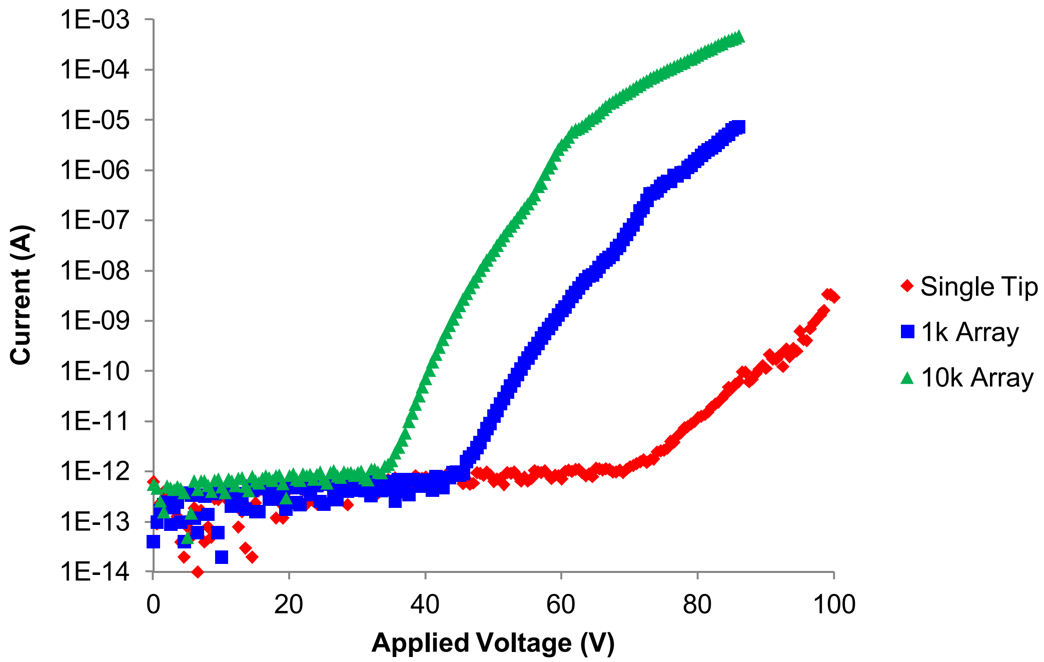
Forward bias



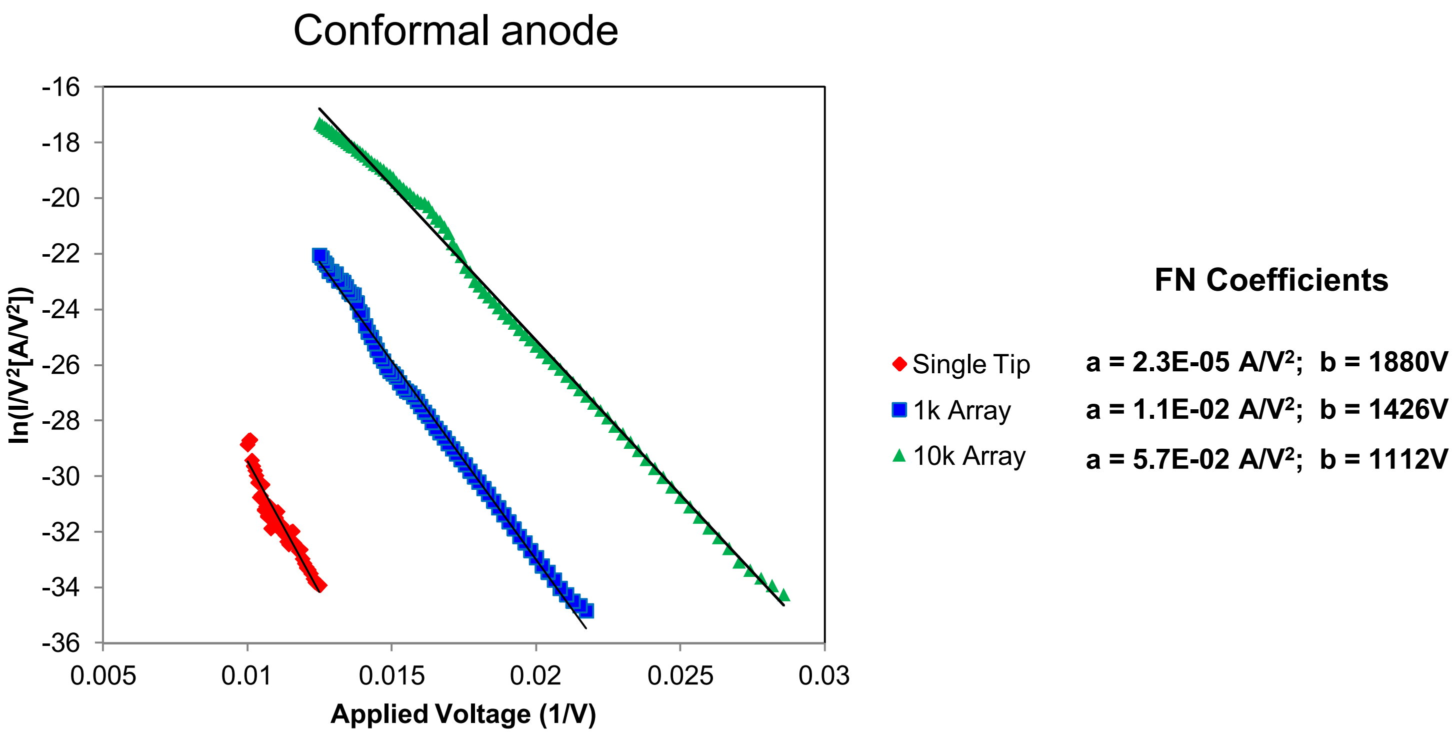
- First sweep is always noisy with lower turn-on voltage
- Space-charge (and/or series resistance) limited current at high applied voltage

Forward bias

Conformal anode: 1, 1000, 10,000 tips



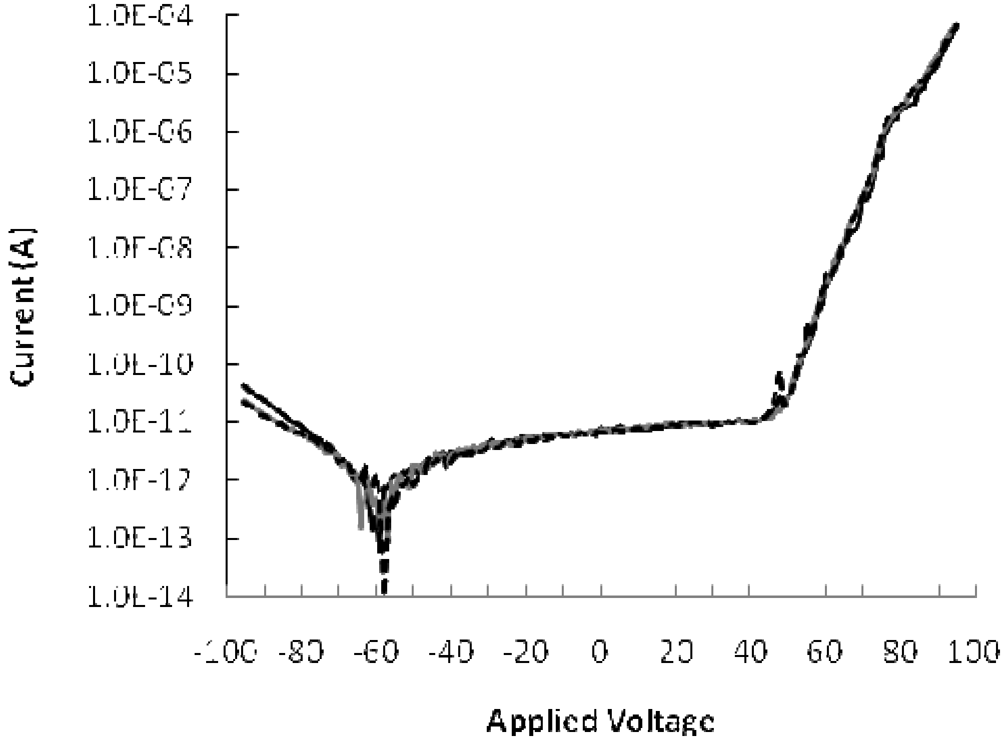
Fowler-Nordheim plots



# of Tips	Turn-on voltage (V @ 1 nA)	Enhancement Factor (cm^{-1})	Tip field at turn-on (V/nm)
1	98	3.3E05	3.2
1,000	57	4.3E05	2.5
10,000	44	5.5E05	2.4

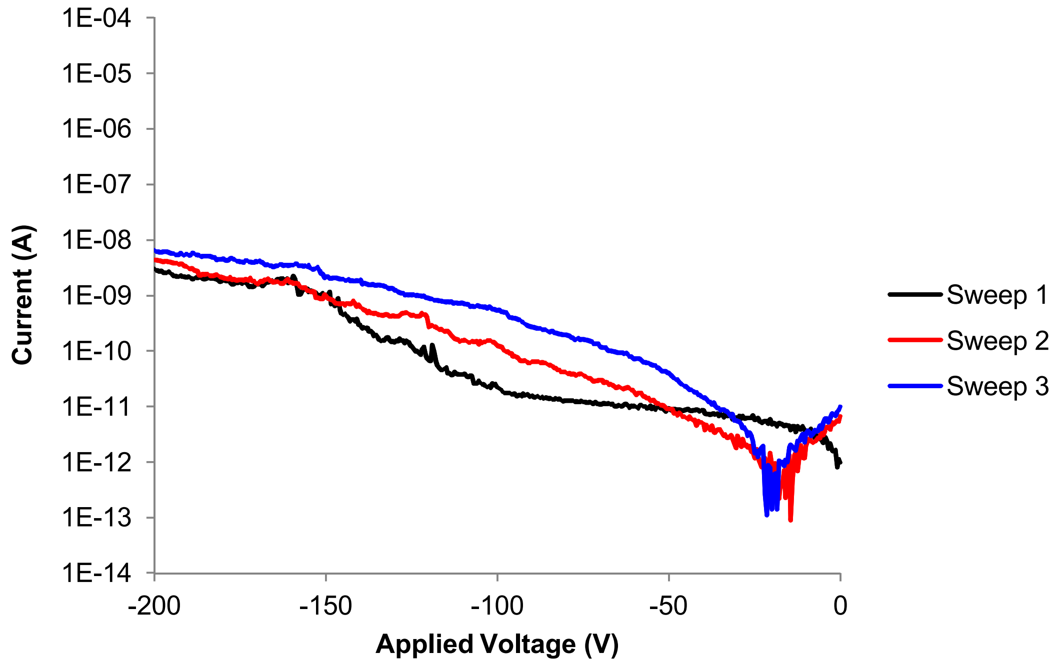
Forward/Reverse bias

25,000 tip array



Reverse bias

25,000 tip array



Leakage current observed at high reverse bias, but no breakdown at up to -200 V applied to anode.

Conclusions

A cold-cathode diode with wafer level vacuum encapsulation has been fabricated and tested.

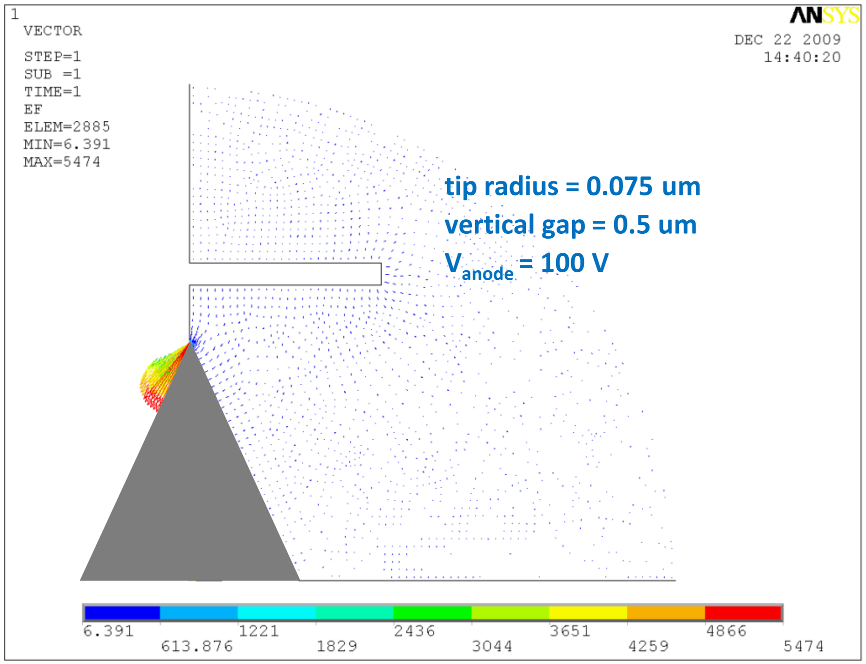
- Vacuum level in microcavities no better than that of metal deposition, ~ 5 mT.
- Sufficient for device operation.
- Anode/Cathode separation is ~ 300 nm.
- Rectifying behavior is seen with a on/off current ratio >7 decades, and no breakdown in reverse bias up to -200 V.
- Process is amenable to larger scale integration, as well as more complex structures (e.g., triode).

Back-up slides

Flat vs. Conformal Anode

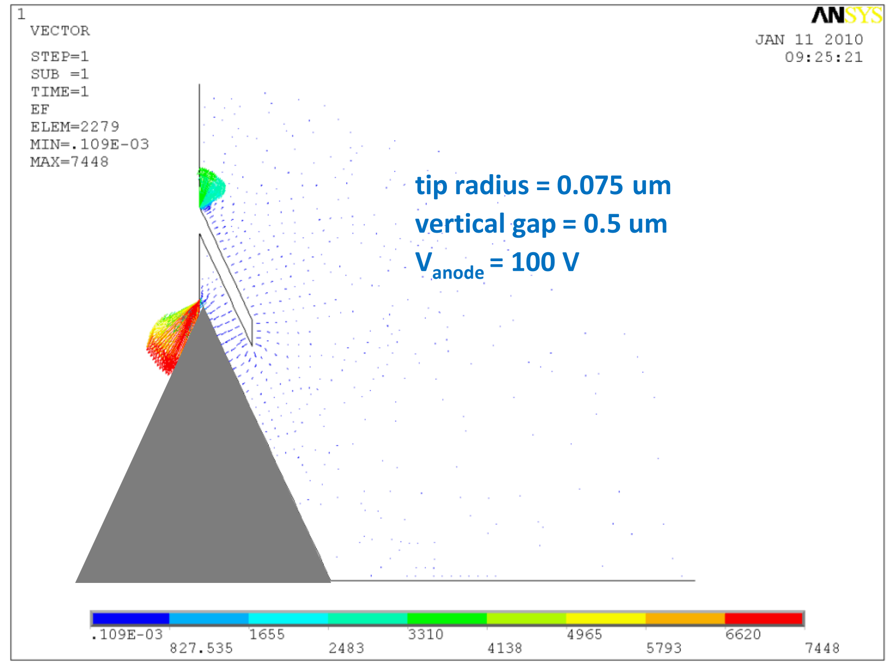
Anode shape and gap space

Flat anode



E_{tip} (max) = 5,474 V/μm

Conformal anode



E_{tip} (max) = 7,448 V/μm

- Simulation suggests conformal anode produces enhanced field at the tip