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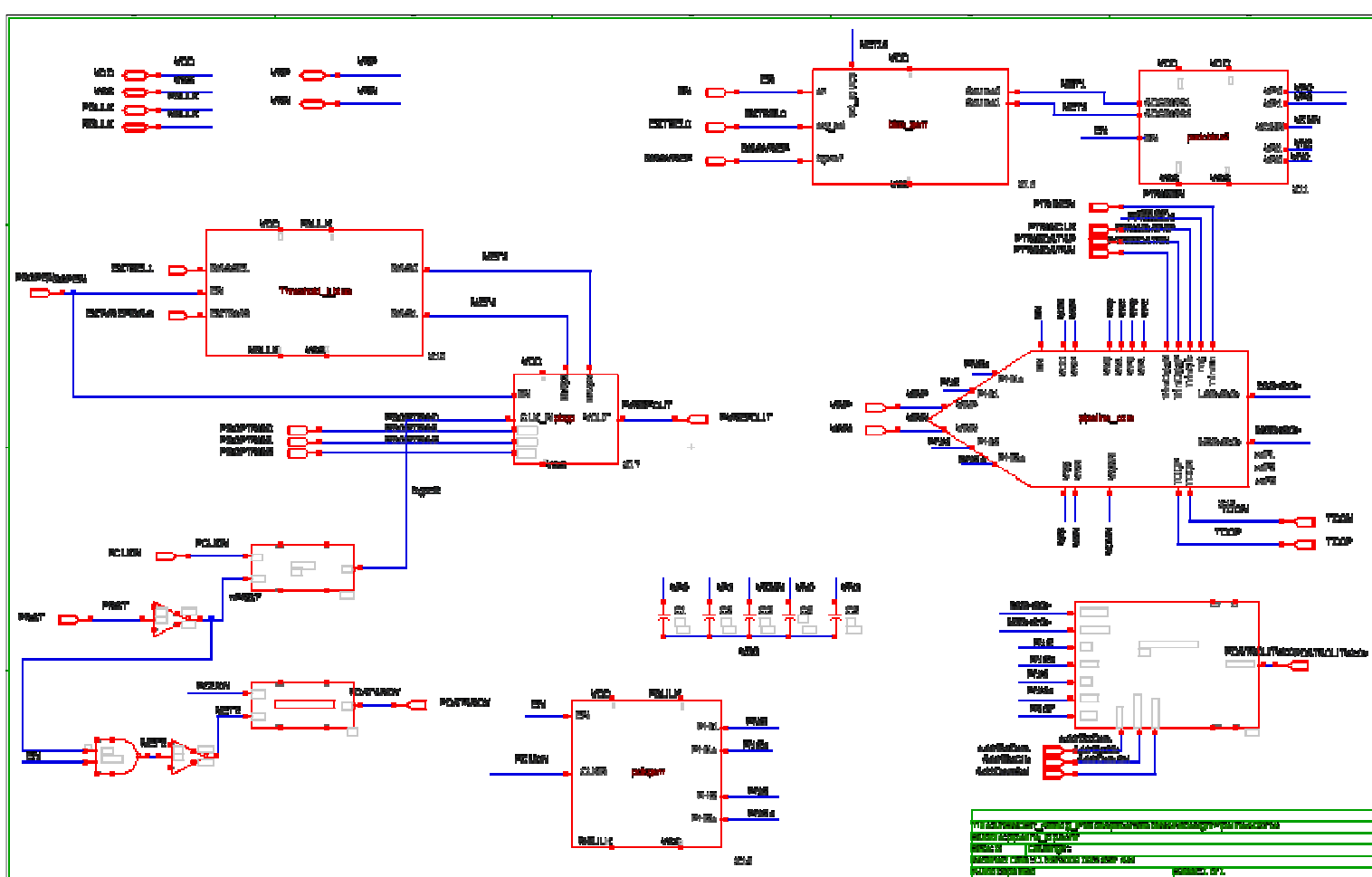
# Updating Sandia's Product Development Kit (PDK)

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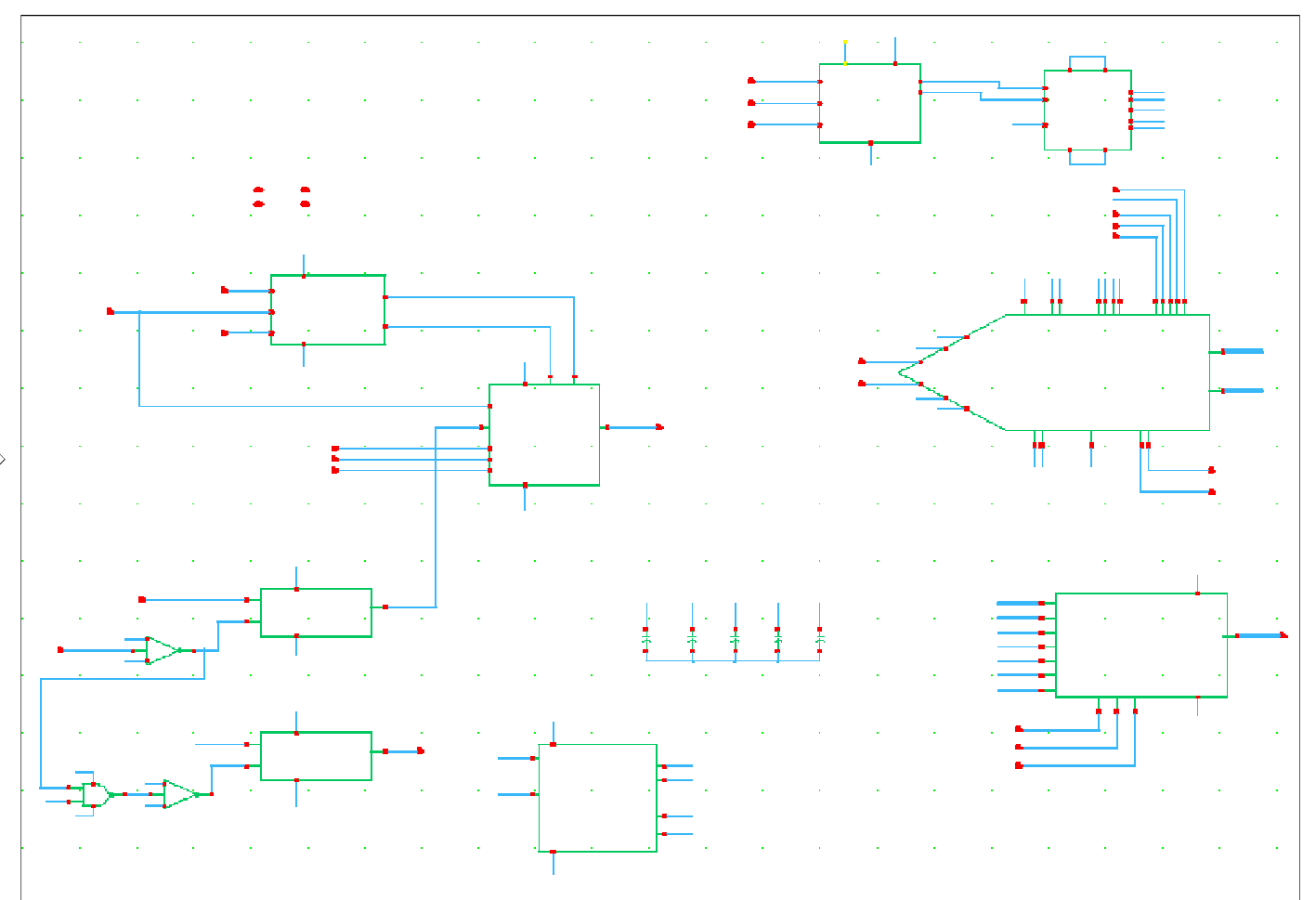
## Abstract

With the onset of advanced technology in microelectronics, more advanced circuit design tools have become a major factor in the building processes and simulation speed of modern day ASICs (Application Specific Integrated Circuits). Today, Cadence has a dominating force in the market of circuit design tools and is currently the main tool of choice by most circuit designers, include engineers at Sandia.

In this work, fundamental building blocks for many of the circuits designed at Sandia were transitioned from older programs to Cadence for easier use in design work by the lab's engineers and customers. The updated designs were validated in two ways: a functional simulation and comparison to the circuit's layout.

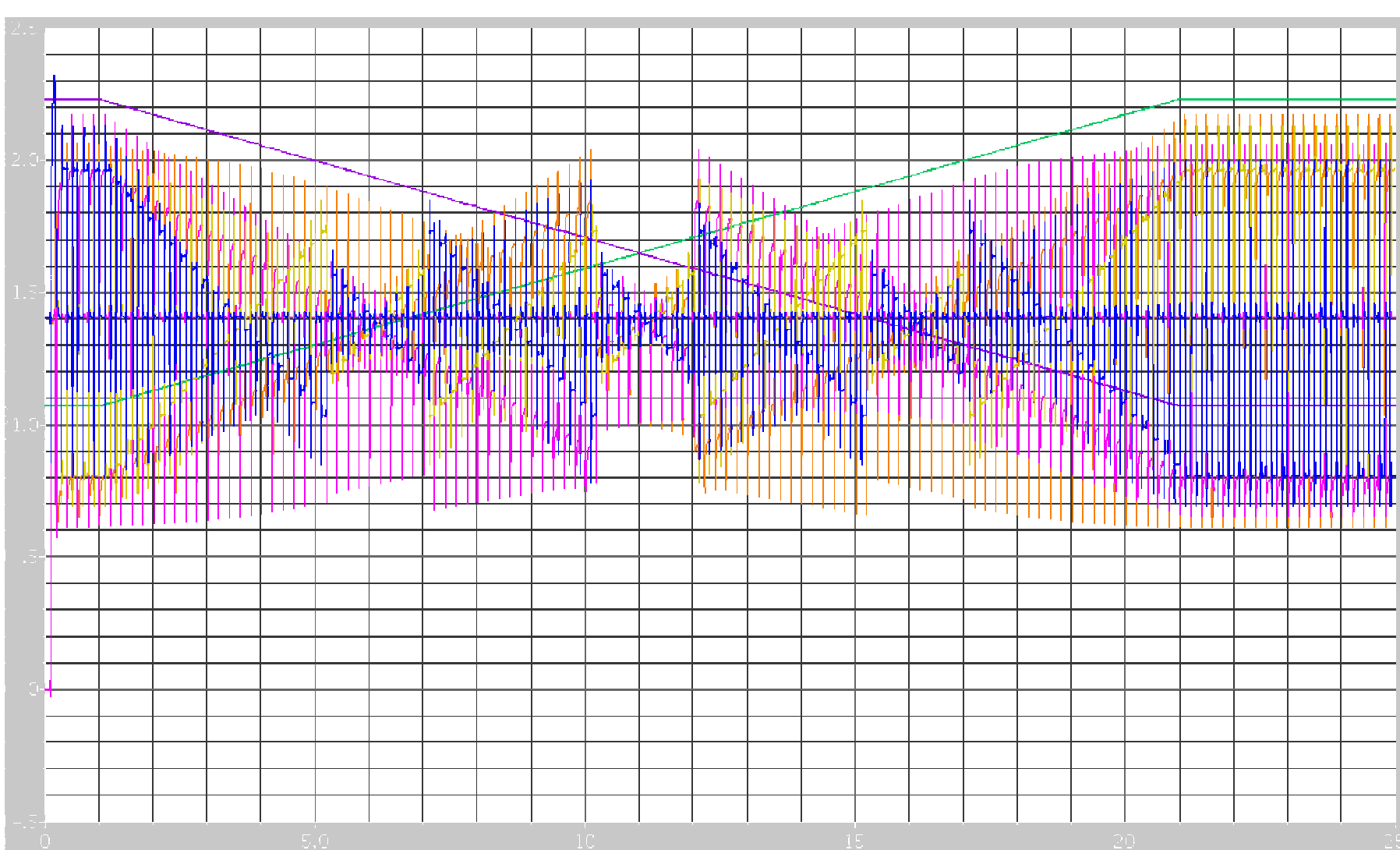


Original Schematic in Gateway

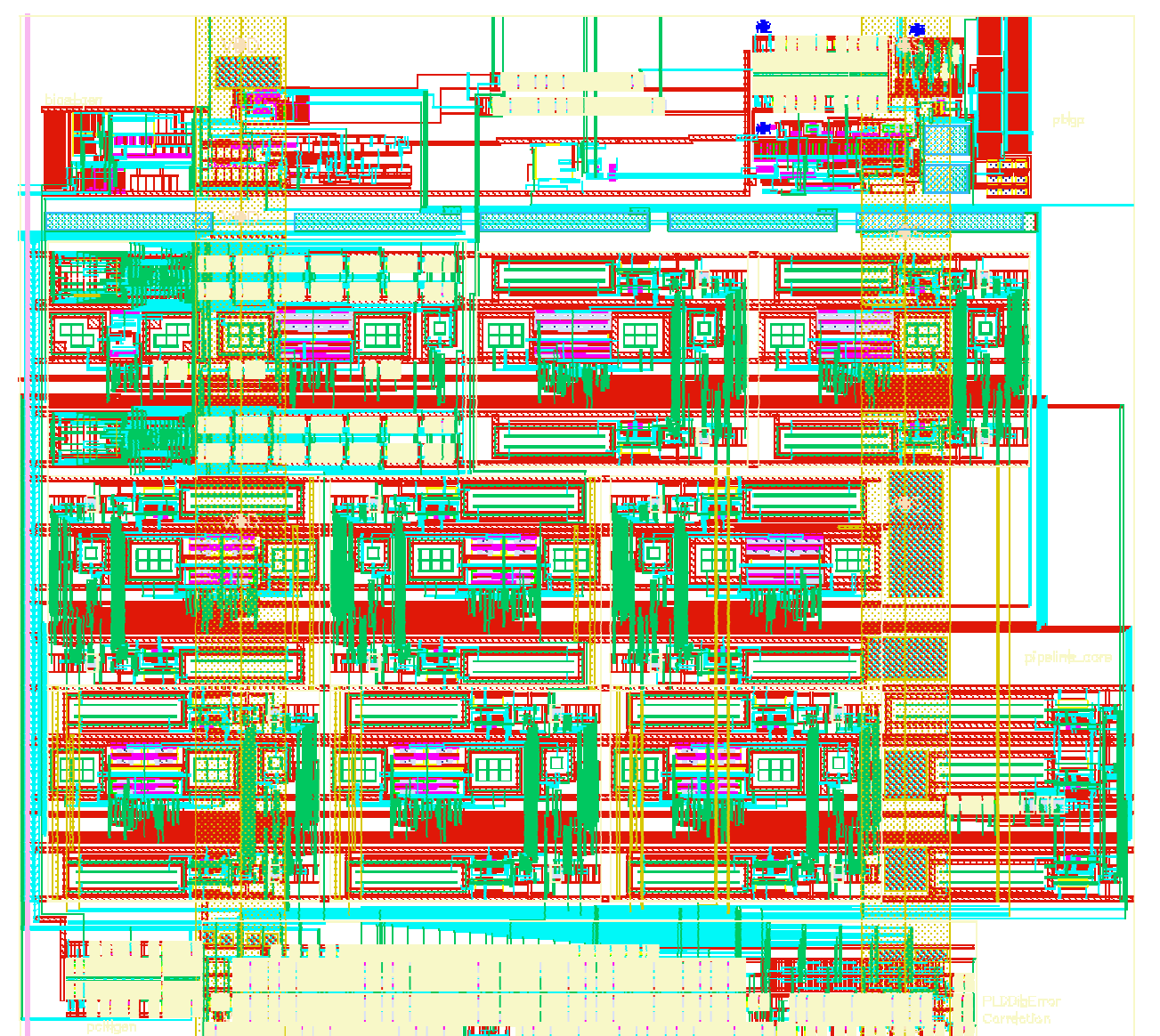


Updated Schematic in Cadence

## Design Validation



1. Functional Simulation



2. Layout Versus Schematic (LVS)