SAN098-2308J

Effect of Temperature on GaGdO/GaN Metal Oxide Semiconductor Field Effect Transistors

F. Ren, M. Hong, S. J. Pearton#, C. R. Abernathy#, J. R. Lothian*, S. N. G. Chu*, M. A. Marcus*, M. J. Schurman**, and A. Baca+*
Dept. of Chemical Engineering, University of Florida, Gainesville, FL32606
*Bell Laboratories, Lucent Technologies, Murray Hill, NJ 07974
**EMCORE Inc., Somerset, NJ 07061
+Sandia National Laboratories, Albuquerque, NM 87185
#Dept. of Materials Science and Engineering, University of Florida, Gainesville, FL 32606

ABSTRACT

$Ga_2O_3(Gd_2O_3)$ was deposited on GaN for use as a gate dielectric in order to fabricate a depletion metal oxide semiconductor field effect transistor (MOSFET). This is the first demonstration of such a device in the III-Nitride system. Analysis of the effect of temperature on the device shows that gate leakage is significantly reduced at elevated temperature relative to a conventional metal semiconductor field effect transistor (MESFET) fabricated on the same GaN layer. MOSFET device operation in fact improved upon heating to 400°C. Modeling of the effect of temperature on contact resistance suggests that the improvement is due to a reduction in the parasitic resistances present in the device.

DISCLAIMER

DISCLAIMER

Portions of this document may be illegible in electronic image products. Images are produced from the best available original document.

A number of GaN field effect transistors (FETs) and AlGaN/GaN heterostructure FETs have been reported showing excellent device breakdown characteristics[1-11]. To date however all show evidence of performance degradation due to the presence of high parasitic resistances.[4] The conventional low resistance n^+-cap layer structure used to reduce parasitic resistances in GaAs technology is generally not applied in nitride devices as it is difficult to perform the gate recess step. This is due to the high chemical stability of GaN which makes wet etching very difficult except at high temperatures or under optical stimulation.[12,13] and the drawbacks of dry etching for pattern transfer, which often results in ion bombardment induced damage. This damage then causes a low gate breakdown voltage.[14]

These problems can be overcome by using a metal oxide semiconductor FET (MOSFET) approach of the type recently reported for GaAs and InGaAs. In the $Ga_2O_3(Gd_2O_3)$/GaAs MOSFET, the oxide films were deposited on GaAs using e-beam evaporation from a single crystal of $Ga_2O_3(Gd_2O_3)$ in an MBE chamber. Using this approach, a mid-gap surface state density of 2 x 10^{10} $cm^{-2}eV^{-1}$ was obtained.[15] As a result, both n- and p-type enhancement mode MOSFETs could be demonstrated.[16,17] In this study, a similar approach has been applied to fabrication of $Ga_2O_3(Gd_2O_3)$/GaN devices resulting in the demonstration of the first GaN MOSFET. The effect of temperature on this device has also been investigated and compared with that of a conventional metal semiconductor FET (MESFET).

The GaN layer structure was grown on c-Al_2O_3 substrates prepared initially by $HCl/HNO_3/H_2O$ cleaning and an in-situ H_2 bake at 1070°C. A GaN buffer <300Å thick was grown at 500°C using trimethylgallium and ammonia and crystallized by ramping the temperature to 1040°C. The same precursors were used again to grow ≥ 3 μm of undoped GaN ($n < 10^{16}$ cm^{-3}) and an ~8000Å Si-doped ($n = \sim 3 \times 10^{17}$ cm^{-3}) active layer.[18] An oxide deposition technique similar to that previously reported for GaAs MOSFET formation was employed in this study as well. The sample was loaded into a solid source MBE chamber and the GaN native oxides were thermally desorbed at a temperature of 600°C. After oxide desorption, the wafer was transferred

under vacuum into a second chamber and the oxide was deposited onto the GaN using e-beam evaporation from a single crystal $Ga_2O_3(Gd_2O_3)$ source at a substrate temperature of 550°C.[19] The dielectric thickness and interface roughness were measured with X-ray reflectivity.[20,21] Device isolation was achieved with Cl_2/Ar dry etching in a Plasma Therm ICP system. Ti/Al/Pt/Au and Pt/Ti/Pt/Au were used as ohmic and gate contacts, respectively.

In order to investigate the MOS-gate breakdown voltage and the breakdown field distribution between the gate oxide and the GaN, a depletion-mode GaN MOSFET was fabricated. The oxide thickness was ~ 200Å. X-ray reflectivity was used to study the interfaces between the oxide and the GaN and between the oxide and the metal. Both interfaces were determined to be extremely smooth, as illustrated in Figure 1. The slope of the x-ray reflectivity curve at different x-ray incident angles can determine the roughness of the $Ga_2O_3(Gd_2O_3)$/GaN interface, as well as the air/$Ga_2O_3(Gd_2O_3)$ interface. Also, the oxide thickness can be determined from the width of the x-ray reflectivity oscillation period. From Figure 1, the root mean square roughness of the $Ga_2O_3(Gd_2O_3)$/GaN and air/$Ga_2O_3(Gd_2O_3)$ interfaces were estimated to be 3Å and 10Å, respectively. This atomic level (3Å) smoothness for the $Ga_2O_3(Gd_2O_3)$/GaN interface should provide a high carrier mobility and the smoothness of both interfaces should prevent localized high breakdown fields.

From C-V measurement, the dielectric constant was determined to be ~14.6, which is much higher than that of GaN at ~9. The breakdown field distribution is proportional to the ratio of dielectric constants of gate oxide and semiconductor. In this material system, the breakdown field distribution between GaN and $Ga_2O_3(Gd_2O_3)$ is 1 to 0.62. Therefore, the gate breakdown voltage of the MOSFET should be higher than for the Schottky gate. This improved breakdown has in fact been observed in our D-MOSFET where a MOS-gate voltage of > 35V was demonstrated as compared to the 16V of the Pt Schottky gate on the same GaN epi-layer. Figure 2 shows the drain I-V characteristics of a $1 \times 50\ \mu m^2$ gate dimension GaN MOSFET. This is the first demonstration of a GaN MOSFET. The device shows an extrinsic transconductance of 5 mS/mm. The high

parasitic resistance in the low drain bias region is a result of the ohmic contact not yet being alloyed. Figure 2 also shows the device in operation at 400°C where the parasitic resistance in the low drain bias region appears to be reduced significantly. The effect of temperature on the gate diode (dia.=500 μm) characteristics was also investigated. As expected, the Pt Schottky gate diode began to exhibit significant gate leakage current at around 100°C while the oxide gate still maintained fairly low gate leakage current even up to 200°C (Figure 3).

In order to explain the reduction in parasitic resistance at elevated temperature, the effect of measurement temperature on resistance was studied in more detail. Au/Ti metallization was used to form n-type ohmic contacts on n-GaN. It was found that the sheet resistance increased as the measurement chuck temperature was elevated. This is due to the reduction in the electron mobility by phonon scattering.[22] However, the specific contact resistivity decreased initially as the chuck temperature increased, and reached a minimum at around 250ºC. As the chuck temperature reached 300ºC, the resistivity then increased.

A model was developed to explain this behavior. Total specific contact resistivity, R, is the sum of the ohmic contact metallization resistance, R_m, and the contact resistance between the ohmic metal and the GaN, R_c.

$$R = R_c + R_m$$

For the thermionic emission case:

$$R_c = [K/(\alpha^*T)]\exp[(q\Phi_B)/KT)]$$

where K is the Boltzman constant, α^* is the Richardson constant, T is the absolute temperature, q is the magnitude of the electrical charge, and Φ_B is the Schottky barrier height. The metal resistance can be expressed as

$$R_m = AT^3$$

where A is a constant. As the sample temperature is increased initially, the thermionic emission current increases, therefore the specific contact resistivity is reduced. However, as the sample

temperature is further increased, the resistance from the metallization increases and becomes the dominant component thus causing an increase in the total resistance. As shown in Figure 4, if we plot RT verses 1/T, a linear region is obtained in the low temperature region (<200°C). The current transport is dominated by the thermionic emission and the resistance is governed by the metal resistance at higher temperature (>250°C). From the proposed model and curve fitting, the Φ_B of the Ti/Au contact on n-GaN is estimated around 0.3 eV. This is within the range of past reports, i.e. 0.2 – 0.6 eV.[22-25]

In summary, a $Ga_2O_3(Gd_2O_3)$/GaN depletion mode MOSFET was fabricated for the first time. Analysis of the effect of temperature on the device shows that gate leakage is significantly reduced at elevated temperature relative to a conventional MESFET fabricated on the same GaN layer. The MOSFET I-V characteristics in fact improved upon heating to 400°C. Modeling of the effect of temperature on contact resistance suggests that the improvement is due to a reduction in the parasitic resistances present in the device.

The authors gratefully acknowledge the U. S. Office of Naval Research under Contract No. N00014-98-1-0204, and DARPA/EPRI under contract MDA972-98-1-0006 for support of this work. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed-Martin Company, for the U. S. Department of Energy under Contract DEAC04-95AL85000.

References

[1]P. M. Asbeck, E. T. Yu, S. S. Lau, G. J. Sullivav, J. Van Hove and J. M. Redwing, Electron. Lett. **33** 1230 (1997).

[2]S. C. Binari, W. Kruppe, H. B. Dietrich, G. Kelner, A. E. Wickenden and J. A. Freitas, Solid State Electron. **41** 1549 (1997).

[3]M. S. Shur, Mat. Res. Soc. Symp. Proc. **483** 15 (1998).

[4]J. Burm, K. Chu, W. J. Schaff, L. F. Eastman, M. A. Khan, Q. Chen, J. W. Yang and M. S. Shur, IEEE Electron. Dev. Lett. **18** 141 (1997).

[5]R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. A. Khan and M. S. Shur, IEEE Electron. Dev. Lett. **18** 492 (1997).

[6]M. A. Khan, Q. Chen, C. J. Sun, M. S. Shur and B. Gelmark, Appl. Phys. Lett. **67** 1429 (1995).

[7]Y.-F.Wu, B. P. Keller, P. Fini, S. Keller, T. J. Jenkins, L. T. Kenias, S. P. DenBaars and U. K. Mishra, IEEE Electron. Dev. Lett. **19** 50 (1998).

[8]Y. F. Wu, B. P. Keller, S. Keller, D. Kapolneck, P. Kozodoy, S. P. DenBaars and U. K. Mishra, Appl. Phys. Lett. **69** 1438 (1996).

[9]G. J. Sullivan, M. Y. Chen, J. A. Higgins, J. W. Yang, Q. Chen, R. C. Pierson and B. T. McDermott, IEEE Electron. Dev. Lett. **19** 198 (1998).

[10]A. T. Ping, Q. Chen, J. W. Yang, M. A. Khan and I. Adesida, IEEE Electron. Dev. Lett. **19** 54 (1998).

[11]O. Akatas, Z. F. Fan, A. Botcharev, S. N. Mohammad, M. Roth, T. Jenkins, L. Kehias and H. Morkoc, IEEE Electron. Dev. Lett. **18** 293 (1997).

[12]M. S. Minsky, M. White and E. L. Hu, Appl. Phys. Lett., **68** 1531 (1996).

[13]C. Youtsey, I. Adesida and G. Bulman, J. Elecgtron. Mater. **27** 282 (1998).

[14]F. Ren, J. R. Lothian, Y. K. Chen, R. Karlicek, L. Toan, M. Schurman, R. A. Stall, J. W. Lee and S. J. Pearton, Solid State Electron. **41** 1819 (1997).

[15]M. Passlack, M. Hong, J. P. Mannaerts, R. L. Opila, S. N. G. Chu, N. Moriya, F. Ren and J. Kwo, IEEE Trans. Electron. Dev. **44** 214 (1997).

[16]F. Ren, M. Hong, J. M. Kuo, W. S. Hobson, J. R. Lothian, H. S. Tsai, J. Lin, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen and A. Y. Cho, 1997 IEEE GaAs IC Symposium, Anaheim, CA Oct. 12-15, 1997.

[17]F. Ren, J. M. Kuo, M. Hong, W. S. Hobson, J. R. Lothian, J. Lin, H. S. Tsui, J. P. Mannaerts, J. Kwo, S. N. G. Chu, Y. K. Chen and A. Y. Cho, IEEE Electron. Dev. Lett. **19** 309 (1998).

[18]M. J. Schurman, T. Salgaj, C. Tran, R. Karlicek, I. Ferguson, R. Stall and A. Thompson, Mater. Sci. Eng. B, **43** 222 (1997).

[19]M. Hong, M. Passlack, J. P. Mannaerts, J. Kwo, S. N. G. Chu, N. Moriya, S. Y. Hou and V. J. Fratello, J. Vac. Sci. Technol. B, **14** 2297 (1996).

[20]D. Y. Noh, Y. Hwu, H. K. Kim and M. Hong, Phys. Rev. B, **51** 4441 (1995).

[21]L. G. Parratt, Phys. Rev. **95** 359 (1954).

[22]Q. Z. Liu and S. S. Lau, Solid State Electron. **42** 677 (1998).

[23]S. C. Binari, H. B. Dietrich and E. E. Haller, Electron. Lett., **30** 909 (1997).

[24]M. T. Hirsch, K. J. Duxstad and E. E. Haller, Electron. Lett. **33** 95 (1997).

[25]A. T. Ping, A. C. Schmitz, M. A. Khan and I. Adesida, Electron. Lett. **32** 68 (1996).

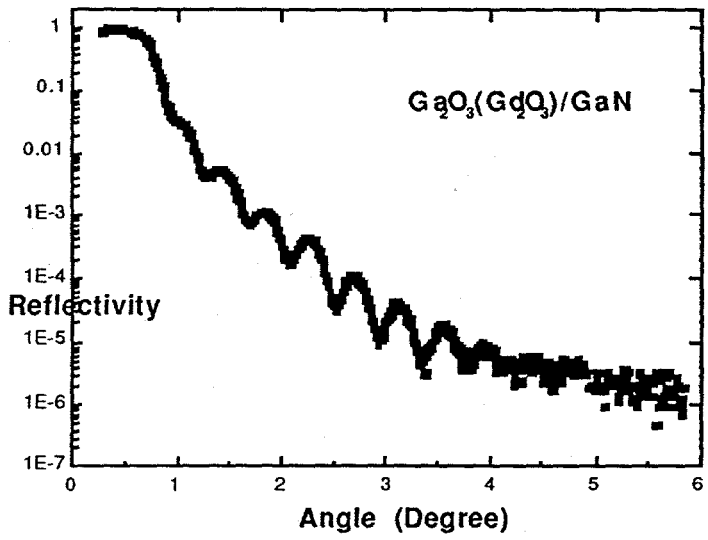
Figure Captions

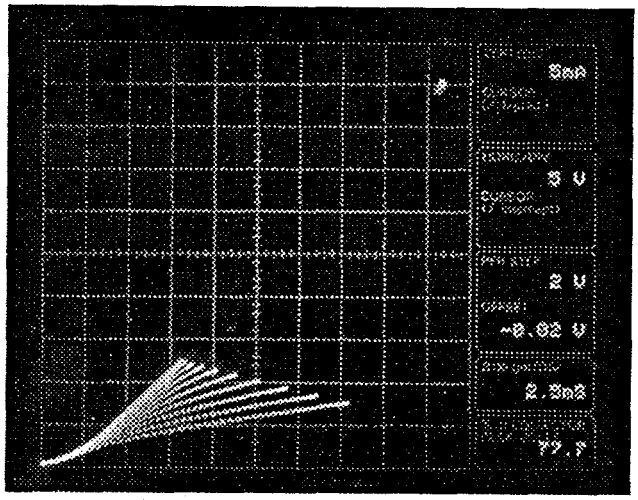
Figure 1. X-ray reflectivity spectrum of the dielectric/GaN interface in the D-mode device.

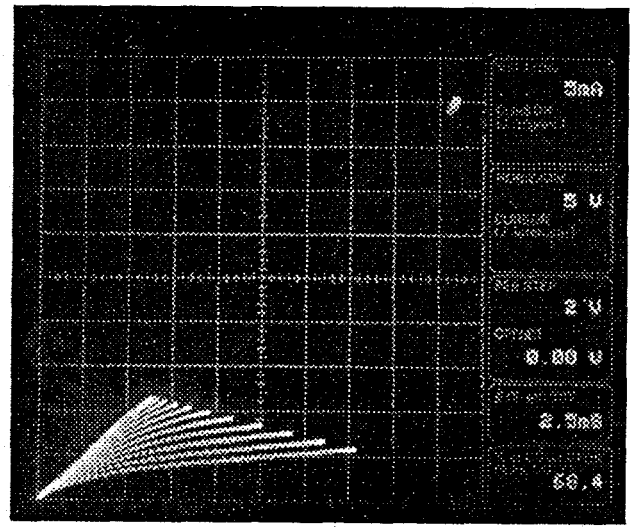
Figure 2. Drain I-V characteristics of a GaN MOSFET (top) measured at room temperature and (bottom) measured at 400°C.

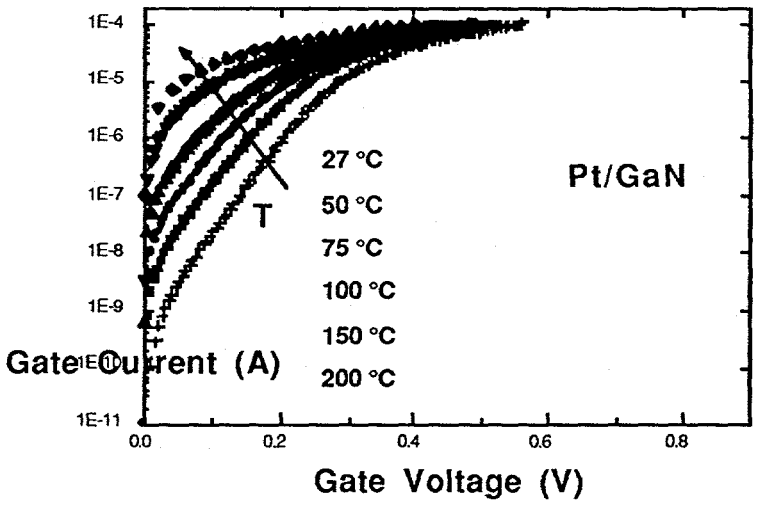
Figure 3. Gate forward characteristics as a function of measurement temperature for (top) Pt/GaN Schottky and (bottom) Pt/$Ga_2O_3(Gd_2O_3)$/GaN.

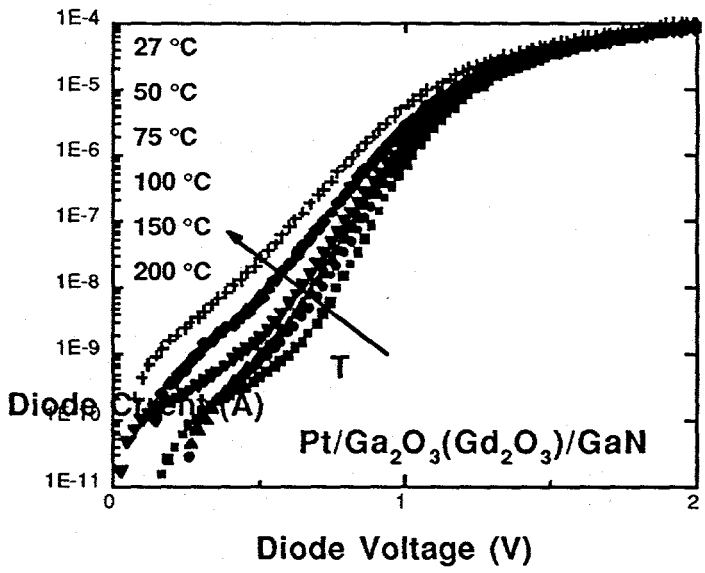
Figure 4. Total specific contact resistivity, R, multiplied by the measurement temperature, T, as a function of 1/T.

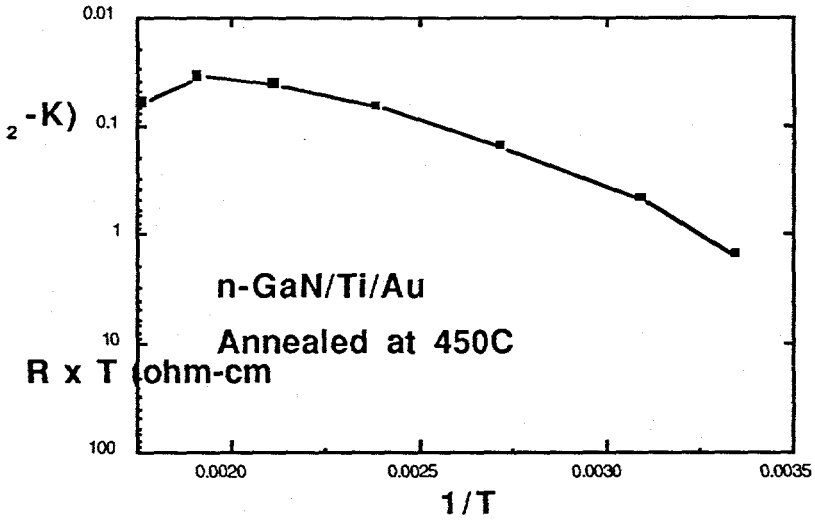

1
0.1
0.01
1E-3
1E-4
1E-5
1E-6
1E-7
Reflectivity
0
1
2
3
4
5
6
Angle (Degree)
Ga2O3(Gd2O3)/GaN


5 V
2 V
~0.02 V
2.2ms
72.1


5 V
2 V
0.00 V
2.2ms
60.4


1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
0.0
0.2
0.4
0.6
0.8
27 °C
50 °C
75 °C
100 °C
150 °C
200 °C
T
Pt/GaN
Gate Current (A)
Gate Voltage (V)


1E-4
1E-5
1E-6
1E-7
1E-8
1E-9
1E-10
1E-11
0
1
2
27 °C
50 °C
75 °C
100 °C
150 °C
200 °C
T
Pt/Ga2O3(Gd2O3)/GaN
Diode Current (A)
Diode Voltage (V)


0.01
0.1
1
10
100
n-GaN/Ti/Au
Annealed at 450C
R x T (ohm-cm
0.0020
0.0025
0.0030
0.0035
1/T