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# Accelerated Life Testing of PV Arc-Fault Detectors

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***Abstract* — As of 2011, the *National Electrical Code®* (*NEC*) has required arc-fault circuit interrupters (AFCIs) to be incorporated into photovoltaic (PV) systems to prevent fires. Some manufacturers are designing AFCIs to consist of arc-fault detectors (AFD) incorporated into inverters or combiner boxes in order to take advantage of the DC switching functionality of the existing hardware. Since AFCIs and AFDs are safety devices, it is critical to ensure the long-term functionality of AFD devices in these harsh environments. Sandia National Laboratories (SNL), in collaboration with Texas Instruments (TI), has performed accelerated life tests on 10 TI arc-fault detectors. The devices were tested after being subjected to the thermal damage equivalent of 1.7-year increments in an inverter until 77.6 equivalent years of solder fatigue damage. 30% of the boards experienced component failures but there were no solder failures, indicating solder fatigue is not the primary failure mode. Based on these results, TI is creating a burn-in process to screen AFD boards prior to shipping.**

***Index Terms* — photovoltaic systems, arc-fault detectors, accelerated life testing, rainflow counting, thermomechanical solder fatigue**

## I. INTRODUCTION

Arc-fault circuit interrupter (AFCIs) safety devices, required by the 2011 *National Electrical Code®* [1], must reliably function while installed on the photovoltaic (PV) system. While there has been extensive work to create functionally robust arc-fault detectors [2-4], little emphasis has been placed on ensuring they remain operational for the lifetime of the PV system (~30 years). Manufacturers of PV AFCIs have suggested putting them in different locations on the PV array, but in nearly all cases they will be exposed to diurnal temperature cycles. To minimize the cost, many companies are designing AFCIs to be integrated into the inverter in order to utilize the inverter or combiner DC disconnect. For instance, Texas Instruments (TI) has created an AFCI evaluation board that can be installed in the inverter, combiner box, or implemented as a stand-alone product [5]. Sandia National Laboratories (SNL) and TI are collaborating to estimate the lifetime of their inverter-integrated AFCIs to ensure their products would survive 30 years in the field.

While the failure mode for these devices is unknown, microelectronic and discrete component solder bonds are known to fail on printed wiring boards as a result of harsh thermal environments. Thermomechanical solder fatigue failure is common in thermal cycling environments such as those seen by automotive electronics (e.g., [6]), so it is believed that this would be one of the leading causes of AFCI failure since similar thermal cycling conditions exist in outdoor inverters. Additionally, Tigo Energy has performed accelerated life testing of their AFCIs and found solder connection failures to be a common failure mode [7].

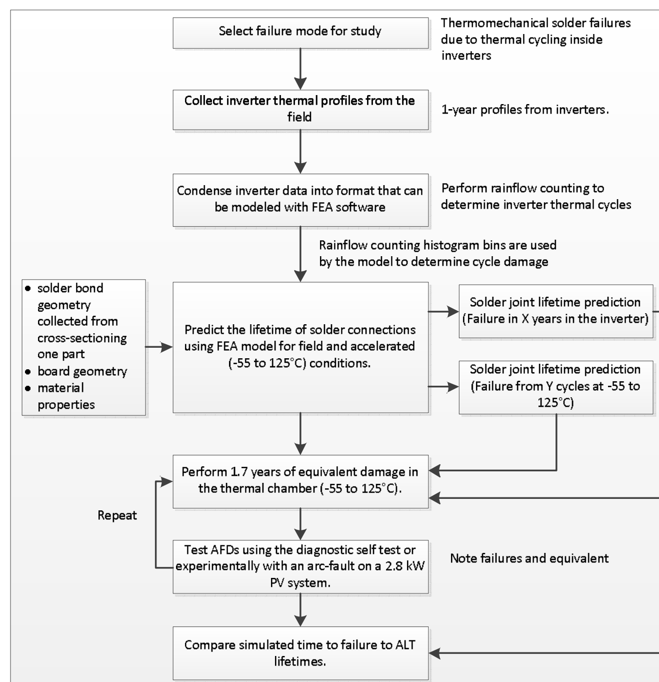


Fig. 1. Process for determining the equivalent lifetime of the arc-fault detectors for the solder fatigue failure mode.

The process to estimate the lifetime of the AFCIs is shown in Figure 1. To find the number of accelerated thermal cycles which produce 1-year of equivalent inverter exposure, a SNL-developed finite element analysis (FEA) code with Unified Creep Plasticity Damage (UCPD) material models for solder [8-9] was run for inverter thermal profiles [10] and compared to simulations of the -55 to 125°C cycle. The number of equivalent accelerated cycles was determined for the following thermal histories:

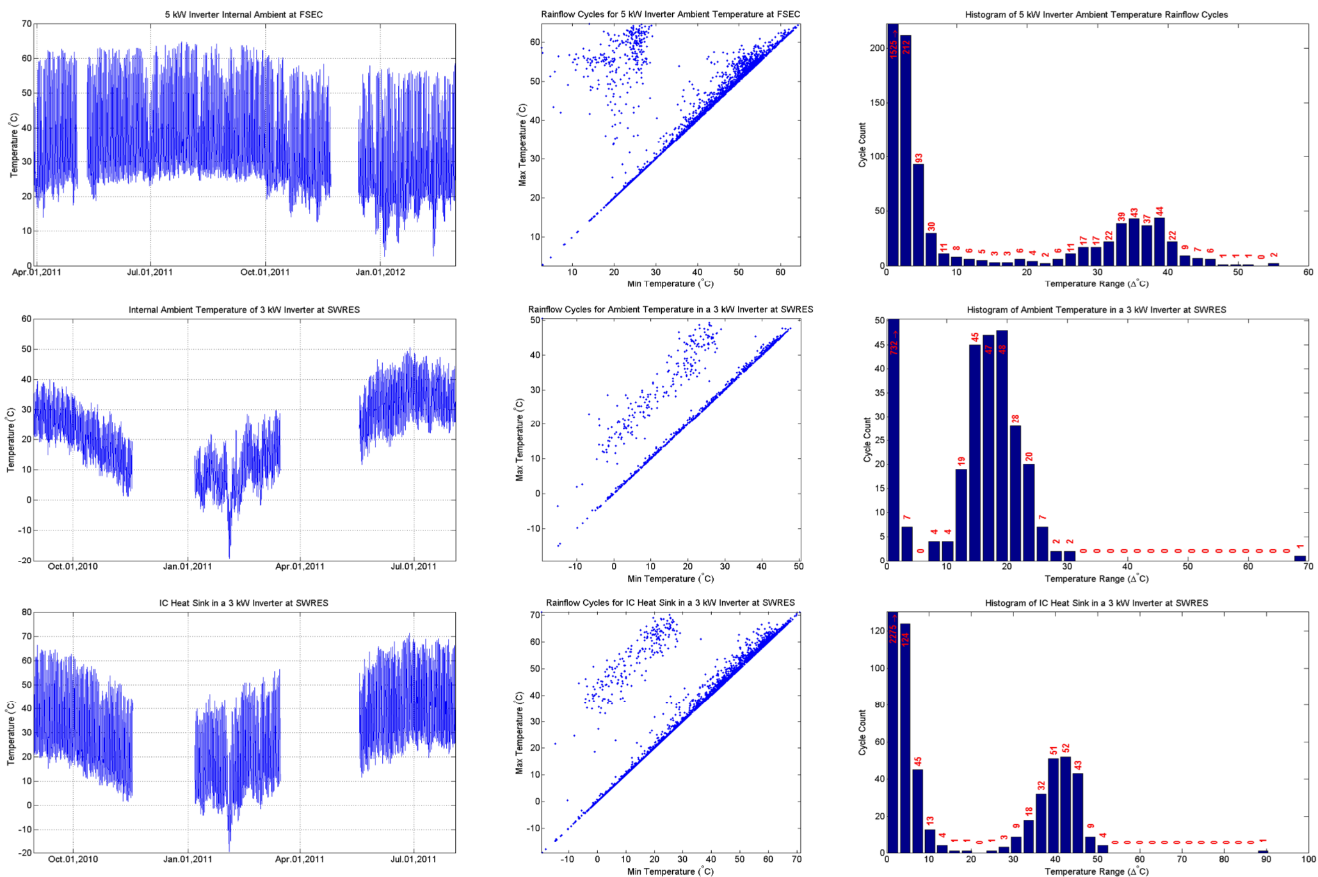


Fig. 2. Thermal histories of three locations in PV inverters, associated rainflow matrices, and resulting histograms of rainflow counts.

1. ambient temperature within a 5 kW inverter at the Florida Solar Energy Center (FSEC)
2. ambient temperature within a 3 kW inverter at the Southwest Region Experiment Station (SWRES) at the New Mexico State University in Las Cruces, NM.
3. integrated circuit heat sink temperature within a 3 kW inverter at SWRES (theoretical comparison only).

Due to computational limitations, the actual thermal profiles collected from instrumented inverters cannot be used as direct inputs into the FEA code. Therefore, thermal profiles were condensed using a rainflow counting algorithm [11-12]. Rainflow counting sorts the thermal profile into bins based on the temperature swings (ΔTs) that compose the overall thermal profile. The binned data were represented as histograms for various thermal cycle sizes. Like other cumulative damage theories [13], simulations with the UCPD solder model [9] assume each bin produces a specific quantity of damage, represented as a fraction of the part life. These field damage values were used to determine the number of accelerated cycles (-55 to 125°C) for three FR4 board-mounted components to represent one year of field damage. The joint with the worst predicted life in the two inverter ambient temperatures dictated the number of accelerated cycles.

Eleven TI arc-fault detection boards were cycled from -55 to 125°C to accelerate the solder failure. The parts were tested every year of equivalent damage using the self-check function in the TI firmware and after every 5 years of equivalent damage using an arc-fault generator on a PV system.

## II. MODELING SOLDER FATIGUE

The thermal profiles shown in Fig. 2 were collected in a 5 kW inverter in FL and a 3 kW inverter in NM. These profiles were used to generate the rainflow counts shown in the middle column of Fig. 2 using [14], and the counts were tallied into bins in the histograms on the right column of Fig. 2. Since the thermal histories were not full years, the cumulative damage predicted for the three Sn-Ag-Cu solder joints (parameters in [15-16]) shown in Fig. 3 were multiplied by a scaling factor to represent a full year, e.g., 365/307.7 for FSEC and 365/225.0 for SWRES. The smallest bin was removed from the simulations because it likely resulted from thermocouple noise/errors and would only provide small, elastic (non-damaging) strains within the solder. The remaining bins were combined in sets of three with cycle size determined by weighting the upper bound of the bins by the cycle count in each bin.

The simulations predicted that the ambient inverter profile at FSEC would yield an AFD life of 68 years, the ambient inverter profile at SWRES would result in 759 years in the field before failure, but if the AFD was located next to the IC heat sink it would only survive 34 years. This indicates that it is critical to locate AFD boards away from power electronics that significantly modify the local thermal environment or the lifetime of the AFD will be reduced. Failure rates for the solder joints are shown in Table 1 for the gull-wing 16-lead small outline integrated circuit (SOIC), 6-joint leaded ceramic chip carrier (LCCC) clock, and 1206 capacitor. The lifetime prediction in Table 1 is based on the crack initiation failure criteria. However, it is unlikely that crack initiation would cause the AFD to fail, so more conservative failure criteria of 50% crack propagation and 100% crack failure were also used to calculate the lifetimes.

The damage breakdown for the three different failure criteria for clock subjected to FSEC ambient temperature (the worst case ambient lifetime) is shown in Table 2. The damage per cycle, per thermal profile, and per year are calculated for each of the failure criteria for each of the bins. Then the total damage for each of those failure criteria was calculated by summing the damage from each of the bins. The equivalent number of years to failure for the fielded part and the number of cycles to failure for the accelerated part (both calculated with the FEA program) were then used to determine the equivalent accelerated cycles that produced one year of damage in the inverter. Based on the thermomechanical solder fatigue model, 1.25 cycles of -55 to 125°C are equivalent to one year of damage if crack initiation produces a failure, while 1.51 accelerated cycles is one year of damage if 50% solder cracking produces a failure, and 2.90 accelerated cycles is one year of damage if the crack must fully propagate through the solder joint. In all cases, the solder joint is expected to survive beyond the life of the inverter and not cause the arc-fault detector to fail. In the analysis, the 100% crack propagation failure criterion is used because it is the most conservative (requiring the most ALT cycles to reach the lifetime of the inverter) and realistic failure (electrical conductivity must be broken for the AFD to stop functioning) criteria for the boards.

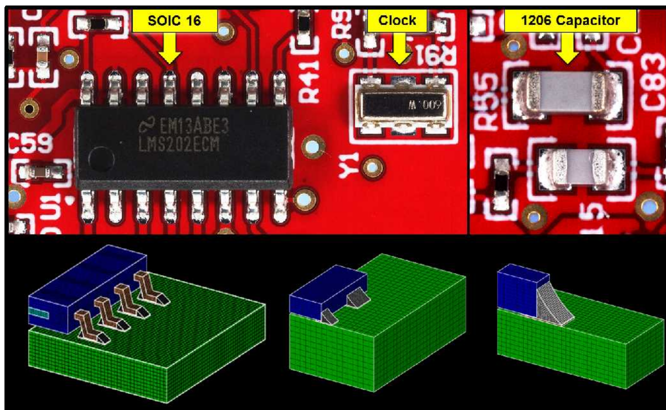


Fig. 3. Solder joints of interest: gull-wing 16-lead SOIC, LCCC clock with six joints, and 1206 capacitor, ¼ section FEA models.

TABLE 1.
FEA damage and lifetime prediction using crack initiation as the failure criterion for each solder connection.

| *Inverter Thermal Profile* | *Component* | *Damage/yr* | *Lifetime (yrs)* |
|---|---|---|---|
| FSEC Ambient | SOIC 16 | 0.000170 % | 587,000 |
| | Clock | 1.462 % | 68 |
| | 1206 Cap | 0.204 % | 490 |
| SWRES Ambient | SOIC 16 | 0.000016 % | 6,120,000 |
| | Clock | 0.132 % | 759 |
| | 1206 Cap | 0.015 % | 6,530 |
| SWRES IC Heat Sink | SOIC 16 | 0.000356 % | 281,000 |
| | Clock | 2.923 % | 34 |
| | 1206 Cap | 0.414 % | 242 |

## III. EXPERIMENTAL RESULTS

All 10 of the AFD boards were exposed to 225 accelerated thermal cycles (Figure 4). After every five cycles, the boards were tested using the internal diagnostic self test function on the PWBs using the RS232 serial communication port. The diagnostic self test injects a noise signal into the frontend of the AFD circuitry to verify the filter, analog to digital conversion, and digital processing are functioning correctly. The only component that is not included in the diagnostic self test is the CT, but, nearly all component and solder failures that the AFDs experience will be detected with the self test.

After 45 cycles (15.5 years of equivalent solder damage), physical arc-fault tests were conducted at the Distributed Energy Technologies Laboratory (DETL) at SNL. These tests verified the arc-fault detector sensitivity remained sufficient for detecting small PV arc-faults on the order of ~100 W. The test configuration is shown in Figure 5.

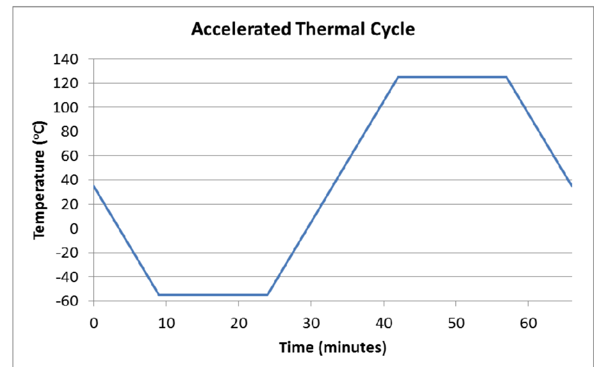


Fig. 4. 66 minute accelerated thermal cycle profile with 15 minute soak times, as per JEDEC Standard No. 22-A104D.

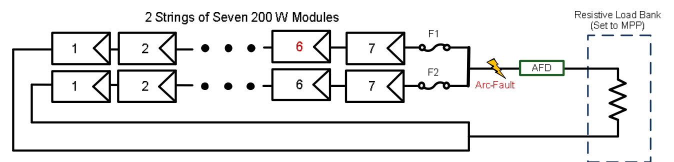


Fig. 5. Arc-fault testing setup using a load bank and a PV array of 14 modules.

The diagnostic self test and arc-fault test results for each of the boards is shown in Table 3. There were three component infant mortalities present in boards 5, 6, and 8 before reaching 45 cycles. It is unknown at this time as to which component caused the failure of the boards, but not the same component failed on each unit because it was observed that, when the boards were powered up, different sets of LEDs were illuminated. In all the failed boards, visual inspection of the solder joints was performed and all solder joints were in excellent condition. There were no indications of catastrophic failures of the interconnections. Unfortunately, the equivalent damage of the boards was calculated for the solder fatigue failure mode but not for the components failures experienced in the accelerated life tests. As a result, it is not possible to correlate the number of thermal cycles to the lifetime of the part in the field. However, the tests have identified weak components in the design that could be culled with a burn-in process. The prototypes did not experience a burn-in to eliminate infant mortalities, but the manufacturer is considering this in the future because of the severity of the service environment (nearly a "military application") versus conditions of typical consumer electronics. The failed AFD boards were sent back to the manufacturer for a more detailed analysis of the component failures.

It is important to note that the diagnostic self-test will be capable of correctly identifying the failed component in all the failures. This function could be invoked during inverter startup to verify the AFD circuitry is functioning correctly and catch the failures that were experienced in these thermal cycling tests. If the inverter does not receive a positive test result, it could alert the system owner to the problem with an alarm and not export energy until corrected.

## IV. CONCLUSIONS

The *National Electrical Code* requires arc-fault protection on PV systems in order to prevent electrical fires. Many companies are creating arc-fault detectors and circuit interrupters to meet this requirement; however, few are performing accelerated lifetime tests or accelerated stress tests on the devices. Sandia National Laboratories, in collaboration with Texas Instruments, calculated the thermal loading on inverter-integrated AFD components using the rainflow counting algorithm. This thermal profile was used to perform finite element analysis of the solder connections of three components: a SOIC, LCCC clock, and 1206 capacitor. The lifetime of the parts was calculated for three different failure criteria based on the crack propagation through the solder joint. Using the number of accelerated cycles (-55 to 125°C) to failure, the accelerated life test failures were used to predict lifetimes of the arc-fault detectors (AFDs) in the inverter if the failure mode of the boards was solder fatigue. Unfortunately, after the 225 accelerated cycles there were no failures from solder fatigue. Rather, there were infant mortality failures of several components; the lifetimes of those parts had not been determined as part of this study. However, the testing revealed an infant mortality issue with some of the components used on the AFD board and burn-in could be used to identify poorly functioning components due to the harsh service environments. Further, the diagnostic self testing functionality of the AFD was found to accurately determine when the boards had experienced a failure.

## ACKNOWLEDGEMENT

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## REFERENCES

[1] National Electrical Code, 2011 Edition, NFPA70, National Fire Protection Association, Quincy, MA.

[2] J. Johnson, M. Montoya, S. McCalmont, G. Katzir, F. Fuks, J. Earle, A. Fresquez, S. Gonzalez, and J. Granata, "Differentiating series and parallel photovoltaic arc-faults,"38th IEEE PVSC, Austin, TX, 4 June, 2012.

[3] J. Johnson, B. Pahl, C.J. Luebke, T. Pier, T. Miller, J. Strauch, S. Kuszmaul and W. Bower, "Photovoltaic DC arc fault detector testing at Sandia National Laboratories," 37th IEEE PVSC, Seattle, WA, 19-24 June 2011.

[4] J. Johnson, C. Oberhauser, M. Montoya, A. Fresquez, S. Gonzalez, and A. Patel, "Crosstalk nuisance trip testing of photovoltaic DC arc-fault detectors," 38th IEEE PVSC, Austin, TX, 5 June, 2012.

[5] Texas Instruments, AN-2154 RD-195 DC Arc Detection Evaluation Board Documentation, Dec. 2012, Accessed: 24 Jan, 2012, URL: http://www.ti.com/lit/ug/snoa564f/snoa564f.pdf.

[6] J.C. Suhling, et. al, "Thermal cycling reliability of lead free solders for automotive applications," Thermal and Thermomechanical Phenomena in Electronic Systems, ITHERM '04, Vol. 2, pp. 350- 357, 1-4 June 2004.

[7] Arc-Fault Circuit Interrupt Module Highly Accelerated Life Test Report, Reliant Labs H.A.L.T. Report Number 2202-A (private communication).

[8] M. Neilsen, P. Vianco, A. Kilgo, and E. Holm, "A Capability to Model Crack Initiation and Growth in Solder Joints," Proc. ASME IPACK2009, IPACK2009-89230, San Francisco, CA, 2009.

[9] M. Neilsen and P. Vianco, Unified Creep Plasticity Damage (UCPD) Model for Solder, ASME IMECE, Denver, IMECE2011-65387, Nov. 11-17, 2011.

[10] N.R. Sorensen, E. Thomas, M.A. Quintana, S. Barkaszi, A. Rosenthal, Z. Zhang and S. Kurtz, "Thermal Study of Inverter Components," 38th IEEE PVSC, Austin, TX, 5-8 June, 2012.

[11] M. Matsuishi and T. Endo, Fatigue of metals subjected to varying stress, Japan Soc. Mech. Engineering, 1968.

[12] S. D. Downing and D.F. Socie, Simple rainflow counting algorithms, International Journal of Fatigue, Vol. 4, No. 1, Jan, 31-40, 1982.

[13] W. Hwang and K.S. Han, Cumulative Damage Models and Multi-Stress Fatigue Life Prediction, Journal of Composite Materials, Vol. 20, No. 2, pp. 125-153, Mar. 1986.

[14] P.A. Brodtkorb, P. Johannesson, G. Lindgren, I. Rychlik, J. Rydén and E. Sjö, "WAFO - a Matlab toolbox for analysis of random waves and loads". Proceedings of the 10th International Offshore and Polar Engineering Conference, Seattle, Vol III, pp. 343-350, 2000.

[15] P. Vianco, J. Rejent, and A. Kilgo, "Creep Behavior of the Ternary 95.5Sn-3.9Ag-0.6Cu Solder: Part I – As-Cast Condition," Journal of Electronic Materials, Vol. 33, pp. 1389 – 1400, 2004.

[16] P. Vianco, J. Rejent, and A. Kilgo, "Creep Behavior of the Ternary 95.5Sn-3.9Ag-0.6Cu Solder: Part II – Aged Condition," Journal of Electronic Materials, Vol. 33, pp. 1473 – 1484, 2004.

## TABLE 2
### DAMAGE BREAKDOWN BY RAINFLOW CYCLES FOR THE AFD CLOCK IN THE FSEC INVERTER.

| | | *Crack Initiation Failure Criterion* | | | *50% Solder Crack Failure Criterion* | | | *Complete Crack (Open) Failure Criterion* | | |
|---|---|---|---|---|---|---|---|---|---|---|
| *Bin (ΔT)* | *Count* | *Damage per cycle* | *Damage per history* | *Damage per year* | *Damage per cycle* | *Damage per history* | *Damage per year* | *Damage per cycle* | *Damage per history* | *Damage per year* |
| 4.482 | 335 | 5.52E-12% | 1.85E-09% | 2.19E-09% | 2.08E-13% | 6.98E-11% | 8.28E-11% | 1.04E-13% | 3.49E-11% | 4.14E-11% |
| 10.580 | 25 | 2.10E-06% | 0.00005% | 0.00006% | 1.04E-07% | 2.60E-06% | 3.09E-06% | 5.21E-08% | 1.30E-06% | 1.55E-06% |
| 16.086 | 11 | 0.00005% | 0.00056% | 0.00066% | 4.65E-06% | 0.00005% | 0.00006% | 2.15E-06% | 0.00002% | 0.00003% |
| 21.282 | 12 | 0.00028% | 0.00337% | 0.00400% | 0.00003% | 0.00036% | 0.00043% | 0.00001% | 0.00016% | 0.00020% |
| 27.953 | 34 | 0.00088% | 0.03002% | 0.03561% | 0.00011% | 0.00389% | 0.00461% | 0.00005% | 0.00177% | 0.00210% |
| 33.350 | 78 | 0.00216% | 0.16811% | 0.19942% | 0.00028% | 0.02167% | 0.02572% | 0.00013% | 0.01016% | 0.01206% |
| 38.323 | 124 | 0.00438% | 0.54338% | 0.64457% | 0.00062% | 0.07654% | 0.09086% | 0.00026% | 0.03280% | 0.03894% |
| 43.061 | 38 | 0.00811% | 0.30807% | 0.36544% | 0.00115% | 0.04368% | 0.05185% | 0.00047% | 0.01784% | 0.02118% |
| 48.113 | 8 | 0.01393% | 0.11147% | 0.13223% | 0.00185% | 0.01481% | 0.01759% | 0.00074% | 0.00588% | 0.00698% |
| 55.334 | 3 | 0.02258% | 0.06773% | 0.08035% | 0.00278% | 0.00833% | 0.00989% | 0.00106% | 0.00319% | 0.00379% |
| **Total** | 668 | 0.05237% | 1.23277% | 1.46233% | 0.00682% | 0.16934% | 0.20101% | 0.00273% | 0.07183% | 0.08527% |
| **Years to Failure in Field** | | 68.4 | | | 497.5 | | | 1173 | | |
| Damage per -55 to 125°C Cycle | | 1.1700% | | | 0.13333% | | | 0.02941% | | |
| Accelerated Cycles to Failure | | 85.5 | | | 750 | | | 3400 | | |
| **Accelerated Cycles per 1 Year in Field** | | 1.25 | | | 1.51 | | | 2.90 | | |

## TABLE 3
### PASS/FAIL RESULTS FROM THE DIAGNOSTIC SELF TESTS (DST) AND ARC-FAULT TESTS (AFT) FOR EACH AFD PRINTED CIRCUIT BOARD.

| AFD Number | Thermal Cycles | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 0 | | 5 | 10 | 15 | 20 | 25 | 30 | 35 | 40 | 45 | | 50 | 55 | 60 | 65 | 70 | 75 | 80 | 85 | 90 | | 95 | 100 | 105 | 110 | 115 | 120 | 125 | 130 | 135 | |
| | DST | AFT | DST | DST | DST | DST | DST | DST | DST | DST | DST | AFT | DST | DST | DST | DST | DST | DST | DST | DST | DST | AFT | DST | DST | DST | DST | DST | DST | DST | DST | DST | AFT |
| 1 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P |
| 2 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P |
| 3 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P |
| 4 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P |
| 5 | P | P | F | | | | | | | | | F | | | | | | | | | | | | | | | | | | | | |
| 6 | P | P | P | P | P | P | P | P | F | | | F | | | | | | | | | | | | | | | | | | | | |
| 7 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P |
| 8 | P | P | P | F | | | | | | | | F | | | | | | | | | | | | | | | | | | | | |
| 9 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P |
| 10 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P |
| Open Failure Criterion (years) | 0.0 | | 1.7 | 3.4 | 5.2 | 6.9 | 8.6 | 10.3 | 12.1 | 13.8 | 15.5 | | 17.2 | 19.0 | 20.7 | 22.4 | 24.1 | 25.9 | 27.6 | 29.3 | 31.0 | | 32.8 | 34.5 | 36.2 | 37.9 | 39.7 | 41.4 | 43.1 | 44.8 | 46.6 | |

| AFD Number | Thermal Cycles | | | | | | | | | | | | | | | | | | | | Cycles to Failure | Years to Failure |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 140 | 145 | 150 | 155 | 160 | 165 | 170 | 175 | 180 | | 185 | 190 | 195 | 200 | 205 | 210 | 215 | 220 | 225 | | | |
| | DST | DST | DST | DST | DST | DST | DST | DST | DST | AFT | DST | DST | DST | DST | DST | DST | DST | DST | DST | AFT | | |
| 1 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | | |
| 2 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | | |
| 3 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | | |
| 4 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | | |
| 5 | | | | | | | | | | | | | | | | | | | | | 5 | N/A |
| 6 | | | | | | | | | | | | | | | | | | | | | 35 | N/A |
| 7 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | | |
| 8 | | | | | | | | | | | | | | | | | | | | | 10 | N/A |
| 9 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | | |
| 10 | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | P | | |
| Open Failure Criterion (years) | 48.3 | 50.0 | 51.7 | 53.4 | 55.2 | 56.9 | 58.6 | 60.3 | 62.1 | | 63.8 | 65.5 | 67.2 | 69.0 | 70.7 | 72.4 | 74.1 | 75.9 | 77.6 | | | |