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Reduction of Distribution Feeders for Simplified PV Impact Studies

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***Abstract* — With increasing connections of distributed rooftop PV to the distribution system, a method for simplifying the complex system to an equivalent representation of the feeder is useful to streamline the interconnection impact studies. This paper presents a method of reducing feeders to specified buses of interest while retaining equivalent electrical characteristics of the system. These buses of interest can be potential interconnection locations or buses where distribution engineers want to evaluate circuit performance. A methodology is presented showing equivalence of the reduction method with supporting equations and examples. Validation is performed for snapshot and time-series simulations with variable load and solar energy to demonstrate equivalent performance of the reduced circuit with the interconnection of PV.**

***Index Terms* — distributed power generation, photovoltaic systems, power distribution, power system interconnection, power system modeling, solar power generation**

I. INTRODUCTION

With increasing capacity of PV being connected on the distribution system, a method for simplifying the complexity of the distribution system to an equivalent representation will help streamline interconnection impact studies. These studies are required to examine the electrical impacts of high levels of PV deployment on a distribution system when the interconnection does not pass the screening requirements. Performing a high-resolution, time-series power flow simulation of the entire detailed distribution system model can be resource-intensive to fully quantify the electrical impacts for all PV output and load scenarios [1, 2].

A simplified equivalent circuit can retain the relevant characteristics of the distribution system while reducing the modeling effort. The simplified representation preserves any user-specified buses. All other circuit details are simplified to the minimum amount of necessary information. A good example of the potential benefits of reduction could be seen in extended high-resolution time-series simulations investigating distribution system regulator controls that take many hours to run a 1-year simulation at 1-second resolution [3].

One benefit of a simplified feeder representation is the ability to reduce the feeder complexity, improving the ease of converting the circuit from one software package to another. The simplified feeder can also provide faster and more accurate interconnection screening criteria by being reduced to a circuit with only the key parameters. If a full interconnection study is required, an equivalent representation would decrease the simulation system size while preserving accuracy, which is particularly useful for detailed, time-series analyses.

II. BACKGROUND

Many methods for circuit reduction have been published for different purposes and are often a reapplication of basic analysis techniques to calculate circuit parameters for a simpler representation [4]. One key circuit equivalencing technique that deserves special attention comes from the WECC guideline for modeling wind power plant [5-7]. WECC published a similar guideline for modeling PV systems in large-scale load flow simulations based on the wind guideline [8]. Both WECC guidelines use the same method of approximating the equivalent impedance for a single-machine representation, and it is also well established in other literature [9, 10].

The WECC equivalencing method is designed for studying the impact of DG on the bulk electric transmission system. The method does not provide any information inside the distribution system about the impact of DG. Extreme voltages on the distribution feeder will not be in the equivalent circuit, as it only includes the “average” voltages. Furthermore, much of the locational value of solar with impacts to specific parts of the feeder is lost in the equivalent circuit. Because the method assumes fixed voltage on all buses, it would probably also not work well for equivalencing large distributed PV systems connected on the secondary system of the distribution system where the voltage varies significantly at locations around the feeder.

III. LOAD BUS REDUCTION FORMULATION

To improve PV interconnection studies, a method is developed and demonstrated for load bus reduction that combines a load bus into the two adjacently connected buses, thus removing the bus from the circuit. With reduction, all bus voltages and the current going into the network remain the same. In this manner, the circuit is fully equivalent to the original circuit power flow except with fewer buses.

The load bus reduction method is based on the key assumption that all loads on the feeder are to be fixed current loads. This is an important deviation from many power flow simulations that assume constant power P/Q loads. EPRI has done research on conservation voltage reduction (CVR) that shows every 1% reduction in voltage results in an average of 0.8% reduction in real power, or a CVR=0.8% [11]. From this research, modeling loads as fixed current loads (where CVR=1%), is a valid assumption. As shown in [12], the load model selected for simulations also only has a minor impact on the results. The reduction method also assumes balanced loads, balanced wire impedance, no shunt capacitance, and no mutual coupling. Future research will further investigate the impacts of these factors in the reduction of the circuit.

The method for load bus reduction is shown for the simplest case with two line sections with impedances Z_1 and Z_2 with loads L_1, L_2, L_3 on each side of the line section shown in Fig. 1. If bus 2 is unnecessary in the equivalent circuit, it can be removed by combining L_2 into L_1 and L_3, resulting in a single line section Z_{eq} and only two loads L_{eq1} and L_{eq2}. The resulting reduced circuit has the same voltages V_1 and V_3 and the same current I_s coming into the circuit.

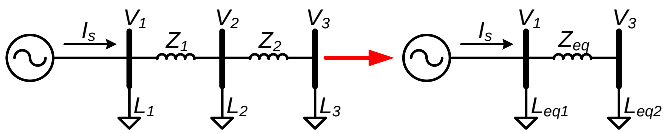

Fig. 1 Load bus reduction.

The values for the equivalent circuit are shown in (1) - (3). Note that the impedance between bus 3 and bus 1 remains the same, so all results for short circuit and protection studies are unchanged. The total circuit load is also the same with $L_{eq1} + L_{eq2} = L_1 + L_2 + L_3$.

$$Z_{eq} = Z_1 + Z_2 \tag{1}$$

$$L_{eq1} = L_1 + \frac{Z_2}{Z_1 + Z_2} L_2 \tag{2}$$

$$L_{eq2} = L_3 + \frac{Z_1}{Z_1 + Z_2} L_2 \tag{3}$$

The above process can be repeated any number of times (recursively). Any chain of loads can be reduced into two buses. If the voltage on a branch or lateral is not required in the reduced circuit, all loads on the branch can be reduced by combining the loads onto the location of the branch split from the path that contains buses of interest. If there is a bus of interest on a branch in the feeder, the branch cannot be removed in the reduced circuit otherwise the topology of the feeder would be modified in the equivalent circuit. Details and mathematical proofs shown in [12] demonstrate that the load bus reduction method is a fully equivalent circuit with the same total load, voltage drop, feeder impedance, and line losses.

IV. Example Feeder Reduction to Evaluate PV Impact

The formulation and equivalence of the circuit reduction method is applied to an example distribution feeder to demonstrate the reduction steps and math. The 15-bus feeder shown in Fig. 2a meets all the specified conditions and limitations of the method, and V_1 and V_2 are the selected buses of interest. The circuit reduction process reduces the 15-bus feeder to 4 buses. During the process, two additional buses of interest were added at the generator and at the junction between the two buses of interest to maintain the feeder topology. The voltages and currents in Fig. 2 are the results from the solved power flow in PowerWorld, demonstrating the equivalence of the reduced feeder in simulation.

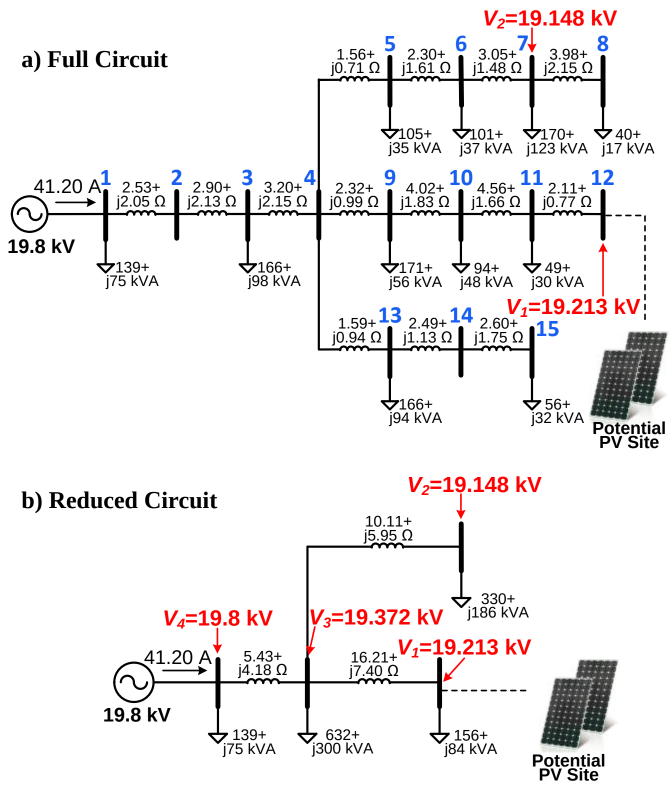

Fig. 2 Full feeder reduction. a) original 15-bus feeder, b) final, simplified circuit.

A. Reduction Steps

Step 1: User selects any specific buses that should remain in the reduced circuit. The algorithm automatically identifies additional buses of interest such as capacitors, voltage regulators, step transformers between buses of interest, and junctions required to maintain the topology in the reduced circuit. This step would identify buses 1 and 4 in Fig. 2 as additional buses of interest.

Step 2: Remove all buses without objects on them or junctions of multiple lines. This removes all lines that are at the end of a feeder without a load connected to them. It also removes all unnecessary buses that were originally only used for line routing in visualizations and calculating line lengths. This step removes buses 2 and 14 in Fig. 2.

Step 3: Reduce all loads not on the paths to buses of interest. All loads are condensed to the nearest upstream bus on a path between the substation and a bus of interest. This often moves loads from their interconnection on the end of a triplex line to the medium voltage feeder backbone. This step reduces buses 8, 13, and 15 in Fig. 2.

Step 4: Perform load bus reduction using (1)-(3) to recursively move loads to the adjacent buses. This step removes buses 3, 5, 6, 9, 10, and 11 in Fig. 2.

V. IMPLEMENTATION

In Section IV, the circuit reduction method was shown for a small 15-bus circuit so that all line parameters and load magnitudes could be displayed as an example. The main advantage of the method though is for reducing full complex distribution systems like the one shown in Fig. 3.

To apply the method to a large circuit with hundreds or thousands of components, the load bus reduction was implemented in MATLAB for full automation. The distribution system modeling is done using OpenDSS, which is an open source 3-phase distribution system simulator from EPRI [13]. The original circuit is a full distribution system model with many lines and components, including the secondary system with the service transformers and triplex lines to the loads. MATLAB communicates with OpenDSS through the COM interface to obtain the circuit parameters such as line impedances, line lengths, and load ratings. The circuit reduction is performed in MATLAB and the resulting reduced circuit is then saved back out to OpenDSS where the power flow simulations are performed for validation.

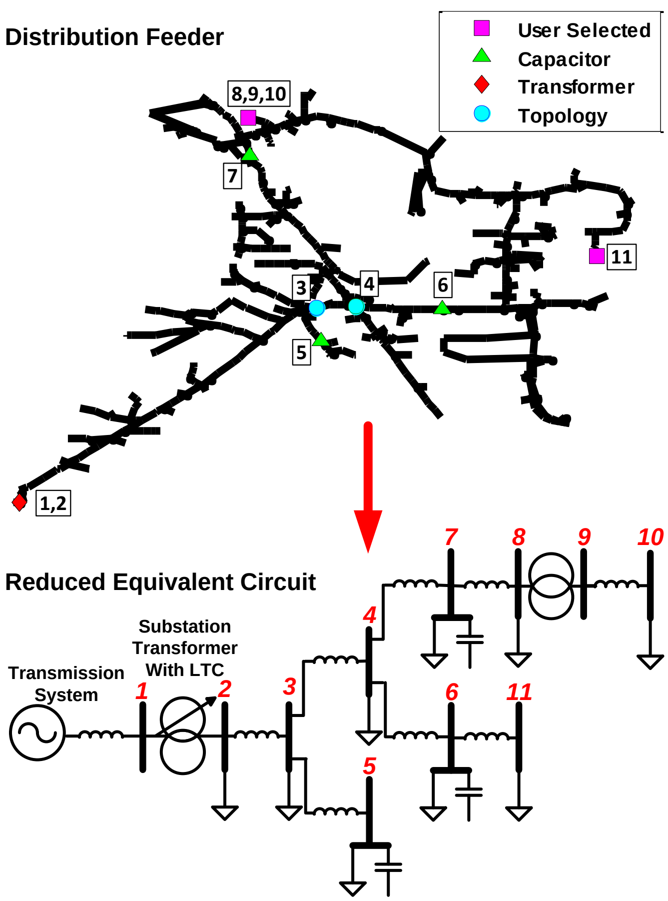

Fig. 3 A full distribution system feeder reduced to a simple equivalent representation.

A. Circuit Reduction

A distribution system with more than 1000 nodes, such as the one shown in Fig. 3, can be reduced to only a few buses. During Step 1 of the reduction process discussed in Section IV, buses 10 and 11 were selected as buses of interest. Any buses could be selected by the user, such as extreme ends of the feeder or at locations with important customers that require high power quality. All other buses in the reduced equivalent circuit are automatically identified as additional buses of interest by the reduction algorithm. Each capacitor bank (buses 5, 6, and 7) must remain in the reduced circuit as a bus of interest to correctly model the reactive power output as well as any capacitor switching. Buses 3 and 4 are identified as necessary to maintain the topology of the reduced circuit. Finally, the transformers between buses of interest (buses 1, 2, 8, and 9) must also remain in the final circuit.

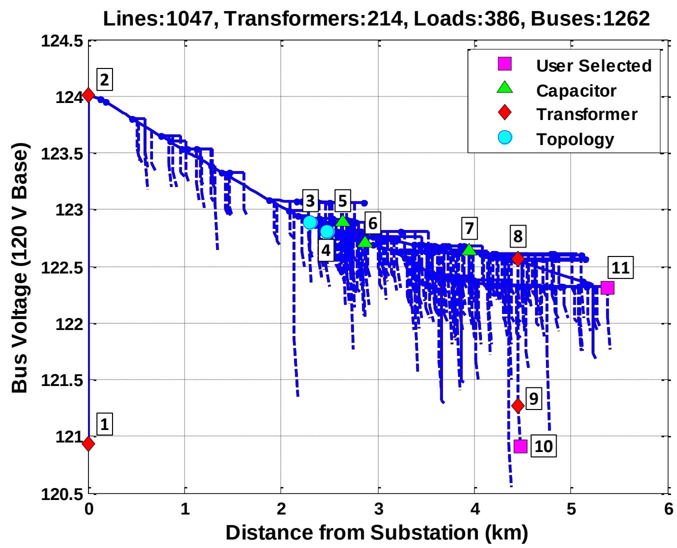

Fig. 4 Snapshot voltage profile solution for the full feeder model.

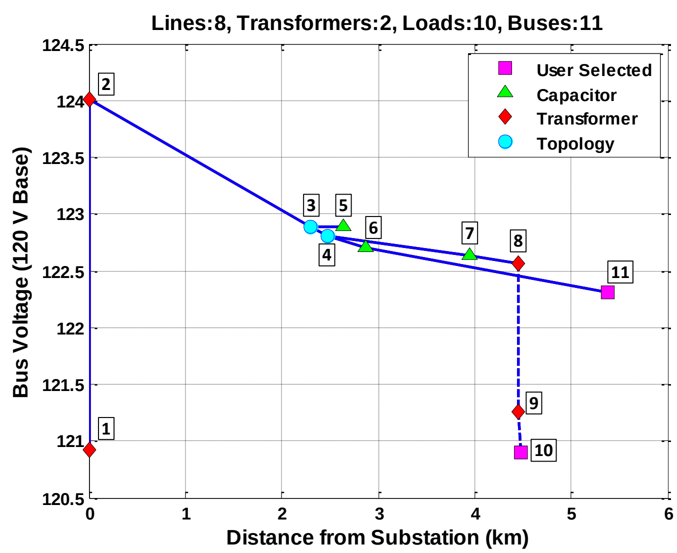

Fig. 5 Snapshot voltage profile solution for reduced circuit.

After all buses of interest have been identified, the algorithm begins to reduce the circuit. Before reduction, the distribution feeder contains 1047 lines, 214 transformers, 386 loads, and 1262 buses. After Step 2 of the reduction, the circuit contains 534 lines, 214 transformers, 386 loads, and 749 buses. After Step 3 of the reduction, the circuit contains 92 lines, 2 transformers, 88 loads, and 95 buses. After Step 4 of the reduction, the circuit contains 8 lines, 2 transformers, 10 loads, and 11 buses. As shown in Fig. 3, this extremely complex system can be reduced to a simple circuit with only a few parameters that wholly and accurately represents the currents and voltages at all buses of interest in the equivalent circuit.
Fig. 4 shows the voltage profile of the full distribution feeder model. Fig. 5 shows the voltage profile of the reduced circuit. These two figures show that during the reduction process, the complexity of the circuit is reduced considerably. However, despite this reduction, the accuracy of the voltage profile at the buses of interest remains unaffected. The reduced circuit also maintains all distances, short circuit currents, and impedances between buses of interest. During the reduction, all other complexity and bus voltages in the original circuit are lost. This is advantageous if the distribution engineer is not interested in the voltage at those thousands of other buses. If the information or characteristics of a bus are desired, it can simply be selected as a bus of interest before reduction.

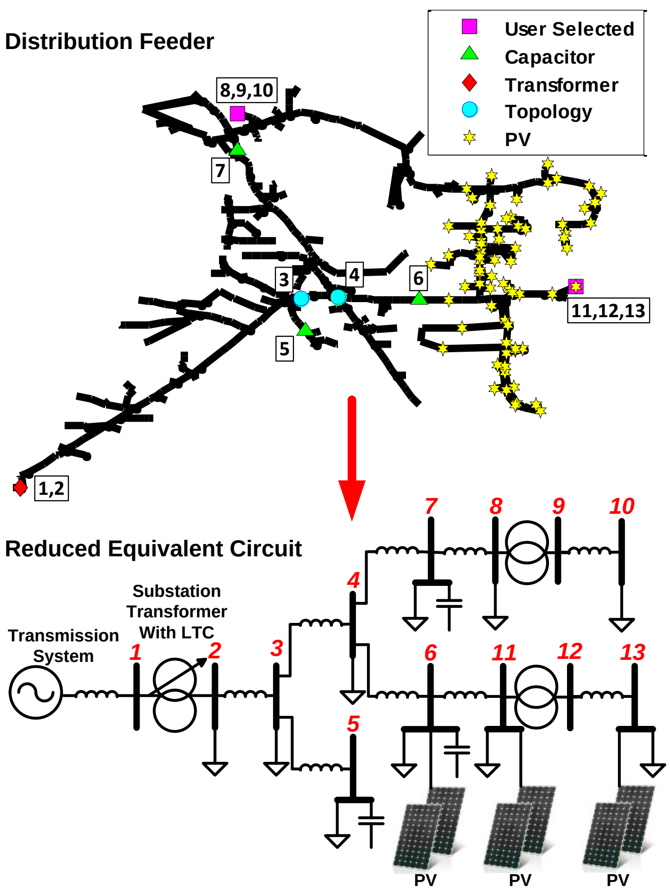

Fig. 6 A full distribution system feeder with distributed rooftop PV reduced to a simple equivalent representation.

B. Circuit Reduction with PV

Circuit reduction can be used to improve and streamline the interconnection of PV on the distribution system by speeding up the analysis process. A distribution system generally only has a few buses that are of concern for voltage and power quality due to their location in the feeder. Circuit reduction can remove feeder complexity while preserving the simulation accuracy at those buses. For example, an interconnection study could be performed for a large PV plant being connected at bus 11 in the circuit in Fig. 3.

The same circuit reduction process can be used for distributed rooftop PV. If there are a large number of PV interconnections, they can be reduced as equivalent PV plants with the same voltages at buses of interest. For example, the feeder in Fig. 6 has 70 PV interconnections that are reduced to

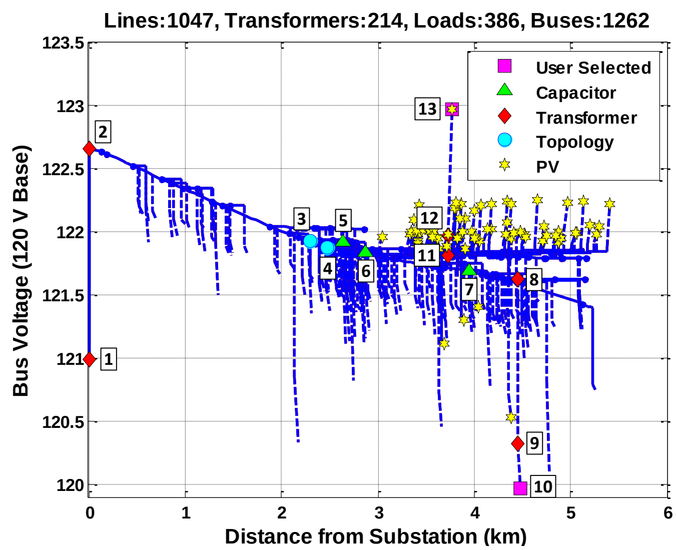

Fig. 7 Snapshot voltage profile solution for full distribution feeder with distributed rooftop PV.

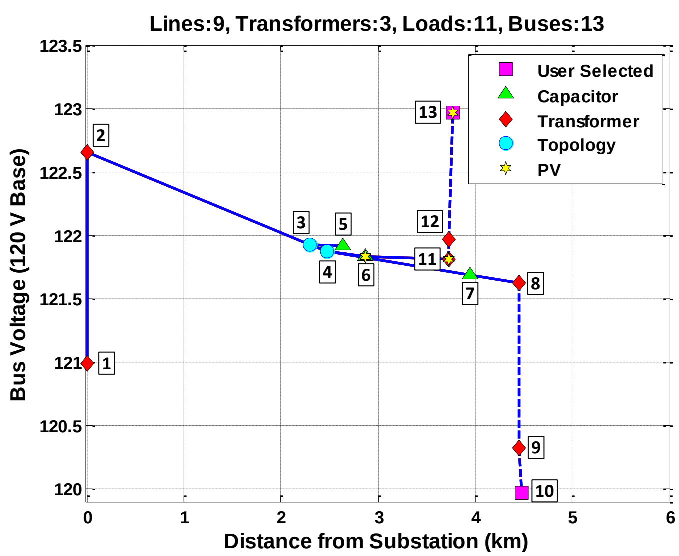

Fig. 8 Snapshot voltage profile solution for reduced equivalent circuit with distributed rooftop PV also reduced.

three equivalent PV plants with all buses of interest being equivalent in the reduced circuit. The user selected buses of interest for this analysis are bus 10, which is the same as the previous analysis, and bus 13, which is selected due to the high voltage seen in simulation with PV. The process for reducing PV plants is the same as reducing loads for Steps 3 and 4 in Section IV. The voltage profile for the full feeder model can be seen in Fig. 7 and the reduced circuit in Fig. 8 with equivalent voltages at the buses of interest.

VI. Validation

A methodology was presented for simplifying feeders to only specified buses of interest while maintaining accuracy. The method was proved to be mathematically equivalent in [12], and to numerically demonstrate the accuracy of the resulting reduced circuit in simulation, both snapshot and time-series solutions are compared for each feeder representations.

To equivalence of the reduced circuit is analyzed by comparing the voltages for the snapshot simulation shown in the voltage profile plots. The differences for the power flow solution bus voltages between Fig. 4 and Fig. 5 are shown in Table 1. The error is generally in the order of 10^{-6}. This error is likely due to small rounding differences in the reduction process, and differences of 0.000001 are small enough to be insignificant during the interconnection process. For the PV case, the differences for the bus voltage between Fig. 7 and Fig. 8 are shown in Table 2 and are of a similar magnitude.

A time series analysis was conducted as well to show the preservation of accuracy with varying load, voltage regulation equipment, and switching capacitors. A week long simulation is shown Fig. 10 for both the full circuit and the reduced circuit from Fig. 3. It is clear that the accuracy shown in the snapshot analysis is preserved when solving over time as well. Note that the LTC tap changes and capacitor switching also match between the two time-series simulations. The PV reduction case from Fig. 6 is also simulated, shown in Fig. 9, with both load and PV generation varied independently through time.

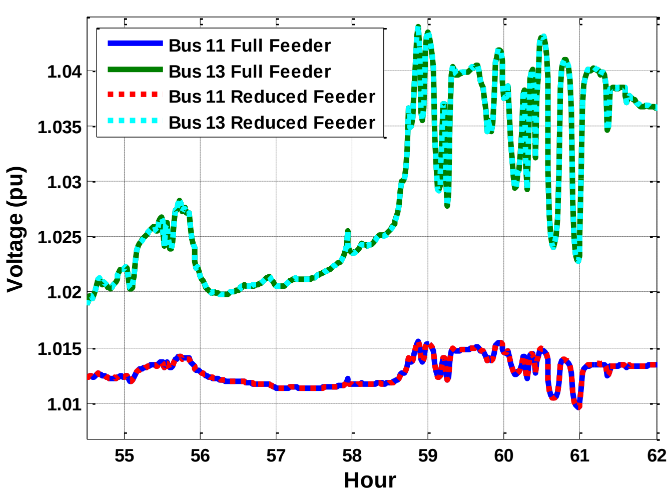

Fig. 9 Time-series analysis with distributed rooftop PV, comparison of full vs. reduced circuit for selected buses of interest.

TABLE 1
SNAPSHOT ANALYSIS OF VOLTAGES FOR BUSES OF INTEREST

Bus	Full (kV)	Reduced (kV)	Difference (pu)	Diff (120V base)
1	115.8891	115.8892	1.04E-06	1.25E-04
2	20.4616	20.4618	1.19E-05	1.43E-03
3	20.2774	20.2774	2.06E-06	2.48E-04
4	20.2640	20.2640	1.14E-06	1.37E-04
5	20.2760	20.2760	2.04E-06	2.45E-04
6	20.2468	20.2467	-3.00E-07	-3.60E-05
7	20.2341	20.2341	-3.42E-07	-4.11E-05
8	20.2238	20.2238	-4.82E-07	-5.78E-05
9	0.4851	0.4851	-4.66E-06	-5.59E-04
10	0.4836	0.4836	-5.80E-06	-6.97E-04
11	20.1820	20.1820	4.80E-07	5.76E-05

TABLE 2
VOLTAGES FOR BUSES OF INTEREST WITH PV

Bus	Full (kV)	Reduced (kV)	Difference (pu)	Diff (120V base)
1	115.9471	115.9471	-3.46E-08	-4.15E-06
2	20.2375	20.2375	-8.16E-07	-9.79E-05
3	20.1170	20.1170	7.52E-07	9.02E-05
4	20.1088	20.1088	7.49E-07	8.99E-05
5	20.1156	20.1156	7.52E-07	9.03E-05
6	20.1028	20.1028	8.96E-07	1.07E-04
7	20.0787	20.0787	3.68E-07	4.42E-05
8	20.0684	20.0684	-2.22E-06	-2.66E-04
9	0.4813	0.4813	4.28E-07	5.14E-05
10	0.4799	0.4799	4.28E-07	5.14E-05
11	20.0993	20.0993	-1.93E-06	-2.31E-04
12	0.4878	0.4878	-1.92E-06	-2.31E-04
13	0.4919	0.4919	-1.90E-06	-2.28E-04

VII. Advantages from Circuit Reduction

Circuit reduction has significant advantages in that it takes less memory and less processing time for simulations. Table 3 shows the improvements in reducing the circuit from Fig. 3. One of the most significant benefits of circuit reduction is the decreased simulation time for long high-resolution time-series simulations. For example, a one-week simulation at 1-second resolution that takes 14 minutes to run for the full distribution model performs with the same accuracy in 15 seconds for the reduced circuit.

TABLE 3
MAGNITUDE OF REDUCTION FROM FULL CIRCUIT

	Full Circuit	Reduced Circuit	% of Original
Circuit Memory (MB of RAM)	15.5	0.4	2.58%
Time (seconds) to perform a week simulation at 1-second resolution	837.94	15.48	1.85%
Circuit – Number of Lines	1047	8	0.76%
Circuit – Number of Transformers	214	2	0.93%
Circuit – Number of Loads	386	10	2.59%
Circuit – Number of Buses	1262	11	0.87%

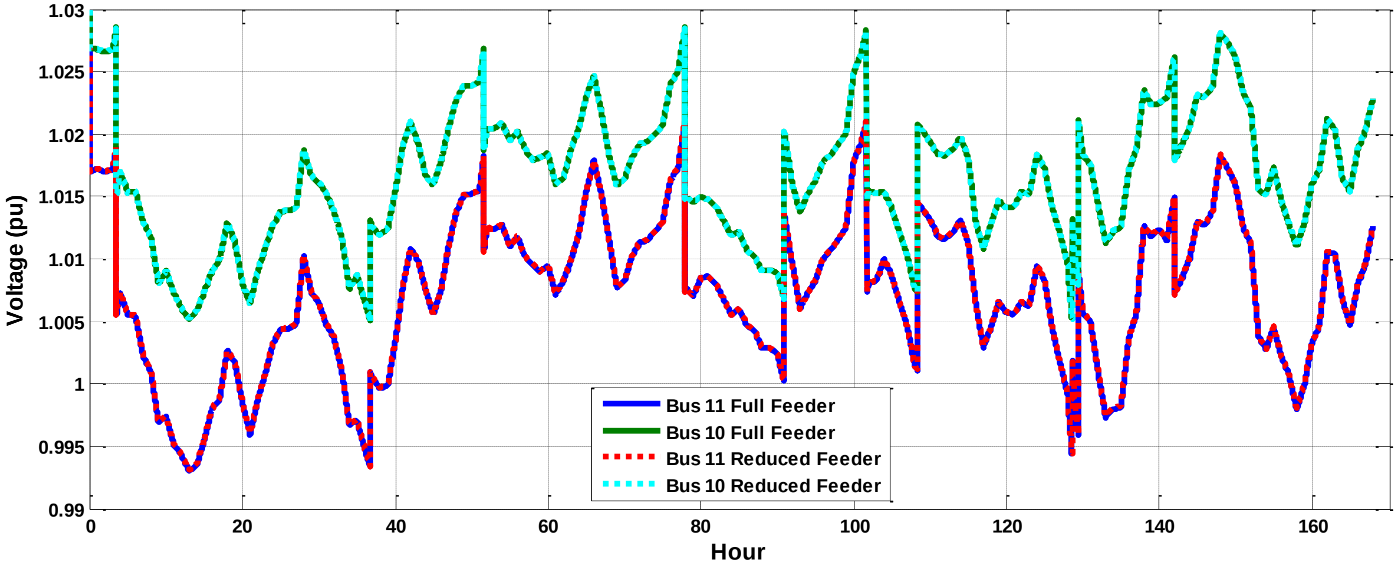

Fig. 10 Time-series comparison of full vs. reduced circuit for selected buses of interest.

The magnitude of the reduction and the number of buses in the reduced circuit depends on how many buses of interest are selected (*n*), plus some buses of interest to represent the topology of the distribution system. The final reduced circuit will contain between n and 2**n*, with no more than twice the selected buses of interest in the reduced circuit. For example, a distribution feeder with 6 capacitor banks and 4 voltage regulators would reduce to less than 20 buses, independent of the number of loads or the length of the feeder. The buses of interest are retained in the reduced circuit, maintaining equivalent performance as the full circuit, and all other circuit details are simplified to the minimum amount of necessary information.

VIII. CONCLUSIONS

A methodology was presented for simplifying feeders to only specified buses of interest while maintaining accuracy and the feeder topology. The method is demonstrated with distributed rooftop PV on a 1262-bus feeder with two buses of interest that is reduced to a 13-bus circuit. The accuracy of the method was shown for both a snapshot as well as a time series analysis with the error generally in the order of 10^{-6}. In future work this method will be expanded to include unbalanced currents in order to be able to handle more realistic distribution systems. The equivalent circuit reduction method accurately represents the full circuit for time-series simulations and was shown to be equal even with time-varying load profile and variable solar generation.

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