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Performance and Reliability Characterization of 1200 V Silicon Carbide Power MOSFETs at High Temperatures

R. J. Kaplar, D. R. Hughart, S. Atcitty, J. D. Flicker, S. DasGupta, and M. J. Marinella
Sandia National Laboratories, Albuquerque, NM, USA

Abstract

Commercially available, 1200 V SiC power MOSFETs have been characterized under bias-temperature stress conditions. Two generations of devices from a single manufacturer were tested. For the first-generation MOSFETs, both plastic- and metal-packaged devices were evaluated, whereas for the second-generation MOSFETs, only plastic-packaged devices were tested. Threshold voltage was observed to decrease with increasing temperature in the absence of gate bias stress, as expected. Drain leakage current increased with increasing temperature above the rated temperature of 125˚C for first-generation plastic-packaged parts, with the leakage ~10× higher for the plastic-packaged parts compared to the metal-packaged parts. A negative gate voltage was shown to reduce drain leakage current for the metal-packaged parts only, suggesting a parasitic leakage path associated with the plastic packaging. The threshold voltage shift ΔV_T was minimal for T < 125˚C. ΔV_T increased with increasing temperature above 125˚C, and was larger for negative gate voltage bias stress, suggesting that the oxide is more sensitive to trapping of holes than trapping of electrons. ΔV_T was insensitive to the type of package. The second-generation SiC MOSFET showed significantly less susceptibility to bias temperature stress, especially for negative gate voltage, indicating good improvement in device fabrication with respect to bias-temperature instability. Switching gate stress showed complex behavior, with a rapid initial shift in V_T followed by a much slower shift. Initial testing indicates a strong dependence on duty cycle and possible influence of self-heating due to switching loss. More detailed study of reliability under switching conditions is needed.

I. Introduction

THE low intrinsic carrier concentration and high thermal conductivity of the wide-bandgap semiconductor Silicon Carbide (SiC) make it a strong candidate for high-temperature power switching applications. In particular, the SiC power MOSFET is attractive due to the ability to thermally grow a Silicon Dioxide (SiO_2) gate oxide on SiC, similar to what is done for established Si technology. However, the small band offset between SiC and SiO_2, coupled with a high density of electrically active bulk and interface states, results in threshold voltage (V_T) instability and potentially unreliable device operation at high temperature [1]. In this work, we have characterized commercially available, 1200 V SiC MOSFETs at high temperatures. Packaging technology for high-temperature operation is critical, and as such we have evaluated devices in both plastic and metal packages. Under forward blocking conditions, first-generation parts showed minimal drain leakage current up to the rated temperature of 125˚C for plastic-packaged parts, with leakage current monotonically increasing as the temperature increased further. For temperatures exceeding 125˚C, the metal-packaged parts showed approximately ten times less leakage current compared to the plastic-packaged parts. Moreover, a negative gate voltage could be used to reduce the leakage current for the metal-packaged parts, whereas for the plastic-packaged parts the leakage current was independent of gate voltage. This suggests the presence of a parasitic leakage path in the plastic-packaged parts, unrelated to the semiconductor die. The shift in threshold voltage (ΔV_T) was evaluated as function of temperature and gate voltage, and was shown to increase monotonically with both variables. Further, ΔV_T was independent of packaging type, suggesting that this degradation mechanism is inherent to the semiconductor device. The dependence of ΔV_T on gate voltage polarity was also examined and found to be larger for negative gate bias, suggesting that hole injection may result in greater V_T instability than electron injection. The same tests were run on second-generation SiC MOSFETs from the same manufacturer, and it was observed that the V_T shift resulting from negative gate stress had significantly decreased, implying much higher robustness to hole-related damage in the gate oxide. Additionally, a second-generation part was stressed using a switching gate bias to simulate the effects of real-world operation more closely. It was observed that the rate of V_T degradation during switching gate bias stress depends strongly on the duty cycle.

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II. Experimental Details

Two generations of SiC power MOSFETs from the same manufacturer were used in these experiments. The first-generation devices were tested in both plastic and metal packages, whereas the second-generation devices were tested in plastic packages only (testing of metal-packaged second-generation devices is planned but has not yet been completed

as of the date of this writing). The MOSFET temperature rating for plastic-packaged parts is 125°C for the first-generation devices and 150°C for the second-generation devices. The temperature rating for the first generation metal-packaged parts is 225°C. Current-voltage measurements were performed using a Keithley 2651A high-current sourcemeter coupled with a Keithley 2601A for gate control. For forward blocking leakage measurements a Keithley 2410 high-voltage sourcemeter was used. First-generation parts were heated using a Corning ceramic hotplate for leakage measurements and a hot chuck for all other tests. Second-generation parts were heated using a VWR aluminum hotplate. The temperature on the hot plates was verified using a temperature probe. When heating a device, the part was allowed to stabilize at a given temperature for thirty to forty minutes, or until the gate sweep curve stopped shifting. Following gate bias stress at a given temperature, gate-sweep characterization curves were measured to ascertain changes in the MOSFET's V_T. Following this, in order to revert the device to its original condition, a gate bias of opposite polarity to the stress gate bias was applied in small time increments until the characterization gate sweep curve matched the initial gate sweep curve at that temperature. V_T is taken to be the voltage resulting in I_D = 10 mA, with the drain voltage at 100 mV. For leakage current measurements, the drain voltage was swept from 0 V to 900 V for gate biases of 0 V, -2 V, and -5 V at various temperatures.

III. Results

SiC power MOSFETs are expected to endure high voltages and currents at elevated temperatures. Two of the key metrics for evaluating their reliability at these temperatures are the threshold voltage shift ΔV_T and the drain leakage current. V_T decreases significantly for SiC MOSFETs compared to Si MOSFETs simply as a function of temperature, without considering bias stress. This is due to the higher interface trap density of the gate oxide for SiC devices, since at elevated temperature the surface potential under strong inversion is reduced along with the concentration of interface traps that must be charged or discharged to achieve that potential [2]. The first-generation devices illustrate this trend in Fig. 1. Fig. 1(a) shows gate sweep curves for plastic-packaged parts while Fig. 1(b) plots the change in temperature-dependent V_T compared to room temperature (25°C) for both plastic and metal packaged parts. This reduction in V_T is significant at elevated temperatures for leakage current, as the device may not be completely off at a gate voltage of 0 V. A negative gate voltage is recommended by the manufacturer for turning off the device. Additionally, the low V_T makes further V_T shifts with bias stress more concerning, particularly negative shifts.

A. Drain Leakage Current

Leakage current from plastic- and metal-packaged first-generation devices increases with increasing temperature, as expected. Leakage current versus drain voltage, with a gate bias of 0 V applied, is plotted for metal-packaged parts in Fig. 2(a), and for plastic-packaged parts in Fig. 2(b). Parts of both packaging types show drain current lower than 1 µA at 140°C over the entire tested range of drain voltage. Drain current for the metal-packaged parts remains below 1 µA until the temperature exceeds 200°C. Significantly, plastic-packaged parts show roughly double the leakage current of metal packaged parts at temperatures below 200°C, but above 200°C show an order of magnitude larger leakage current than the metal-packaged parts. Recall that the rated temperature of the plastic-packaged parts is 125°C, so all elevated-temperature tests were conducted in excess of the rated temperature for these devices, and our results thus indicate very robust performance below the rated temperature.

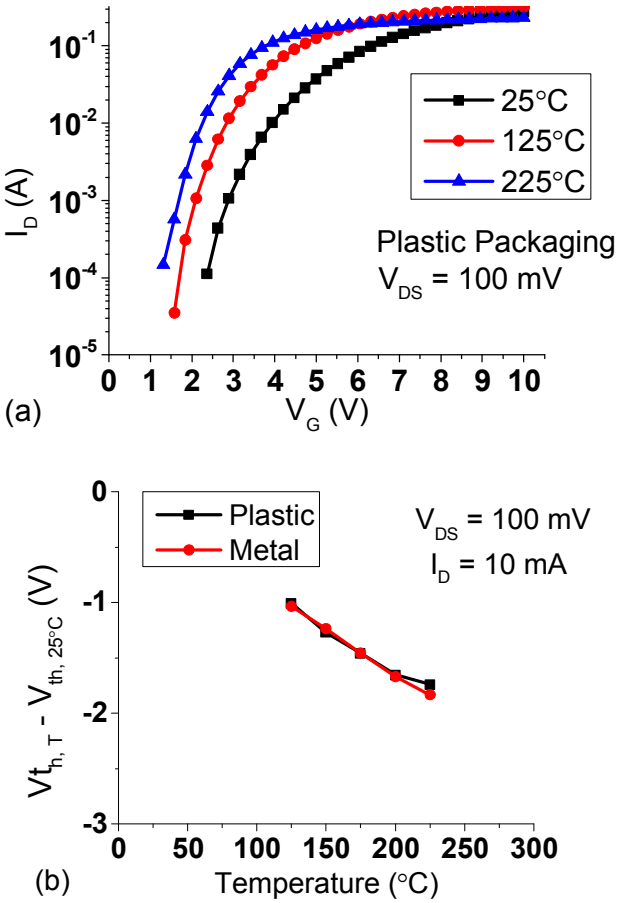

Fig. 1. (a) Drain current vs. gate voltage curves for first-generation 1200 V SiC MOSFETs in plastic packages, measured at various temperatures. (b) Difference in threshold voltage compared to 25°C for elevated temperature, for both plastic- and metal-packaged MOSFETs.

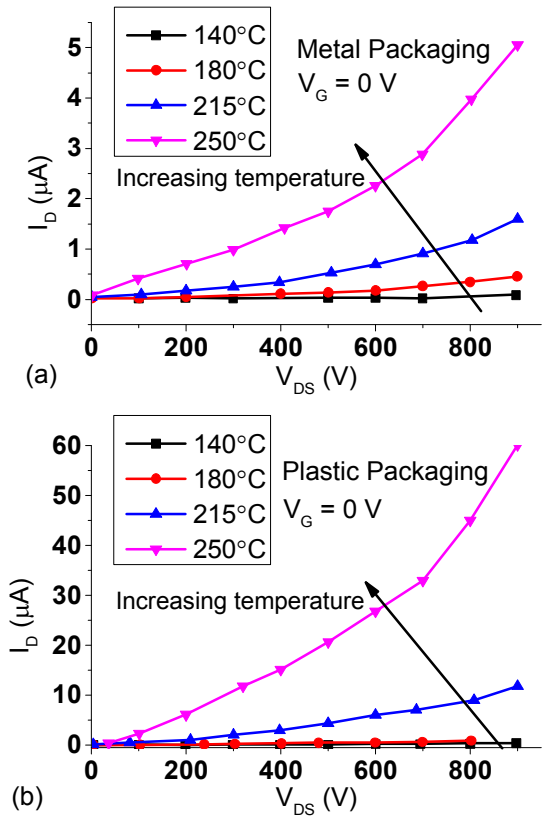

Fig. 2. Drain current vs. drain voltage in the forward-blocking state (V_G = 0 V) for first-generation 1200 V SiC MOSFETs for the indicated temperatures, shown for (a) metal-packaged parts and (b) plastic-packaged parts.

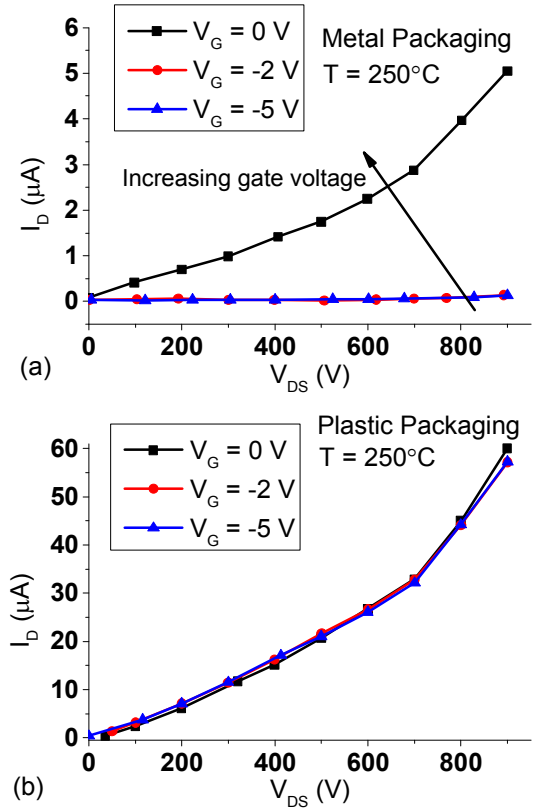

Fig. 3. Drain current vs. drain voltage in the forward-blocking state for first-generation 1200 V SiC MOSFETs at 250°C and V_G = -2 V and -5 V, for (a) metal-packaged parts and (b) plastic-packaged parts.

The reduced V_T at elevated temperature can increase the leakage current, so the leakage current was also measured using gate biases of -2 V and -5 V. Results at 250°C are plotted for metal-packaged parts in Fig. 3(a) and for plastic-packaged parts in Fig. 3(b). A gate bias of -2 V reduces the leakage current from the metal-packaged parts to less than 10 nA over the entire measured range of drain bias at a temperature of 250°C, with similar results observed for the other four temperatures measured. Conversely, there was no significant reduction in leakage current due to $V_G < 0$ for any of the four temperatures measured (representative 250°C case shown in Fig. 3(b)) for the plastic-packaged parts. This suggests that an extrinsic packaging-related mechanism dominates the leakage current for the plastic-packaged parts, and that ΔV_T is masked by this effect. Once again it is important to note that all data reported here was recorded for temperatures exceeding the rated temperature of 125°C for plastic-packaged parts.

B. Threshold Voltage Shift – Fixed Bias

Devices from both generations stressed under fixed gate bias show varying amounts of V_T shift, depending on the magnitude and polarity of the bias, as well as the temperature. Each MOSFET was stressed for 30 minutes at various temperatures and gate bias values. Fig. 4 plots V_T shift versus temperature for first-generation devices in both plastic and metal packages, for gate biases of 20 V and -20 V. The values plotted show ΔV_T relative to the initial V_T at the stress temperature, not the shift in room temperature V_T. For each type of packaging and for all temperatures, the positive V_T shift (which is likely due to electron injection from the inverted SiC channel into the oxide, Fig. 4(b)) is less severe than the negative V_T shift (which is likely due to hole injection from the accumulated p-type SiC into the oxide, Fig. 4(c)). Holes are well-known to cause significant reliability degradation in SiO_2 on Si, e.g. by changing the charge state of the oxygen vacancy (E' defect) [3], and a similar model has been proposed for SiO_2 on SiC [4]. Plastic-packaged parts may have slightly worse negative V_T shift, but the differences are small enough such that the packaging appears to have little effect on ΔV_T. At the rated temperature for plastic-packaged parts of 125°C the negative V_T shift is roughly 1 V, and monotonically increases to 4 V by 225°C. The positive V_T shift is 100 mV or lower at temperatures up to 150°C, and reaches 1 V at 225°C.

The manufacturer recommends an off-state voltage of -5 V, so the devices were also stressed using a gate bias of -5 V, with results plotted in Fig. 5. Neither packaging type shows significant degradation until the V_T for the plastic packaging shifts at 250°C, double the rated temperature of 125°C, again indicating good robustness of the gate oxide to bias and

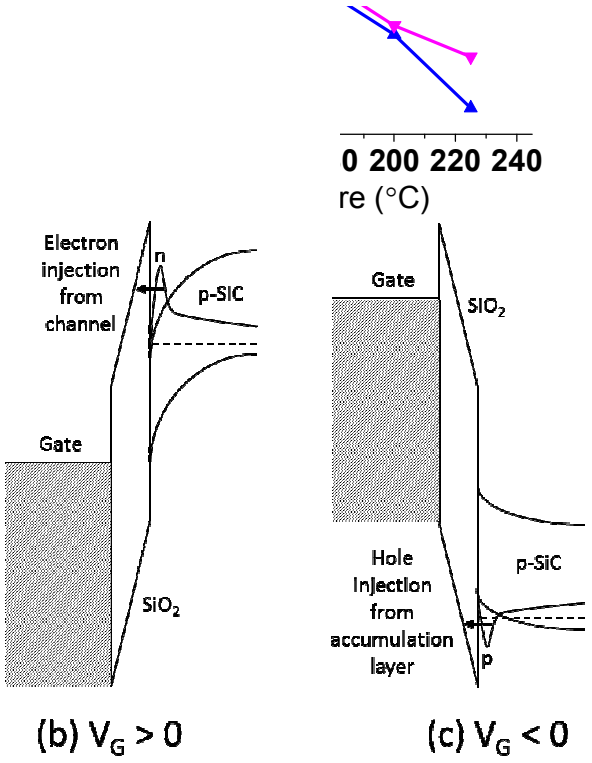

Fig. 4. (a) ΔV_T for first-generation plastic- and metal-packaged parts stressed at ±20 V as a function of temperature. Schematic band diagrams illustrating (b) electron injection for $V_G > 0$ and (c) hole injection for $V_G < 0$.

temperature stress.

Second-generation MOSFETs in plastic packages were also stressed for 30 minutes with gate biases of 20 V, -20 V, and -5 V at various temperatures. The results are plotted in Fig. 6(a) with comparisons to first-generation plastic-packaged devices in Fig. 6(b). Negative V_T shifts are significantly reduced at all temperatures tested (up to 175°C). At 175°C, the V_T shift for the second-generation devices is roughly -0.3 V after a gate bias stress of -20 V, compared to a V_T shift of -1.5 V for first-generation devices. The positive V_T shifts are small, only 100 mV at 150°C and above. The drastic reduction in ΔV_T, particularly after negative gate bias stress, indicates that the manufacturer has significantly improved the fabrication process to better enable high-temperature operation if the SiC power MOSFET.

C. *Threshold Voltage Shift – Switching Bias*

In real-world applications, the power MOSFET will have a rapidly switching gate bias applied to it. Previous data has shown that V_T shifts can be smaller when using a switching bias on the gate, even when tested for months [5]. A second-generation SiC MOSFET was tested using a switching gate bias of +20 V / -5 V at a frequency of 100 Hz and a 50% duty cycle (50% of time at +20 V, 50% of time at -5 V) at 150°C for 120 hours. After recovering the device to its initial state, it was stressed again using a 90% duty cycle (90% of time at +20 V, 10% of time at -5 V) at 150°C for 165 hours. Stress was interrupted and V_T was sampled in half-hour increments. The results are plotted in Fig. 7. For both cases, a very rapid initial drop in V_T (the first point recorded was after one-half hour of switching stress) is observed. Following this initial drop, V_T continues to shift in the negative direction, indicating that the device is more sensitive to hole injection under switching stress conditions. This is surprising for the 90% duty cycle case, since the gate is exposed to hole injection for only 10% of the time. The rapid initial drop in V_T after half an hour for 50% duty cycle is roughly 150 mV, compared to 50 mV following a constant 30-minute stress of -5 V at 150°C on another part. The increased shift under switching stress may be due to self-heating resulting from switching loss, similar to what we have reported previously [6] (the temperatures reported here are applied temperatures, and thus self-heating is not taken into account). After an initial drop and slight recovery, the V_T shift gradually increases at a rate of -2.5 mV/hr. The final V_T shift after 120 hours is approximately -370 mV. Between stresses the device was recovered using a +20 V gate bias in short time increments until the gate sweep IV curve was identical to the initial unstressed gate sweep curve. The initial rapid V_T shift after one-half hour of stress for the 90% duty cycle case was even more severe (-335 mV), although the subsequent degradation was minimal. After an initial small recovery ending after 25-30 hours (similar to the 50% duty cycle case) the negative V_T shift increases to -364 mV at 165 hours. The rate of change following the initial rapid shift is -0.26 mV/hr.

IV. Discussion and Conclusion

Fig. 5. ΔV_T plotted vs. temperature for -5 V gate bias stress on plastic- and metal-packaged first-generation SiC MOSFETs.

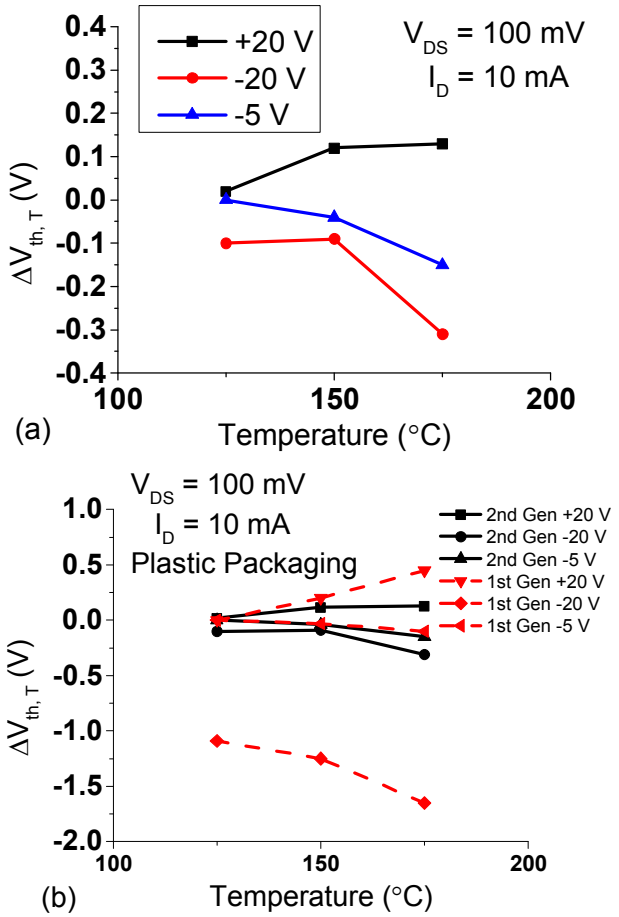

Fig. 6. (a) ΔV_T for plastic-packaged second-generation SiC MOSFETs plotted vs. stress temperature, for ±20 V and -5 V gate bias stress conditions. (b) Direct comparison of first- and second-generation plastic-packaged parts for ±20 V and -5 V V gate bias stress condition.

One of the most significant reliability concerns for SiC MOSFETs is the quality of the oxide. The high density of interface traps have historically contributed to significant shift in V_T with respect to temperature, and the reduced band offset compared to SiO_2/Si makes the oxide vulnerable to charge trapping that causes V_T to shift as a result of bias and temperature stress. However, the quality of the packaging material has also been a concern for SiC power devices [7]. Our results have shown that parts with plastic packaging have higher drain leakage currents under the forward-blocking state than do parts with metal packaging. Further, unlike the metal-packaged parts, the plastic-packaged parts do not show reduced leakage current when biased with a negative gate voltage, implying that the limiting factor is not the low V_T. Rather, the difference is likely due to the packaging material – since the leakage current appears to be independent of gate bias, there is likely an extrinsic leakage path introduced by the plastic packaging, limiting the temperature at which such parts can operate. Other parameters, like sub-threshold swing and $R_{DS(on)}$, showed no difference when measured at temperatures up to 225°C for parts with plastic and metal packaging.

Applying negative gate bias to metal-packaged parts at elevated temperature reduces the leakage current, indicating

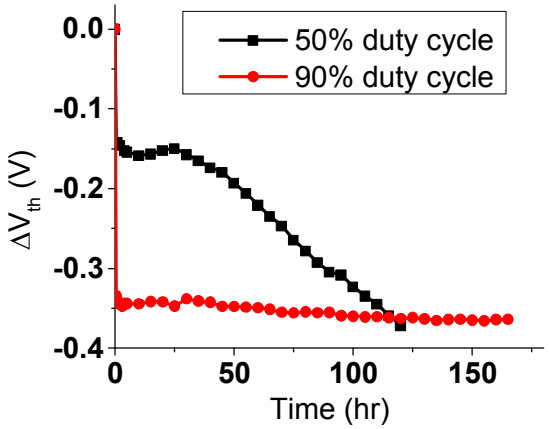

Fig. 7. ΔV_T for a second-generation SiC MOSFET subjected to 50% and 90% duty cycle, +20 V / -5 V gate switching stress at 150°C. Inset shows expanded view of first several hours of stress.

that the low V_T contributes to the high leakage current when not limited by packaging. Applying a -2 V bias significantly reduces the leakage up to 900 V drain bias at temperatures up to 250°C (Fig. 3(a)). For metal packaging, biasing the gate at -5 V has little effect on V_T shift up to at least 250°C (Fig. 5), making the use of a negative gate bias a possible solution to leakage issues.

However, switching gate bias testing indicates that using a negative gate bias can cause V_T to shift increasingly negative, suggesting that hole injection dominates electron injection. The rate of degradation appears to be related to the duty cycle, although the situation is quite complex (Fig. 7) and merits further detailed study. Significantly, even at 90% duty cycle (i.e. electron injection 90% of the time and hole injection 10% of the time), hole injection appears dominate. The V_T shift clearly exhibits a two-phase shift, with a very rapid initial shift followed by a much slower rate of shift, where the detailed nature of the degradation is again sensitive to duty cycle.

Other factors also may affect the direction and rate of degradation. A higher frequency may alter the degradation, since shorter lengths of time are spent at a given bias before switching. Using a smaller negative gate bias may cause a smaller shift in V_T, while still helping issues like leakage current (e.g. Fig. 3). The initial switching bias tests performed indicate that there may be cumulative degradation between stresses, despite the recovery of the gate sweep curve. The first stress may create additional defects that remain in the oxide, or electrons may be trapped at defects and form a dipole without recombining, and may subsequently be emitted when a negative gate bias is applied, returning the device to a state similar to the previous condition. Thus, the oxide could be in the same charge state, but contain defects that were not previously present. Such a situation has been described previously for radiation-induced defects (E' centers) in SiO_2 on Si [8]. If there are cumulative effects that are not easily annealed, this implies that the degradation suffered under worst case conditions may endure for the lifetime of the device. This is especially concerning for devices that will see a variation in parameters like duty cycle over the course of their

lifetime.

Despite these concerns, it is clear that much progress has been made in addressing the reliability of SiO_2 on SiC. Even for the first-generation MOSFETs, we had to stress them significantly above the rated operating temperature for plastic-packaged parts to induce degradation. Further, a significant improvement in gate reliability, especially under negative gate stress, was observed in second-generation MOSFETs, indicating that device manufacturers are learning how to fabricate more robust gate oxides. Understanding SiC MOSFET reliability under realistic switching conditions remains a challenging problem that warrants further investigation.

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