SAND2013-3192C

IRPS 2013

Influence of Barrier Design on Current Collapse in High Voltage AlGaN/GaN HEMTs

S. DasGupta[1], L. Biedermann[1], M. Sun[2], R. J. Kaplar[1], M. J. Marinella[1], K. R. Zavadil[1], S. Atcitty[1] and T. Palacios[2]

[1]Sandia National Laboratories, Albuquerque, NM USA,

[2]Massachusetts Institute of Technology, MA, USA

Purpose

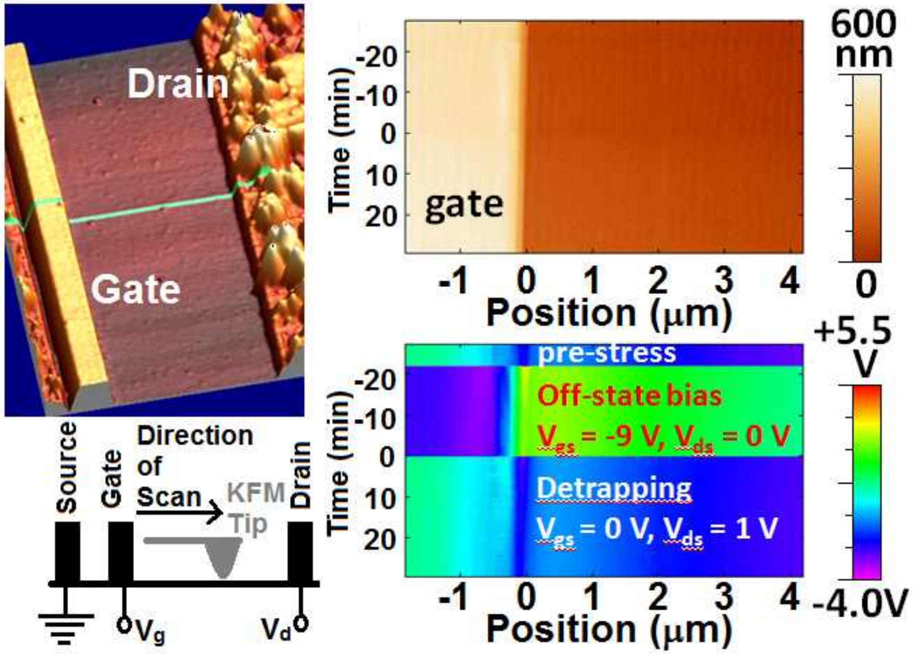
- **Considerable consensus regarding dominant defect E_a in AlGaN/GaN systems (defect with $E_a \sim 0.6$ eV)**
- **Less agreement on location of defect (GaN buffer, bulk AlGaN, AlGaN/GaN interface or AlGaN surface).**

- **What determines dominant trapping location ?**
- **Are all defects equally relevant to HEMT operation ?**

Outline

- Introduction
- Two Different Epitaxial Structures
- Current Collapse vs Surface Potential Measurements
- Determination of Charge Trapping Location from Current Collapse, Surface Potential Measurements and TCAD
- Relating Results to Design and Electric Fields during Device Operation
- Summary

Introduction: Simultaneous Surface Potential and I_d Recovery Transient Measurements



SP recovery post-stress measured using Kelvin Probe Force Microscopy (KPFM)

I_d recovery transients measured simultaneously

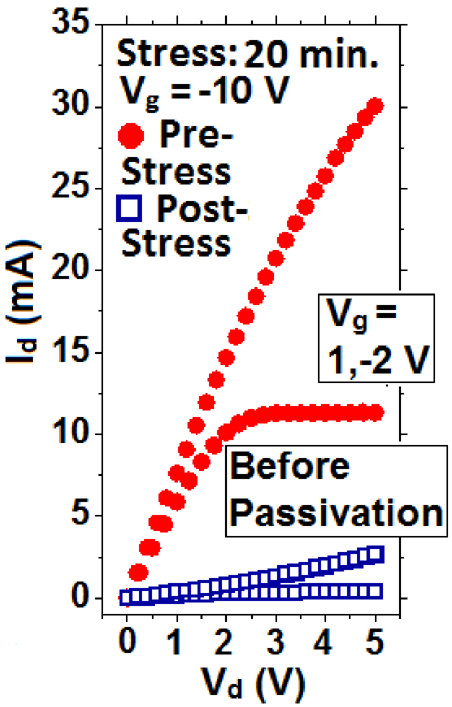
Charge trapping location evaluated using device simulations *simultaneously* satisfying SP measurements and I_d

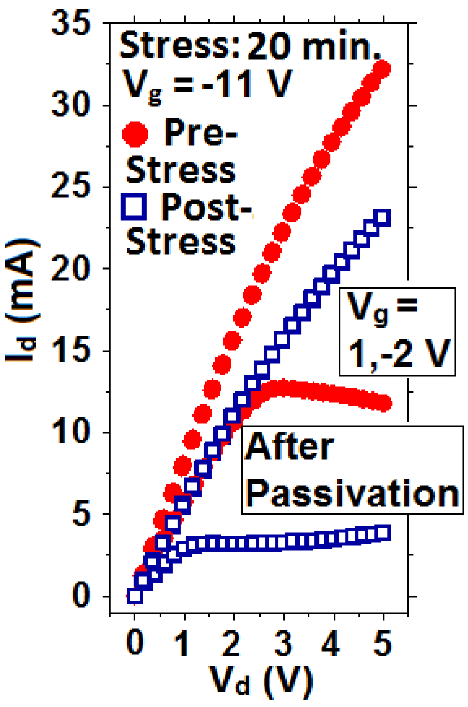
Device A vs Device B

Device type	AlGaN Barrier	GaN Buffer	Passivation
A	50 nm $Al_{0.15}Ga_{0.85}N$	Carbon doped	ALD deposited $Al_2O_3/SiO_2/Al_2O_3$
B	20 nm $Al_{0.26}Ga_{0.74}N$	Undoped	None

Device A: Expect *bulk* trapping

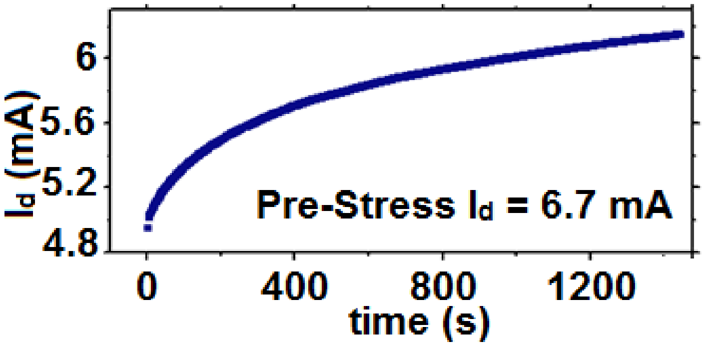
Device B: Expect *surface* trapping

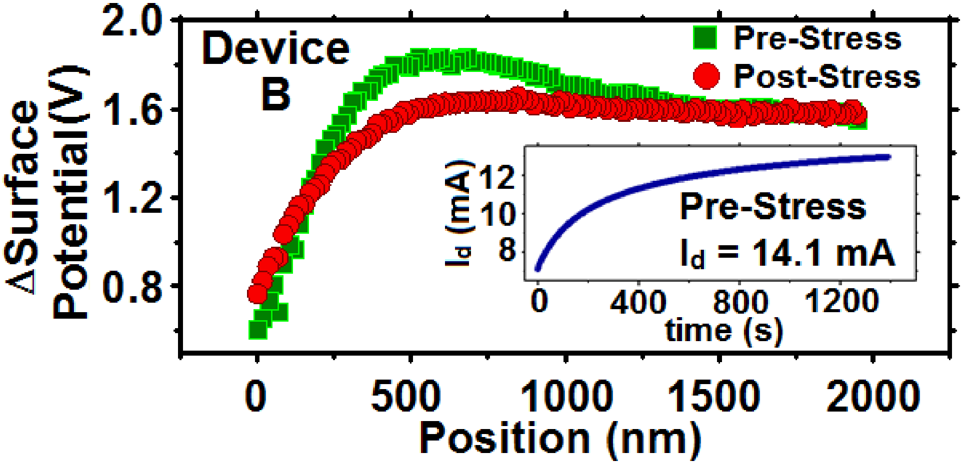


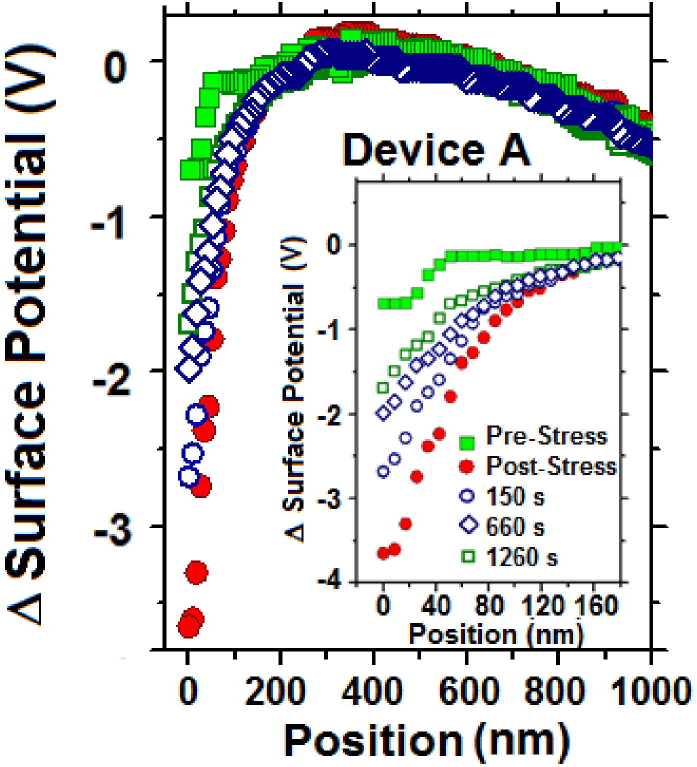


The ALD $Al_2O_3/SiO_2/Al_2O_3$ passivation stack is very effective in reducing current collapse.

Correlated I_d Collapse vs Surface Potential Shifts





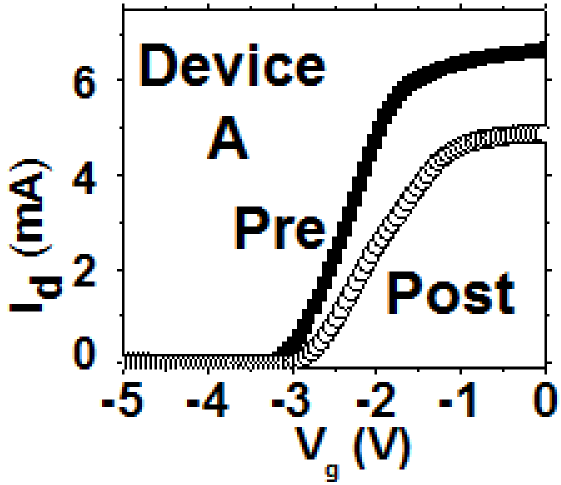


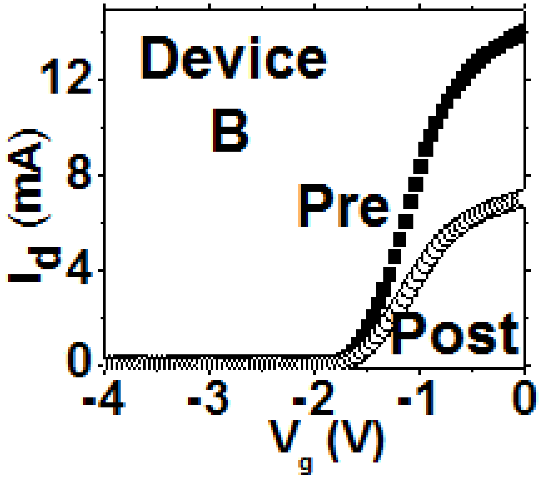
Device A: ***Large*** **change in surface potential near the gate edge**

Device B: ***Negligible*** **change in surface potential throughout the drain extension**

Results inconsistent with expectations based on buffer doping and surface passivation

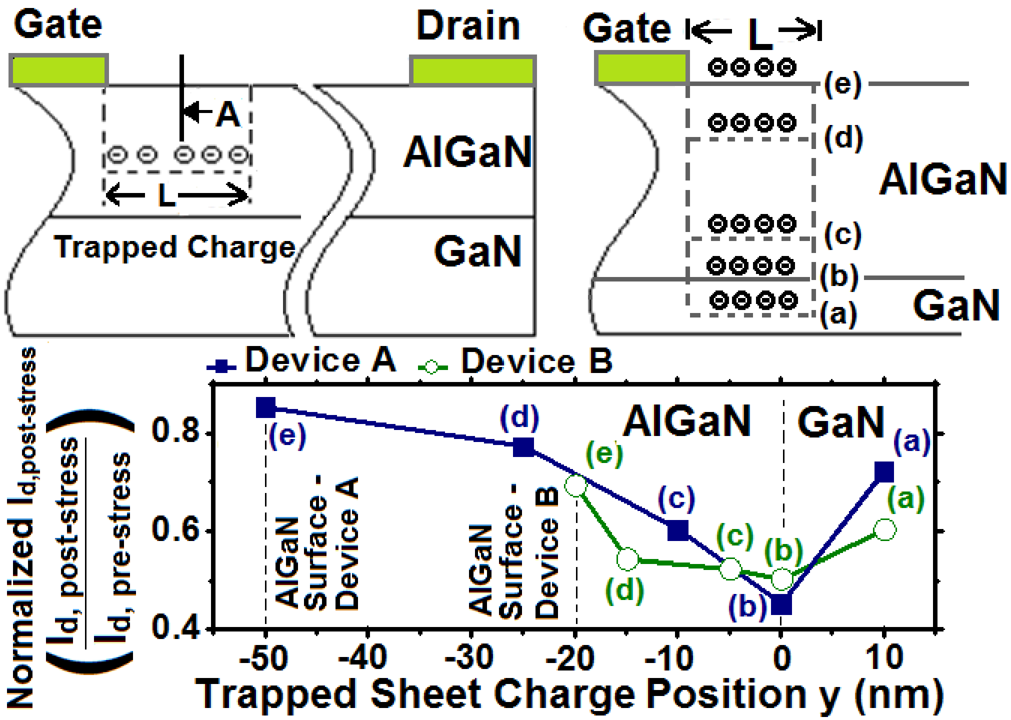
Trapping Under Gate vs. Trapping in the Access Region





- **No ΔV_{th} in Device B at all.**
- **Small ΔV_{th} of ~0.3 V in Device A.**
- **At detrapping bias (V_{ds} = 1 V, V_{gs} = 0), g_m of both devices is negligible (< 1mS/mm).**
- **For ΔV_{th} = 0.3 V, ΔI_d less than 5% of the total ΔI_d post-stress.**
- **Most of the I_d (at the bias under which detrapping transients are recorded) comes from access region trapping.**

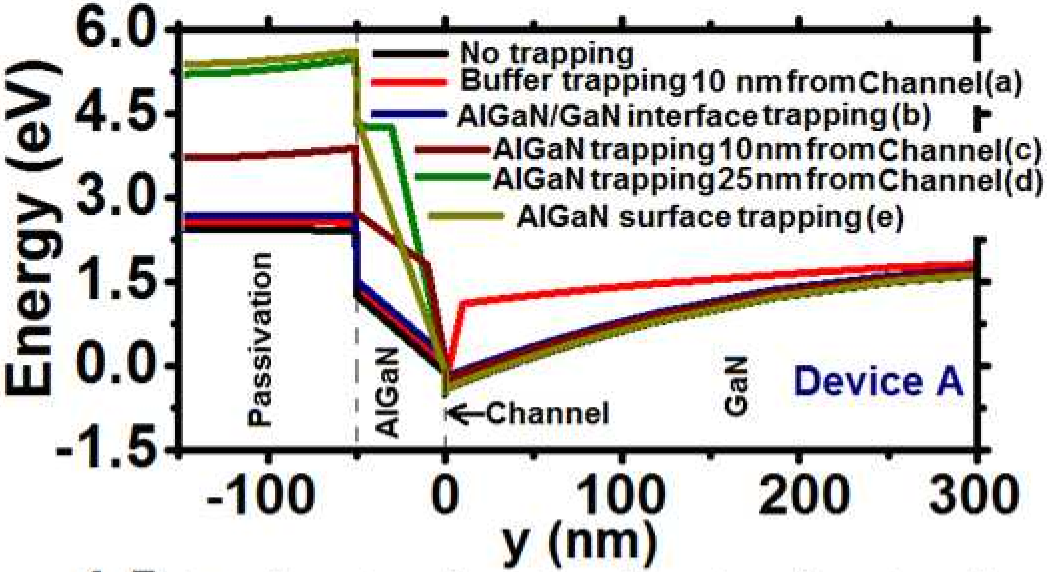
Current Collapse Simulations - I

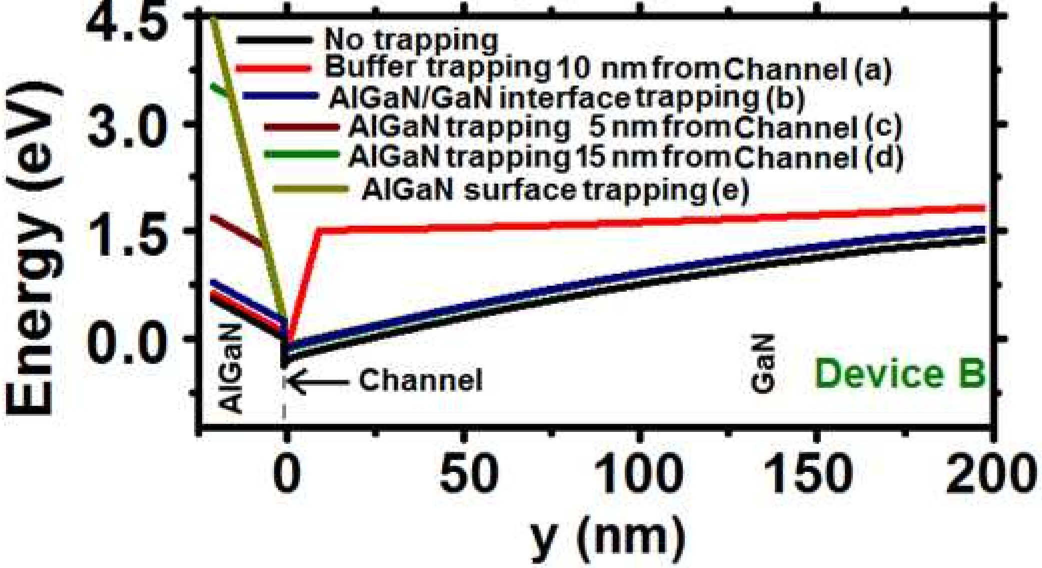


I_d **collapse simulated using sheet of charge with variable density at a) GaN bulk, b) AlGaN/GaN interface, c),d) AlGaN bulk and e) AlGaN surface.**

Closer to Channel – More *I_d* collapse

Current Collapse Simulations - II

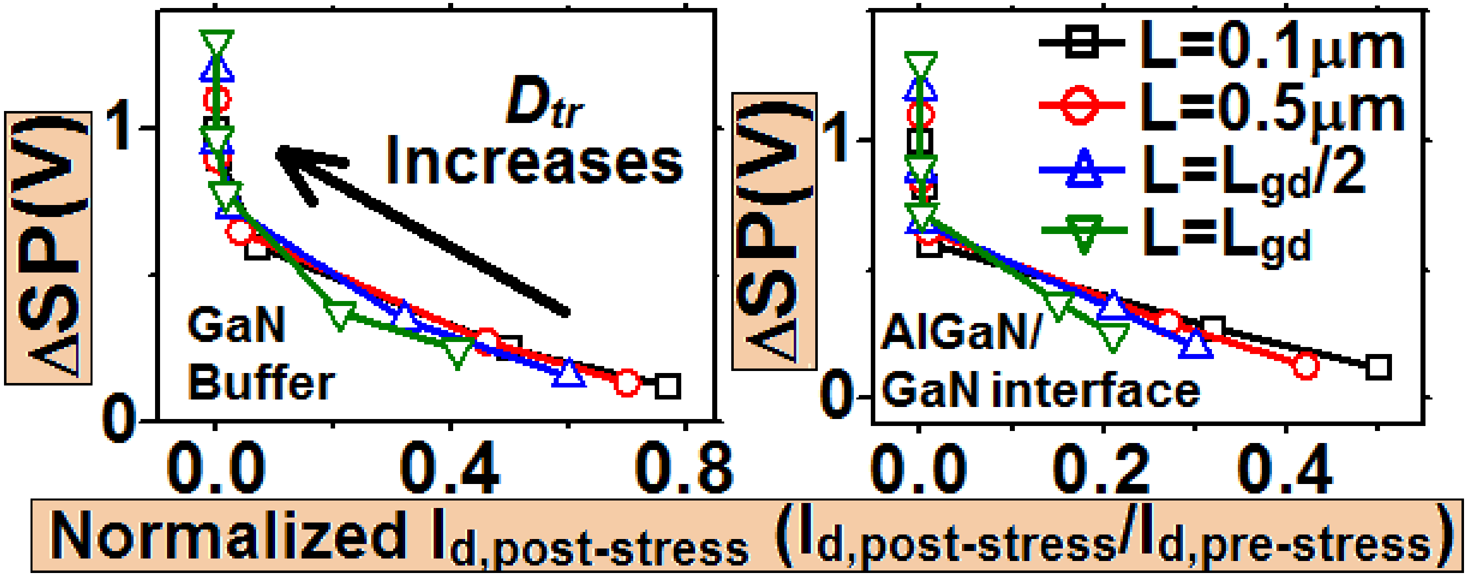




- **Closer the trapped charge to AlGaN surface, greater the change in SP, smaller the I_d collapse**

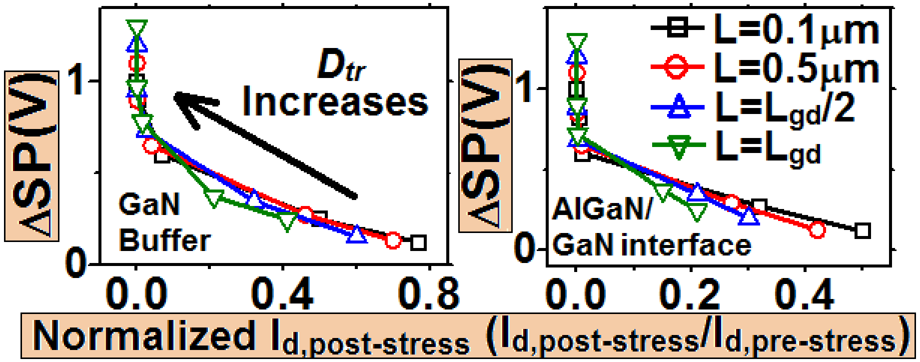
- **Conversely, charge trapping closer to AlGaN/GaN interface → I_d collapse large and change in surface potential small**

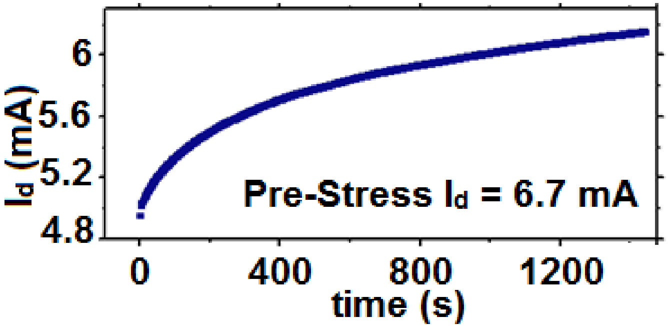
Comparison between I_d collapse and ΔSP – Device A - I



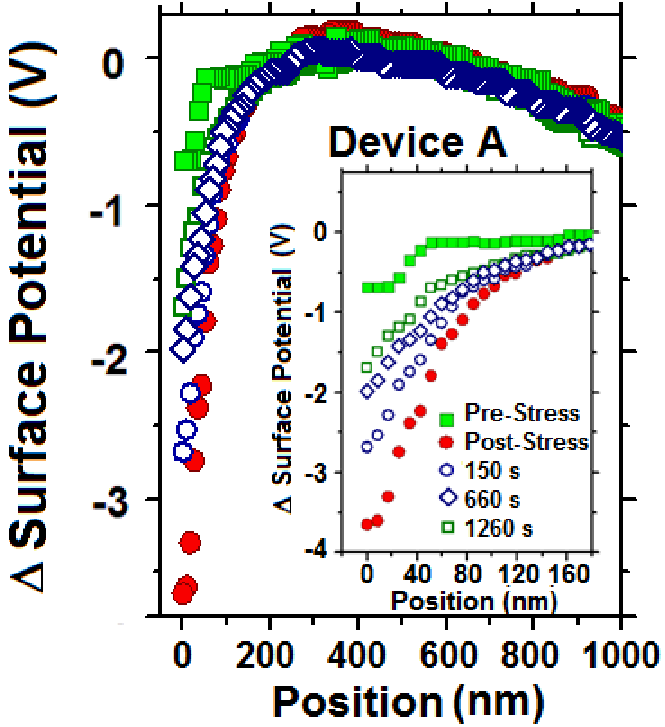
- For all cases, $I_{d,post-stress}$ completely pinched-off significantly before ΔSP > 1 V.
- Further increase in ΔSP requires higher D_{tr} (reduces I_d even further).

Comparison between I_d collapse and ΔSP – Device A - II

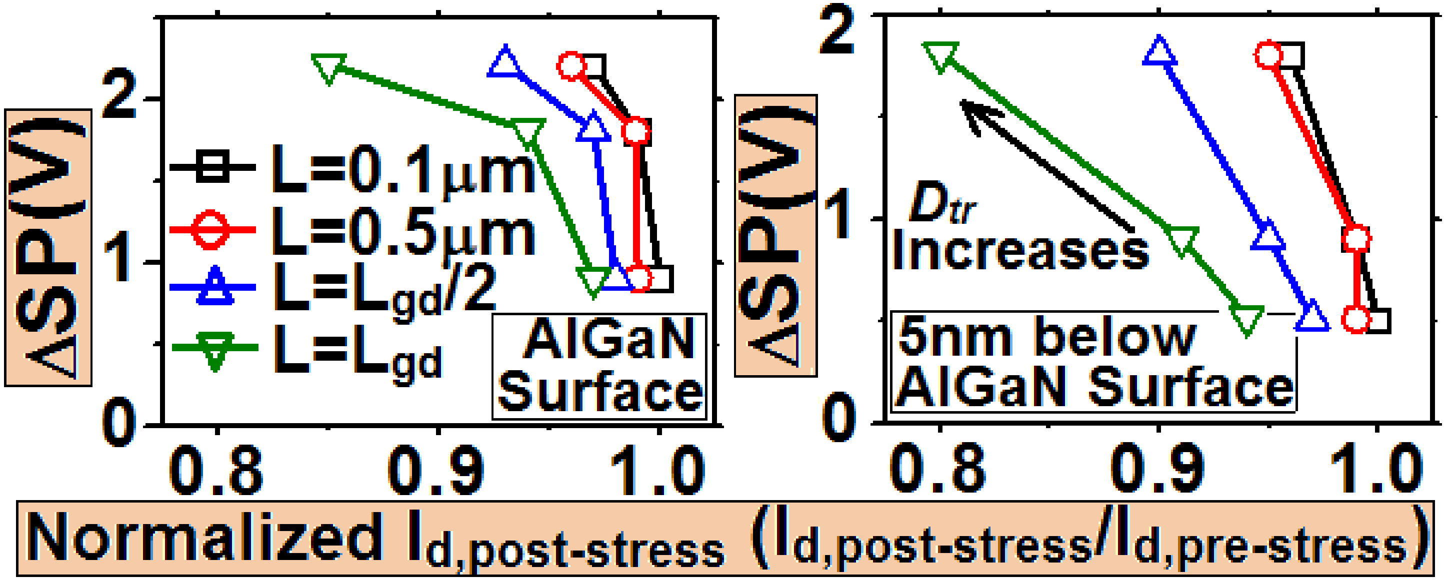




- In Device A, ΔSP (~ 3 V) and high $I_{d,post-stress}$ (~ 0.75 $I_{d,pre-stress}$), cannot be simultaneously satisfied with any density or lateral extent of trapping in GaN buffer or at the AlGaN/GaN interface
- Trapping must be in from AlGaN traps.

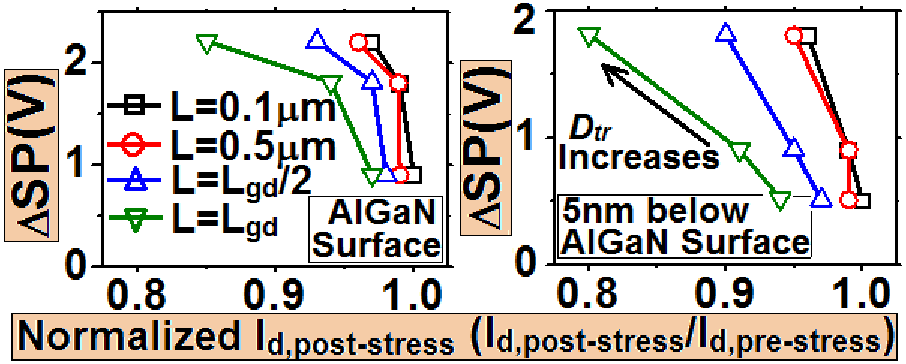


Comparison between I_d collapse and ΔSP – Device B - I



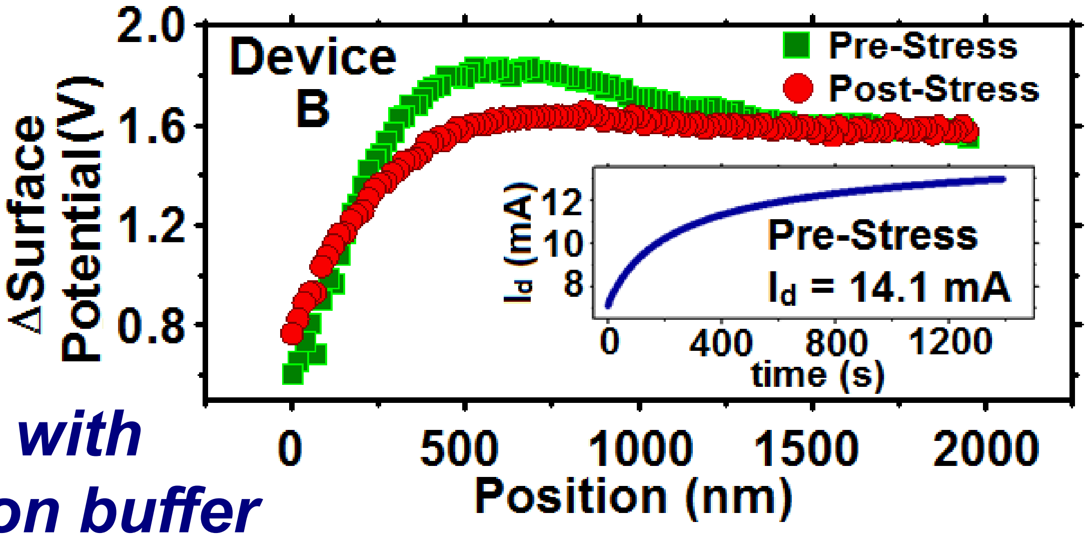
- For all cases, ΔSP much more than the experimentally observed 0.25 V, I_d collapse < 5% ($I_{d,pre\text{-}stress}/I_{d,pre\text{-}stress}$ > 0.95).
- ΔSP ~ 0.25 V → further lowering D_{tr}, tends to almost eliminate any I_d collapse.

Comparison between I_d collapse and ΔSP – Device B - II



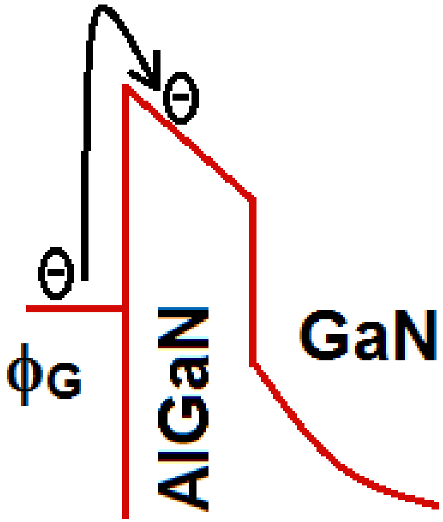
For all lateral variation of trapping locations, it is impossible to reach experimental $I_{d,post\text{-}stress}$ (only 0.5 $I_{d,pre\text{-}stress}$) with very low ΔSP ~ 0.25 V

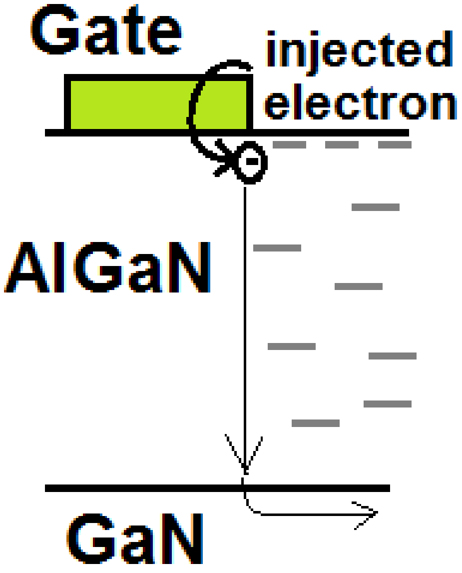
- **Trapping in Device B → negligible surface component**
- **Must be mostly near the AlGaN/GaN interface**



Results inconsistent with expectations based on buffer doping and surface passivation

Trapping Dependence on Electric Field



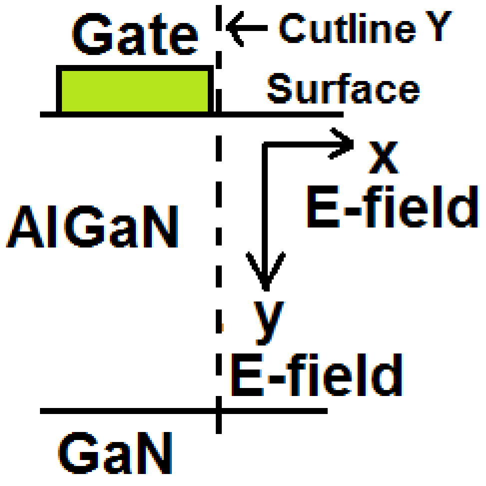


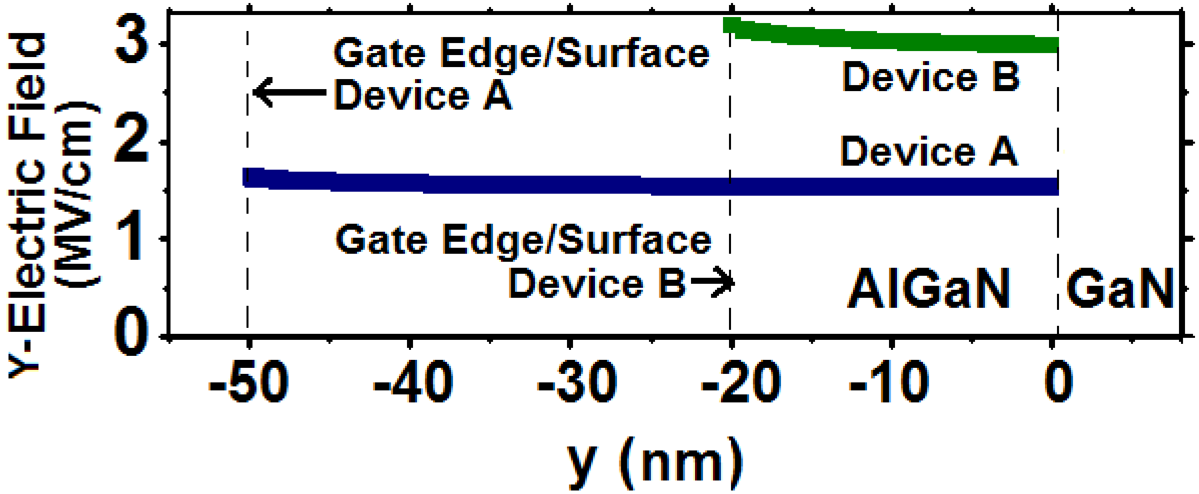
- In OFF-state, trapping in AlGaN surface states or bulk states (electrons injected from gate metal).

- If electric field is high normal to AlGaN/GaN interface, injected electrons are hot

Can reach channel access region without getting trapped in the AlGaN bulk.

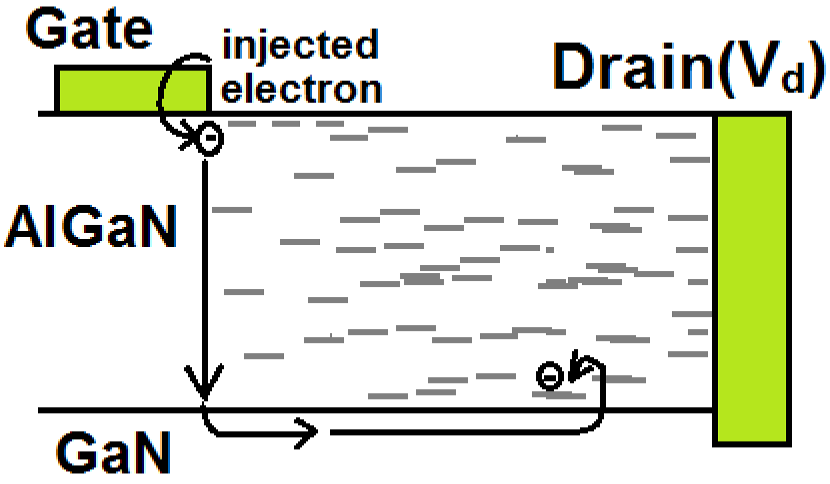
Y-Electric Field: Device A vs Device B





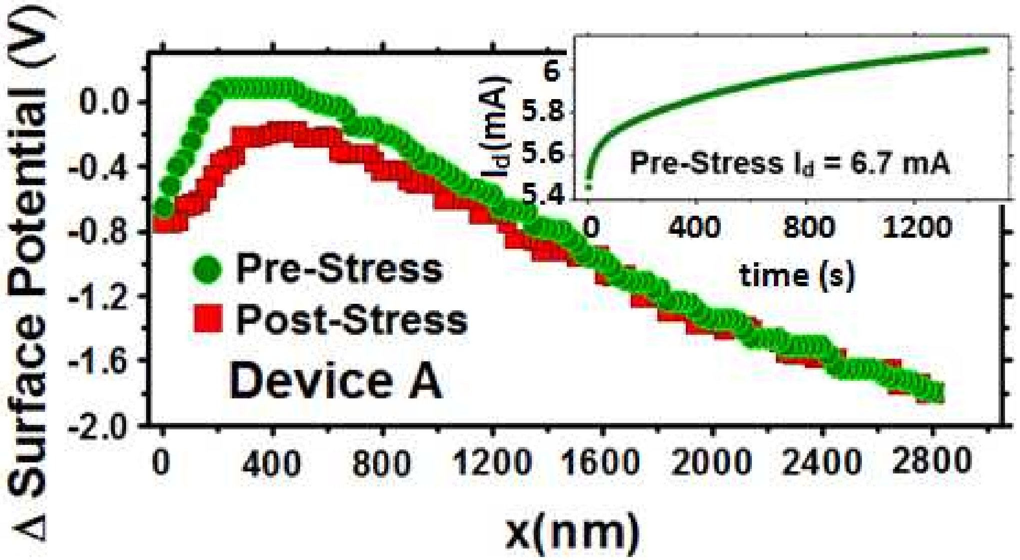
- •Much higher e-field in Device B in y-direction than in thick-barrier Device A
- •Higher energies for electrons injected from gate
- •Absence of significant surface potential shift for unpassivated Device B → thin AlGaN barrier and higher gate edge e-field responsible for electrons being transported through barrier layer without being trapped.

Trapping in Device B

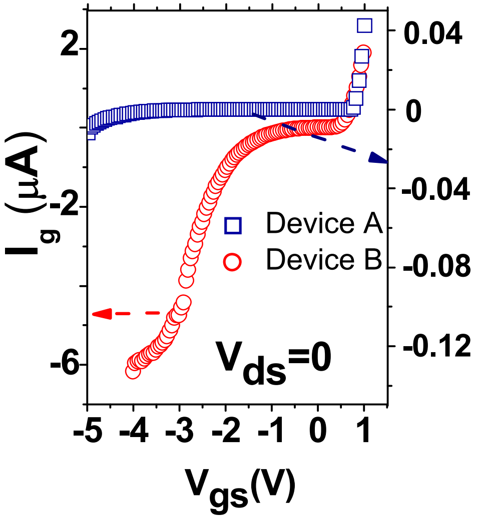


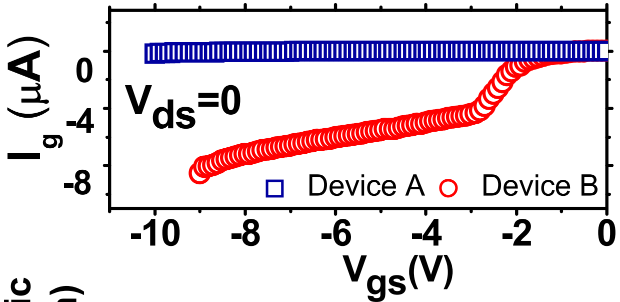
If **electrons injected from gate in Device B mostly reach channel, trapping should be similar to ON-state trapping.**

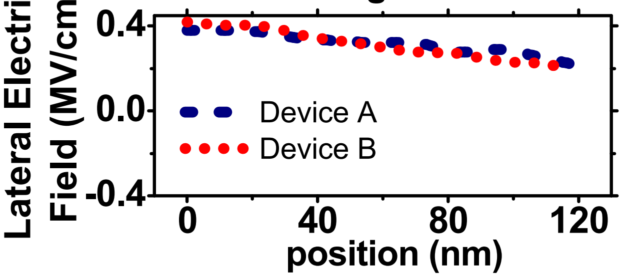
ON-state trapping in Device A indeed similar to OFF-state trapping in Device B



Device A: AlGaN Bulk or Surface Trapping?



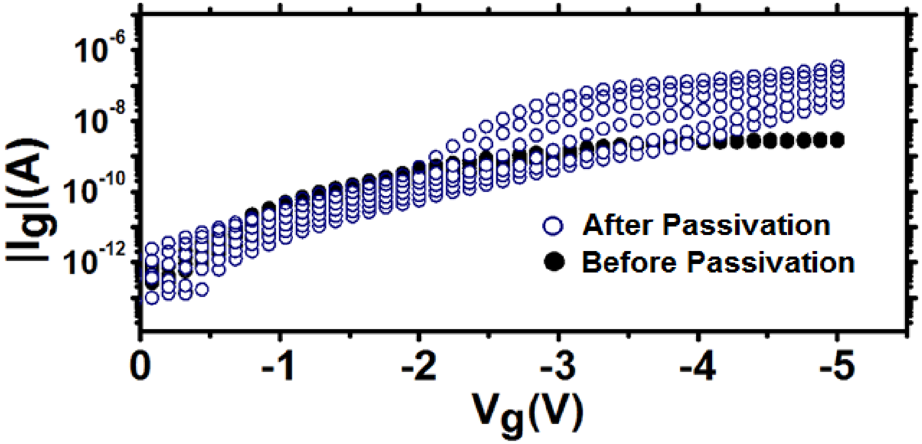




Device B → higher I_g than Device A. Dearth of surface trapping in Device B, (than Device A), not explained by absence of carriers injected from gate.

- **Surface e-field in horizontal direction very similar for Device B and Device A.**
- **Higher I_g and surface e-field in Device B (similar to Device A) inconsistent with surface charge trapping being the predominant trapping component in Device A. Near interface trapping in Device A more likely due to bulk AlGaN traps.**

Effect of Passivation: Surface States vs AlGaN bulk traps



- Elimination of charge trapping by surface passivation usually attributed to actual elimination of surface states
- Strong increase in gate edge field post passivation (surface charge elimination)
- Improvement in I_d collapse post-passivation might be due to reduced trapping in bulk AlGaN states due to increased vertical e-fields.

High V_{BD} vs. Reduced I_d collapse

- Total gate edge field → $(E_x^2 + E_y^2)^{1/2}$
- For high V_{BD} , *low* (E_y/E_x) intended (E_x can be maximized to support blocking voltages)
- Low (E_y/E_x) seems to increase I_d collapse
- Balanced design might be more critical for power than for RF.

Conclusions

- **Simultaneous KFM and I_d transient measurements strongly suggest that:**

  - Location of charge trapping affected more by design of device and e-field profile than by actual trap distribution resulting from a given passivation or doping scheme

  - Dominant component of I_d collapse in devices with thick AlGaN barrier comes from AlGaN traps.

  - Careful design optimization important for balancing between high V_{BD} and low I_d collapse.

Sandia National Laboratories is a multi-program laboratory managed and operated by Sandia Corporation, a wholly owned subsidiary of Lockheed Martin Corporation, for the U.S. Department of Energy's National Nuclear Security Administration under contract DE-AC0494AL85000. This work was performed under funding from the GIGA program managed by Dr. Mike Soboroff of the DOE Office of Electricity Delivery and Energy Reliability.