

Electrical Biasing and Voltage Contrast Imaging in a Focused Ion Beam System

Ann N. Campbell, Jerry M. Soden, Randall G. Lee^{*}, and James L. Rife
Sandia National Laboratories, P. O. Box 5800, Albuquerque, NM 87185-1081
*Micrion Corporation, One Corporation Way, Peabody, MA 01960-7990

To be presented at the 21st International Symposium for Testing and Failure Analysis (ISTFA 95)
5 - 10 November 1995, Santa Clara, CA

Abstract

We present two new techniques that enhance conventional focused ion beam (FIB) system capabilities for integrated circuit (IC) analysis: *in situ* electrical biasing and voltage contrast imaging. We have used *in situ* electrical biasing to enable a number of advanced failure analysis applications including (1) real time evaluation of device electrical behavior during milling and deposition, (2) verification of IC functional modifications without removal from the FIB system, and (3) ultraprecision control for cross sectioning of deep submicron structures, such as programmed amorphous silicon antifuses. We have also developed FIB system voltage contrast imaging that can be used for a variety of failure analysis applications. The use of passive voltage contrast imaging for defect localization and for navigation on planarized devices will be illustrated. In addition, we describe new, biased voltage contrast imaging techniques and provide examples of their application to the failure analysis of complex ICs. We discuss the necessary changes in system operating parameters to perform biased voltage contrast imaging.

THE IMPORTANCE OF FOCUSED ION BEAM (FIB) SYSTEMS as a tool for integrated circuit (IC) failure analysis has increased greatly in the past few years and will grow further as device geometries continue to shrink. FIB systems are used routinely for precision cross sectioning and modification of microelectronic devices in support of root cause failure analysis and design debugging (1,2). However, to date, little work has been done to integrate FIB system analysis with electrical failure analysis techniques. Since FIB systems are used routinely to make IC design modifications, it would be advantageous to be able to test the modified IC *in situ* to determine if the modifications were successful.

Beyond that, electrical characterization techniques can be combined with the FIB system's capabilities to achieve some unique results. One effective application is the use of the FIB to cross section programmed antifuses to localize the conducting filament. The physical extent of the conducting filament is so small (~100 nm) that it is virtually impossible to localize it by mechanical or other cross sectioning techniques. However, by electrically biasing the antifuse during FIB cross sectioning, a change in its resistance can be used to indicate when the filament has been reached. A second important application is ion beam voltage contrast (VC) imaging in the FIB system. Passive voltage contrast (PVC) imaging, which can be performed on unbiased devices, is very useful for imaging subsurface conductors and hence for navigation on planarized ICs. Biased voltage contrast imaging enables detailed examination of the electrical functioning of an IC in the FIB system. There are a few applications in the literature that involve passive voltage contrast imaging in a FIB system to detect open conductor defects (3,4). However, the application of FIB systems for voltage contrast analysis of ICs has not been widely exploited.

The use of ion beams for IC analysis does pose certain challenges. While an ion beam at 25 to 30 keV does not penetrate as deeply (2 to 3 nm) as a low energy electron beam (20 to 30 nm), ion beam irradiation is potentially more damaging to microelectronic devices. The sample surface is gradually sputtered away during ion beam imaging, gallium is implanted into the sample, and charging effects can be severe. Approaches for minimizing these difficulties are discussed.

Background: Electron and Ion Beam Voltage Contrast

Commercial FIB systems use a gallium liquid metal ion source to produce a positive (Ga^+) ion beam. When a sample is exposed to the ion beam, Ga^+ ions are implanted into the

MASTER

SEP 18 1995

OSTI

DISCLAIMER

**Portions of this document may be illegible
in electronic image products. Images are
produced from the best available original
document.**

sample and secondary particles (electrons, ions, and neutrals) are emitted from the surface by sputtering. The sputter yield of secondary electrons is about 10 times greater than that of secondary ions (most of which are positively charged). This effect, combined with the implantation of positively charged Ga^+ ions, results in a net positive charge on the sample surface.

A positive surface charge also results from low energy (~ 1 keV) electron beam (e-beam) imaging that is typically used for e-beam VC. Thus, it is anticipated that ion beam VC effects in a FIB system will be analogous to those observed during low energy e-beam VC in a scanning electron microscope (SEM). With this in mind, we briefly review the basics of e-beam VC analysis.

SEM Voltage Contrast Imaging. VC techniques based on SEMs have been widely used for over 20 years to analyze the internal operation of ICs (5-7). These techniques take advantage of the interaction between a charged beam and local electric fields resulting from the presence of voltage (charge) on the surface. Local electric fields on the device in turn modulate the secondary electron image intensity. E-beam voltage contrast imaging is typically performed at low beam energy to minimize hydrocarbon contamination, radiation damage to active regions, and surface charging. The rate of electron emission is greater than that of electron arrival (primary beam current), so the sample surface acquires a net positive charge.

Three types of SEM voltage contrast imaging are performed: passive, static, and capacitive coupling voltage contrast (5-11). Information can be obtained from unbiased ICs in passive voltage contrast (PVC) imaging due to the relative ability of different structures on the sample to dissipate the charging effects of the e-beam. For biased ICs, two VC options exist: static voltage contrast (SVC) and capacitive coupling voltage contrast (CCVC) imaging. SVC is performed with the top dielectric layer (passivation) removed, and the image intensity is largely determined by the static voltages on the IC. Variations in the image brightness are used to determine logic levels of digital ICs and the voltages on internal test nodes. CCVC is a method for viewing dynamic voltages on conductors beneath passivation layers and can also reveal unbiased, subsurface conductors. The passivation layer acts as the dielectric of a discharging capacitor to generate an image of changing subsurface voltages. The transient contrast due to switching voltages decays very rapidly. Signal averaging is often used to enhance CCVC images.

FIB Voltage Contrast Imaging. VC information in a FIB image arises from modulation of the secondary electron emission caused by surface charging due to the ion beam and the presence of applied voltages on the sample. Local voltage differences on a sample surface can be detected in the FIB system with secondary electron mode imaging.

The secondary electrons sputtered from the sample surface by impinging gallium ions have an energy distribution from 0 to approximately 5 eV, with an average of about 2 eV for a 30 keV ion beam energy (12). The electrons are accelerated toward the detector by the extraction field provided by both the MCP detector and the electron floodscreen (described in the Experimental Approach section). Simulations describing the modulation in secondary electron trajectory as a function of voltage on the sample surface have been performed using the SIMION program (13). These simulations show for adjacent unpassivated conductor lines that, while most of the secondary electrons sputtered from a 0 V line are detected, most of the secondary electrons generated from a +5.0 V line are recaptured.

Experimental Approach

FIB System for *in situ* Electrical Stimulus. The experiments were carried out in a Micron 9000D FIB system that operates with a maximum 30 keV primary ion beam energy. Electrical biasing in the FIB system is accomplished by using a modified stage that provides 120 pin electrical biasing capability for both electrical testing and voltage contrast analysis. The device to be analyzed is inserted into a socket on a printed circuit board that is transported into the FIB process chamber through the system's load lock. Electrical connection to the PC board is made *in situ* via a clamshell style motor-driven clamping mechanism. The electrical socket and clamping mechanism are illustrated in Figure 1. Electrical stimulus is provided to the device by appropriate equipment, such as a parameter analyzer interfaced through a switchbox or a digital tester. In addition to the electrical biasing capability, the FIB system's stage has the capability to rotate a full 360° and can be tilted up to a 60° angle.

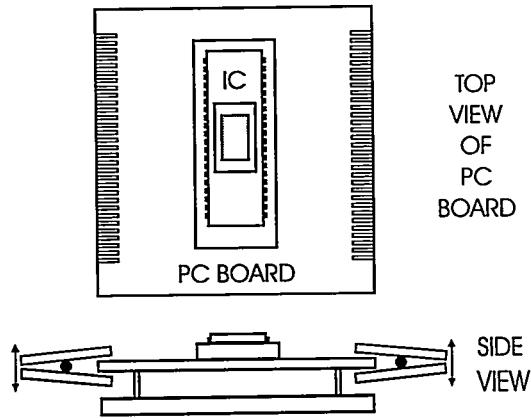


Fig. 1. The PC board, load lock transport frame, and clamshell clamping mechanism for electrical testing of ICs in the FIB system. The side view shows the clamps in the open position.

Imaging in the FIB System. Imaging in the FIB system is accomplished by rastering the beam over the sample and collecting the secondary particles, either positive (ions) or negative (electrons) on a pixel by pixel basis. The image contrast at each pixel is proportional to the number of detected secondary particles. The image is a superposition of the "normal" or topographical image plus the modulation due to VC effects.

Secondary Particle Detection. The FIB system uses a microchannel plate (MCP) detector (14) mounted at the bottom of the FIB column, directly above the sample surface for secondary particle detection. The MCP detector consists of an array of hundreds of hollow tubes, or channels, in a lead glass substrate that acts as an electron multiplier. An electron shower is generated inside a channel when a particle (secondary electron or ion) strikes the channel's interior surface. By applying a voltage between the top and bottom faces of the MCP detector, these electrons are accelerated along the channels, generating more electron showers when they strike the surface deeper into the channel. The total charge is collected at the output of the channels and sampled at specific time intervals. The MCP measured charge is indicative of the number of collected secondary particles from the region (pixel) struck by the ion beam.

The channels generate electron showers regardless of whether the impinging particle is an electron or ion. Therefore, the MCP detector can easily be switched from detecting secondary ions to secondary electrons (and vice-versa) by simply changing the bias on the detector. Normal MCP biases for imaging are +400 V for secondary electrons and -1400 V for positive secondary ions. The MCP detector is shown in Figure 2.

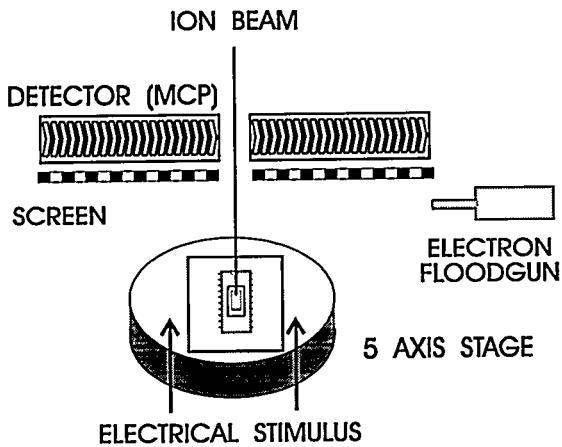


Fig. 2. The MCP detector, electron floodgun, electron floodscreen, and sample surface in the FIB system.

Charge Neutralization. This system also has an electron floodgun which directs low energy electrons onto the sample surface to neutralize the positive charge buildup due to implanted Ga^+ . The electron floodgun is normally active in secondary ion mode (SIM) and is effective in reducing sample charging and electrostatic discharge damage. The floodgun cannot be active during secondary electron mode imaging because the MCP detector would be swamped by electrons from the floodgun, preventing detection of secondary electrons. A mesh screen between the MCP detector and the sample is used to steer low energy electrons down to the sample surface. The electron floodscreen bias voltage is negative during SIM imaging and is positive (~80 V) during secondary electron mode operation. The electron floodgun and floodscreen are also shown in Figure 2.

Implementing Voltage Contrast Imaging in the FIB System. The implementation of PVC imaging does not require any system modifications. The biased SVC and CCVC techniques require that power be applied to the IC in the FIB chamber, as discussed a previous section. Secondary electron imaging in the FIB system is used to acquire voltage contrast information.

Controlling the ion dose delivered to the sample is important for successful PVC and CCVC imaging of passivated conductors. This is the case because the local electric field effects that cause PVC and CCVC are quickly overcome by the charging effect of the ion beam. The ion dose is determined by the raster parameters, the number of rasters performed, and the ion beam current. The raster parameters that can be controlled are the dwell time at each pixel (i.e., the scan rate), the number of pixels in the raster, and the field of view (FOV). The number of rasters can be controlled by "grabbing" one image raster at a time rather than by continuous imaging. The ion beam current is determined by the size of the beam-limiting aperture. The FIB system used for these experiments has apertures and associated beam currents ranging from $50 \mu\text{m}$ (12.0 pA) to $750 \mu\text{m}$ (7.9 nA).

In general, VC imaging was performed at the lowest possible beam current. PVC and CCVC effects could be achieved only with the smallest possible ion doses. The PVC and CCVC results reported here were all obtained by "grabbing" single rasters. Often the effects disappeared by the second or third raster. Once the contrast faded due to charging from the beam, the VC effect could be reproduced by first grabbing a SIM image (the electron floodgun neutralizes the surface charge) and then reimaging in the secondary electron mode.

By comparison with PVC and CCVC, SVC is relatively insensitive to the ion dose. However, although SVC imaging can be performed with larger beam currents and ion doses, it is not advisable to do so since the sample is being sputtered away as it is imaged, and the surface damage increases with ion dose.

Experimental Results: Electrical Biasing in the FIB System

We divide our experimental results into two categories: those that involve electrical biasing only and those that involve the sample's interaction with the ion beam (voltage contrast). The former category is discussed in this section.

We have used the ability to bias samples electrically in the FIB system chamber to (1) perform real time evaluation of device electrical (parametric) behavior during milling and deposition, (2) verify IC functional modifications without removing the sample from the FIB system, and (3) perform ultraprecise cross sectioning of deep submicron structures. We discuss the first two and illustrate the third.

Real Time Evaluation of Device Electrical Behavior. Real time evaluation of device electrical behavior during milling and deposition provides the capability to control device parameters interactively, such as the resistance of milled or deposited interconnections. In addition, direct and indirect ion beam effects can be used to alter certain device parameters, such as threshold voltage and gate oxide leakage. These effects can be monitored with parametric test equipment, such as an HP4145 parameter analyzer, interfaced to the device through the vacuum feedthrough electrical connectors.

Verification of IC Functional Modifications. FIB systems are commonly used to modify the digital functionality of ICs. The use of *in situ* biasing to interface an IC in the system to digital test equipment enables device modifications to be monitored, assuring that the intended changes are correct prior to removing the IC from the system. The test equipment used ranges from a simple switch matrix to sophisticated digital testers, depending upon the complexity of the IC and the desired modifications.

Ultraprecise Cross Sectioning. Another capability provided by *in situ* biasing is ultraprecise control for cross sectioning. If the sample has an electrical parameter that is a known or measurable function of the cross sectioning process, this parameter can be used for precise control. An example of this is the cross sectioning of programmed antifuses.

Antifuses are the programmable elements for some types of PROMs, FPGAs, and other ICs. They are typically constructed of thin (~ 100 nm) insulating layers of oxide or amorphous silicon sandwiched between conductive layers such as Al and TiW (15). The lateral dimension of the antifuse is normally about 1 to 2 μm . Amorphous silicon antifuses typically have a resistance in the range of 100 to 1000 $\text{M}\Omega$ prior to programming that decreases to 50 to 300 Ω after programming. Programming is achieved by applying an elevated voltage across the insulating layer, causing localized breakdown with an associated reduction in resistance. The damaged region that forms the low resistance connection between the conductors typically has an effective radius of about 100 nm.

To make process changes to enhance the reliability and electrical properties of antifuses, it is very desirable to be able to analyze the spatial location and microstructure of the low resistance fused region. Because the fused region may occur anywhere within the several μm^2 area of the antifuse, it would be tedious, if not impossible, to accurately locate and cross section this site for a specific antifuse with conventional techniques. Mechanical cross sections through a row of many antifuses may, by chance, result in a section through a low resistance region, but a more selective technique is desired.

We have developed a FIB technique for localizing the low resistance region in antifuse structures. First, an initial FIB cross section is made adjacent to the antifuse of interest. Power is then applied to the IC so that the resistance of the antifuse can be monitored during subsequent milling. Next, incremental cross sections are made through the antifuse while observing the magnitude of the resistance. As the ion beam encounters the low resistance region and begins to mill it away, the resistance increases. Precise polish mills are used to move slowly through the antifuse structure. The size of the milled region and the milling rate are selected to ensure that when the resistance change is first detected, there will be an opportunity for at least one more mill to provide a high quality image of the antifuse profile. Imaging of the fused region was performed with a field emission SEM (FESEM) to prevent further milling of the region and for improved spatial resolution. An FESEM image of a cross sectioned antifuse is shown in Figure 3.

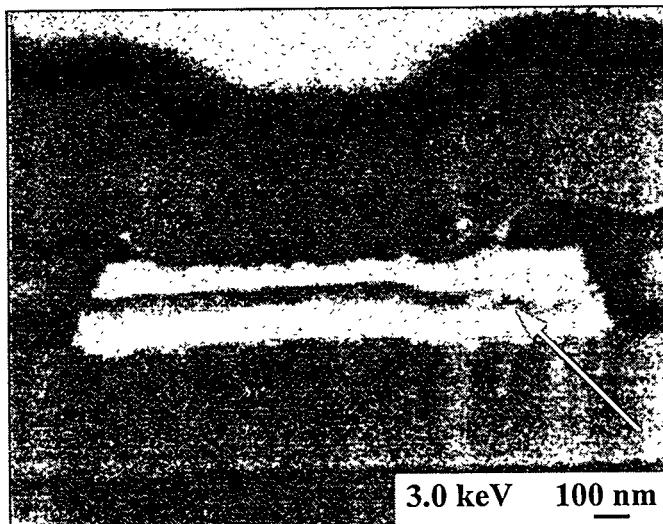


Fig. 3. Field emission SEM image of a FIB cross section through a programmed antifuse. The low resistance region is indicated by the arrow.

Experimental Results: Voltage Contrast Imaging in the FIB System.

We have performed PVC, VC, and CCVC imaging in the FIB system. We present examples of each and discuss their utility in IC analysis.

Passive Voltage Contrast Imaging. Passive voltage contrast imaging effects arise during imaging with a Ga^+ ion beam in the FIB system when portions of a sample acquire a net positive charge buildup relative to the surrounding areas. PVC effects are readily apparent in most secondary electron mode images taken with a FIB system, including cross sections. As an example, consider the cross section of an IC pictured in Figure 4. The dielectric materials acquire a positive charge due to implanted Ga^+ , recapture secondary electrons, and appear dark as a result. The conductors (metal and polysilicon) normally have a bright contrast because they are conductive enough to neutralize the implanted Ga^+ , and hence the secondary electron yield is much higher from these layers. The metal-1 (M1) layer in the pictured cross section illustrates this. However, if a portion of a conductor is electrically floating (as is the case for the M2 line and the polysilicon gate electrode in this figure), it will also charge positively and have a dark contrast.

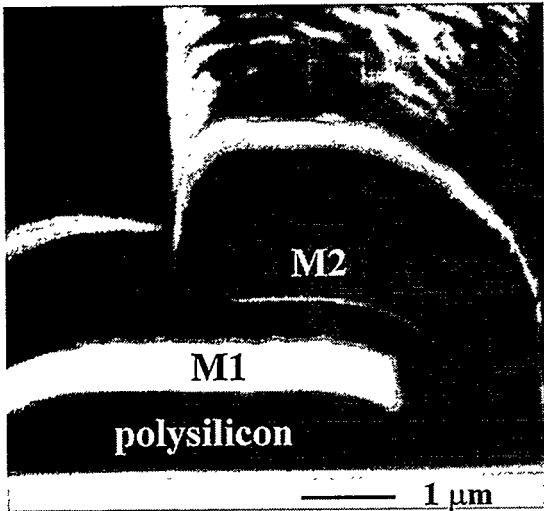


Fig. 4. Voltage contrast effects in a secondary electron mode image of a FIB cross section. The M2 and polysilicon are floating conductors.

Another example of this effect is observed in Figure 5, which shows an unpassivated (i.e., no dielectric material on top of the metal interconnects) metal via chain structure containing an open contact. This device is a test structure for Sandia's 0.5 μm CMOS VI technology. The interconnect

material is Al-0.5% Cu with Ti interfacial layers and W studs for vias. Planarization in this technology is accomplished through chemical-mechanical polishing (CMP).

Figure 5a is a secondary electron mode image showing that the section of the chain at the upper right images dark compared with the metal in the rest of the chain. This implies that the dark region is electrically disconnected from the rest of the test structure, and has acquired a net positive charge from the Ga^+ ion beam. As a result, secondary electrons emitted by that region of the conductor are recaptured, resulting in a darker image contrast for that portion of the chain. By comparison, the electrically disconnected portion of the chain does not have a different contrast in a SIM image of the same FOV as shown in Figure 5b. The electron floodgun is active during SIM imaging, neutralizing the effect of charge buildup due to Ga^+ implantation.

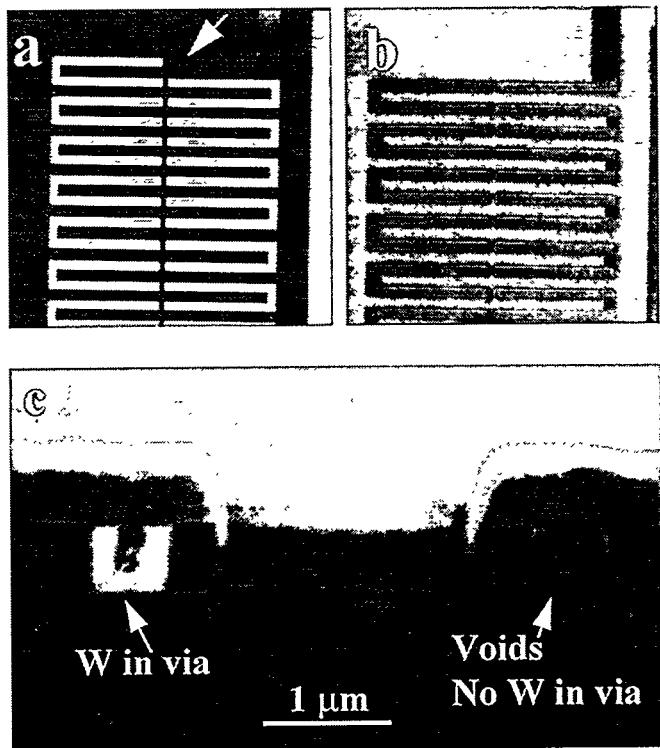


Fig. 5. (a) Secondary electron mode image showing extinction of contrast from the electrically disconnected portion of the via chain. (b) Secondary ion mode image of the same region, showing no difference in contrast. (c) FESEM image of FIB cross section through the defective contact.

The contacts at the end of the conducting portion and the beginning of the isolated portion of the chain were cross sectioned with the FIB system. An FESEM was used to image the cross section, and the result is shown in Figure 5c. The

contact via on the left hand side of the figure is properly filled with tungsten, but the via on the right (the contact to the electrically isolated section of the chain) is voided and does not contain W but rather (as shown by subsequent analysis) a corrosion product.

This example illustrates the power of PVC imaging in a FIB system. The FIB is used both to identify and to cross section the defective contact.

The PVC effects which are observed on passivated devices are similar to those for CCVC imaging. The effects are of short duration, lasting only until exposure by the ion beam overwhelms the small localized differences in surface charge. The ideal approach is to navigate to the area of interest and then grab a single frame image, reneutralizing the surface by grabbing an SIM image as necessary.

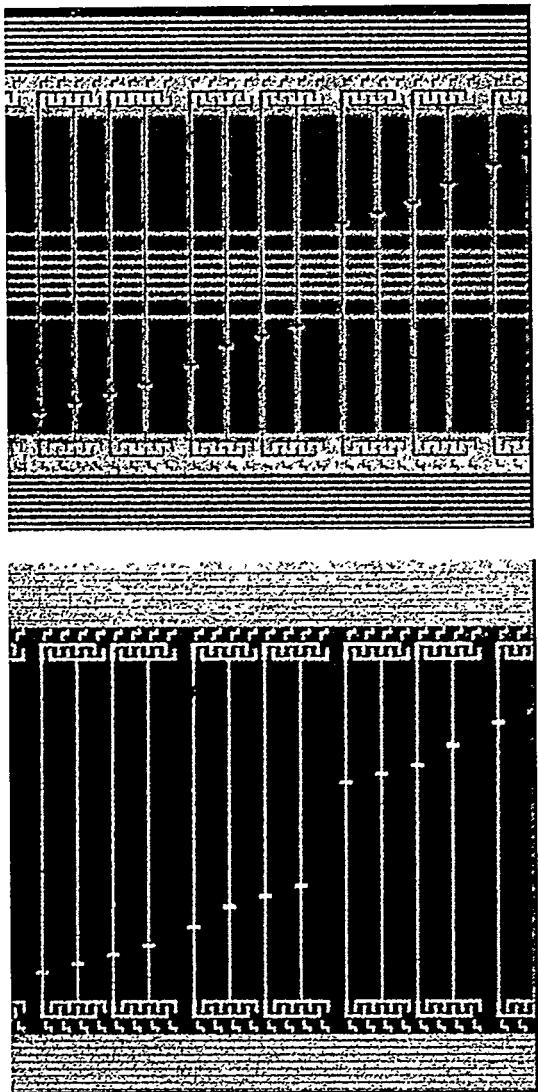


Fig. 6. (a) SVC image showing planarized M1 lines (horizontal). (b) SVC effect is no longer visible in next scan.

This PVC effect is very useful for navigation on planarized or partially planarized devices and is illustrated in Figure 6 for a 256K SRAM which is planarized except for the top level metal (M2). This IC is implemented with a 2-level metal, 1-polysilicon, 0.8 μm CMOS technology. Figure 6a is a secondary electron mode image that shows an area in the peripheral circuitry of the IC where the M1 lines (horizontal in the figure) are visible due to the PVC effect. The vertical lines in the figure are unplanarized M2. This image was the first raster scan acquired after first neutralizing the surface with an SIM scan. Figure 6b is the secondary electron mode image collected on the second scan without changing the MCP detector gain; the PVC effect had decayed and only the unplanarized metal-2 lines are visible in this image.

As for the previous example, the power of the technique is the ability to use the FIB both to locate and to modify or cross section a feature of interest (in this case, a subsurface conductor on a planarized device).

Biased Voltage Contrast Imaging. All that is required to perform biased voltage contrast imaging in a FIB system is to be able to apply power to the IC. As described in a previous section, our system was modified to include a 120-pin electrical biasing capability. In addition, the MCP detector bias and electron floodscreen voltage can be varied to modify the secondary electron extraction field for certain applications, but in general the typical operating floodscreen and detector biases were used.

Static Voltage Contrast Imaging. A 16K SRAM fabricated with a 2 level metal, 2 μm CMOS technology was examined with SVC imaging, and the results are given in Figure 7. The IC was deprocessed to remove the glass passivation to permit SVC analysis. Power was applied to the IC. For this SRAM, $V_{DD} = 5\text{ V}$ and $V_{SS} = 0\text{ V}$. Several cells in the memory array are visible in Figure 7a, two of which are outlined. When power is applied to the SRAM, each memory cell latches to a logic 0 or logic 1. The voltage on the M1 drain strap (shown in Figure 7a) indicates the logic state of each cell. If the drain contact adjacent to the bit line (BL) is at 0 V (bright contrast), the cell is in the 0 state. The two outlined cells are in the 1 state. The fact that a SVC image is obtained of the voltage on the M1 drain strap indicates that M1 as well as M2 was exposed during deprocessing. A cross section of one of the tested devices confirmed this.

Next, the two highlighted memory cells were written to the "0" state, as shown in Figure 7b. It was observed that prolonged viewing of these memory cells (e.g., with several scans at a slow scan rate) can cause memory cells to change state. It can be seen by comparing Figure 7c (acquired after a few slow scans) with Figure 7b that several of the memory cells have changed state. In addition, one of the cells (outlined in Figure 7c) changed state during the scan as evidenced by the M1 drain straps changing contrast during the scan. These findings demonstrate that the ion beam of a FIB system can be used for logic state control of sequential circuit

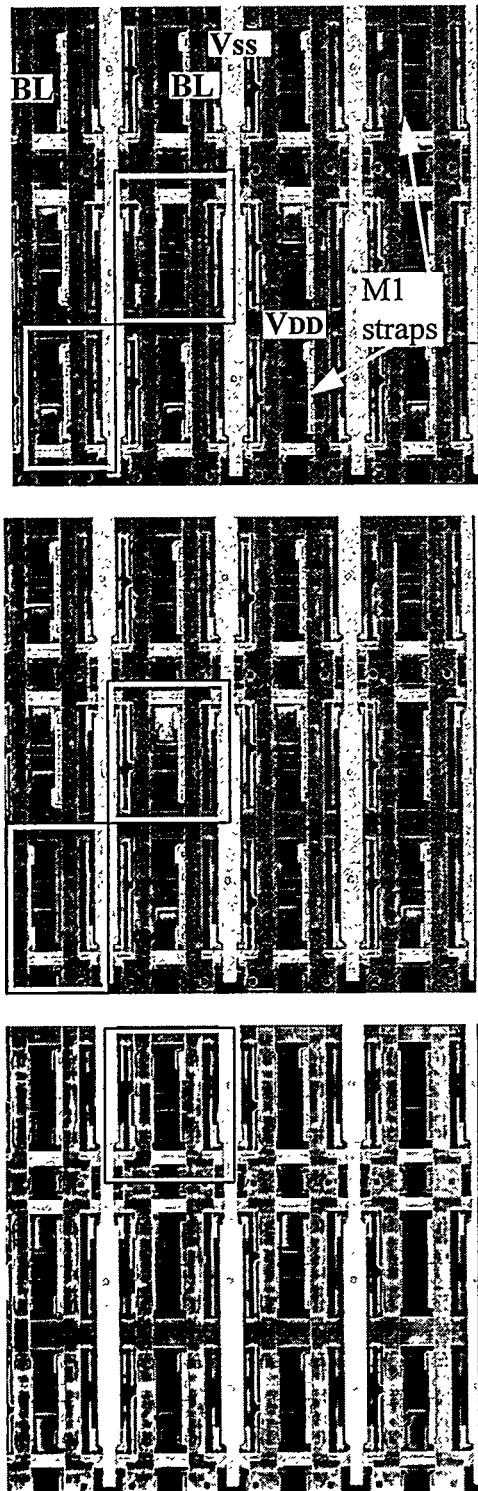


Fig. 7. SVC imaging of a 2 μ m, 2-metal CMOS technology SRAM, 40 μ m FOV. (a) Several SRAM cells indicating the cell components. (b) Two memory cells (outlined) written to the 1 state. (c) Repeated imaging with a slow scan rate can cause cells to change state. The outlined cell changed state during acquisition of this image.

elements in a manner similar to that achieved with the photon beam of a scanning optical microscope (16). They also indicate that care must be exercised to keep the ion dose as low as possible during SVC imaging.

Aside from logic state changes in the memory cells, the SVC effect was not sensitive to the ion beam parameters. SVC was performed successfully with both small and moderately high ion beam currents and doses. The SVC image persists during continuous scanning, permitting the change from one logic state to another to be observed.

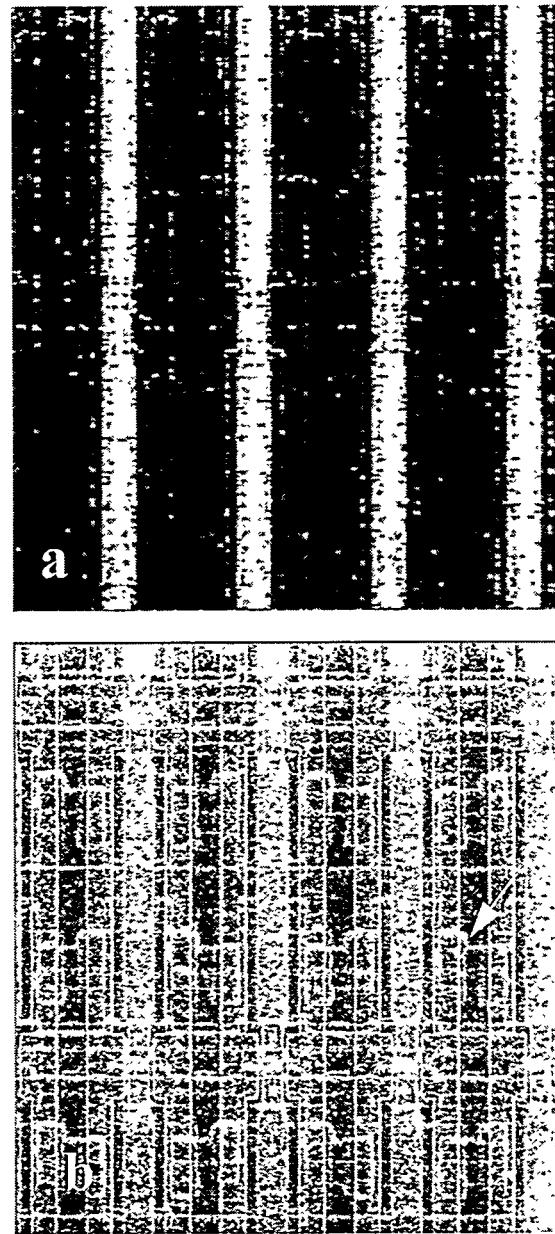


Fig. 8. CCVC images of the 2 μ m SRAM, 40 μ m FOV, showing the V_{ss} lines at 0 V (bright contrast). (a) High contrast image. (b) Lower contrast image showing more detail of the IC structure.

FIB milling could be used for local, selective removal of the passivation on the M1 drain straps or other features of interest on the IC. This would permit SVC imaging of the voltages at those points without requiring that the entire IC be deprocessed.

Dynamic (Capacitive Coupling) Voltage Contrast Imaging. Moving to the next level of complexity, we used CCVC to image voltages on a passivated 16K SRAM with the V_{SS} lines biased at 0 V and the bit lines at 5 V. Two images of the IC are shown in Figure 8. Figure 8a is a high contrast image that shows the V_{SS} lines (bright contrast) clearly, but little structural detail can be resolved. Figure 8b is the same FOV imaged to enhance the background contrast. The bright contrast on the V_{SS} lines can still be observed, but it is less pronounced than in Figure 8a. The dark contrast on the bit lines could not be readily distinguished from the background contrast in either figure. The M1 drain straps are visible in Figure 8b, as indicated by the arrow, and in most cases a contrast difference between the two drain straps in each cell can be distinguished. It is anticipated that the effectiveness of the CCVC technique will be improved by further reduction in the ion beam current. This could be achieved by using smaller apertures than were available during these experiments.

Electrical Effects of Voltage Contrast Imaging. Our experiments with the 16K SRAM indicated that the power supply current, I_{DDQ} , is sensitive to ion irradiation *while the IC is biased*. Certain portions of the IC were more sensitive than others, and passivated ICs were more sensitive than those with the top passivation removed. For a depassivated SRAM, if only the memory cells were imaged, the increase in I_{DDQ} (from 100's of nA before ion beam exposure to a few μ A after exposure) was moderate and gradual. The increase in I_{DDQ} often decayed at room temperature, and was bake-recoverable. However, when the row and column decoders and I/Os on the SRAM were exposed to the ion beam, I_{DDQ} rose sharply. Specifically, when one 16K SRAM was first powered up, the power supply current was 500 nA. I_{DDQ} jumped to about 19 μ A when a field of view including portions of the memory array and row and column decoders was imaged. Continued exposure to the ion beam caused the current to rise to 500 μ A. When not exposed to the beam, the IC recovered to the nA range. Repeated imaging of the memory array only while the IC was powered resulted in I_{DDQ} on the order of 10 - 20 μ A.

Discussion

We have presented a number of examples of the use of electrical biasing and voltage contrast imaging in the FIB system for advanced IC failure analysis. These examples have demonstrated the ability to localize circuit defects and features of interest *in situ*. The required FIB modifications or cross sections can then be made and the modifications can be verified before removing the sample from the FIB chamber.

The ability to make precise incremental cross sections through structures such as antifuses while measuring their resistance enhances structural characterization and provides information needed for manufacturing process improvement. The capability permits characteristics of the structure of interest to be more directly investigated, such as resistance uniformity and spatial features of the antifuse programmed region, and the relationship between programming voltage and physical defects.

We have demonstrated that voltage contrast imaging can be performed in a FIB system with an MCP detector. Operating with the normal high MCP bias (+400 V) and screen (+70 to 80 V) voltages used for secondary electron mode imaging allowed us to perform SVC imaging of 0 V and 3.3 to 5 V states on unpassivated conductors and 0V and 5 V states on passivated conductors. Preliminary work has indicated that it is necessary to operate at low MCP and screen voltages (~ 0 V each) to distinguish small (0.5 V) differences in voltage between conductors. However, at the reduced MCP and screen voltages, the number of secondary electrons reaching the detector is greatly reduced as evidenced by a sharply attenuated signal and reduced signal to noise ratio. Further development of FIB system voltage contrast techniques will include optimizing the extraction field for different imaging applications.

As expected, many of the ion beam voltage contrast effects observed are analogous to those of electron beam (SEM) based VC. We have observed passive, biased static, and biased dynamic (CCVC) voltage contrast imaging techniques. Two important differences were noted between electron and ion mode voltage contrast imaging. First, the implantation of Ga^+ into the sample leads to permanent physical change of the device. We observed that this gallium implantation eventually impairs the ability to image the sample, leading to a reduced number of secondary electrons reaching the detector, even after neutralization of the surface with the electron floodgun. Second, we found that focused ion beam imaging of an IC (either passivated or with the passivation removed) *when the IC is powered* can lead to greatly increased power supply current. This effect is apparently due to the deposition of charge on the sample.

Our experience indicates that PVC and CCVC results improve as ion dose per area decreases. We performed the described experiments with the lowest possible ion dose with our present system configuration. In the future we will explore performing PVC and CCVC with further reduced ion doses. The reduced ion doses will also permit SVC imaging with less damage to the sample.

Conclusions

We have developed a variety of failure analysis applications based on electrical biasing in a focused ion beam system. We have shown that electrical biasing in the FIB

system can be used to perform precision cross sections of structures such as amorphous silicon antifuses. We demonstrated that the FIB system can be used to perform both passive and biased voltage contrast imaging and that these VC effects are similar to those observed in e-beam voltage contrast. Passive voltage contrast imaging has been used to localize open circuit defects and subsurface conductors for FIB cross sectioning. Both SVC and CCVC imaging were used to investigate operating ICs in the FIB system.

The real power of FIB system biasing and voltage contrast techniques is the ability to localize a circuit defect *in situ*, make the required FIB modifications, and then verify that the modifications have been made.

Acknowledgments

The authors thank Bruce Draper, Rich Flores, and Henry White of Sandia for providing test samples; Tom Olson at Micrion Corp. for simulations of secondary electron paths; and Ken Peterson, Pai Tangyunyong, and Rich Anderson of Sandia for careful review of the manuscript. This work performed at Sandia National Laboratories was supported by the US Department of Energy under contract number DE-AC04-94AL85000.

References

1. Perrin, D. and W. Seifert, Solid State Technology, October 1994, 95 -96.
2. Stevie, F. A., T. C. Shane, P. M. Kahora, R. Hull, D. Bahnck, V. C. Kannan and E. David, Surface and Interface Analysis, 23, 61 - 68 (1995).
3. Lin, H. T., J. F. McDonald, J. C. Corelli, S. Balakrishnan and N. King, Thin Solid Films, 166, 121 - 130 (1988).
4. Ogawa, H., K. Tamuru, K. Matsuyama, M. Fukumoto and H. Iwasaki, in Extended Abstracts of the 22nd Conference on Solid State Devices and Materials, Sendai, Japan, 1990, p. 405.
5. Cole Jr., E.I., C R. Bagnell Jr., B.G. Davies, A.M. Neacsu, W.V. Oxford and R.H. Propst, Scanning Microscopy, 2, 133-150 (1988).
6. Cole Jr., E.I. and J.M. Soden, "Microelectronics Failure Analysis Desk Reference", 3rd ed., p. 163, ASM International, Materials Park, Ohio (1993).
7. Soden, J.M. and R.E. Anderson, Proc. IEEE, 81, 703-715 (1993).
8. Gorlich, S., K. D. Hermann, W. Reiners and E. Kubalek, Scanning Electron Microscopy, II, 447 - 464 (1986).
9. Cole Jr., E. I., C. R. Bagnell, F. A. DiBianca, D. Johnson, W. Oxford, C. Smith and R. H. Propst, Appl. Phys. Lett., 48, 599 - 600 (1986).
10. Colvin, J., in Proceedings of the 16th Internat. Symp. for Testing and Failure Analysis, Los Angeles, CA, Oct. 29 - Nov. 2, 1990, p. 331.
11. Cole Jr., E. I., C. R. Bagnell Jr., B. Davies, A. Neacsu, W. Oxford, S. Roy and R. H. Propst, J. Appl. Phys., 62, 4909 - 4915 (1987).
12. Benazeth, N., Nuclear Instruments and Methods, 194, 405 - 413 (1982).
13. Dahl, D. A., Idaho National Engineering Laboratory, Idaho Falls, ID, Document No. EGG-CS-7233, 1994.
14. Wiza, J. L., Nuclear Instruments and Methods, 162, 587 - 601 (1979).
15. K. E. Gordon and R. J. Wong, IEDM, 27 - 30 (1993).
16. Cole Jr., E. I., J.M. Soden, J.L. Rife, D.L. Barton and C.L. Henderson, in Proceedings 32nd Inter. Rel. Phys. Symp., San Jose, CA, April 12 -14, 1994, p. 388.

DISCLAIMER

This report was prepared as an account of work sponsored by an agency of the United States Government. Neither the United States Government nor any agency thereof, nor any of their employees, makes any warranty, express or implied, or assumes any legal liability or responsibility for the accuracy, completeness, or usefulness of any information, apparatus, product, or process disclosed, or represents that its use would not infringe privately owned rights. Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise does not necessarily constitute or imply its endorsement, recommendation, or favoring by the United States Government or any agency thereof. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.