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Evaluation of Low-Residue Soldering for Military and Commercial Applications: A Report from the Low-Residue Soldering Task Force

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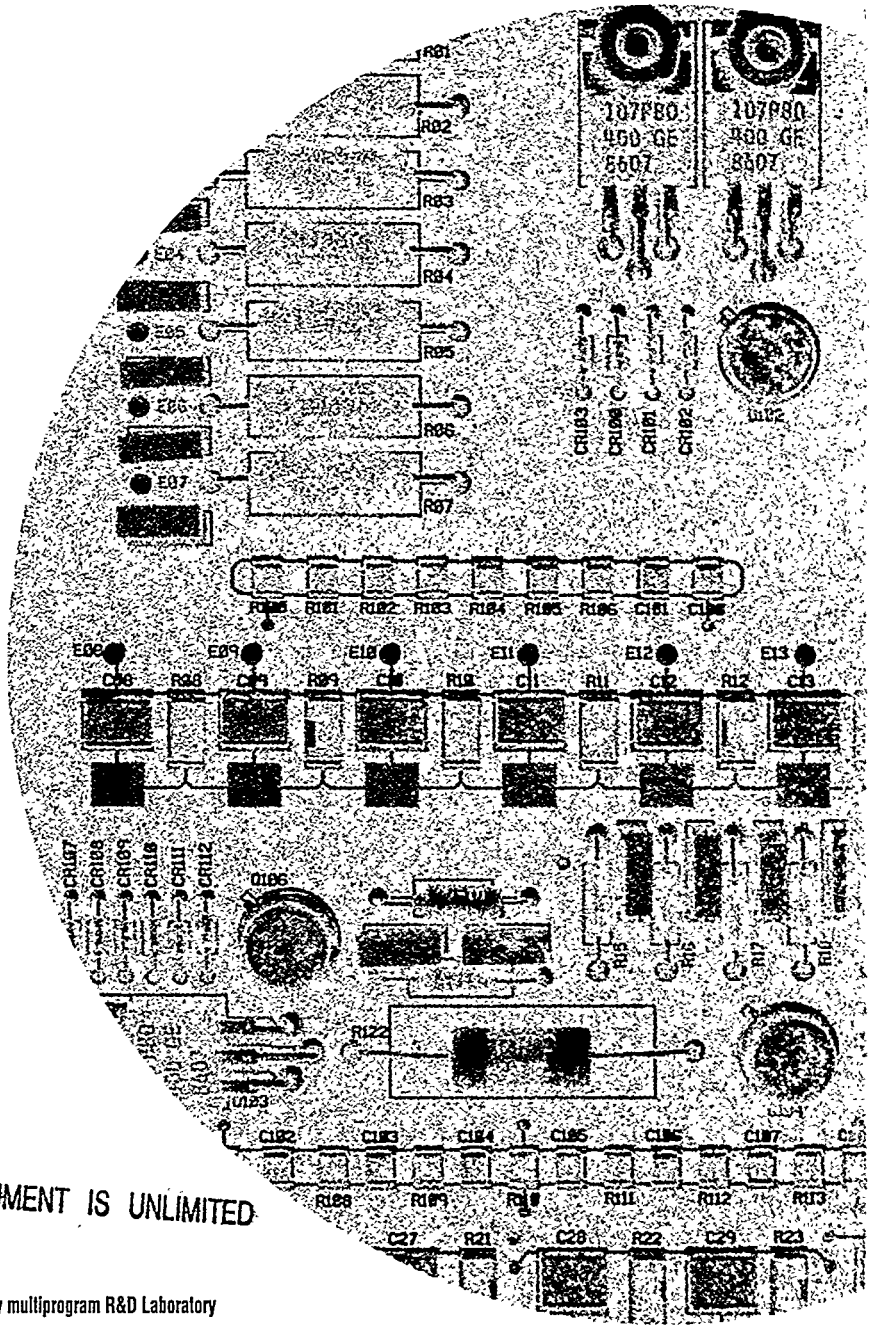

June 1995

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Evaluation of Low-Residue Soldering for Military and Commercial Applications: A Report from the Low-Residue Soldering Task Force

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June 1995

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Chris Matzke, Naval Warfare Assessment Center
Becky McKelvey, Texas Instruments
Eddie Moltz, Texas Instruments
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James Savage, Airco
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Executive Summary

Low-Residue Soldering Task Force (LRSTF)

The LRSTF was formed in April 1993 by Sandia National Laboratories and combined the joint efforts of industry, military, and government to evaluate low-residue (LR) soldering processes for military and commercial applications. The organizations participating in the task force are listed on the back cover.

Sandia's participation in the program was funded by the Department of Energy through an Energy and Environment Technical Area Coordinating Team. This funding was used to purchase testing materials and to support AlliedSignal's Kansas City Division participation in the program (AlliedSignal is a DOE production facility). Texas Instruments, Alliant Techsystems, and Hughes Electronics each signed Cooperative Research and Development Agreements (CRADAs) with Sandia, which formalized their participation and specified the amount of their contributions to the program. The military participants also made significant contributions to the program, but were not designated as CRADA partners due to their support by the government. This report presents the complete details and results of the task force evaluation. A previous informal document provided details of the test plan used in this evaluation. Most of the details of that test plan are contained in this report.

Background

Conventional soldering processes typically use a rosin-based flux to remove oxides and other surface contaminants prior to soldering. If the residues from these fluxes are not removed from the solder assembly after soldering, they may lead to current leakage and possible corrosion failures. Low-residue (a.k.a. no-clean) soldering processes use flux chemistries designed to leave minimal, benign residues on the assemblies after soldering. Therefore, the need for a final cleaning can be eliminated, which significantly minimizes waste streams, reduces production time, and produces significant savings in cost of materials.

Goal of the LRSTF

The goal of the LRSTF was to conduct an evaluation of LR processes that encompassed the concerns of the tri-services with respect to acceptance of the LR technology. The LRSTF was well aware that process changes, such as the use of LR soldering, come about only through establishing an early understanding of customers' concerns. The LRSTF had a diverse membership to ensure that these concerns were considered during the planning stages of the program. In addition, the LRSTF actively solicited input from all concerned parties at each stage in the development of the test plan.

Test Plan Development

At its initial meeting, the LRSTF developed a list of possible requirements for its evaluation that included the following areas of interest: circuit characteristics, materials, circuit technology, solder processes, flux application, testing, and analysis. This list was refined through a series of conference calls and meetings among task force members. In addition, two open review meetings were held to solicit input from individuals outside the task force.

Test Vehicles

The LRSTF used three test vehicles in its evaluation. The primary test vehicle was an electrically functional assembly designed by the LRSTF to meet specific requirements originating from its members and from individuals attending the industry/military open review meetings. The assembly design was completed by Sandia engineers and contained the following circuitry: (1) high current and low voltage, (2) high voltage and low current, (3) high speed digital, and (4) high frequency. The design incorporated both plated through hole (PTH) and surface mount technology (SMT) components. Half the assemblies used polyimide as the substrate material and the other half used FR-4 epoxy. Half the assemblies were conformally coated and half were cleaned. The IPC-B-24 board was selected for surface insulation resistance (SIR) testing since this board was readily available, has been widely studied, was inexpensive, and is an industry standard. The MIL-I-46058C test coupon was used for testing conformal coating adhesion.

Texas Instruments, Hughes Electronics, Alliant Techsystems, and AlliedSignal each produced 80 printed wiring assemblies (PWAs) with their LR processes. In addition, AlliedSignal produced 40 PWAs with rosin mildly activated (RMA) processing to serve as a control for the experiment. *Each site received only five "practice" boards to check out their LR processes, which deprived them of the opportunity to optimize their processes as would be done in a normal production mode.*

Half the assemblies were subjected to three weeks of environmental stress screening (ESS) at 85°C and 85% relative humidity. During the first week of environmental

conditioning, a 5-volt bias was applied to the high speed digital circuits and a 500-volt bias was applied to the high voltage circuits for 1 hour a day. Electrical measurements were recorded before ESS and at the end of each week of ESS. A brief summary of the test results is now given.

High Current Low Voltage

Five amperes were applied to parallel PTH and SMT resistor networks and the resulting voltages were measured. All LR test boards behaved similarly to the RMA control group. Conformally coated boards had slightly higher voltage readings than the uncoated boards at pre-test. Two LR PWAs were just above the test criterion for increase in voltage at the end of week 1 of ESS, but were within the criterion at the conclusion of ESS.

High Voltage Low Current

Five hundred volts were applied to series PTH and SMT resistor networks and the resulting currents were measured. All LR PWAs gave results comparable to the RMA control group. Sixteen PWAs (including RMA controls) gave readings outside the interval for expected circuit performance, but none were due to the solder process.

High Speed Digital

A 25 ns pulse was applied to the inputs of PTH and SMT high-speed integrated circuits and the output pulse rise and fall times were measured. Performance of the Texas Instruments boards was equivalent to RMA throughout the test and the AlliedSignal LR boards had somewhat longer rise and fall times than RMA. Hughes Electronics and Alliant Techsystems LR boards had significantly greater variability during pre-test and week 1 electrical tests; however, the variability decreased with time.

High Frequency Low-Pass Filters

A 50 MHZ to 1 GHz sine wave was applied to PTH and SMT three-stage low pass filters and the output responses were measured. The performance of the LR boards was comparable to the RMA boards and all groups were well within the stated test criterion and behaved in a similar manner throughout the test.

High Frequency Transmission Line Coupler

A 50 MHz to 1 GHz sine wave was applied to a transmission line coupler and the forward and reverse null responses were measured. All forward measurements were within the stated criterion. One LR board slightly exceeded the test criterion for the reverse null response at pre-test, but did not do so during the remaining tests. The performance of the LR boards was comparable to the RMA boards, but the measurement repeatability was better for LR than for RMA with the exception of Alliant Techsystems, which was similar to RMA. Lack of repeatability is a performance and reliability issue; indicating that LR may be superior to RMA for high-frequency circuits.

Other Circuits

Five volts were applied to a pin grid array and to 10-mil spaced pads on the board and the leakage current was measured. All the boards performed essentially the same except the RMA boards exhibited more variability at pre-test. The presence of solder mask decreased the variability of the RMA boards.

SIR Test Results

Overall SIR test results for LR processes were comparable to RMA even though the LR processes were not optimized. Boards processed by Hughes had high levels of ionics, but ironically produced the highest average SIR performance over all processing groups.

Coating Adhesion

Coating adhesion ratings for wave and hand LR solder processes were essentially the same as RMA. The lowest ratings occurred for some of the LR reflow processes.

Ionics

Three of the four LR sites had lower ionic contamination than RMA when the boards were cleaned. In addition, the Texas Instruments LR boards without cleaning had lower ionics than RMA. Alliant Techsystems boards were equivalent to RMA. Hughes had high levels of ionics, but this did not translate to degraded performance.

Conclusions

The performance of the LR boards was comparable to the RMA control boards in all electrical tests, even though the LR processes were not optimized. Test results were not influenced by type of substrate; cleaning had little noticeable impact on the performance of the LR boards; and good conformal coating adhesion was achieved without cleaning.

Table of Contents

List of Abbreviations

AC	alternating current
AS	AlliedSignal
AT	Alliant Techsystems
BW	bandwidth
CFC	Chlorofluorocarbons
CMOS	complimentary metal oxide semiconductor
CRADA	Cooperative Research and Development Agreement
CSL	Contamination Studies Laboratories, Inc.
DC	direct current
DI	deionized
DIP	dual in-line package
DOD	Department of Defense
DOE	Department of Energy
ECM	electrochemical migration
EMPF	Electronics Manufacturing Productivity Facility
EPA	Environmental Protection Agency
ESD	electrostatic discharge
ESS	environmental stress screening
GLM	general linear model
GW	gull wing
HCLV	high current low voltage
HE	Hughes Electronics
HF	high frequency
HSD	high speed digital
HVLC	high voltage low current
IC	integrated circuit
IPA	isopropyl alcohol
IPC	Institute on Interconnecting and Packaging of Electronic Circuits
IQR	interquartile range
IR	infrared
IWRP	Industrial Waste Reduction Program
LC	inductor capacitor
LCC	leadless chip carrier
LPF	low pass filters
LR	low-residue
LRSTF	Low-Residue Soldering Task Force
NAWC	Naval Air Warfare Center
ODC	ozone-depleting chemical
OUM	oscillating ultrasonic mister
PGA	pin grid array
PTH	plated through hole
PWA	printed wiring assembly
PWB	printed wiring board
RH	relative humidity
RMA	rosin mildly activated
SIR	surface insulation resistance
SMT	surface mount technology
TI	Texas Instruments
TLC	transmission line coupler
UV	ultraviolet
WOA	weak organic acids

Trademark and Product Names

The following trademark and product names appear in this report.

AMI Presco
Binks
CAM/ALOT
Contract Systems
Contronic Devices
Corpane
Despatch
Dexter
Dow Corning
Electronic Control Devices
Electrovert
ESP
Fuji
Harwil
Hollis
Humiseal
Indium
Ionograph
Kapak
Keithley
Kester
KIC Prophet
Leister
Metcal
Multicore
Oakite OkemClean
Pace Craft
PC Flex Mask
Praxair
SEHO USA Inc.
SPT International
TDK
TechForm Labs
Triebe
Unger
Universal Instruments
Vitronics
Weller

1. Introduction

1.1 Background

Conventional soldering processes typically use a rosin-based flux to remove oxides and other surface contaminants prior to soldering. If the residues from these fluxes are not removed from the solder assembly after soldering, they may lead to current leakage and possible corrosion failures. A presidential mandate to eliminate the production of ozone-depleting substances by the end of 1995 and US EPA labeling requirements in compliance with the Clean Air Act of 1990 have forced many companies and organizations to adopt alternate processes that do not use ozone-depleting chemicals (ODCs). Semi-aqueous cleaning is an alternative cleaning method that has been offered for those who want to continue to use rosin fluxes. Another alternative is water soluble fluxes, but these fluxes still require a cleaning operation and produce a waste stream. Low-residue (a.k.a. no-clean) fluxes provide yet another alternative. These latter fluxes can eliminate the need for cleaning of electronic equipment after assembly.

1.2 Low-Residue Soldering Task Force (LRSTF)

The LRSTF combined the efforts of industry, military, and government to evaluate low-residue soldering processes for military and commercial applications. These processes were selected for evaluation because they provide a means for the military to support the presidential mandate while producing reliable hardware at a lower cost.

This report presents the complete details and results of a testing program conducted by the LRSTF to evaluate low-residue soldering for printed wiring assemblies. A previous informal document provided details of the test plan used in this evaluation. Many of the details of that test plan are contained in this report. The test data are too massive to include in this report, however, these data are available on disk as Excel spreadsheets upon request.

The LRSTF was managed by Sandia National Laboratories. The following organizations participated in the evaluation of low-residue soldering:

Sandia National Laboratories
Texas Instruments
Alliant Techsystems
Hughes Electronics
AlliedSignal / Kansas City Division
Naval Air Warfare Center at China Lake
Naval Air Warfare Center at Indianapolis
US Army - MICOM, Huntsville
US Air Force Materiel Command
Electronics Manufacturing Productivity Facility, Indianapolis

Sandia's participation in the program was funded by the Department of Energy through an Energy and Environment Technical Area Coordinating Team. This funding was used to purchase testing materials and to support AlliedSignal's participation in the program (AlliedSignal is a DOE production facility). Texas Instruments, Alliant Techsystems, and Hughes Electronics each signed Cooperative Research and Development Agreements (CRADAs) with Sandia, which formalized their participation and specified the amount of their contributions to the program. The other participants also made contributions to the program, but were not designated as CRADA partners due to their support by the government.

1.3 Low-Residue Soldering

Low-residue soldering processes use flux chemistries that leave minimal, benign residues on the assemblies after soldering. Therefore, the need for a final cleaning can be eliminated. This not only significantly minimizes waste streams, but also reduces production time and cost of materials. The task force built on previous programs and work that demonstrated the potential of low-residue soldering technology as a reliable, cost-effective alternative to the traditional rosin flux/solvent cleaning of electronic circuits in wave soldering applications. These programs include the following:

- CRADA evaluation by Sandia and Motorola (IWRP No. CR91-1026)
- EPA/IPC/DOD/Industry Ad Hoc Solvents Working Group Phase I Benchmark
- IPC Phase III No-Clean and Controlled Atmosphere Soldering Task Groups

1.4 Goal of the LRSTF

The goal of the LRSTF was to conduct an evaluation of low-residue processes that encompassed the concerns of the tri-services with respect to acceptance of the low-residue technology. The LRSTF was well aware that process changes, such as the use of low-residue soldering, come about only through establishing an early understanding of customers' concerns. The LRSTF had a diverse membership to ensure that these concerns were considered during the planning stages of the program. In addition, the LRSTF actively solicited input from all concerned parties outside the task force at each stage in the development of the test plan. The LRSTF held its first meeting on April 23, 1993 at the Texas Instruments facility in Lewisville, TX. As a first order of business, the following vision and mission statements were developed:

Vision: Eliminate Waste Streams in Military and Commercial Electronics Manufacturing Processes

Mission: Develop and Conduct a Test Plan that will Lead to Approval of Low-Residue Soldering Processes, Using Military Electronics Applications as the Vehicle

1.5 Test Plan Development

At the meeting in Lewisville, the LRSTF developed a lengthy *shopping list* of possible requirements for its evaluation. This list covered the following areas of interest: circuit characteristics, materials, circuit technology, solder processes, flux application, testing, and analysis. The LRSTF realized the impossibility of developing a test program that would meet everyone's requirements and agreed the test program should aim to satisfy 80% of the requirements. The LRSTF used the 80% rule to identify the key components on the original shopping list. This list was refined through a series of conference calls and meetings among task force members. In addition, two open review meetings were held to solicit input from individuals outside the task force. A complete list of the meetings of the LRSTF is as follows.

Lewisville, Texas - April 23, 1993
Subgroup Meeting at Scottsdale - June 10, 1993
Albuquerque - June 24, 1993
Dallas - July 15, 1993
Open Review Meeting in Dallas - July 16, 1993
Albuquerque - July 27-28, 1993
Minneapolis - October 12-13, 1993
Orlando - November 17, 1993
Albuquerque - December 6-7, 1993
Open Review Meeting in Albuquerque
December 8, 1993
Albuquerque - Jan 13-14, 1994
Dallas - Jan 20-21, 1994
Subgroup Meeting at the Electronics Conference
NAWC, China Lake - February 23-25, 1994
Subgroup Joint Planning Meeting at Motorola in
Scottsdale - March 23, 1994
McKinney, TX - May 24-25, 1994
Albuquerque - August 19, 1994
Albuquerque - September 28-30, 1994
Albuquerque - October 17-19, 1994
Albuquerque - November 7, 1994
Environmentally Conscious Soldering Conference
Albuquerque - November 8-9, 1994
Dallas - January 18-19, 1995
19th Electronics Manufacturing Seminar
China Lake - February 24, 1995

1.6 Overview of Test Vehicles

The task force decided to use three primary test vehicles in its evaluation of low-residue soldering. The vehicles are as follows.

LRSTF Assembly

The primary test vehicle was an electrically functional assembly designed to meet specific requirements originating from task force members and from individuals attending the open review meetings. This test assembly was designed by Sandia engineers with input from other task force members. The LRSTF test assembly has circuitry divided into four major sections:

- High current and low voltage
- High voltage and low current
- High speed digital
- High frequency

Each of these major sections has both plated through hole (PTH) and surface mount technology (SMT) components. Half the assemblies used polyimide as the

substrate material and the other half used FR-4 epoxy. The functional assembly is discussed in detail in the next section. Fabrication drawings and schematics for the functional assembly and a list of components are available upon request.

IPC-B-24 Board

The IPC-B-24 board was selected for surface insulation resistance (SIR) testing since this board was readily available, has been widely studied, and was inexpensive. Section 5 of this report presents the SIR test results.

MIL-I-46058C Test Coupon

The MIL-I-46058C test coupon (Para. 4.7.1.1) was used for testing conformal coating adhesion. Results of the coating adhesion tests appear in Section 6.

1.7 Technology Transfer

Many environmental and cost constraints have been placed on soldering processes used in the production of electronic equipment. These constraints include the following:

- A presidential mandate to eliminate production of ODCs by the end of 1995
- EPA labeling requirements for products manufactured with ODCs
- The international Montreal Protocol agreement
- Elimination or reduction of waste streams
- Declining budgets
- Cost of ODCs
- Energy consumption
- Factory floor space

These constraints have created a demand from industry for answers. In response to this demand, the LRSTF called on experience from many different sectors to formulate plans for the evaluation of low-residue soldering. The LRSTF has also undertaken efforts to transfer the low-residue technology to industry and to the military. Figure 1.1 illustrates the flow of technology transfer efforts for this project.

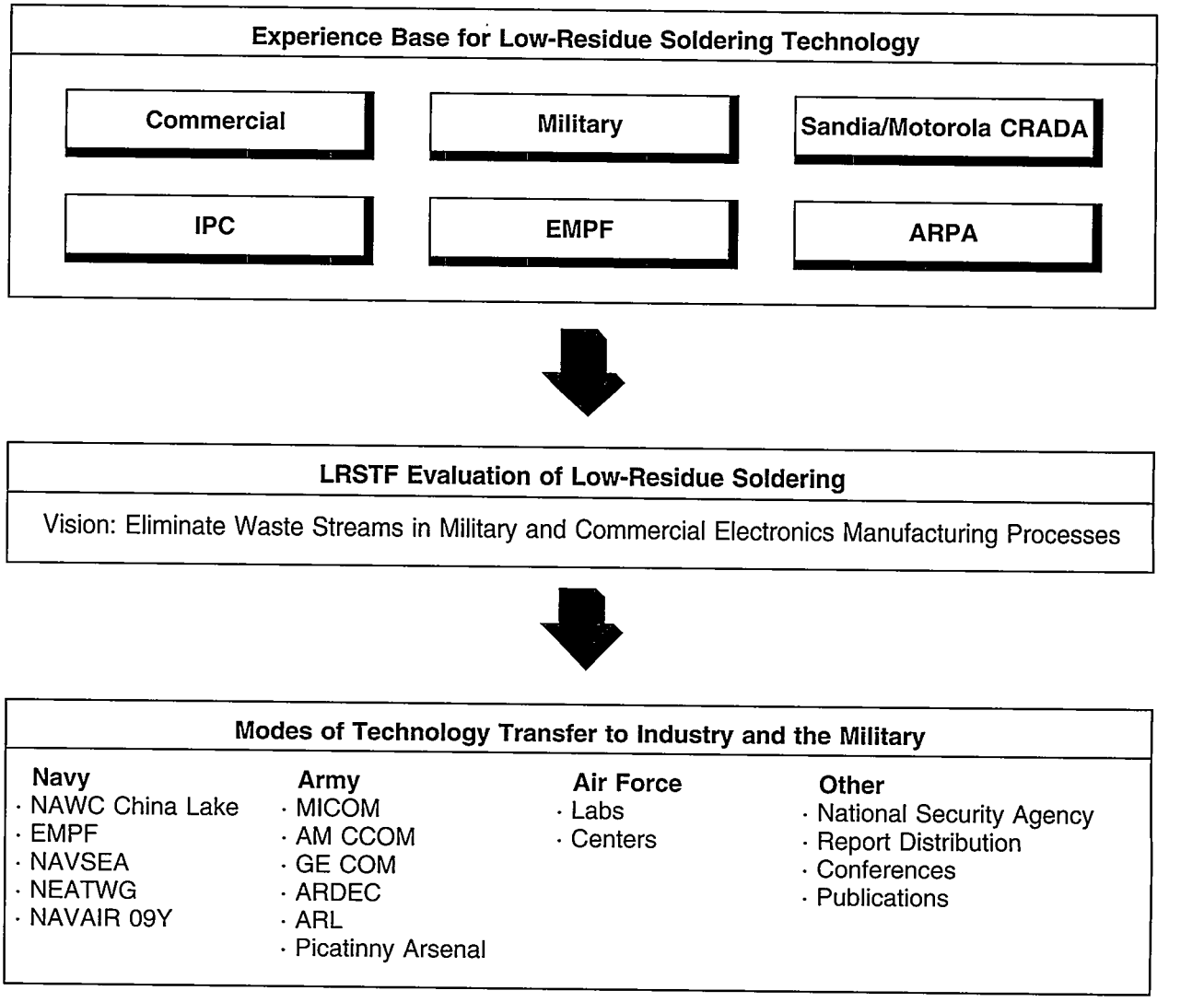

Figure 1.1 Low-Residue Technology Transfer Mechanism

2. The LRSTF Assembly and Board

2.1 Design of the LRSTF Printed Wiring Assembly

The primary test vehicle used in the LRSTF evaluation of low-residue technology was an electrically functional printed wiring assembly (PWA). This assembly was designed at Sandia based on input from task force members and input received during the open review meetings.

The PWA measured 6.05" x 5.8" x 0.062" and was divided into quadrants, each containing one of the following types of electronic circuits:

a. High current low voltage (HCLV)
b. High voltage low current (HVLC)
c. High speed digital (HSD)
d. High frequency (HF)

Each quadrant has subsections for PTH and SMT components, each forming separate electrical circuits. The layout of the LRSTF functional assembly is shown in Figure 2.1. Photos of both sides of the manufactured assembly are shown in Figures 2.2 and 2.3. The PWA also includes a large common ground plane, components with heat sinks, and mounted hardware.

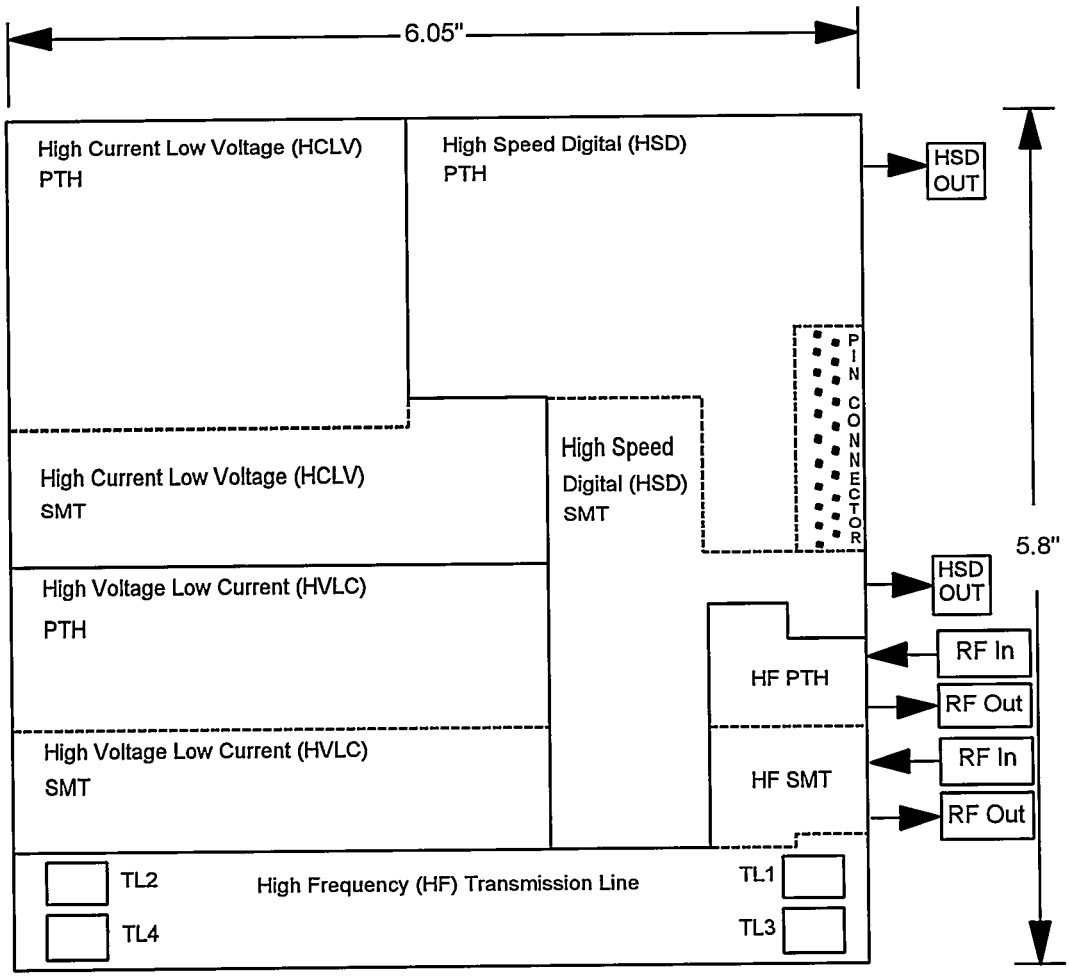

Figure 2.1 Layout of the PWA Illustrating the Four Major Sections and Subsections

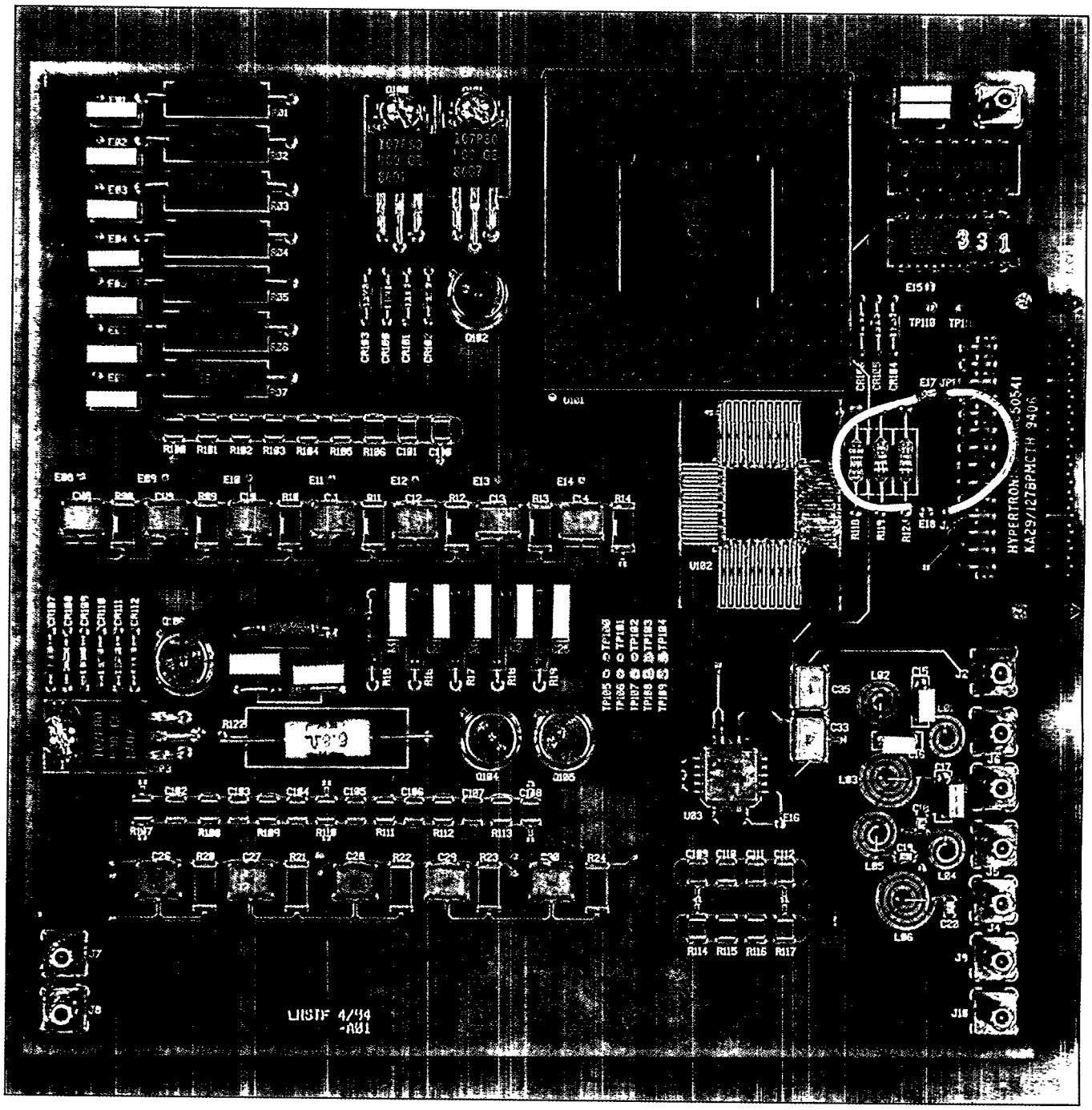

Figure 2.2 Top Side of a Manufactured LRSTF Assembly

Each subsection shown in Figure 2.1 contains both functional and nonfunctional components (added to increase component density). A 29-pin PTH edge connector was used for circuit testing. High frequency connectors were used to ensure proper impedance matching and test signal fidelity as required. Board fabrication drawings, schematics, and a complete listing of all components are available in separate cover.

Two board configurations were defined. The *01* configuration was electrically functional and was subjected to environmental and electrical testing. The *02* configuration (partially electrically functional) contained a nonfunctional

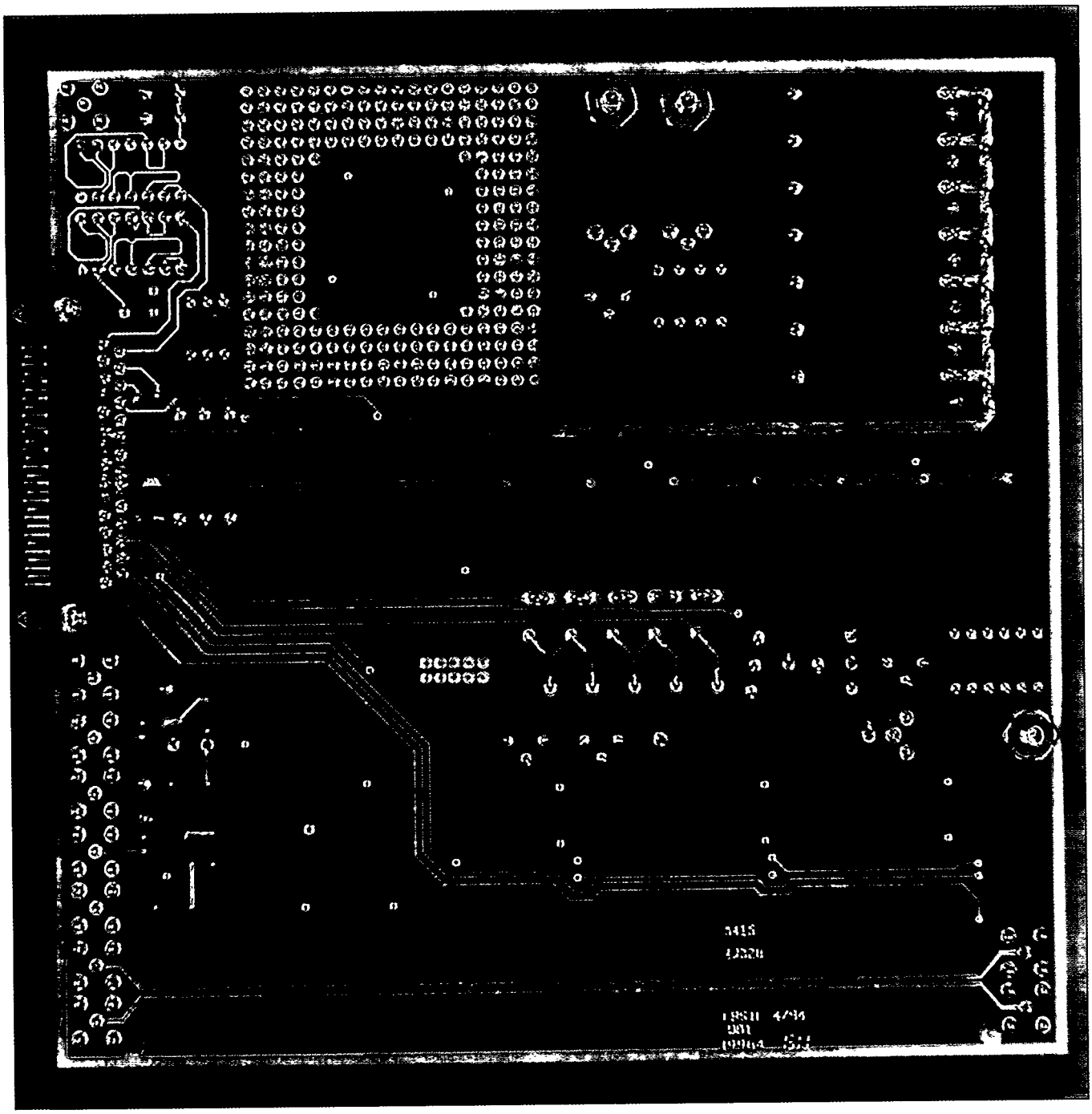

Figure 2.3 Bottom Side of a Manufactured LRSTF Assembly

SMT integrated circuit (IC), 10Ω in place of 10MΩ resistors in the HVLC/SMT subsection, and 30Ω in place of 10Ω resistors in the HCLV/PTH subsection. The *02* boards were subjected to ionic cleanliness, high pressure liquid chromatography (HPLC), and ion-chromatography testing, but not to environmental and electrical testing.

The material cost for each assembly was approximately $120 using full military specifications for the board and the functional parts. The Gerber files for the board design are available from Sandia National Laboratories upon a written request that includes the following:

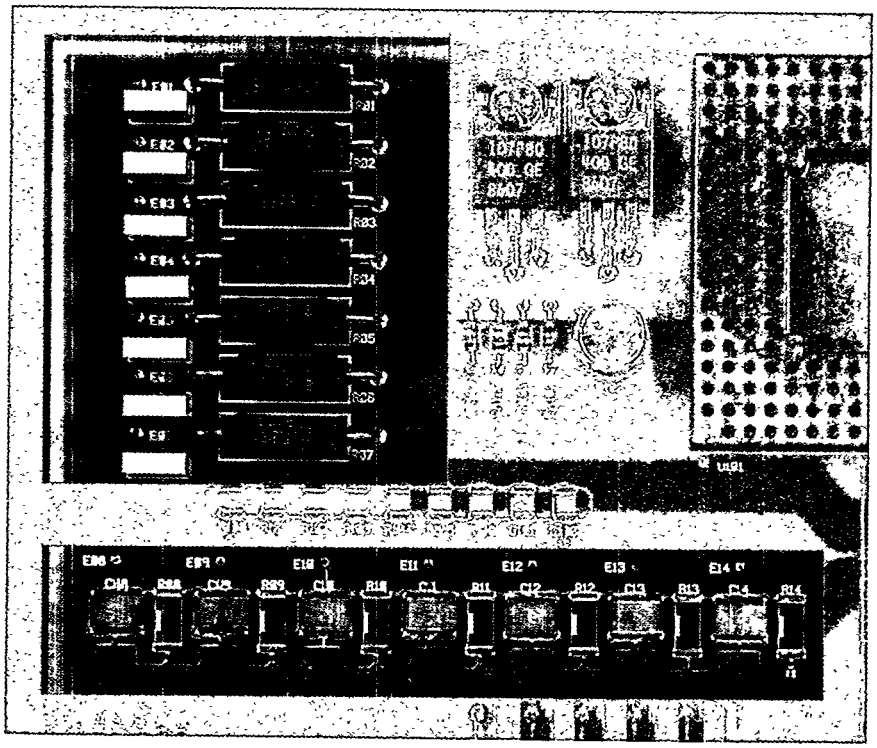

Figure 2.4 HCLV Subsection of the LRSTF PWA

- A brief statement of purpose
- Recognition of the LRSTF as the board designer in any formal reports
- Brief summary of any test results
- Notification of any board changes or recommendations

The following sections contain descriptions of the functional circuits.

2.2 High Current Low Voltage

The HCLV section of the board (upper left-hand quadrant of Figure 2.2) is shown in Figure 2.4. The vertical subsection in the corner contains PTH components and the horizontal subsection contains SMT components. Figure 2.5 shows a simplified schematic of the HCLV circuits.

Purpose of the HCLV Experiment

Performance of high-current circuits is affected by series resistance. Resistance of a conductor (including solder joints) is determined by the following equation:

$$R = \frac{\rho L}{A_C} \; ohms(\Omega) \qquad (2.1)$$

where ρ = resistivity, the proportionality constant

L = length of the conductor

A_C = cross-sectional area of the conductor (solder joints)

Resistance is most likely to change due to cracking or corrosion of the solder joint that may be related to the soldering process. These conditions decrease the cross-sectional area of the solder joints, thus increasing resistance as shown in Equation 2.1. Use of high current to test solder joint resistance makes detection of a change in resistance easier. A 5 Amperes (A) current was selected as a value that would cover most military applications. A change of resistance is most conveniently determined by measuring the steady state performance of the circuit, which will now be discussed.

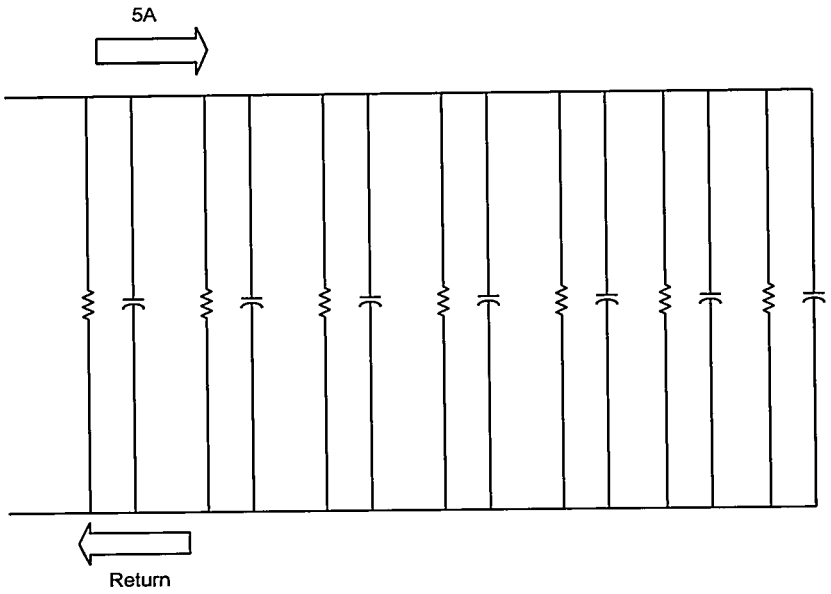

Figure 2.5 Simplified Schematic of the HCLV Subsection

Steady State Circuit Performance

Overall circuit resistance, R_{total}, is the parallel combination of the seven resistors, R_1, R_2, ..., R_7, used in the HCLV circuit:

$$\frac{1}{R_{total}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + \cdots + \frac{1}{R_7}$$

$$= \frac{7}{10\Omega} \text{ since all resistors} = 10\Omega \qquad (2.2)$$

$$R_{total} = \frac{10\Omega}{7} \qquad (2.3)$$

Since a current (I) of 5A was applied to the circuit, the resulting voltage (V), according to Ohm's Law, is

$$V = IR = 5A \times \frac{10\Omega}{7} = 7.14V \qquad (2.4)$$

Changes in resistance are thus detected by changes in voltage. However, a pulse width had to be chosen that would not over-stress the circuit components. With current equally divided among the seven parallel resistors, the power (P) dissipated in each resistor, according to Joule's Law, is:

$$P = I^2R = \left(\frac{5A}{7}\right)^2 \times 10\Omega = 5.1Watts(W) \qquad (2.5)$$

Since the power rating for the PTH wire-wound resistor is 3W, the rating is exceeded by a factor of 1.7 for steady state (5.1 ÷ 3). Design curves from the resistor manufacturer indicate the PTH wire-wound resistors could tolerate the excess power for about 100ms. The SMT resistors are rated at 1W, so the steady state rating is exceeded by a factor of five. With the manufacturer unable to provide the pulse current capability of the SMT resistors, a pulse derating factor could not be determined. A pulse width of 100µs was selected, which is three orders of magnitude less than the capability of the wire-wound resistors. This width is also sufficiently long for the circuit to achieve steady state before the measurement is taken.

Circuit Board Design

Traces carrying the 5A current were placed on an inner layer of the circuit board because: (1) the primary concern was the possible degradation of the solder connections as discussed above and (2) the bulk electrical characteristics (resistivity) of the traces should not be affected by flux residues. High-current trace widths were designed to be 250 mils whenever possible, following MIL-STD-275. This width with a 5A current should cause no more than a 30°C temperature rise under steady-state conditions.

The resistor and capacitor values were selected to be readily available. If other values are used, care should be taken to not over-stress the parts, as discussed above.

2.3 High Voltage Low Current

The HVLC circuitry is shown in Figure 2.6. The PTH circuitry is in the upper part of this subsection and the SMT circuitry is in the lower subsection. Figure 2.7 shows a simplified schematic of these circuits.

Purpose of the HVLC Experiment

Flux residues could decrease the insulation resistance between conductors. The impact of this decrease could be significant in circuits with a high voltage gradient across the insulating region. Decreased resistance can be detected by an increase in current when a high voltage is applied to the circuit. A voltage of 500V was selected as the high potential for this test, but the design specified intermediate voltages on some traces. The change in leakage current is determined by measuring the steady-state performance of the circuit, which will now be discussed.

Steady State Circuit Performance

Steady-state operation of the HVLC circuit can be determined by considering only the resistors. The total resistance of the series combination is the sum of the resistances:

$$R_{total} = R_1 + R_2 + R_3 + R_4 + R_5 \qquad (2.6)$$

$$= 50M\Omega \text{ since all resistors are } 10M\Omega \text{ each}$$

From Ohm's law, the current flowing into the circuit with 500V applied is

$$I = \frac{V}{R} = \frac{500V}{50M\Omega} = 10\mu A \qquad (2.7)$$

Care was taken to not over-stress the individual components in the circuits. The voltage stress across each resistor-capacitor pair is one-fifth of the applied 500V, or 100V. The voltage ratings are 250V for the PTH resistors, 200V for the SMT resistors, and 250V for all the capacitors. Power rating is not a concern due to the low current.

Circuit Board Design

High voltage traces were placed next to ground potential traces by design. The spacings between the high voltage and intermediate traces were selected using MIL-STD-275.

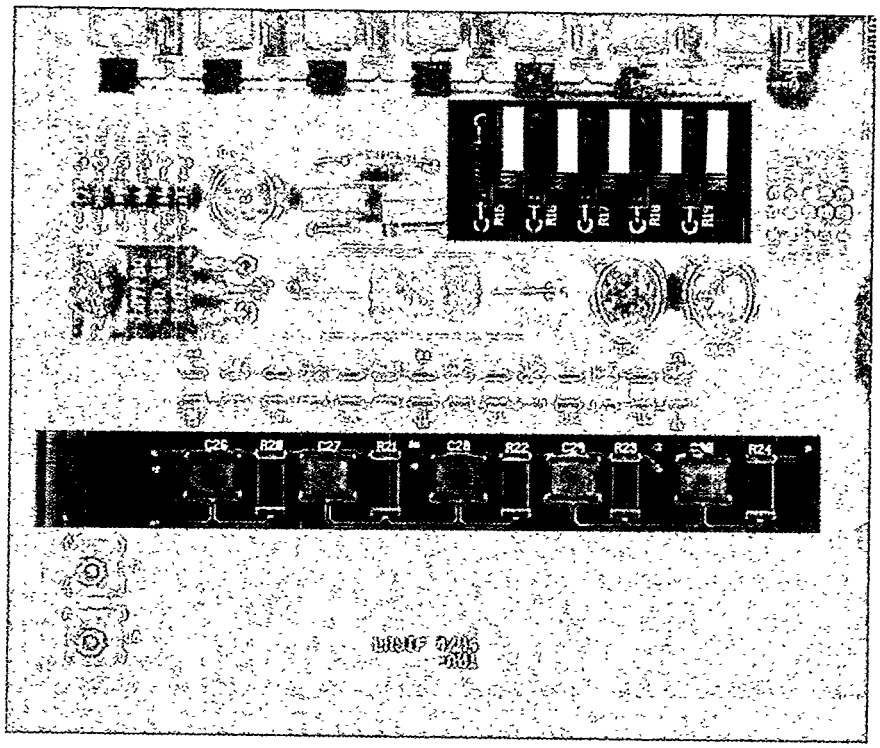

Figure 2.6 HVLC Subsection of the LRSTF PWA

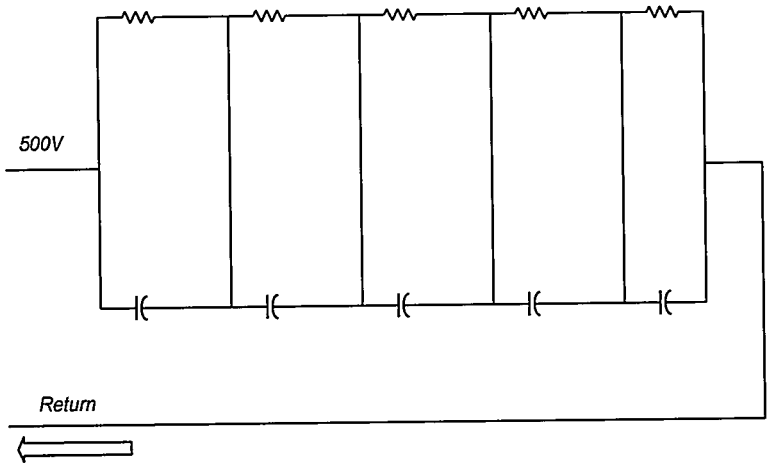

Figure 2.7 Simplified Schematic of the HVLC Subsection

Technology	Trace Connected to: Resistor	Capacitor	Potential (V)	Trace Length At Potential (in)	Spacing (mils)
PTH	R15	C21	500	0.8	30
			400	0.4	15
	R16	C22	400	0.4	15
			300	NA	
	R17	C23	300	NA	
			200	0.4	10
	R18	C24	200	0.4	10
			100	NA	
	R19	C25	100	NA	
SMT	R20	C26	500	5.0	30
			400	1.0	15
	R21	C27	400	1.0	15
			300	NA	
	R22	C28	300	NA	
			200	0.9	10
	R23	C29	200	0.9	10
			100	NA	
	R24	C30	100	NA	

NA = not applicable since no 100V or 300V traces were adjacent to ground potential

Figure 2.8 HVLC Circuit Board Trace Potentials

Voltage	Spacing Between Traces (mils)
0 - 100	5
101 - 300	15
301 - 500	30

These guidelines were followed except the 5-mil spacing, where 10 mils was used to facilitate board fabrication.

Figure 2.8 lists the voltage on various board circuit traces and the spacing to the adjacent ground trace.

Resistors and capacitors were selected to have readily available values — different values could have been used to achieve particular experimental goals. For instance, higher resistance values could be used with lower value capacitors. Reverse biased, low-leakage diodes could also be used for higher sensitivity to parasitic leakage resistance.

2.4 High Speed Digital

The HSD circuitry is shown in Figure 2.9. The subsection in the upper right-hand corner contains the PTH circuitry and consists of two 14-pin Dual In-line Package (DIP) integrated circuits (ICs). The SMT subsection IC is a single 20-pin leadless chip carrier (LCC) package. Each of these ICs is a "Fast" bi-polar digital "QUAD-DUAL-INPUT-NAND-GATE." Both subsections contain two ceramic capacitors that bypass spurious noise on the power input line (VCC) to the ICs and an output high-frequency connector. Inputs to both subsections are applied through the edge-connector on the right side of the board. Figure 2.10 shows a simplified schematic of the ICs.

Purpose of the HSD Experiment

The output signal of each gate in Figure 2.10 is opposite in polarity to the input signal. If the traces of these two signals are in close proximity on the printed circuit board (capacitively coupled), the gate switching speed might be affected by the presence of flux residues. A 5VDC bias was applied to the VCC inputs during environmental testing to accelerate aging. One PTH IC (U02) was hand soldered during assembly at each site to introduce hand solder flux residue in the experiment.

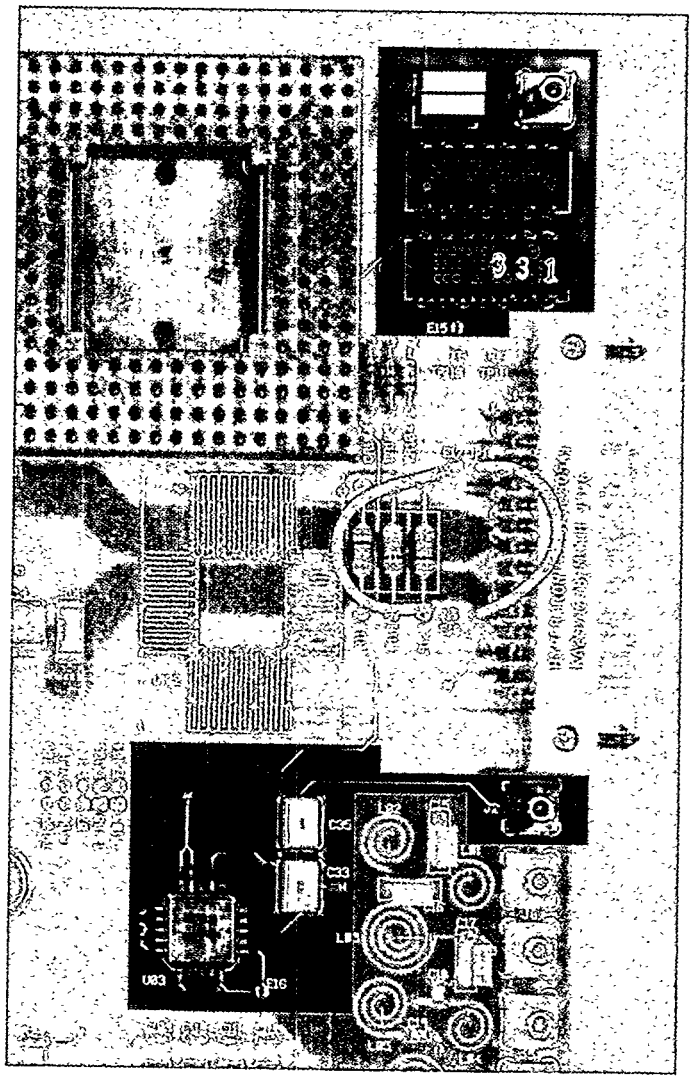

Figure 2.9 HSD Subsection of the Functional PWA

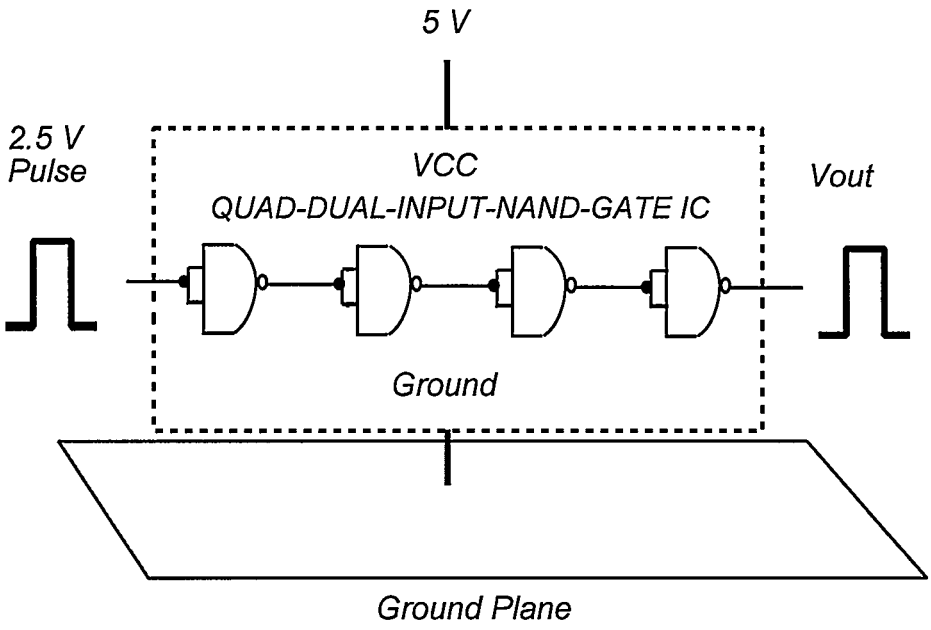

Figure 2.10 Simplified Schematic of the ICs in the HSD Subsection

Circuit Description

The schematic in Figure 2.10 represents the ICs in the PTH and SMT subsections. The ICs are random logic circuits that are NAND (Not AND) gates. An AND gate's output is high only when all inputs are high. The logic of a NAND gate is opposite the logic of an AND gate. Therefore, the output of a NAND gate is low only when all inputs are high, otherwise the output is high. With the two connected inputs, the output of each gate is opposite the input. Since the four gates are connected in series, the output of the last gate is the same logic level (high or low) as the input, with a slight lag.

The output pulse does not change logic levels instantaneously, but the switching times from low to high (rise time) and from high to low (fall time) should be less than 7ns. ICs should perform within these criteria if the VCC input is 5 ± 0.5V DC, the output load does not exceed specifications, and the circuit has a proper ground plane as shown in Figure 2.10.

The HSD circuits also provide an intermediate test for high frequencies, with switching time dictating a high frequency spectrum. The frequency spectrum of switching circuits can be expressed in terms of bandwidth (BW). For a switching circuit, the respective BWs (in Hertz) for rise (t_r) and fall (t_f) times are:

$$BW_r = \frac{0.35}{t_r}\ Hz \quad \text{and} \quad BW_f = \frac{0.35}{t_f}\ Hz \qquad (2.8)$$

Bipolar technology was used rather than a complementary metal oxide semiconductor (CMOS) since it is not as vulnerable to electrostatic discharge (ESD) damage. Available military bipolar technologies have the following typical switching speeds and bandwidths:

Technology	Typical $t_{r\ or\ f}$ (ns)	Bandwidth (MHz)
5404 TTL	12	29
54LS04 Low Power Schottky	9	39
54S04 Schottky	3	117
54F04 Advanced Schottky (Fast)	2.5	140

The Fast technology was selected since it had the shortest switching time and largest bandwidth, which provides the widest frequency spectrum for this test.

Circuit Board Design

In some cases, good design practice was purposely violated in the layout of these circuits to provide a more strenuous test. For example, the output trace of each gate was placed beside the input trace for a short distance at a spacing of 10 mils, producing as much capacitive coupling as possible. The SMT IC output trace was also routed under the two VCC bypass capacitors to see if flux residues trapped under the capacitors would increase rise and fall times.

Ground planes were provided for proper circuit operation of the ICs. The PTH subcircuit utilized the large common ground plane on layer 3 since most of the input and output traces are on layer 4. Since the SMT circuit traces are on the top layer, a smaller ground plane was added on layer 2. The "QUAD-DUAL-INPUT-NAND-GATE" was selected since other solder studies of national attention have used that particular type of IC, which makes direct comparisons with these studies possible.

2.5 High Frequency

The HF section shown in Figure 2.11 contains two major subsections, the low-pass filters (LPF) and the transmission line coupler (TLC). Figure 2.12 shows a simplified schematic of the LPF subsection. The TLC traces on layer 4 of the board are shown in Figure 2.13. The LPF/PTH subsection is above the LPF/SMT subsection as shown in Figure 2.11. Each of these subsections has discrete ceramic capacitors and three inductor-capacitor (LC) filters, with the inductor printed on the circuit board in a spiral pattern. The HF circuits allow evaluation of circuit performance up to 1GHz (1000MHz).

Purpose of the High Frequency Experiment

Flux residues may affect the performance of LPF printed circuit inductors and transmission lines due to parasitic resistances and parasitic capacitances. These inductors were purposely covered with flux during surface-mount solder processing to increase the presence of residues. Since the transmission lines are separated by only 10 mils, flux residues between the lines may affect their performance.

LPF Circuit Description

An inductor-capacitor (LC) LPF consists of a series inductor followed by a shunt capacitor as shown in Figure 2.12. A low-frequency signal passes through the LPF without any loss since the inductor acts as a short circuit and the capacitor acts as an open circuit for such signals. Conversely, a high-frequency signal is blocked by the LPF since the inductor acts as an open circuit and the capacitor acts as a short circuit for such signals.

When a sine wave test signal is passed through an LPF, its amplitude is attenuated as a function of frequency. The relationship between the output and input voltage amplitudes can be expressed as a transfer function. The transfer function, V_{out} / V_{in}, was measured to determine any effects of the low-residue fluxes.

The transfer function is measured in decibels (dB) as a function of frequency. A decibel can be expressed in terms of voltage as follows:

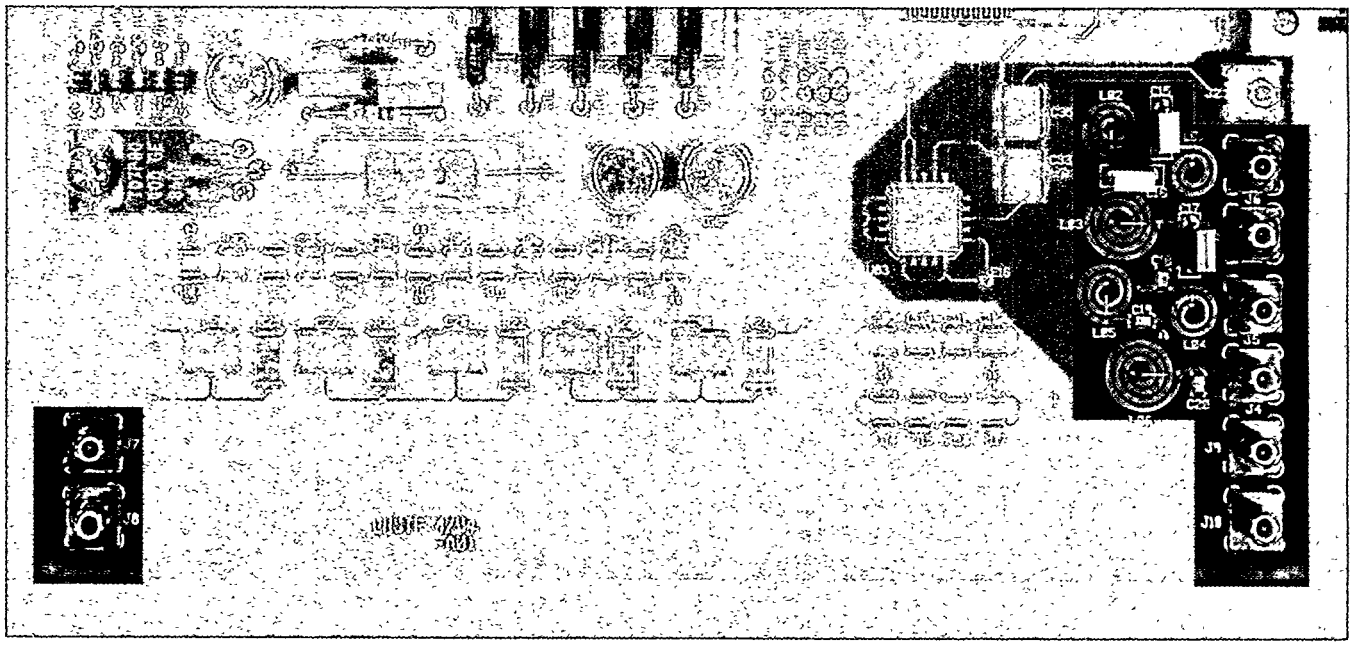

Figure 2.11 HF Subsection of the Functional PWA

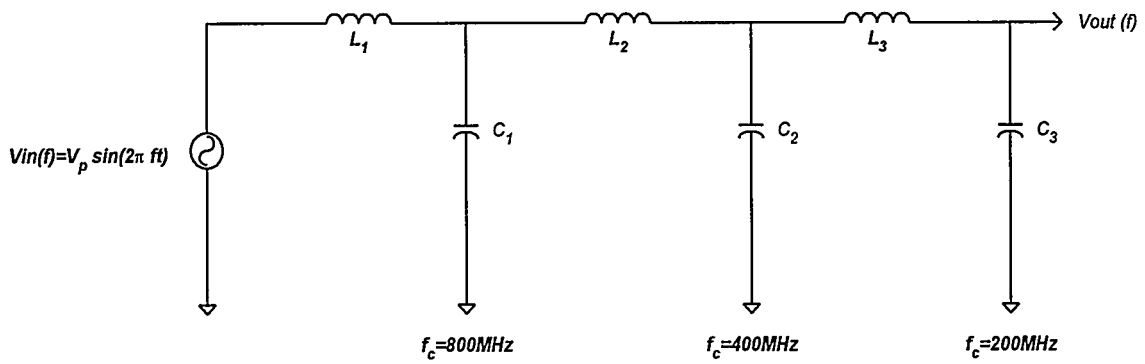

Figure 2.12 Simplified Schematic for the HF/LPF Subsection

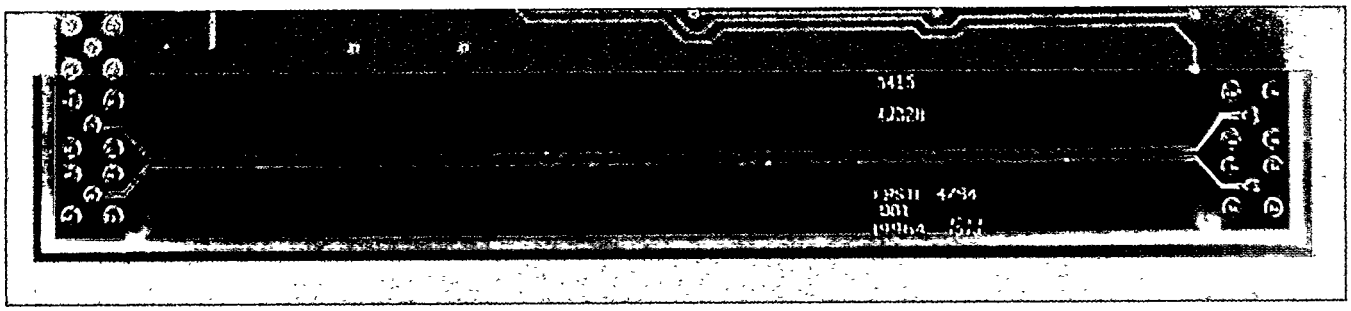

Figure 2.13 Location of HF/TLC Traces on Layer 4

$$dB = 20\log_{10}\left(\frac{|V_{out}|}{|V_{in}|}\right) \qquad (2.9)$$

The PTH transfer function differs from the SMT transfer function due to the self inductance of the capacitor through-hole leads. Figure 2.14 shows plots of typical LPF/SMT and LPF/PTH measured transfer functions.

LPF Circuit Board Design

The three LC LPFs for each of the SMT and PTH circuits were designed to have the following cutoff frequencies: 800, 400, and 200 MHz. Cutoff frequency is that frequency for which the transfer function is -3 dB. The respective component values chosen for the LC filters are 16 nH (nano-Henries) and 6.4 pF (pico-Farads), 32 nH and 13 pF, and 65 nH and 24 pF. Most LPF circuitry was placed on Layer 1, with Layer 2 used as a ground plane. Crossovers needed to connect the LPF circuits are on Layer 4.

The LPF circuits were designed to operate with a 50Ω test system, so all interconnect traces longer than 0.10 in were designed as 50Ω transmission lines to avoid signal distortion. The LPF circuits were predicted to have less than 2 dB loss below 150 MHz, approximately 6 dB loss near 235 MHz, and greater than 40 dB loss at 550 MHz and beyond. The measured response of the LPF/SMT circuit is close to that predicted except that the transfer function decreases more rapidly than predicted above 350 MHz . As stated previously, the PTH circuit transfer function did not perform similarly to the SMT, particularly at frequencies above 150 MHz (see Figure 2.14).

TLC Circuit Description

Figure 2.15 shows a diagram of the TLC subsection. The LPFs described above are *lumped element* circuits since the capacitors are discrete components. The TLC lines are *distributed element* circuits with the resistors, inductors, and capacitors distributed along the lines. A circuit model for the lines is shown in Figure 2.16.

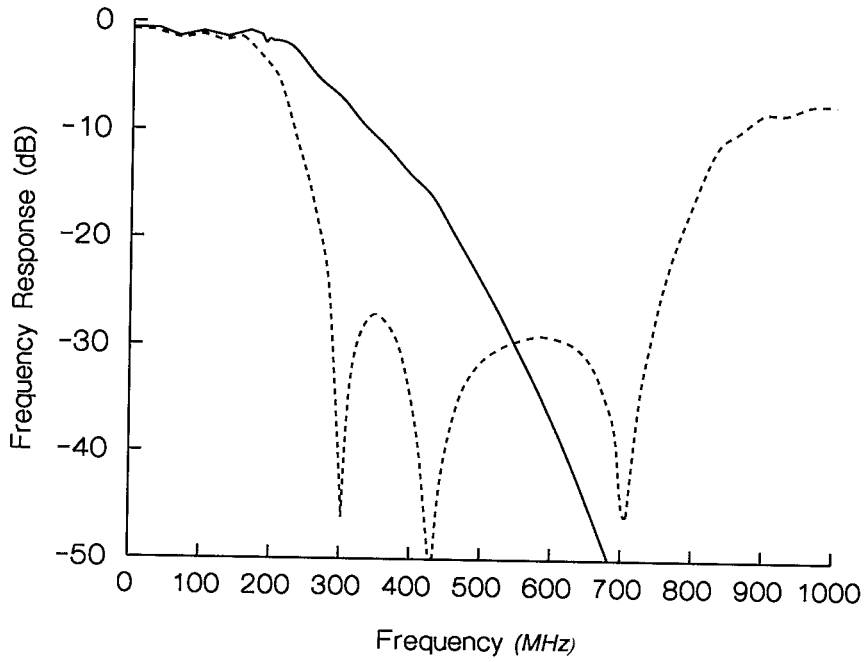

Figure 2.14 Measured Transfer Functions for LPF/SMT (solid line) and LPF/PTH (dashed line)

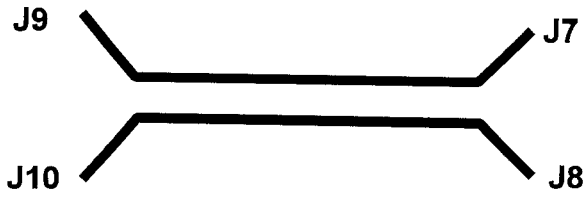

Figure 2.15 Diagram of the HF/TLC Subsection

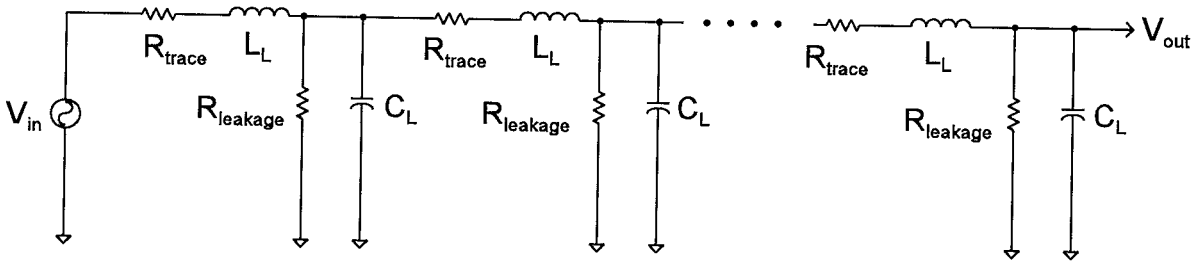

Figure 2.16 HF/TLC Distributed Element Model

The inductance and capacitance for a transmission line with a ground plane are, respectively:

$$L_L = 0.085 R_0 \sqrt{\epsilon_r}\ nH/in \qquad (2.10)$$

$$C_L = \frac{85}{R_0} \sqrt{\epsilon_r}\ pF/in \qquad (2.11)$$

where R_0 = characteristic resistance and ϵ_r = dielectric constant of the board material.

The TLC R_0 was designed to be 50Ω for operation with a 50Ω test system. For FR-4, L_L is about 9.6 nH/in and C_L is about 3.8 pF/in. The inductance and capacitance for polyimide were similar to those for FR-4.

The TLC was tested with a sine wave signal similar to the one used in testing the LPFs. The source resistance was 50Ω and the three output terminals were connected to 50Ω loads. The measured forward coupling frequency response from connector J9 to connector J8 is shown as the solid line in Figure 2.17 and the reverse coupling frequency response from J9 to connector J10 is shown as the dashed line.

TLC Circuit Board Design

The transmission line coupler (TLC) circuit has a pair of coupled 50Ω transmission lines with required measurable performance frequencies less than 1000 MHz. Layer 4 of the printed wiring board (PWB) was used to route the TLC circuit, with Layer 3 used as the ground plane. The TLC circuit is a 5-in long pair of 0.034-in wide 50Ω transmission lines spaced 0.010 in apart. The circuit design incorporated the board dielectric constant of about 4.8 and the .020-in spacing between copper layers. A computer-aided circuit design tool (Libra) was used to model the TLC circuit. Performance measured on a test PWB agreed very closely with the forward and reverse coupling predictions between 45 MHz and 1000 MHz.

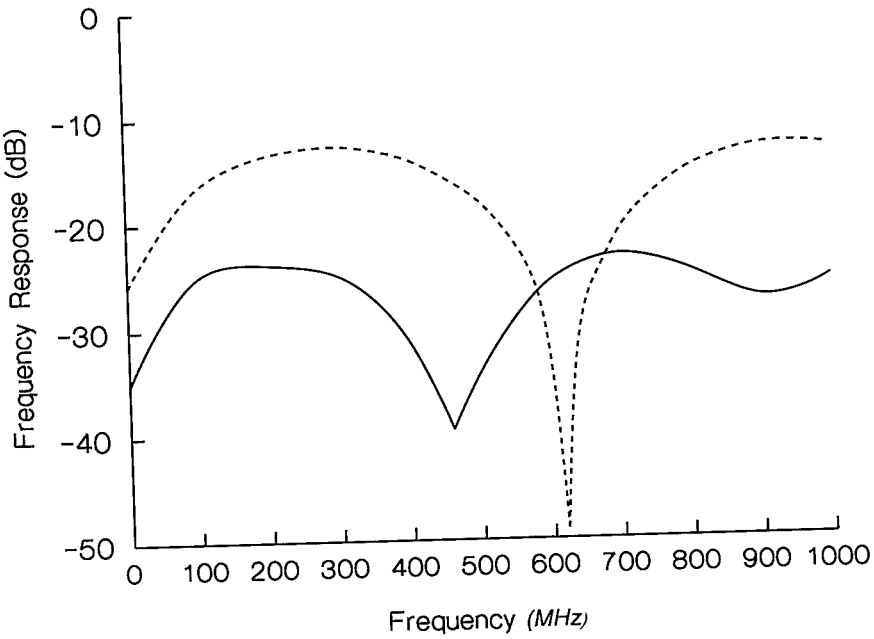

Figure 2.17 TLC Forward Coupling Frequency Response (solid line) and TLC Reverse Coupling Frequency Response (dashed line)

2.6 Other Networks (Leakage Currents)

The LRSTF board also contains three test patterns to provide tests for current leakage: (1) the pin grid array (PGA), (2) the gull wing (GW), and (3) 10-mil spaced pads. Figure 2.18 shows the location of these test patterns. A 5V source was used to generate leakage currents.

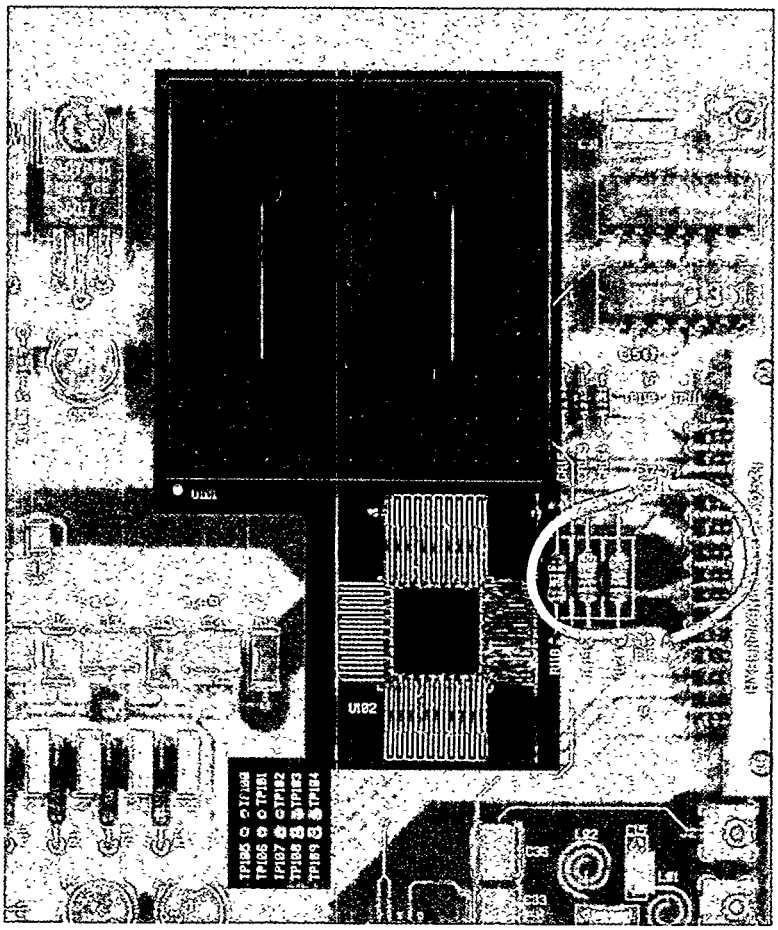

Figure 2.18 Location of Other Networks

Purpose of the Experiments

The PGA, GW, and 10-mil pads allow leakage currents to be measured on test patterns that are typical in circuit board layouts. These patterns contain several possible leakage paths and the leakage could increase with the presence of flux residues and environmental exposure. In addition, solder mask was applied to portions of the PGA and GW patterns to evaluate its effect on leakage currents and the formation of solder balls.

Pin Grid Array

The PGA hole pattern has four concentric squares that are electrically connected by traces on the top layer of the board as shown in Figure 2.19. The pattern also has four vias just inside the corners of the innermost square that are connected to that square. Four vias were also placed inside the innermost square to trap flux residues. Two leakage current measurements were made: (1) between the two inner squares (PGA-A) and (2) between the two outer squares (PGA-B), as shown in Figure 2.19. Solder mask covers the holes of the two outer squares on the bottom layer, allowing a direct comparison of similar patterns with and without solder mask.

Rather than an actual PGA device, a socket was used since it provided the same soldering connections as a PGA. Also, obtaining leakage measurements on an actual PGA is nearly impossible due to complexity of it internals semiconductor circuits.

Gull Wing

The upper half of the topmost GW lands and the lower half of the bottommost GW lands were covered with solder mask to create a region that is susceptible to the formation of solder balls. The lands were visually inspected to detect the presence of solder balls.

A nonfunctional GW device was planned to be soldered to the lands with alternating lands connected to provide a land leakage measurement. The lengths of the top and bottom lands were sufficient to allow a GW device to be

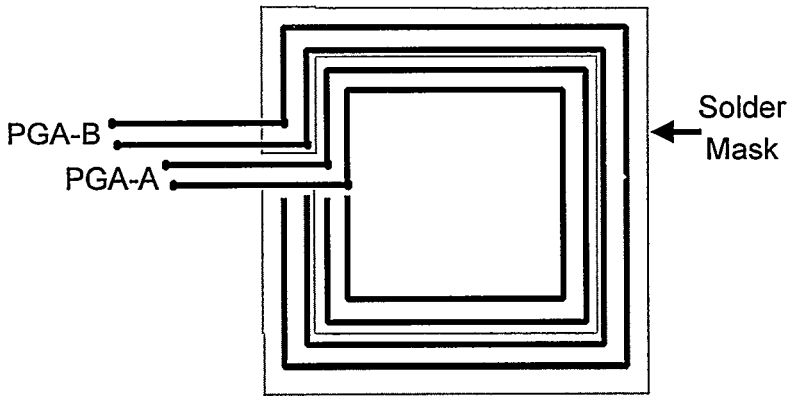

Figure 2.19 PGA Hole Pattern With Solder Mask

mounted without interference from the solder mask. The board was designed for GWs with 25-mil pitch, but the GW device that was received had a 25.6-mil pitch and there was insufficient time to find a replacement. Thus, the GW device was left off the finished PWA and this portion of the experiment was not conducted. The board layout has been revised to the 25.6-mil pitch for future experiments.

10-mil Pads

The 10-mil pads were laid out in two rows of five pads each. The pads within each row were connected on the bottom layer of the board and leakage between the rows was measured.

2.7 Stranded Wires

Two 22-gauge stranded wires were hand soldered just to the left of the edge connector as shown in Figure 2.20. One wire was soldered directly into the board through holes and the other was soldered to two terminals, E17 and E18. One end of each wire connects to the ground plane (layer 3). Each wire was 1.5 in long, was silver coated, and had white PTFE insulation. All wires were stripped, tinned, and cleaned by the EMPF in preparation for the soldering process.

Purpose of the Stranded Wire Experiment

Stranded wires were used to evaluate flux residues and subsequent corrosion. Electrical tests were added using the 100 µs 5A constant current source used for testing the HCLV circuit.

Circuit Description

A diagram of the circuit is shown in Figure 2.21. A voltage measurement was taken by probing between the edge connector pins and grounded shell of the high-frequency connector J1 — the points closest to the wires. The procedure bypassed the significant voltage drop across the test cable.

2.8 Nonfunctional Parts

Locations of the nonfunctional parts are shown in Figure 2.22. These parts were used to fully populate the board, to provide information on component-induced ionic or organic contamination, and to serve as possible flux residue traps. A variety of part types was used, including power transistors that required mounting hardware to the board. Nonfunctional parts were not procured to meet military specifications.

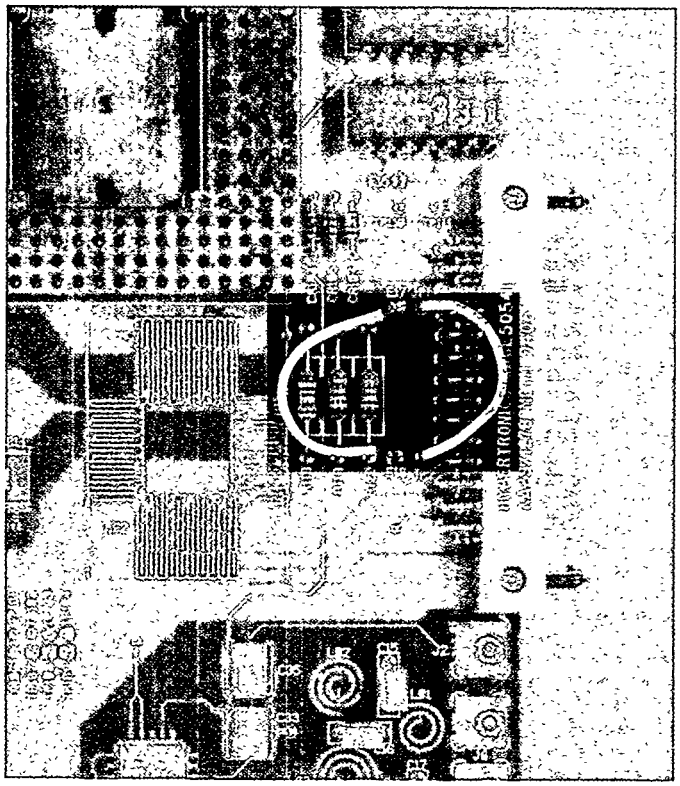

Figure 2.20 Location of Stranded Wires

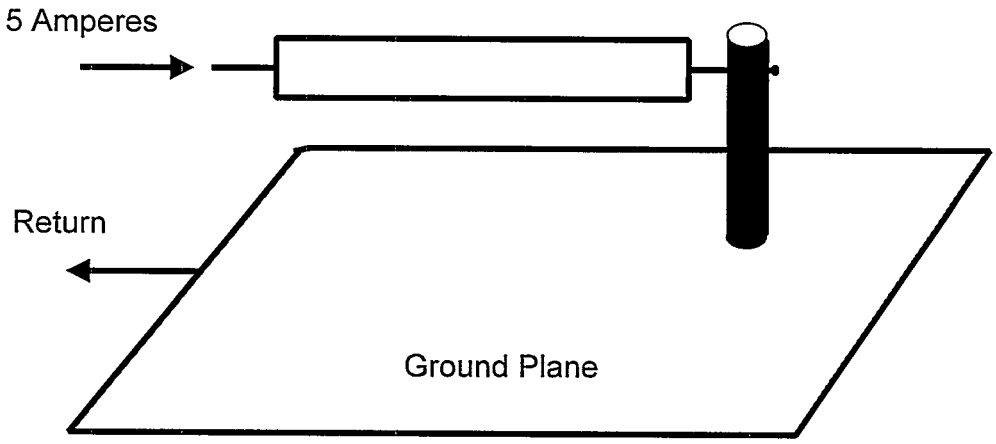

Figure 2.21 Diagram of the Stranded Wire Circuit

2.9 Components

All functional component types conformed to military specifications and were ordered pre-tinned (to the extent possible). All ICs used on the *01* boards were electrically tested upon receipt. Sandia performed incoming inspection of all functional components (five samples per component type). Components were not pre-cleaned before use. Each component type was tested using ion chromatography to document incoming cleanliness levels.

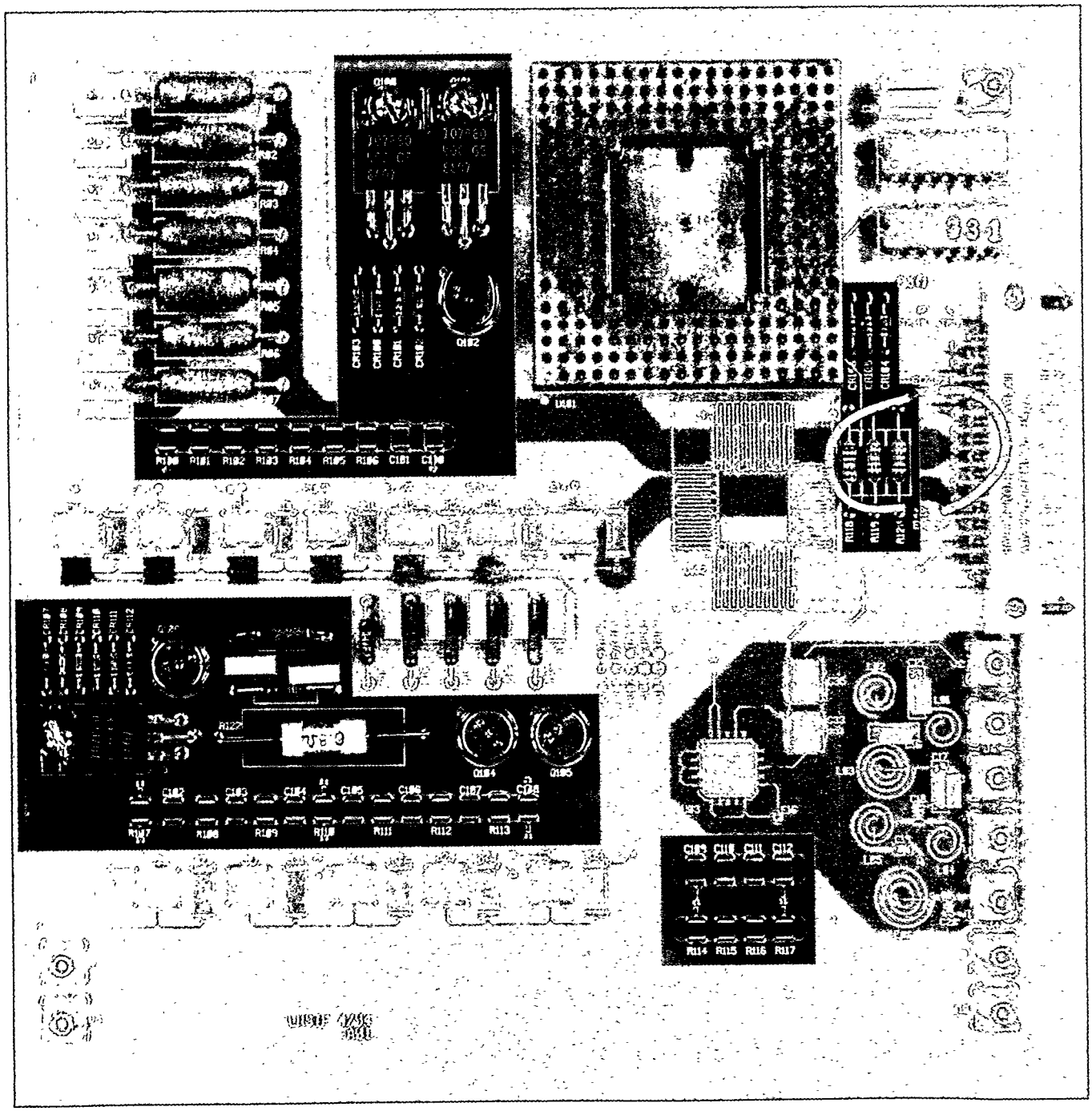

Figure 2.22 Nonfunctional Components on the PWA

Solderability testing was performed using dip and look testing per MIL-STD-202, Method 208 with type R flux per MIL-F-14256. Several nonfunctional components did not pass solderability testing, but were not replaced due to scheduling constraints. All functional components were required to pass solderability testing.

2.10 Boards

The four-layer LRSTF PWBs had exposed traces on both sides and were manufactured to meet the requirements of MIL-P-55110. The substrate material for half the boards was FR-4 epoxy and the other half was polyimide. Starting copper weight was 1 ounce per square foot. The boards were tin/lead plated and reflowed (hot air leveled).

An ionic cleanliness level of 5 or less $\mu g/in^2$ NaCl equivalence was specified. A sample of incoming PWBs did not satisfy cleanliness requirements as measured by an Ionograph 500 at the EMPF. Subsequently, all boards were shipped to the EMPF for in-line machine cleaning with heated deionized (DI) water.

3. Processing at the Four Test Sites

3.1 An Overview of the Assembly and Processing Operations

As noted in Section 1.6, the LRSTF evaluation of the low-residue technology utilized three test vehicles: the LRSTF functional assembly, the IPC-B-24 board for surface insulation resistance testing, and the MIL-I-46058C Y-coupon for evaluating coating adhesion. The assembly and soldering of these vehicles were performed at four low-residue sites: Texas Instruments, Hughes Electronics, Alliant Techsystems, and AlliedSignal. Each site produced 80 LRSTF assemblies, 30 IPC-B-24 boards, and six MIL-I-46058C Y-coupons on panels. RMA control assemblies were processed at AlliedSignal using an RMA flux and RMA paste, followed by d-limonene cleaning. RMA controls included 40 LRSTF assemblies, 18 IPC-B-24 boards, and six MIL-I-46058C Y-coupons panels. The task force did not feel it was necessary to process the RMA assemblies at each site.

The low-residue processing of the functional assembly involved three separate soldering process operations: (1) *reflow* for surface mount components, (2) *wave* soldering for plated-through-hole components, and (3) *hand* soldering for one component and two stranded wires in the HSD section (in addition to needed rework). Upon completion of the soldering operations, the assemblies were further processed in one of four categories: (1) cleaned but not conformal coated, (2) cleaned and then conformal coated, (3) not cleaned and then conformal coated, and (4) not cleaned nor conformal coated. Figure 3.1 provides a three-dimensional overview of processing for the LRSTF assembly (the X in this figure denotes an empty cell).

As mentioned above, each site produced 80 low-residue assemblies and AlliedSignal also produced 40 RMA assemblies to use as controls. Due to a problem in obtaining sufficient quantities of functional components, each site produced 40 assemblies that were fully functional electrically and 40 assemblies that were *partially* functional electrically as determined by the components used. These groups are identified in Figure 3.1 as *functional* and *nonfunctional*.

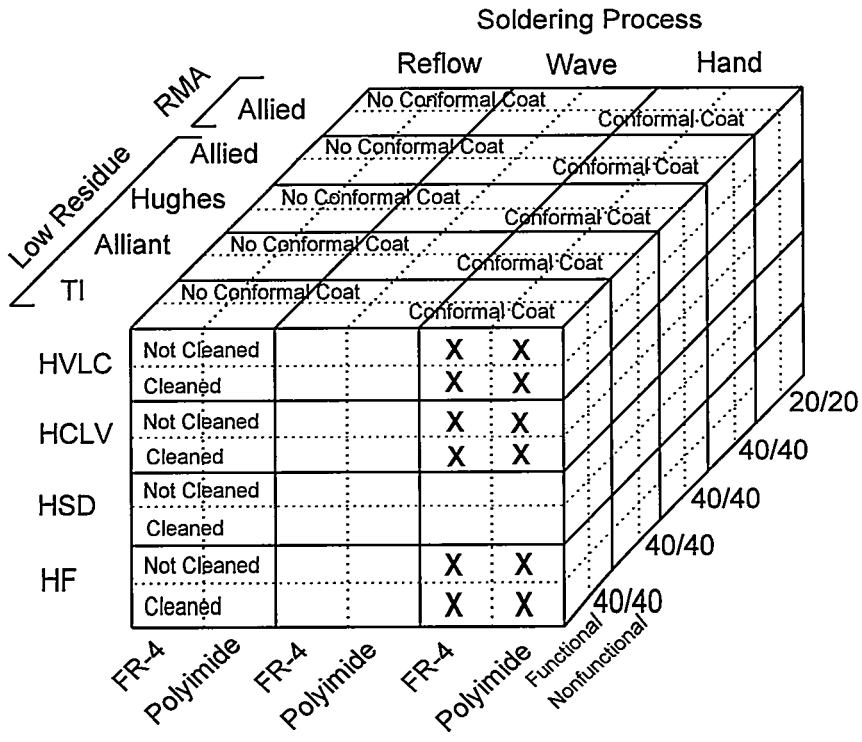

Figure 3.1 An Overview of the Processing of the LRSTF Functional Assembly (X denotes an empty cell)

Each manufacturing site used its soldering equipment and followed its procedures for low-residue soldering. These processes ranged from a fully nitrogen inerted wave soldering process at Texas Instruments to completely open-atmosphere wave soldering at AlliedSignal. The materials used by each site for processing the functional assembly are shown in a table in Figure 3.2 and the equipment used is shown in a table in Figure 3.3.

Processing details for each site are given in the next four sections (including a summary of the lessons learned). The RMA processing is included in the AlliedSignal discussion. Any modifications for processing the IPC-B-24 boards and the MIL-I-46058C test Y-coupons are discussed within the following sections.

3.2 Low-Residue Processing at Texas Instruments

The materials and equipment used for processing the three test vehicles at Texas Instruments (TI) are listed in Figures 3.2 and 3.3, respectively. Assembly and soldering of the test vehicles were completed at TI's Microelectronics Packaging Systems (MPS) automated surface mount assembly factory and McKinney Board Shop (MBS) plated-through-hole assembly factory. The MPS factory features high resolution solder printing, vision assisted component placement, and convection reflow soldering. The MBS factory features automated and semi-automated component insertion, fully nitrogen inerted wave soldering, and automated dip conformal coating.

All test vehicles were handled using clean gloves or finger cots and were placed in Kapak bags between processes to prevent contamination. Individual travelers were used to record the processing data for each test vehicle. All test vehicles were handled as ESD sensitive.

Solder Paste Application (TI)

The solder paste, Indalloy NC-SMQ-81, was allowed to stabilize at room temperature for one hour before use. The selection of this solder paste was supported by the IPC Phase 3, No-Clean results. A 12-mil thick, stainless steel, chemically etched stencil with an 8-mil stepdown zone was used to apply the paste. The paste was screen printed using a Fuji GSP11-4000 automated screen printer. Paste was applied to the Y-coupon through use of a manual dispensing unit.

The stenciling parameters were:

Squeegee hardness:	85 Durometer
Squeegee speed:	1.0 in/sec
Squeegee pressure:	270 left, 315 right (machine setting)
Snap off:	0.08 in
Squeegee length:	13.75 in

These stenciling parameters produced a 15 psig squeegee pressure and a contact print.

SMT Component Placement (TI)

The surface mount components were placed using a Universal Omni Place 4621A pick and place. Component C19 was hand placed and component U102 was not placed.

Reflow Soldering (TI)

The test vehicles were reflow soldered using an SPT International ZCR-181 forced convection reflow oven. Reflow parameters were:

Conveyor speed: 1.64 ft/min
Temperature settings:
- Zone 1: 190°C
- Zone 2: 185°C
- Zone 3: Not Used
- Zone 4: 195°C
- Zone 5: 230°C
- Zone 6: 310°C
- Zone 7: 310°C

Cleaning of test vehicles after reflow, where required by the test plan, was completed using DI water and an ECD aqueous batch cleaner.

Temporary Solder Masking (TI)

Locations to be hand soldered were temporarily masked from the solder wave using PC Flex Mask, a latex, peelable mask. This mask is commonly used for conformal coat masking in the MBS and was readily available.

Wave Soldering (TI)

After lead forming and manual insertion of through hole components, test vehicles were wave soldered using a SEHO Nitrogenous NGW fully nitrogen inerted wave solder machine. This machine includes independent conveyors in the fluxer, preheat, and solder sections; flux application by SEHO's Oscillating Ultrasonic Mister (OUM); seven bottom side infrared (IR) preheaters; and dual solder

waves for soldering mixed technology PWB assemblies. This machine is computer controlled. Preheating and soldering are completed at oxygen concentrations of less than 50 ppm.

Multicore X33-04 low-residue flux was used for wave soldering the test vehicles. This flux was chosen based on results of a TI screen of five commercially available low-residue fluxes. This screen determined which flux had the lowest corrosion potential with the soldering performance most comparable to the RMA controls. The tests used to assess corrosion potential were the copper mirror and British corrosion. Soldering performance was assessed on a wetting balance using both deoxidized copper and temperature aged, tin-lead coupons. Of the low-residue and control fluxes tested for corrosion potential, only the Multicore X33-04 low-residue flux passed both corrosion potential tests. This flux also yielded soldering results comparable to the RMA controls in the TI screen.

The flux was applied using the OUM, a bottom-side spray fluxer. Flux amount applied is determined by the fluxer conveyor speed. Flux transfer to the PWB component side is by natural capillary action.

Wave solder parameters for the functional board were:

Fluxer conveyor speed: 3.45 ft/min
Preheater conveyor speed: 4.60 ft/min
Preheater temperature settings:
Preheater 1: 365°C
Preheater 2: 375°C
Preheater 3: 385°C
Preheater 4: 390°C
Preheater 5: 390°C
Preheater 6: 390°C
Preheater 7: 390°C
Solder conveyor speed: 3.30 ft/min
Solder wave 1 height setting: 7.14 (on 0 to 10 scale)
Solder wave 2 height setting: 9.18 (on 0 to 10 scale)
Solder temperature: 246°C
Solder contact length:
Wave 1: 0.60 in
Wave 2: 0.75 in
Distance between waves: 3.75 in
Solder angle: 8 degrees

Dedicated fixturing was used to process the functional board. Temporary solder masking was peeled from masked areas following wave soldering.

The IPC-B-24 and the Y-pattern coupons were processed pattern side down using universal fixturing and comparable wave solder parameters to those used for the functional board.

Cleaning after wave soldering, where required by the test plan, was completed using the DI water rinse stages of a Corpane In-line Semi-aqueous Cleaner.

Hand Soldering (TI)

Two terminals, two stranded wires, and component U02 were installed and hand soldered using Metcal soldering irons with 700°F tips. Tip size selection was at the discretion of the soldering operator. Kester 245 low-residue flux cored Sn63 solder wire was used for soldering. This flux was one of three products recommended in an industry review conducted by TI. Several operators assessed soldering performance of the three products, all cored, low-residue wires, and chose Kester 245 for use. No external flux was used in the hand soldering operation. All hand soldering was performed by operators certified to MIL-STD-2000A.

Cleaning of test vehicles after hand soldering, where required by the test plan, was completed manually using isopropyl alcohol and a cotton swab.

Inspection (TI)

All solder joints were inspected per MIL-STD-2000A by certified inspectors. Defects and process variances were documented on the traveler for each test vehicle.

Rework (TI)

Rework of defective solder joints was accomplished using the same tools and materials specified above for hand soldering. Test vehicles that required cleaning per the test plan were cleaned after rework using isopropyl alcohol and a cotton swab. Assemblies were distributed among the specific test groups so that rework was equally represented.

Conformal Coating (TI)

Test vehicles were conformal coated with Dow Corning 1-2577 silicone conformal coating. This is the standard production conformal coating used on the majority of TI's military PWB assemblies. Conformal coating was applied using TI's Dip Robotic Conformal Coating system. Curing of the applied conformal coating was per standard shop practices. PC Flex Mask and masking tape were used to mask required areas of the test vehicles prior to coating application. The masking was removed by peeling following cure of the conformal coating.

Post-Process Handling (TI)

Completed test vehicles were packaged in clean Kapak bags and shipped to the test sites.

Process Step	Baseline (RMA)	Low-Residue			
	AlliedSignal	AlliedSignal	Texas Instruments	Alliant Techsystems	Hughes Electronics
Reflow	ESP 6-Sn63-221-AA	ESP 6Sn63-521-AA	Indium NC-SMQ-51	Multicore NC40	Kester 244
Wave Soldering	Kester 185 (RMA)	Kester 922CXF	Multicore X33-04	Multicore X33-04	Kester 952D
Hand Soldering	Kester 197 (RMA)	Kester 922CXF	Kester 245	Multicore X38C	Kester 245 and Kester 952D
Machine Cleaning (when/where required)	ECD Semi-Aqueous Based Batch Cleaner (d-limonene) followed by IPA Spray	IPA Spray	DI Water	IPA (75%) and DI Water (25%)	DI Water and Oakite OkemClean
Hand Cleaning (when/where required)	Brushed with IPA	Brushed with IPA	Brushing with IPA	Brushing with IPA	DI Water Brush and IPA Rinse
Conformal Coating (when/where required)	Urethane Dexter Laminar X-500	Urethane Dexter Laminar X-500	Silicone Dow Corning 1-2577	Urethane Humiseal 1A20	Urethane UV 7900 Polyurethane Grace Specialty Polymers (Touch-Up With Humiseal 131B)
Temporary Solder Mask	Contronic Devices PC Flex Mask	PC Flex Mask	PC Flex Mask	Tech Form Labs TC527	Tech Form Labs PC Flex Mask TC 527 (HB)

Figure 3.2. Materials Used in Processing the Functional Assembly

Process Step	Baseline (RMA)	Low-Residue			
	AlliedSignal	AlliedSignal	Texas Instruments	Alliant Techsystems	Hughes Electronics
Screen Printer	CAM/A LOT Syringe Dispenser	CAM/ALOT Syringe Dispenser	Fuji GSP11-4000	AMI Presco A11S	Manually with MPM Stencil
Component Placement (SMT)	QUAD Pick and Place	QUAD Pick and Place	Universal Instruments Omni Place 4621A	Hand Place	TDK Pick and Place Machine
Component Placement (PTH)	Contract Systems Component Locator	Contract Systems Component Locator	Hand Place	Hand Place	Hand Place
SMT Reflow	Vitronics Unitherm SMR-800 Forced Air Convention with Nitrogen Inerting	Vitronics Unitherm SMR-800 Forced Air Convection with Nitrogen Inerting	SPT International ZCR-181 Forced Convection Reflow	Hollis Single Pass IR Reflow	Vitronics 722 Ambient Conditions
Fluxer	Foam	Foam Spray	Oscillating Ultrasonic Mister	Hand Spray	Wave Fluxer
Wave Solder	Hollis XL7 (ambient)	Hollis XL7 (ambient)	SEHO Nitrogenous NGW (Fully Inerted System)	Electrovert Econopac SMT 2 (Inerted Solder Wave)	Electrovert U-2000 Contour Wave (Inerted Omega Wave)
Hand Solder	Metcal Irons 600°F tips	Metcal Irons 600°F tips	Metcal Irons 700°F tips	Metcal Irons 600°F tips	Weller and Metcal Irons 650°F - 700°F
Inspection	As per DOE 9913000	As per DOE 9913000	As per 2000A	As per 2000A	As per 2000A
Cleaner	ECD Batch	Hand Spray	Corpane (DI Rinse Section Only)	Ionograph 500	Trieber Cleaning System (In Line)

Figure 3.3. Equipment Used in Processing the Functional Assembly

Lessons Learned (TI)

Among many lessons learned, the following are significant:

- The low-residue reflow soldering process requires further development before process implementation is pursued (based on IPC-B-24 and Y-coupon results)
- The amount of solder paste applied for reflow soldering with low-residue fluxes is critical; both visible flux residues and solder balls were produced on test vehicles
- LRSTF assembly reflow results were comparable to RMA for testing completed
- Cleaning with DI water was ineffective in removing the flux residues and solder balls produced in the reflow soldering process
- Visible wrinkling of conformal coating on reflow soldered Y-pattern coupons was present although no mealing or cracking of the coating was evident
- Low-residue wave soldering results were very satisfactory and validated results recorded for TI's production low-residue wave soldering process
- Virtually no post-process residues were observed on wave soldered test vehicles
- No conformal coating material compatability issues were seen on wave soldered test vehicles
- Hand soldering operations were sometimes difficult; this was attributed to lower flux activity and the need to master techniques required for soldering with the low-residue flux
- Low-residue hand soldering techniques required heating the connection before applying the heat bridge and intermittent rather than continuous feeding (pumping) of the solder wire to the connection
- Rework of solder joints was best accomplished by completely removing the solder from the joint followed by re-formation of the joint by hand

3.3 Low-Residue Processing at Hughes Electronics

The materials and equipment used for processing the three test vehicles at Hughes Electronics are listed in Figures 3.2 and 3.3, respectively. All boards were handled using surgical blue gloves to ensure proper cleanliness throughout processing and placed in Kapak bags between processes to prevent contamination. Individual production traveler sheets were used to record the processing data for each board. The floor operators were trained at Delco Electronics and the inspectors were certified to MIL-STD-2000A. All rework was done by MIL-STD-2000A certified personnel. The boards and coupons were labeled and serialized before processing.

The coupons and test boards were processed, inspected, and tested as follows:

- Assembly, soldering and cleaning were performed at Delco Electronics in Kokomo
- Inspection was done at the EMPF in Indianapolis and at Delco Electronics; any subsequent rework was performed at Delco Electronics
- Electrical testing of functional assemblies was conducted at Sandia National Laboratories in Albuquerque
- Conformal coating was applied at Hughes Missile Systems in Tucson

Solder Paste Application (HE)

The solder paste, Kester 244, was allowed to stabilize to room temperature for 24 hours before use. A 10-mil thick stainless steel, laser-etched, trapezoidal aperture stencil on a manual machine was used to apply solder paste on the Y-pattern and IPC-B-24 coupons. The stencil for the functional and nonfunctional LRSTF assemblies was the same except it had a 5-mil step-down for the U102 fine pitch component location.

The stenciling parameters were as follows:

Squeegee hardness:	90 Durometer
Squeegee Speed:	3.0 in/sec
Squeegee Pressure:	30 lbs
Snap off:	0 in
Squeegee length:	12.0 in
Paste Weight:	0.596 g/board

SMT Component Placement (HE)

The SMT components were placed using a TDK Pick and Place machine, except the 10-MΩ resistors R20-R24, which were hand placed on the boards before reflow.

Reflow Soldering (HE)

The LRSTF assemblies, the IPC-B-24 boards, and the Y-coupons were reflowed using a Vitronics IR reflow oven set to the Kester recommended reflow profile. The temperature profile for the reflow process is given in Figure 3.4.

Wave Soldering (HE)

The IPC-B-24 and the Y-coupons were processed pattern side down on universal pallets, three at a time through an Electrovert U-2000 wave solder machine. The coupons were wave fluxed with Kester 952D no-clean flux, preheated and passed over the inerted solder wave.

The LRSTF assemblies were placed in wave soldering fixtures after SMT reflow. Plated through holes planned for hand soldering were covered with a temporary solder mask on the solder side of the board. PTH components were installed on the boards and mounting hardware was secured. These assemblies were stored in covered racks overnight to allow the temporary solder mask to cure. The LRSTF assemblies were processed solder side down on universal pallets, two at a time through an Electrovert U-2000 wave solder machine. Each pallet contained one FR-4 epoxy and one polyimide board.

The U-2000 is continuously monitored by a KIC Prophet Thermal Management System. This system has preset upper and lower thermal control limits for specific zones within the wave soldering system. The KIC system uses data from thermocouples strategically placed throughout the wave solder machine for process control. Additionally, a LRSTF board was instrumented with thermocouples, run through the wave solder machine, and a profile of the LRSTF board was generated. The wave soldering profile is given in Figure 3.5.

Hand Soldering (HE)

Following completion of wave soldering, two terminals, two stranded wires, and the U02 component were installed and hand soldered using Metcal soldering irons, Kester 952D liquid flux, and Kester 245 flux cored solder wire. Soldering iron tips at 650°*F* to 700°*F* with a fine conical profile were used. All hand soldering was performed by operators certified to MIL-STD-2000A.

Aqueous Cleaning (HE)

Following the soldering/reflow operations, previously selected IPC-B-24 boards, Y-coupons, and functional and nonfunctional LRSTF assemblies were cleaned using a Trieber Aqueous cleaner in a heated (140°*F*) solution of DI water and Oakite OkemClean (5% concentration by volume).

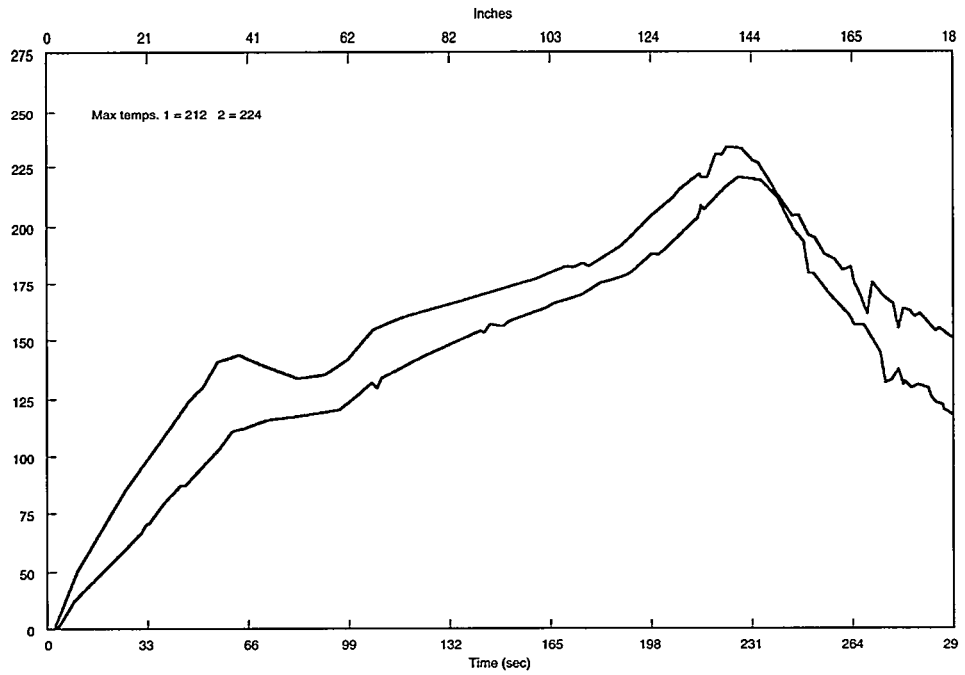

Figure 3.4 Temperature Profile for Hughes Reflow Process

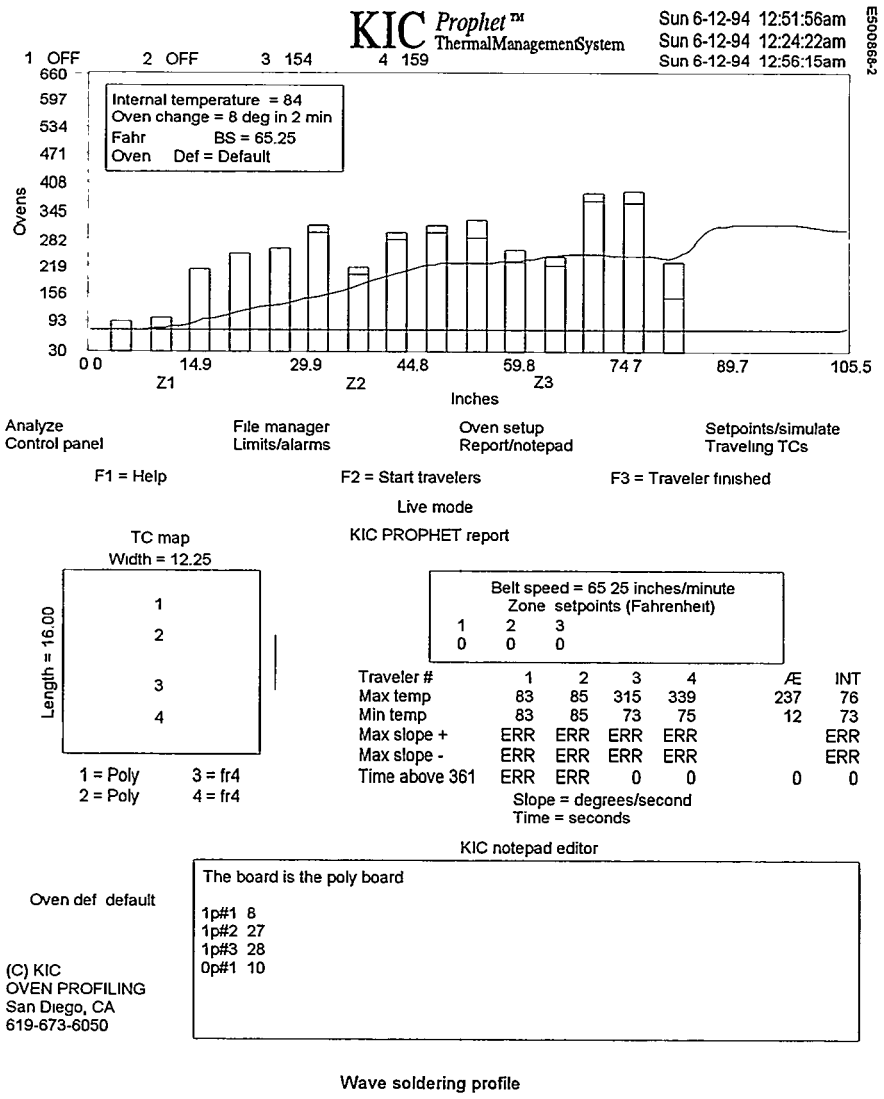

Figure 3.5 Wave Soldering Profile Used by Hughes

Inspection (HE)

After soldering and cleaning (when specified in the test plan), the boards were delivered to EMPF personnel for certified inspection to the requirements of MIL-STD-2000A. Inspections were accomplished with the aid of stereo microscopes. All defects and process variances were documented on inspection sheets that became part of the travelers/records. Due to the nature of this program it was agreed that cleanliness issues would be noted but not reworked, unless cleaning was required as part of the test plan. Defects associated with components documented to have solderability problems were also noted but not reworked, unless the defect would interfere with electrical functions (i.e., bridges, no joints, etc.).

Rework for IPC-B-24 Coupons (HE)

Several IPC-B-24 coupons had one or two shorts across two circuits of the comb patterns. These shorts were reflowed with soldering irons to separate the patterns. Y-pattern coupons were hand soldered using a Weller 2002 soldering iron with a conical tip set to 600°*F*, Kester 952 liquid flux and Kester 245 flux cored solder wire.

Rework (HE)

All defects were reworked to meet the requirements of MIL-STD-2000A. The rework was accomplished using a Metcal soldering iron, Kester 952D liquid flux, Kester 245 flux cored solder wire, bare copper braid and an Unger vacuum desoldering station. Each component and/or

board/coupon area reworked was documented on the associated traveler. Assemblies that required cleaning per the test plan were cleaned again after rework.

Additional rework was required on some functional board assemblies after initial electrical testing at Sandia. These assemblies required component removal and replacement at Sandia. The same individual that did the rework after inspection also did the rework after test except that a Weller soldering iron was used due to availability.

Packaging (HE)

Immediately following soldering, each board or coupon was placed in an individual Kapak bag and sealed for testing or further processing at another facility.

Special ESD care was taken with the functional hardware. Due to the ESD characteristics of Kapak bags, the bags were opened and neutralized with ionized air. The boards were placed inside and the bags were sealed. Each sealed Kapak bag was then sealed in a static safe bag.

Sorting (HE)

All LRSTF boards were assembled and soldered in two lots, electrically functional and partially electrically functional. All assemblies received identical processing except that half were cleaned after processing. The 40 electrically functional boards were sent to Sandia for testing. After testing, the 10 assemblies from each of the four groups (FR-4 cleaned, FR-4 not cleaned, polyimide cleaned, and polyimide not cleaned) were subdivided into groups with equal amounts of rework. Half the assemblies were chosen at random from these subgroups for conformal coating.

Conformal Coating (HE)

Conformal coating was applied with an Integrated Technologies, Inc. spray coating machine, which has a coating spray section, a paper conveyor, and a curing section. The machine has two rows of sprayers and eight spray heads. Boards pass through a preheat oven, a spray application section, and a UV curing system. After the boards exit, they are turned over and returned through the system to coat the reverse side. Some areas of the boards were manually masked before coating. This masking was removed before inspection, which was done with a 4X scope under a black light.

Lessons Learned (HE)

The following lessons were learned in the low-residue manufacturing process:

- Proper process development and coordination between sites is key to successful implementation
- Material compatibility: All materials must be selected to ensure compatibility with each other and with the process equipment used, e.g., coatings, masking materials, fluxes, and cleaning agents (if used)
- Operators need to be familiar with the test plan and product
- If cleaning is required, cleaning material compatibility must be evaluated before implementation
- Co-location of facilities reduces errors
- For the low-residue process to be successful, all opportunities for contamination must be eliminated/ or minimized, e.g., handling, packaging, and/or work surface treatments

3.4 Low-Residue Processing at Alliant Techsystems

The materials and equipment used in processing the LRSTF assemblies at Alliant Techsystems are listed in Figures 3.2 and 3.3, respectively.

Preparation, Handling, Documentation (AT)

Bare printed wiring boards and finished printed wiring assemblies were always placed in clean Kapak bags supplied by Sandia. Black conductive finger cots were used to prevent handling soils from confounding the results of the study. All components and assemblies were handled as ESD-sensitive, which involved wearing wrist or foot straps and using air ionizers when dispensing tape.

Paper travelers were printed for each set of five electrically functional assemblies that required a unique set of processes. Each printed wiring board was mechanically scribed with a serial number and the appropriate serial numbers were written on each traveler. The vendor panel numbers were initially selected as serial numbers for the boards. However, since as many as four different printed wiring boards had the same panel number, the letters A through D were added as suffixes to the serial numbers. Travelers were attached to the Kapak shipping bag in their own static bag. Any special circumstances that arose during the handling or build were documented on the

backsides of the travelers. Some of these notes are included in subsequent paragraphs.

Solder Paste Application, SMT Component Placement (AT)

Stencils were made by Photostencil from 0.006 *in* stock for depositing the Multicore NC40AAS89 Oxide Free solder cream (paste) on the functional assemblies. The pad geometries and locations were supplied by Sandia and forwarded to Photostencil on floppy disks.

The screen printer was a conventional AMI Presco A11S (G926302002). Standard production setup techniques were followed. The operator noted that the paste dried out more quickly than the standard RMA paste. During an unscheduled delay of several hours in getting the components placed on six assemblies, the paste was no longer tacky enough to hold the SMT parts. The paste had to be removed with 1,1,1-trichloroethane and the assemblies were re-screened with new paste. Notes were added to the travelers for these specific reworked assemblies to document this event.

The SMT components were placed into separate, well-marked bins to prevent any mixups. All components were placed by hand-held tweezers due to the limited time available to send them out for proper taping and automatic pick and place. Care was taken to populate the electrically functional boards with all functional components, whereas the nonfunctional boards had some dummy parts substituted. The labels on the component bins helped to highlight which components to use.

Reflow Soldering (AT)

Reflow soldering was performed in the infrared section of a Hollis Single Pass Soldering (SPS) machine (Vol-0500-001) with the liquid fluxer and solder wave options turned off. During the initial run, a MOLE profiler was used to plot the time at temperature that the assemblies experienced. The thermocouple was placed on the U02 component site. After processing the first dark-colored polyimide assembly, it was determined that two different infrared profiles were needed for these boards. The optimal settings for the light green FR-4 assemblies caused delamination in the darker boards.

The settings for the FR-4 (epoxy-glass) and polyimide assemblies were:

Setting	FR-4	Polyimide
Conveyor speed	3.3 ft/min	3.7 ft/min
IR preheater setting 1	350°*F*	350°*F*
IR preheater setting 2	375°*F*	375°*F*
IR preheater setting 3	350°*F*	350°*F*
SPS Module 1 setting	53	50
SPS Module 2 setting	53	50
SPS Module 3 setting	70	60
Airknife 1 angle	45°	45°
Airknife 2 angle	90°	90°
Airknife 1 flowrates	25 psig	25 psig
Airknife 2 flowrates	30 psig	30 psig
Airknife 1 temperature	740°*F*	740°*F*
Airknife 2 temperature	740°*F*	740°*F*
Airknife 1 to bottom ref	.250 in	.250 in
Airknife 2,3,4 to top ref	2.5 in	2.5 in

Temporary Solder Masking (AT)

The plated through holes of one DIP-style IC (U02) and the two jumpers (holes JP1, JP2, E17, and E18) were temporarily masked from contact with the solder wave using TechForm Labs Moldseal TC527 solder maskant. This was a peelable maskant.

Through-Hole Component Insertion (AT)

The nuts supplied for anchoring the transistors Q100 to Q102 did not match the bolts so substitutes were pulled from stock at Alliant Techsystems. Per Sandia instructions, 30Ω resistors were substituted for 10Ω ones listed on the parts list.

A Harwil Company Lead Bender Model N-400 manual lead former was used to form the lead wires. All through hole components were manually inserted. Leads were clinched and side cutters were used to cut lead wires. Components that could not be clinched such as the *J* connectors were installed last to minimize handling and movement of the components.

Liquid Flux Application, Wave Soldering, Maskant Removal (AT)

Multicore X33-04 Halide-Free No Residue liquid flux was used. This flux was used in an undiluted state and applied by manual spraying with a standard spray bottle. The operator attempted to put the same amount of flux on each assembly.

An Electrovert Econopak SMT II retrofitted with a short nitrogen hood (only the solder wave inerted) was used for soldering the plated through hole connections. This so-called short hood covered the last preheater and the wave solder pot with a nitrogen environment. Praxair representatives measured the oxygen level at the flowing solder wave at 37 ppm during the setup of the machine. The nitrogen flow rate was 500 SCFH to each of three diffusers from a common manifold, the nitrogen pressure was 44 psig, and the conveyor speed was 3.0 feet per

minute. Preheater 1 was set at 530°*F* and preheater 2 was set at 350°*F*. Kester Ultrapure Sn63 solder was used with a pot temperature of 500°*F* and solder pump speed of 1100.

All assemblies on the wave soldering machine were processed with the connector at the trailing end of the assembly. A universal fixture was used to hold the boards. The temporary solder maskant was peeled from areas where it was used.

Hand Soldering (AT)

Metcal soldering irons with 600°*F*, 037-type tips were used with Multicore X38C flux-cored wire for hand soldering the IC (U02) and the two stranded wires. The same amount of wire was used for each connection unless a topside fillet was incomplete. In these cases, hand soldering was repeated on the component side of the assembly. This occurred on approximately 40 percent of the hand soldered connections and pointed out the shortcomings of the techniques used by the Category C doing the soldering.

Cleaning (AT)

An Ionograph 500 was used to clean the assemblies cited in the test plan. The cleaning solution was the standard 75 percent IPA and 25 percent deionized water. The cleaning cycle occurred at the conclusion of each soldering operation and lasted approximately 30 minutes.

Inspection (AT)

Inspection was performed with 10X magnification by a single Category C Instructor. Certain exceptions were taken to the normal inspection criteria. Because they failed incoming solderability testing, the components for U101, Q100, Q101, Q103, R118, R119, R120, R121, and R122 were allowed to exhibit non-wetting or de-wetting defects. On the nonfunctional assemblies, unfilled vias, solder balls, and missing parts were ignored. In addition, the inspection ignored tipped parts, leads that were too long, leads that were too short, and SMT capacitors that were too short for their pad span. All these defects were due to factors unrelated to the soldering process and therefore they were not included in the defect tracking.

Rework (AT)

Felt tipped flux pens containing Multicore X38-17 flux and Solder Wick containing the Multicore X38C flux were used for rework. The same rework materials were used following functional testing at Sandia in addition to a Leister hot air gun for component removal. Following rework at Sandia, assemblies cleaned at Alliant Techsystems were cleaned with cotton swabs soaked in isopropyl alcohol. Reworked assemblies were distributed equally among the specific test groups.

Conformal Coating (AT)

Certain areas of the boards were masked with an antistatic tape to prevent coverage by the coating material. The masking tape was dispensed with air ionizers blowing to prevent ESD damage of the assemblies. The following components were masked: E01 to E15, TP100 to TP111, E16 to E18, JP1, JP2, J1 to J10, and edge board connector mating pins.

Humiseal 1A20 polyurethane conformal coating, a type UR coating per MIL-I-46058, was sprayed on the proper assemblies with a Binks spray gun in a spray booth. The coating was cured per normal procedures in the production oven.

Post-Process Handling (AT)

Air ionizers were used when packaging the assemblies for shipping to the test sites to prevent static electricity from damaging the electronics.

Sorting (AT)

Each lot of five identically processed assemblies were sent to the appropriate test site and noted on the traveler.

IPC-B-24 SIR Test Boards (AT)

Simple travelers were drawn up for the IPC-B-24 SIR test boards. Mulitcore X33-04 was hand sprayed on the comb pattern for those boards that were wave soldered. The comb pattern was exposed to the solder wave during processing. The wave solder process for the SIR boards was the same as used with the LRSTF boards.

Paste was applied with a 0.006 *in* thick stencil from Photostencil for those boards requiring solder paste. These boards were infrared reflowed with the same setup as the functional boards. Control boards were not exposed to any fluxing or heating.

Cleaning was performed in the Ionograph 500 when required as specified in the test plan. Conformal coating was applied as with the LRSTF boards (when specified).

Y-Pattern (Conformal Coating Adhesion, MIL-I-46058C) Test Boards (AT)

Simple travelers were drawn up for the Y-coupons used for conformal coating adhesion testing. Multicore X33-04 flux was hand sprayed on the Y-pattern side of those

boards requiring wave soldering. This side was exposed to the solder wave during processing. The wave solder process used for the Y-patterns was the same as used with the LRSTF boards.

Paste was applied manually with a syringe to the Y-shaped traces requiring solder paste. The paste was reflowed with the same setup as used with the LRSTF boards.

Those boards requiring exposure to hand soldering flux had the solder melted from the cored wire with the same tools and technique used on the LRSTF boards. Cleaning was performed in the Ionograph 500 when applicable.

Lessons Learned (AT)

The following lessons were learned in the low-residue manufacturing process:

- The ease with which fluxes were substituted make them nearly drop-in replacements. Excellent connections were made when machine soldering was used.
- Reflow soldering did not require nitrogen inerting
- Hand soldering techniques were just fair and need some improvement to make acceptable connections with one heating
- Flux choice and cleaning agent (if used) must be compatible. Isopropyl alcohol (ambient temperature) and water are not optimum for cleaning these fluxes. Delays of 12-13 days before cleaning are not advised.
- The pot life of this solder paste is limited
- The low-residue processes are forgiving; large amounts of flux applied by manual spraying pre-wave or manually by top and bottom side hand soldering yielded acceptable assemblies.

3.5 Low-Residue and RMA Processing at AlliedSignal

The materials and equipment used in processing the LRSTF assemblies at AlliedSignal are listed in Figures 3.2 and 3.3, respectively.

Solder Paste Application and Component Placement for Reflow (AS)

Solder paste was dispensed using an automated process. ESP formulation number 6SN63-521-AA paste was used for low-residue based on a recommendation from the vendor. ESP formulation number 6-SN63-211-AA paste was used for the RMA process, which is standard with this process. No viscosity, solder ball, or other testing was done in the factory area before the pastes were used.

Paste was dispensed with a CAM/ALOT 1414 machine for both low-residue and RMA boards. The following dispensing parameters were used: Dispenser: 25-gauge needle, dispense height 0.006", dwell = 85msec. Shot sizes for the various configurations were as follows: small capacitors (like C20) = 25msec (2 dots/pad); medium capacitors and resistors(C112, R117) = 40 msec (4 dots/pad); large capacitors (C30) = 60 msec (10 dots/pad); large resistors (R24) = 45 msec (4 dots/pad), and the LCC = 25 msec (3 dots/pad).

Paste was also dispensed on the Y-coupons and IPC-B-24 boards. Sample boards were used to select the dispensing parameters. Paste was dispensed from an EFD dispensor. A line of paste was placed on the combs of the B-24 boards and on the Y-pattern of the Y-coupons.

Components were placed on the boards using a programmed, automated QUAD pick and place machine. This machine can test components electrically before placement, which was done with some resistors.

Reflow Soldering (AS)

A Vitronics model Unitherm SMR-800N with forced nitrogen convection was used for reflow processing. Oxygen concentration in the reflow portion was approximately 30 ppm. Conveyor speed for this equipment was set at 31 in/min. No pallets were used on this machine. Rather, the boards were placed directly on the rail.

The Vitronics machine has 10 controlled temperature zones that were set at the following respective temperatures (°C): 140, 120, 140, 160, 180, 190, 210, 270, ambient (cooling zone), and ambient (cooling zone).

Post-Reflow Cleaning (AS)

RMA boards were cleaned in an Electronic Control Devices (ECD) batch cleaner using food-grade d-limonene (controlled to 1 percent by weight non-volatile residues) as the solvent. The process cycle lasted approximately 15 minutes. De-ionized or reverse osmosis water were not available so the boards were rinsed with a hand-held IPA spray. This spray system (not including d-limonene) was also used for post low-residue cleaning when required by the test plan. The spray pressure was approximately 40 psi. The duration of the spray varied due to the hand

process, but the average spray time was about 45 seconds.

Post-Reflow Visual Inspection (AS)

Boards were visually inspected to a DOE standard after reflow using up to 40X magnification. The DOE standard closely parallels MIL-STD-2000A.

Rework for Surface Mount Devices (AS)

Surface mount components were reworked using a Pace Craft 100A hot nitrogen rework station. Kester 197 was used for boards soldered with RMA paste and Kester 922CXF (low-residue external flux) was used for low-residue boards.

Component Insertion for Wave Soldering (AS)

Through hole components for the wave soldering process were placed using a semiautomatic process with Contract Systems Component Locator CS400C. This equipment directs the operator to proper component location/ orientation, then clips and clenches the component leads.

Temporary Solder Mask for Wave Soldering (AS)

A temporary solder mask was applied to prevent solder from plugging holes that would be hand soldered. A peelable latex maskant, PC Flex Mask 1040, was used. This mask was air cured.

Wave Soldering Flux Application (AS)

Kester 185 flux was applied to the bottom side of the board with a foam fluxer for the RMA baseline process. This material has been used for automated soldering in the RMA production area for the past five years. Kester 922CXF was used for the low-residue process. The same foam fluxer, stone, and process were used; however, the fluxer was thoroughly rinsed and cleaned between the use of the RMA and the low-residue fluxes. Using the same stone may have caused some cross-contamination of the low-residue boards with RMA flux (Figure 4.33 contains more details). The fluxer is in-line with the wave soldering machine, but separated by approximately eight feet of uncovered track between the fluxing and soldering stations.

The bottom sides of the Y-coupons and IPC-B-24 boards were foam fluxed. Topsides were hand fluxed if there were no through-holes through which flux and solder could flow.

Wave Soldering (AS)

A Hollis/Electrovert wave soldering machine model XL7 was used for wave soldering all boards. Fluxing and soldering were done in an ambient atmosphere. The same profile was used for all products (RMA and low-residue functional and nonfunctional boards, Y-coupons, and B-24 boards).

The following processing parameters were used: preheat zone temperature 750°*F*, conveyor speed 3.7 ft/min, solder pot temperature 490°*F*, XL wave 870 RPM, and exit air knife temperature 725°*F* and 10 psi.

Boards were placed in spring loaded fingers on a pallet for soldering. The pallet interfaces with a conveyor chain for transport through the process.

Cleaning after Wave Soldering (AS)

RMA cleaning after wave soldering used the same process, equipment, and materials as the RMA reflow process. When cleaning was required for low-residue, the same process, equipment, and materials were used as those following the low-residue reflow process.

Hand Soldering (AS)

Prior to hand soldering, the temporary maskant was stripped after wave soldering and the boards were cleaned (if required) as described.

Hand soldering for the RMA boards used RMA cored wire and external solder flux (Kester 197). These materials have been used in production areas at AlliedSignal for more than 15 years. The low-residue hand-soldering process used solid wire (63Sn/37Pb conforming to QQ-S-571) and liquid external flux (Kester 922CXF). This flux was selected after an in-house hand soldering flux study for which this product had the least residue combined with the best performance.

Metcal STSS-002 soldering irons were used with 600°*F* model STTC-037 tips for both RMA and low-residue hand soldering processes. If cleaning was required, the low-residue boards were sprayed with IPA at 40 psi. All operators doing soldering operations were certified to DOE Standard 9913000. The requirements in this specification are very close to those found in MIL-STD-2000A.

Handling (AS)

The boards were handled with either finger cots or with gloves throughout the soldering operations. All finger cots and gloves used in the manufacturing areas were

static protective and powder free. The boards were stored and transported in metal film electrically conductive bags.

Post-Wave and Hand Soldering Inspection (AS)

After wave and hand soldering, boards with components were inspected to DOE soldering specification 9913000. This specification is similar to MIL-STD-2000A, but the defect codes are not directly comparable. The actual number of defects on a multi-leaded device is not tracked. Therefore, defect data are complete for DOE standards, but may not be comparable with the other sites.

Rework for Through-Hole Joints (AS)

Solder joint rework used the same materials and equipment as hand soldering. When cleaning was required, IPA was brushed on the joint to remove residues. Following rework, the RMA assemblies were cleaned with d-limonene (machine) followed by an IPA spray, and, if cleaning was required, the low-residue assemblies were sprayed with IPA.

Conformal Coating (AS)

A urethane chemistry (Dexter Laminar X-500) was used for conformal coating. The coating material was mixed with an isocyanate catalyst before application. All conformally coated boards used the same process and the same lot of material. Areas of the boards to be protected from conformal coating were masked with the same temporary solder mask used for wave soldering and were air cured.

Boards were hung vertically while being hand sprayed and were then transferred to a 160°*F* forced convection curing oven. The boards were cured in a vertical position from two to four hours, after which the coating was completely tack-free to touch. The coating continued to cure for up to seven days at ambient conditions.

Assembly Documentation (AS)

Each board was serialized with a unique number when it initially entered the surface mount production department. Processing conditions were documented on a work instruction for each board.

Post-Process Handling (AS)

The finished boards were packed in conductive bags after processing and shipped to Sandia for functional testing and environmental conditioning. The finished nonfunctional boards were forwarded to the EMPF and Contamination Studies Laboratories Inc. (CSL) for testing.

Sorting (AS)

Electrically functional boards were randomly split by substrate for conformal coating. Nonfunctional boards were split as evenly as possible to represent equivalent rework for tests conducted at the EMPF and at CSL.

Lessons Learned (AS)

The following lessons were learned in the low-residue and RMA manufacturing processes:

- The low-residue paste for surface mount processing behaved well as a drop-in replacement for the RMA paste. Part of the reason for this success may have been the method of paste application. The dispenser technique allows customizing paste volume to pads, whereas the stencil or screen thickness and opening size controls the volume. The only difference noted was that the use life ("pot" life) of the low-residue paste was less than that of the standard RMA paste. Tube life of RMA paste usually extends overnight, so it can be used on two consecutive days. However, the low-residue paste would clog the dispenser tips if left overnight.

- Different fluxing techniques should be examined. Foam fluxing applied a large quantity of flux to the backside of the boards, leaving a large amount of residue to remove with the actual soldering process. With the fluxer located remote to the wave soldering unit, the alcohol-based carrier evaporated before the preheat section, rendering the preheat/activation portion of the process ineffective. An alternate fluxing technique to apply less flux volume may be appropriate. Fluxing just before entering the preheat section would also be appropriate to consider.

- Conducting designed experiments to find optimal settings for belt speed, preheat and solder temperatures, solder wave configuration, and air knife conditions would improve the wave soldering process. The limited number of boards available and the short time allowed for the program did not allow this to be done.

- The same parameter settings used to process the functional boards were also used to process the IPC-B-24 boards and the Y-coupons. This is counter to normal operating procedures where parameters are changed for different product lines. Using the same parameter settings contributed to some higher than expected SIR readings for the IPC-B-24 boards (see Section 5).

- The low-residue material was not a drop-in replacement for wave soldering, but may come closer to a drop-in replacement if a nitrogen environment is used. Process development should be used before ambient atmosphere processing. The choice of flux for wave soldering was based on previous testing with hand soldering fluxes due to time limitations. Selection should be made on performance and residue testing for the wave soldering flux. Note that the same flux formulations were not used for hand and wave soldering with RMA because of process differences.

- Solid solder wire was used for hand soldering. Subsequent experience with hand soldering at AlliedSignal has shown advantages with using a low-residue cored wire with external flux instead of the solid wire with external flux.

- IPA was selected for cleaning because it was readily available and the operators were familiar with its use. IPA did not visibly change the low-residue flux residues that remained on the boards. Therefore, a water-based cleaning may have been more effective. However, the ionic conductivity testing showed that IPA had a positive effect on cleanliness. In addition, the environmental conditioning of functional boards showed the remaining residues had no impact on performance.

- Conformal coating chemistry needs to be compatible with the low-residue flux residues. The urethane conformal coating was not compatible with these residues. The conformal coating had an "orange peel" texture. More effective cleaning or an alternative conformal coating chemistry may have eliminated this texture. However, coating adhesion was adequate in this experiment.

4. Test Results for the LRSTF Assembly

4.1 LRSTF Assembly Processing

Forty LRSTF assemblies, for each of two substrate materials (FR-4 epoxy and polyimide), were produced using low-residue soldering processes at each of the four sites. A total of 320 low-residue assemblies were produced (40 boards) x (2 substrates) x (4 sites). Low-residue assemblies are typically not cleaned after processing. However, some of the military representatives on the LRSTF wanted to evaluate the effect of cleaning low-residue assemblies. In response to this request, a typical DI water or IPA process was used on half the boards after each processing step. AlliedSignal soldered 20 LRSTF assemblies with an RMA process for each of the two substrate materials to serve as controls. Figure 4.1 gives a summary of the number of boards for each combination of soldering process and substrate material.

		Low-Residue Site				
Substrate	**Cleaned**	**TI**	**AT**	**AS**	**HE**	**RMA**
FR-4	**Yes**	20	20	20	20	20
	No	20	20	20	20	
Polyimide	**Yes**	20	20	20	20	20
	No	20	20	20	20	

Figure 4.1 Number of LRSTF Assemblies Processed by Site, Substrate Material, and Cleaning

4.2 LRSTF Assembly Testing

Each group of 20 assemblies shown in the cells in Figure 4.1 contained 10 electrically functional assemblies and 10 partially electrically functional assemblies (see Section 3.1). The 10 functional assemblies were subjected to environmental stress screening (ESS), with five being conformal coated before entering ESS. The 10 partially functional assemblies were subjected to extraction tests — five for bulk ionic cleanliness and five for high pressure liquid chromatography (HPLC) and ion chromatography. Each group of 20 assemblies was divided into four groups of 5 for the following tests:

1. Five electrically functional assemblies *without* conformal coating were subjected to three weeks of ESS at Sandia. The ESS was conducted in three 168-hr segments at 85°*C* and 85% relative humidity using a staggered ramp. These assemblies were electrically tested at Sandia prior to ESS, after the first segment of 168 hr of ESS, after the second segment of 168 hr of ESS, and finally at the conclusion of the third 168-hr segment of ESS. The test chamber was ramped down (staggered) to ambient conditions between test sequences. The high voltage section of each board was electrically biased for 1 hr/day during the first 168-hr segment of ESS. Figure 4.2 shows the LRSTF assemblies in the racks in the test chamber. The functional assemblies were electrically biased during ESS as follows:

   a. High-voltage low-current section, 500 VDC (1 hr/day for the first 168 hr only)
   b. High-current low-voltage section, no bias
   c. High-speed digital section, power supply input only, 5 V constant bias
   d. High-frequency section, no bias

2. Five electrically functional assemblies *with* conformal coating were subjected to the same ESS testing as the previous group of five. The conformal coating on these assemblies was inspected before and after ESS.

3. Ionic cleanliness testing was performed by the EMPF in Indianapolis on five partially electrically functional assemblies.

4. HPLC and ion chromatography surface analyses per IPC-TM-650 were performed by CSL on five partially functional assemblies.

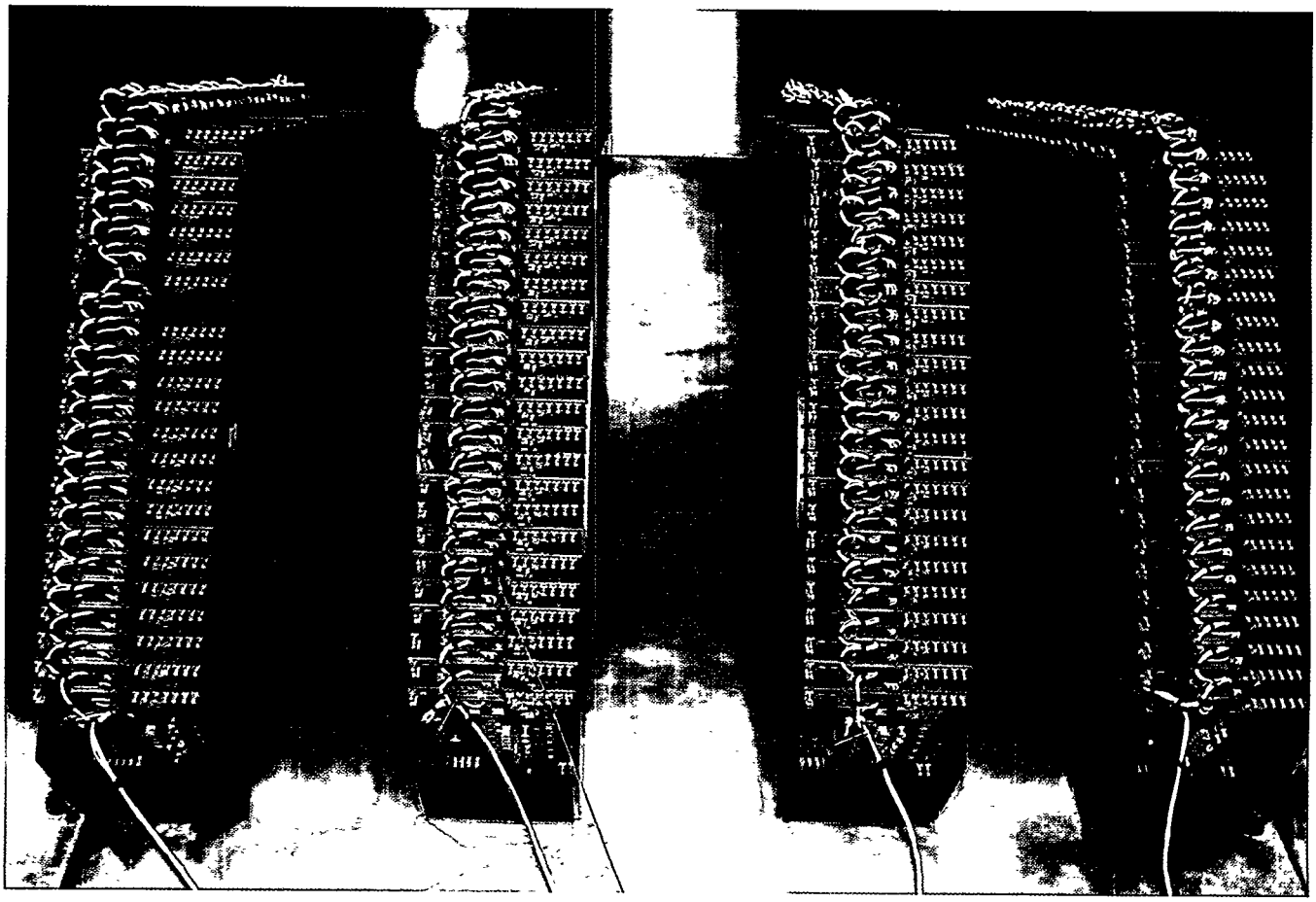

Figure 4.2 LRSTF Assemblies in the Test Chamber Racks

4.3 Statistical Modeling and Analysis of Anomalies

The functionality testing for the board sections and components listed in parts (a)-(d) under group 1 in the previous subsection produced much data. These data were analyzed with statistical models to determine which processing parameters affected the test results. Assemblies producing anomalous test results were subjected to further testing and analyses to determine the source of the anomalies. The results of the statistical modeling and the analysis of anomalies are reported in the following subsections by type of circuitry.

4.4 High Current Low Voltage - Statistical Modeling

Pre-test voltage measurements were made on the LRSTF functional boards before environmental conditioning and after 1, 2, and 3 weeks of ESS. As explained in the next section, the magnitude of the increase in voltage over pre-test conditions is of interest, so the pre-test voltage measurements were subtracted from those made following weeks 1, 2, and 3. That is,

ΔV_1 = Voltage at the end of week 1 of ESS
- Voltage at pre-test

ΔV_2 = Voltage at the end of week 2 of ESS
- Voltage at pre-test

ΔV_3 = Voltage at the end of week 3 of ESS
- Voltage at pre-test

Figure 4.3 gives the mean voltage by site and technology at pre-test, at the end of week 1 of ESS, at the end of week 3 of ESS, and their corresponding differences, ΔV_1 and ΔV_3. As explained in the next subsection, ΔV_2 values were not included in Figure 4.3 or in subsequent analyses due to a technician's error in making the week 2 voltage

		Low-Residue Site				
Test Time	**Technology**	**TI**	**AT**	**AS**	**HE**	**RMA**
Pre-Test	**PTH**	6.88	6.86	7.04	6.90	6.85
	SMT	6.86	6.78	6.94	6.84	6.83
Week 1	**PTH**	7.03	7.04	7.10	7.04	7.03
	SMT	6.98	6.91	7.03	6.94	6.97
Week 3	**PTH**	6.89	6.90	6.86	6.89	6.89
	SMT	6.87	6.83	6.81	6.82	6.88
ΔV_1	**PTH**	.15	.18	.06	.13	.18
	SMT	.12	.14	.09	.10	.14
ΔV_3	**PTH**	.01	.04	-.18	-.01	.04
	SMT	.01	.05	-.13	-.01	.05

Figure 4.3 Mean Voltage Measurements in the HCLV Section and Corresponding Deltas by Site, Technology, and Test Time

measurements. Statistical analyses were performed on ΔV_1 and ΔV_3 using general linear models (GLMs) to determine the effect of various processing parameters. A brief overview of GLMs is now provided.

General Linear Models

A GLM can be expressed as an equation of the following form:

$$Y = \beta_0 + \beta_1 D_1 + \beta_2 D_2 + \beta_3 D_3 + \beta_4 D_4 + \beta_5 D_5 + \beta_6 D_6 + \beta_7 D_7 + \cdots \quad (4.1)$$

The coefficients in the GLM (β_0, ..., β_7) are estimated using ordinary least squares regression techniques. The variables D_1, ..., D_7 are dummy variables. These variables can be easily interpreted by following a simple rule: If a particular site or process is involved in the processing of a particular board, then set the corresponding dummy variable in the GLM to 1, otherwise set it to 0.

The number of terms in the GLM is dictated by the number of processing parameters in the experiment. For example, the dummy variables D_1, ..., D_7 in Equation 4.1 could be defined as follows:

D_1 = 0 if not processed by Texas Instruments
D_1 = 1 if processed by Texas Instruments
D_2 = 0 if not processed by Hughes Electronics
D_2 = 1 if processed by Hughes Electronics
D_3 = 0 if not processed by Alliant Techsystems
D_3 = 1 if processed by Alliant Techsystems
D_4 = 0 if not processed by AlliedSignal
D_4 = 1 if processed by AlliedSignal
D_5 = 0 if board substrate material was FR-4
D_5 = 1 if board substrate material was polyimide
D_6 = 0 if no conformal coating
D_6 = 1 if conformal coating
D_7 = 0 if not cleaned
D_7 = 1 if cleaned

The dummy variables D_1, D_2, D_3, and D_4 are used to identify the effect of individual sites, while D_5, D_6, and D_7 are used to identify the respective effects of substrate material, conformal coating, and cleaning. Joint processing effects can be evaluated by including more than one dummy variable in the individual terms of the GLM. For example, the term $\beta_8 D_6 D_7$ could be introduced in the GLM to determine the joint effect of cleaning and conformal coating. Also, the term $\beta_9 D_1 D_6 D_7$ would determine the joint effects of cleaning and conformal coating at Texas Instruments. The GLM used to analyze voltage changes in the HCLV section of the LRSTF functional board required 60 terms to represent all combinations of site and processing parameters.

Results of the GLM Analyses

The analysis of the GLM for ΔV_1 in the PTH section produced the following estimated model:

$$\begin{aligned} Y_{\Delta V_1} = {} & 0.10 + 0.13 \text{ Conformal Coat} \\ & - 0.13 \text{ AlliedSignal} * \text{Conformal Coat} \\ & + 0.08 \text{ Polyimide} * \text{Not Cleaned} \\ & - 0.11 \text{ Texas Instruments} * \text{Polyimide} \\ & * \text{Not Cleaned} \\ & - 0.05 \text{ Hughes} - 0.06 \text{ AlliedSignal} \\ & - 0.09 \text{ Alliant Techsystems} * \text{Polyimide} \\ & * \text{Not Cleaned} * \text{Conformal Coat} \end{aligned} \quad (4.2)$$

This model contains only those terms that explain a significant amount of the variation observed in ΔV_1. The first term in Equation 4.2 represents a predicted voltage increase (0.10) for the *base case*, which is defined as RMA boards with an FR-4 substrate and no conformal coating. The coefficients of the other terms in the model quantify the magnitude of significant site-process effects on voltage changes.

The second term in the model shows an increase from the base case of 0.13 V for all boards with conformal coating. The average pre-test values for conformally coated boards were 0.11 V and 0.12 V higher in the PTH and SMT subsections, respectively, than for boards without conformal coating. Subsequent measurements at week 1 and week 3 did not show any difference between boards with and without conformal coating. However, ΔV_1 and ΔV_3 are based on subtracting the pre-test voltages where the difference originally existed. This is the reason that conformal coating shows up as significant in the GLM analysis.

The increase due to conformal coating is offset for AlliedSignal by the third term in the model, -0.13 AlliedSignal * Conformal Coat. The fourth term shows an increase of 0.08 V for polyimide substrates that were not cleaned. The other terms in Equation 4.2 have similar interpretations.

The predicted change in voltage for a particular site-process combination is obtained by adding the coefficients of those terms in the model that describe the combination. For example, the predicted change in voltage for a conformally coated polyimide board without cleaning at Alliant Techsystems is found by combining the coefficients of the first, second, fourth, and last terms since these terms all relate to this site-process combination. Addition of these coefficients gives 0.10 + 0.13 + 0.08 - 0.09 = 0.22. Eliminating the first term from this calculation gives the deviation of the prediction from the base case, which is 0.12.

Deviations from the base case for each site-process combination are summarized in Figure 4.4. The empty cells in this figure indicate no deviation from the base case. The values in the non-empty cells are all quite small, indicating that the corresponding site-process combination differed little, if any, from the base case. Several of the deviations are very close to zero as a result of adding two or more coefficients in Equation 4.2 — these values should be regarded as zero for all practical purposes. The deviations in Figure 4.4 for AlliedSignal are mostly negative, which indicates a smaller increase in voltage for their low-residue boards than observed for the RMA controls. Also, as previously discussed, higher voltage increases are noted for those boards with conformal coating.

The GLM analysis for ΔV_1 in the SMT section produced the following estimated model:

$$\begin{aligned} Y_{\Delta V_1} = {} & 0.07 + 0.12 \text{ Conformal Coat} \\ & - 0.11 \text{ AlliedSignal} * \text{Conformal Coat} \\ & + 0.07 \text{ AlliedSignal} * \text{Polyimide} \\ & - 0.03 \text{ Cleaned} \\ & + 0.14 \text{ Alliant Techsystems} * \text{Polyimide} \\ & * \text{Cleaned} * \text{Conformal Coat} \end{aligned} \quad (4.3)$$

The first three terms of this model are similar to those in Equation 4.2. Figure 4.5 gives the deviations from the base case for this model. These deviations are also quite small. One case that stands out is the polyimide boards produced by Alliant Techsystems with conformal coating and cleaning.

The respective models for ΔV_3 in the PTH and SMT subsections are:

$$\begin{aligned} Y_{\Delta V_3} = {} & - 0.03 + 0.11 \text{ Conformal Coat} \\ & - 0.12 \text{ AlliedSignal} * \text{Conformal Coat} \\ & - 0.06 \text{ Cleaned} \\ & + 0.10 \text{ Alliant Techsystems} * \text{Polyimide} \\ & + 0.06 \text{ Cleaned} * \text{Conformal Coat} \\ & - 0.12 \text{ Allied Signal} \\ & - 0.09 \text{ Alliant Techsystems} * \text{Polyimide} \\ & * \text{Conformal Coat} \end{aligned} \quad (4.4)$$

$$\begin{aligned} Y_{\Delta V_3} = {} & 0.00 + 0.11 \text{ Conformal Coat} \\ & - 0.12 \text{ AlliedSignal} * \text{Conformal Coat} \\ & - 0.09 \text{ Hughes} * \text{Cleaned} \\ & - 0.09 \text{ Texas Instruments} * \text{Polyimide} \\ & * \text{Not Cleaned} \\ & - 0.07 \text{ Cleaned} \\ & - 0.07 \text{ Hughes} * \text{Not Cleaned} * \text{Conformal Coat} \\ & - 0.10 \text{ AlliedSignal} \\ & + 0.07 \text{ Hughes} * \text{Polyimide} * \text{Cleaned} \\ & + 0.08 \text{ Cleaned} * \text{Conformal Coat} \end{aligned} \quad (4.5)$$

Substrate	Conformal Coat	Cleaned	Low-Residue Site TI	AT	AS	HE	RMA
FR-4	Yes	Yes	.13	.13	-.06	.08	.13
		No	.13	.13	-.06	.08	
	No	Yes			-.06	-.05	
		No			-.06	-.05	
Polyimide	Yes	Yes	.13	.13	-.06	.08	.13
		No	.10	.12	.02	.15	
	No	Yes			-.06	-.05	
		No	-.03	.08	.02	.02	

Figure 4.4 Predicted Deviations from the Base Case of PTH ΔV_1 (based on Equation 4.2)

Substrate	Conformal Coat	Cleaned	Low-Residue Site TI	AT	AS	HE	RMA
FR-4	Yes	Yes	.09	.09	-.02	.09	.12
		No	.12	.12	.01	.12	
	No	Yes	-.03	-.03	-.03	-.03	
		No					
Polyimide	Yes	Yes	.09	.23	.05	.09	.12
		No	.12	.12	.08	.12	
	No	Yes	-.03	-.03	.04	-.03	
		No					

Figure 4.5 Predicted Deviations from the Base Case of SMT ΔV_1 (based on Equation 4.3)

The first terms in these models are very close to zero, which implies no change from the base case for ΔV_3. The boards with conformal coating show an increase in voltage, as was the case with the ΔV_1 models. Figures 4.6 and 4.7 give the respective deviations from the base case for these models. The deviations in these figures are small and similar to those for the ΔV_1 models. AlliedSignal is again below the base case and actually shows a slight decrease in voltage.

Two statistics, R^2 and s, are commonly associated with the GLMs in Equations 4.2 to 4.5. The R^2 statistic quantifies the percent of the observed variation in ΔV that is explained by the GLM. The statistic s is an estimate of the standard deviation for the GLM. The models in Equations 4.2 to 4.5 all account for a significant amount of the variation in ΔV with the following respective R^2 and s values: 49.4% and .08, 42.2% and .08, 68.1% and .07, 65.2% and .07.

Boxplots of Voltage Increases

Boxplots are graphical displays of sample data. A boxplot contains a box showing the spread between the 25th ($X_{.25}$) and 75th ($X_{.75}$) percentiles of the sample data — the sample interquartile range (IQR). A line parallel to the top and bottom of the box is placed within the box to identify the median of the sample data. (Note: if all data values between $X_{.25}$ to $X_{.75}$ are identical, the box appears as a single line; in other cases the median line may coin-

			Low-Residue Site				
Substrate	Conformal Coat	Cleaned	TI	AT	AS	HE	RMA
FR-4	Yes	Yes	.11	.11	-.13	.11	.11
		No	.11	.11	-.13	.11	
	No	Yes	-.06	-.06	-.18	-.06	
		No			-.12		
Polyimide	Yes	Yes	.11	.12	-.13	.11	.11
		No	.11	.12	-.13	.11	
	No	Yes	-.06	.04	-.18	-.06	
		No			-.12		

Figure 4.6 Predicted Deviations from the Base Case of PTH ΔV_3 (based on Equation 4.4)

			Low-Residue Site				
Substrate	Conformal Coat	Cleaned	TI	AT	AS	HE	RMA
FR-4	Yes	Yes	.12	.12	-.11	.03	.11
		No	.11	.11	-.12	-.05	
	No	Yes	-.07	-.07	-.17	-.07	
		No			-.10		
Polyimide	Yes	Yes	.12	.12	-.11	.03	.11
		No	.02	.11	-.12	.02	
	No	Yes	-.07	-.07	-.17		
		No	-.09		-.10		

Figure 4.7 Predicted Deviations from the Base Case of PTH ΔV_3 (based on Equation 4.5)

cide with either the top or bottom of the box.) Lines are also extended from either end of the box. One line extends from $X_{.25}$ to the smallest observation contained in the interval from $X_{.25}$ to $X_{.25}$ - 1.5 IQR. The other line extends from $X_{.75}$ to the largest observation in the interval from $X_{.75}$ to $X_{.75}$ + 1.5 IQR. Values less than $X_{.25}$ - 1.5 IQR or greater than $X_{.75}$ + 1.5 IQR are regarded as outliers and their locations are identified with asterisks in the boxplot.

Voltage changes are displayed in side-by-side boxplots in Figures 4.8 to 4.12 to show the effect of site, cleaning, conformal coating, and substrate material. Figure 4.8 gives boxplots only by site (all other factors such as cleaning, conformal coating, and substrate material are lumped together for a given site) for the HCLV PTH and SMT sections of the board for ΔV_1. The PTH voltage changes are slightly lower for AlliedSignal while the SMT values are similar for all sites. Figure 4.9 displays ΔV_3 by site. These changes are generally lower than ΔV_1 and AlliedSignal is lower than the other sites for both PTH and SMT.

The boxplots in Figure 4.10 are grouped by cleaning for ΔV_3. The ΔV_1 values had a similar pattern, but with slightly higher values. The first group represents low-residue boards without cleaning, the second group is low-residue with cleaning, and the last group represents RMA. The low-residue boards in both groups have slightly smaller increases in voltage than does the RMA group.

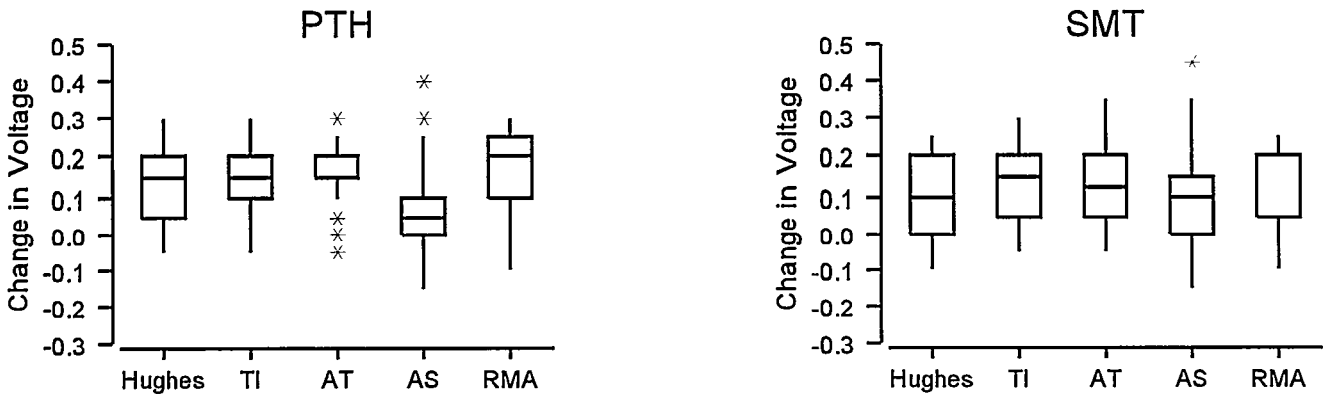

Figure 4.8 Boxplots of ΔV_1 in HCLV PTH and SMT Circuits by Site

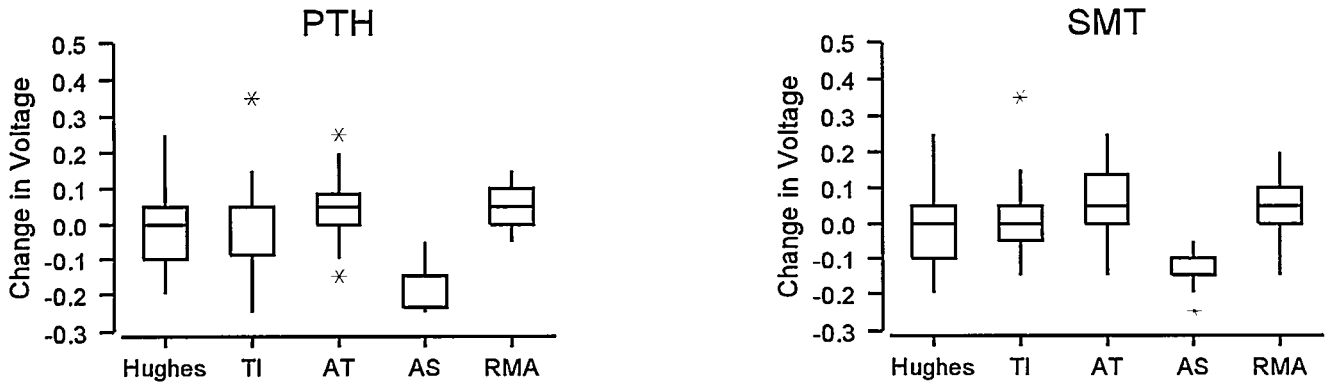

Figure 4.9 Boxplots of ΔV_3 in HCLV PTH and SMT Circuits by Site

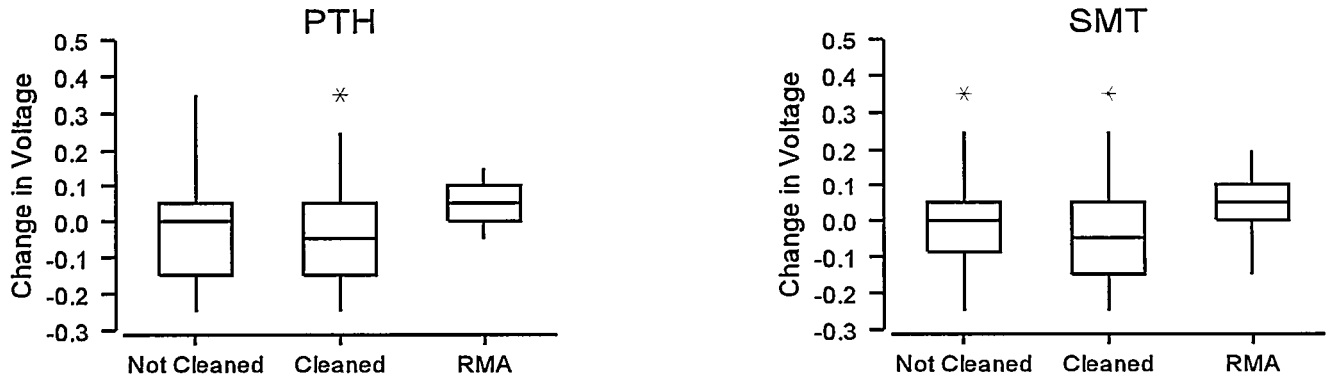

Figure 4.10 Boxplots of ΔV_3 in HCLV PTH and SMT Circuits for Low-Residue Not Cleaned, Low-Residue Cleaned, and RMA Controls

The increase in voltage due to conformal coating that was mentioned earlier is shown very clearly in the ΔV_3 boxplots in Figure 4.11. The plots for ΔV_1 are not shown, but they exhibited a similar pattern.

Figure 4.12 shows boxplots by substrate material for ΔV_3. The ΔV_1 values had a similar pattern, but with slightly higher values. These plots were similar for both substrate materials.

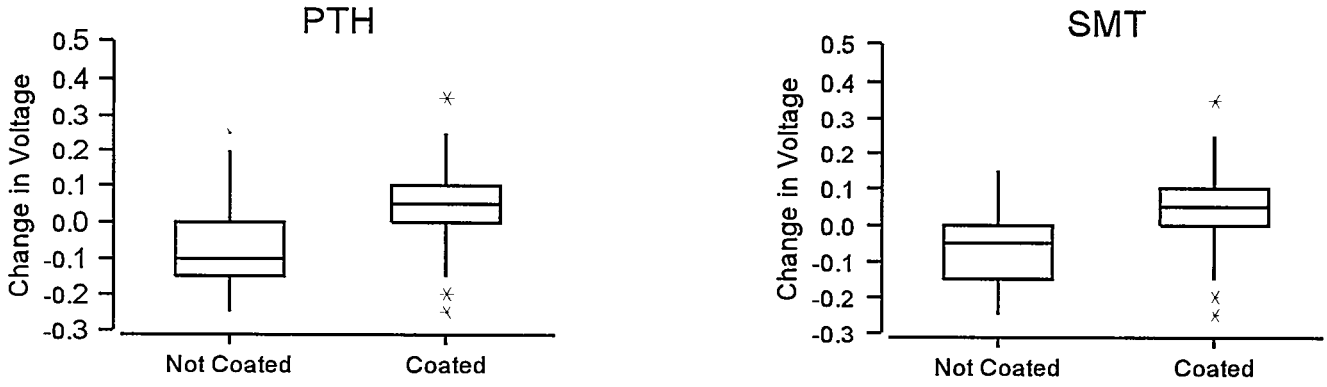

Figure 4.11 Boxplots of ΔV_3 in HCLV PTH and SMT Circuits Grouped by Conformal Coating

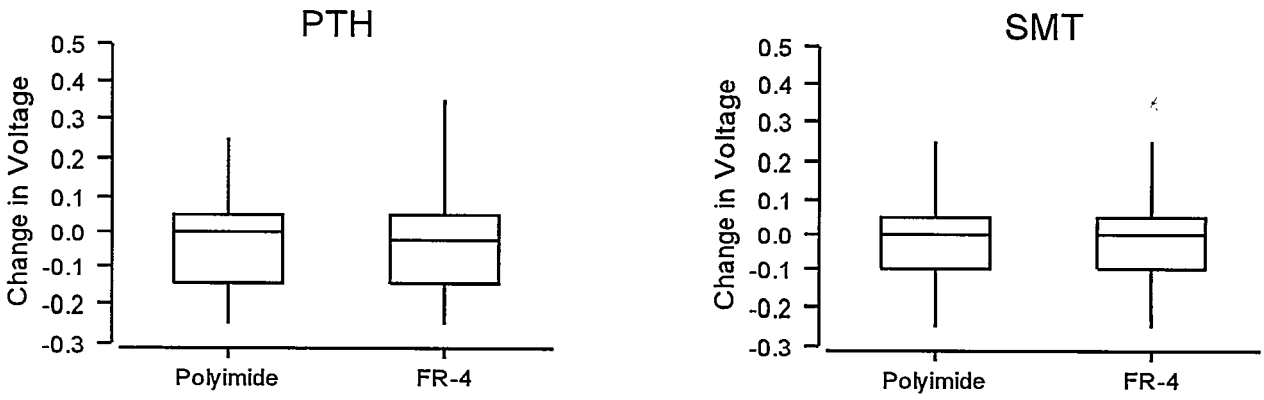

Figure 4.12 Boxplots of ΔV_3 in HCLV PTH and SMT Circuits by Substrate

4.5 High-Current Low-Voltage - Analysis of Anomalies

As stated in the test plan, the increase in voltage due to environmental conditioning was expected to be no more than 0.030 V. Subsequent test measurements on stranded wires provided a reference distribution for common mode noise for the HCLV circuits. These measurements had a mean of 0.140 V with a standard deviation of 0.0143 V. Oscilloscope readings can be resolved to ± 0.05 V (a total spread of 0.10 V). Based on this information, a new criterion for increase in voltage for HCLV circuits was established using a ± 3σ spread for common mode noise as follows:

$$\Delta V > 0.030 + \bar{X} + 6\sigma + 0.1 = 0.030 + 0.140 + 6\times0.0143 = 0.356 \text{ V} \quad (4.6)$$

Voltage increases greater than 0.356 V were cause for further investigation (voltage decreases are not of concern). Thirty-nine values of ΔV_2 from 27 separate LRSTF assemblies exceeded the 0.356 V increase criterion. However, the ΔV_3 values were all below 0.356 V. The disparity in the ΔV_2 and ΔV_3 measurements was traced to a substitute technician that was used for the first time at the end of the second week of ESS. This technician mistakenly made the voltage measurement at the wrong place on the wave form. Thus, the ΔV_2 values were eliminated from the analysis.

One LRSTF assembly produced two anomalous values for ΔV_1, 0.40 V and 0.45 V, that were just above the stated criterion. These values occurred in the PTH and SMT subsections, respectively, and they decreased as the test continued. At the conclusion of ESS, the corresponding values of ΔV_3 were - 0.25 V and -0.20 V, which are no longer of concern.

Figure 4.13 The LRSTF Functional Assembly is Subjected to Electrical Testing between Segments of ESS

4.6 High Voltage Low Current - Statistical Modeling

Current measurements were made on the LRSTF functional boards before environmental conditioning and after 1, 2, and 3 weeks of ESS (see Figure 4.13). These four sets of current measurements are displayed in boxplots in Figures 4.14 and 4.15 for PTH and SMT, respectively. As explained in the next section, the current measurements were expected to be between 9 µA and 11 µA. Dashed horizontal lines have been added to the boxplots at 9 µA and 11 µA for ease of reading. These boxplots show that the vast majority of the measurements for both PTH and SMT were within the 9 µA and 11 µA bounds. In fact, the data exhibited very little variability as most values were either at, or very close to, 10 µA. There are, however, several points that are either above or below the horizonal lines. In particular, at week 3, 16 such points are identified (PTH and SMT combined). As explained in the next section, these 16 measurements were determined to not be related to the soldering processes. Since so many of the data were either equal to, or very close to, 10 µA and exhibited such low variability, the results of the GLM analyses are not presented.

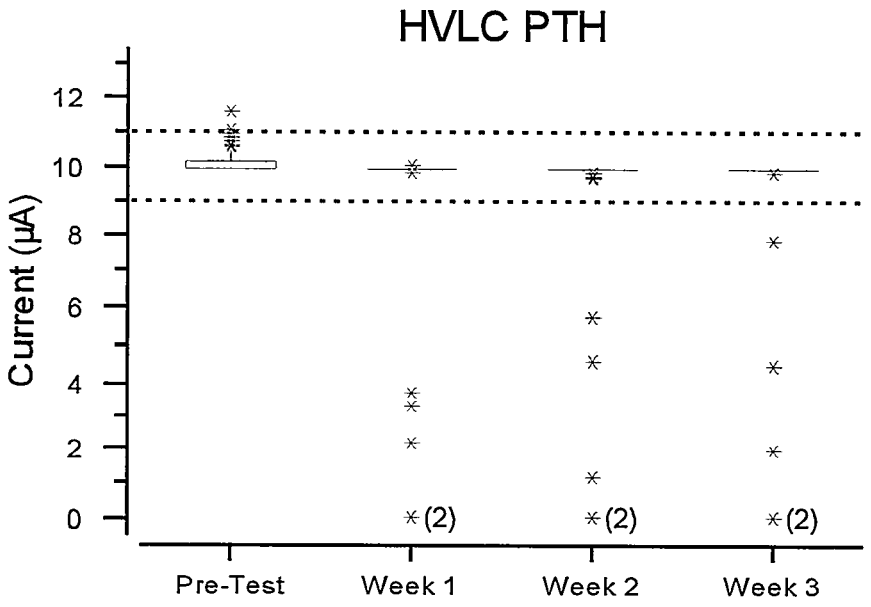

Figure 4.14 Boxplots of Current Measurements (µA) for HVLC PTH Circuits by Test Time

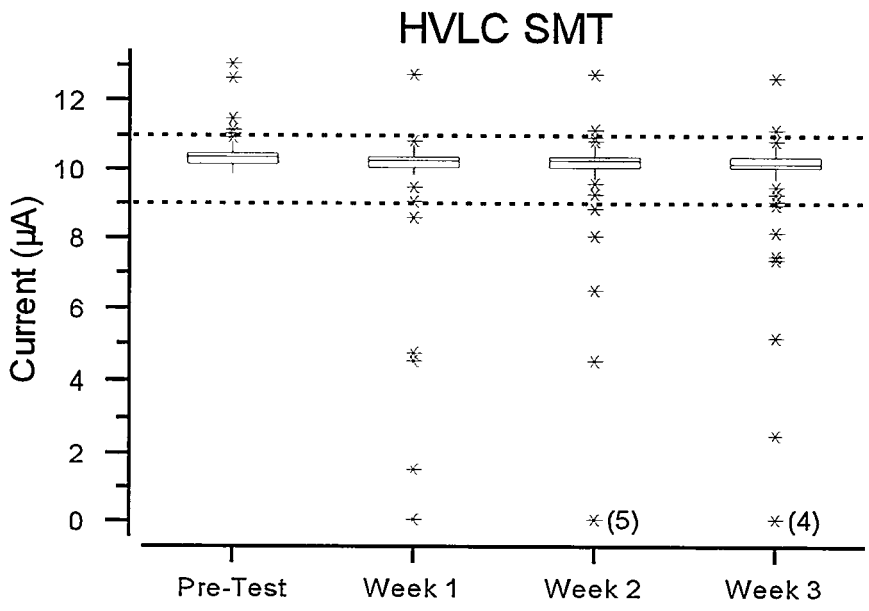

Figure 4.15 Boxplots of Current Measurements (µA) for HVLC SMT Circuits by Test Time

4.7 High Voltage Low Current - Analysis of Anomalies

Current measurements were made on the LRSTF functional boards before environmental conditioning and after 1, 2, and 3 weeks of ESS. Based on expected circuit performance, current readings less than 9 µA or greater than 11 µA were regarded as anomalous. Sixteen circuits had readings outside this interval during the environmental tests, *but none were due to the soldering processes.* The 16 occurrences are summarized as follows: (1) 10 circuit board vias shorted to the ground plane, (2) four resistors had open circuits, (3) one current measurement

slightly exceeded the established criterion, and (4) an incorrect resistor was installed on one board. Each of these areas is now considered in detail.

Shorted Vias

Several vias pass through the ground plane with a design clearance of 8 mils between the via and the ground plane. Due to variation in registration during manufacturing, the actual spacing was as low as 5 mils in some cases. The vias were not intended to be subjected to a 500 V bias with reference to the ground plane. However, a sneak path in the electrical test setup resulted in a 500 V bias appearing between some vias and the ground plane. The sneak path was caused by the HVLC measuring instrument's (an electrometer) AC power ground being common with the AC power ground of the 5 V power supply used for the HSD section. The ground plane serves as the power return for HSD section. MIL-STD-275 recommends at least a 10-mil clearance with a 500 V bias to avoid the possibility of short circuits. The guideline was unintentionally violated in this case.

Even with the sneak path and marginal 5-mil clearance, short circuits did not occur during the electrical pre-test of the boards before ESS. Also, the HVLC circuits were subjected to a 500 V bias for one hour per day during the first week of environmental exposure with no indication of a failure. The 500 V power supply used for these tests automatically turns off in the event of a short circuit and must be manually reset to resume operation, providing a clear indication of any short circuits. There was no indication of a short circuit at a HVLC via during the first week of ESS. However, six of the ten shorted vias occurred during the electrical test after the first week of ESS. The dielectric strength of the boards may have degraded during the first week of ESS. This degradation, in conjunction with the sneak path and minimal spacing, may have caused these six boards to short during the electrical test. These six boards were disconnected from the 500 V power supply for subsequent ESS.

A strip chart recorder was added to the test setup to monitor the 500 V power supply during ESS. The 500 V power supply automatically shut down during the first 15 minutes of applied 500 V bias. The rack of test boards containing the short circuited board was disconnected from the power supply and the 500 V bias was reapplied to the remaining racks. Another short circuit occurred almost immediately so the 500 V bias was discontinued to prevent further short circuits.

Prior to electrical testing at the end of the second week of ESS, a 10KΩ resistor was added to the test setup between the 500 V power supply and the test boards to decrease the possibility of additional short circuits. Electrical testing identified a total of four additional short circuits. A check of the ESS test setup showed that the 500 V power supply ground and the HSD 5 V power supply ground (which connects to the ground plane) had been inadvertently connected. This connection was responsible for two, and possibly all four, shorts.

All shorts were electrically isolated and confirmed by measuring the resistance between the via and the ground plane. Vias from three boards were micro-sectioned and confirmed the shorts at the ground plane and the 5-mil minimum spacing between the via and the ground plane.

Open Resistors

Two PTH and two SMT resistors opened during the test. The coating was removed from the two PTH resistors and a scanning electron microscope was used to verify the open circuits. The opens were traced to component failures and were not investigated further. The two SMT resistors had fractures that resulted in the open circuits.

Out-of-Tolerance Measurement

One SMT circuit exceeded 11 µA throughout the test (see the uppermost point in Figure 4.15) due to the installation on an incorrect resistor. An additional SMT circuit was marginally out of tolerance after two weeks of ESS. The current was 11.2 µA and the test criterion was no more than 11 µA. This out-of-tolerance condition could not be repeated during an analysis of the anomalies.

4.8 High Speed Digital - Statistical Modeling

Rise and fall time measurements were made on the PTH and SMT HSD circuits on the LRSTF functional boards before environmental conditioning and after 1, 2, and 3 weeks of ESS. The four sets of measurements for PTH circuits are displayed in boxplots by site in Figures 4.16 and 4.17. Figures 4.18 and 4.19 provide similar displays for SMT circuits. All graphs have the same vertical scale to facilitate comparisons. As explained in the next section, the rise and fall times were both expected to be less than 7 ns. A dashed horizontal line has been added to each set of boxplots at 7 ns for ease of reading.

The boxplots for PTH circuits show that the vast majority of the rise and fall times are below 7 ns, except for a few for Alliant Techsystems at week 1. AlliedSignal also has one rise and fall time above 7 ns at week 1. The fall times

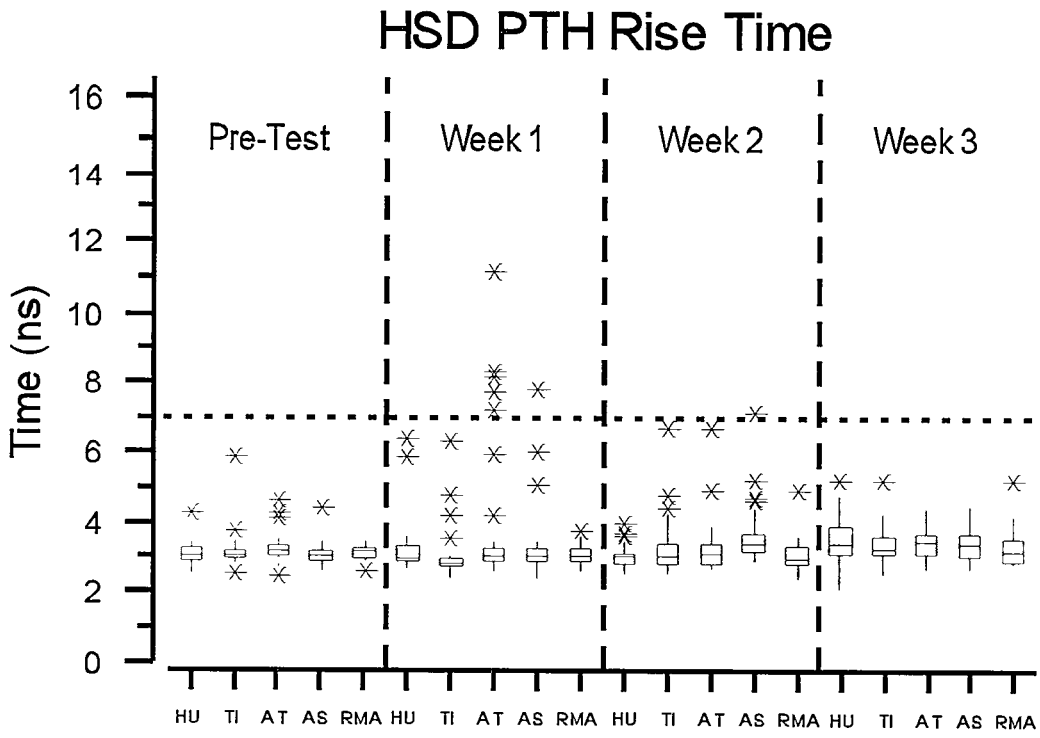

Figure 4.16 Boxplots of Rise Times for HSD PTH Circuits by Site and Time of Test

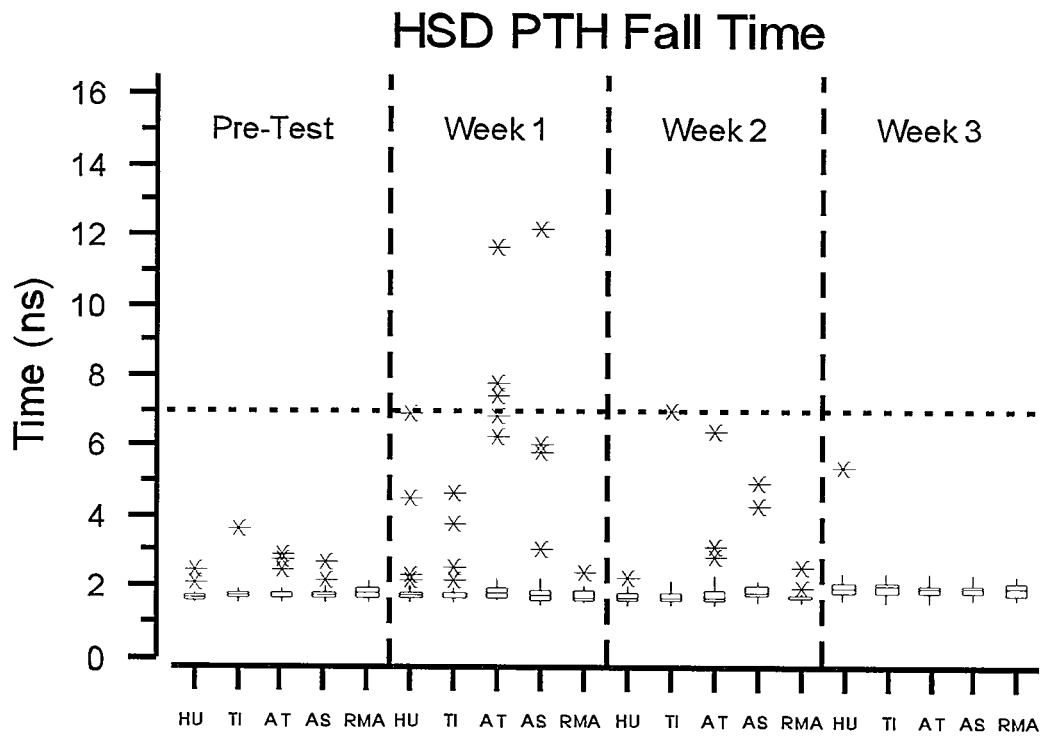

Figure 4.17 Boxplots of Fall Times for HSD PTH Circuits by Site and Time of Test

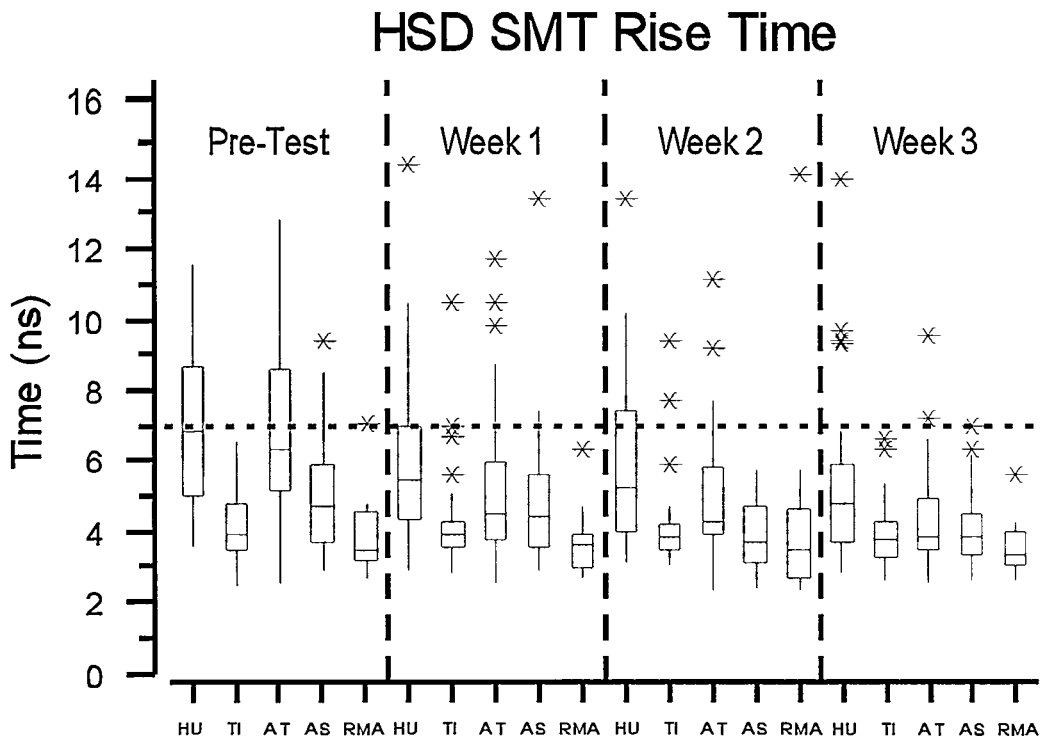

Figure 4.18 Boxplots of Rise Times for HSD SMT Circuits by Site and Time of Test

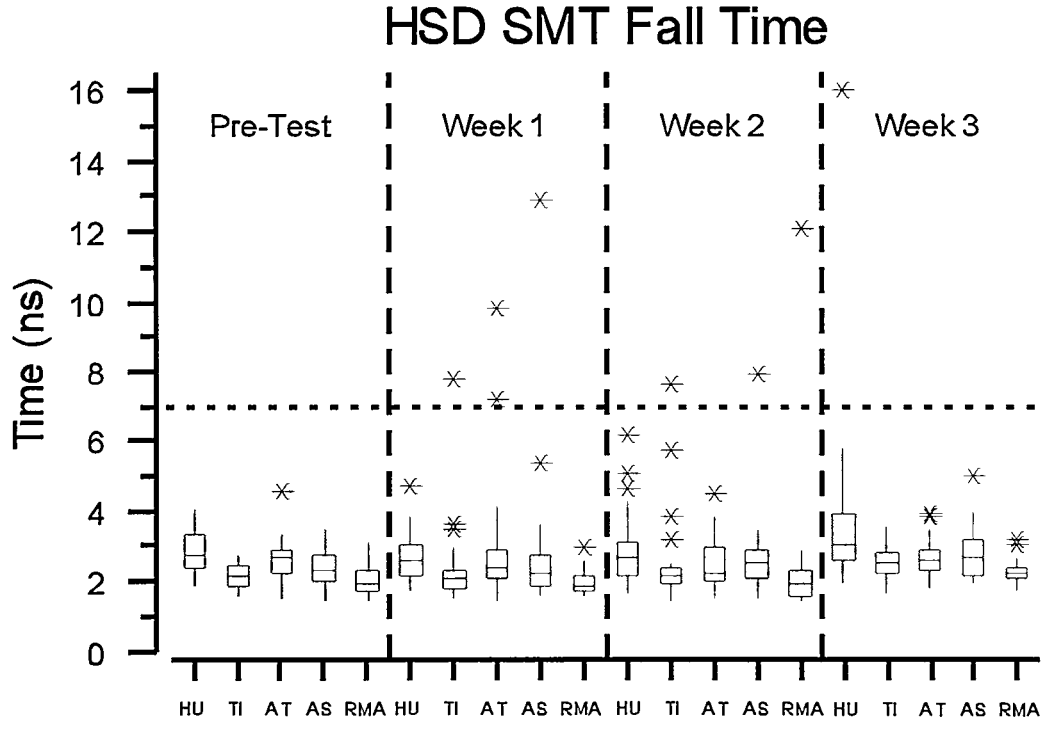

Figure 4.19 Boxplots of Fall Times for HSD SMT Circuits by Site and Time of Test

are approximately 1.5 ns shorter than the rise times and overall the data exhibited very little variability. The box portion of the boxplots are very similar from site to site for PTH circuits. As might be expected with such small variability, the GLM analyses did not identify any noteworthy processing parameters. Hence, the results of the GLM analyses are not presented.

The boxplots for SMT circuits show considerably more variability than the corresponding graphs for the PTH circuits. However, the vast majority of the fall times are below 7 ns, except for four observations at week 1, three at week 2 (including one RMA), and one at week 3. As was noted for the PTH circuitry, the fall times are also less than the rise times for SMT circuits.

The SMT rise times for Texas Instruments were essentially equivalent to RMA throughout testing, with AlliedSignal only slightly higher. The pre-test rise time measurements for Hughes and Alliant Techsystems were clearly higher than other sites and produced many values greater that 7 ns. Figure 4.18 shows that the rise times for SMT circuits have greater variability than those in Figures 4.16, 4.17, and 4.19, but this variability decreases over ESS and all but a few measurements were below 7 ns at week 3. The HSD SMT circuit rise times were subjected to GLM analyses to help identify the source of the higher rise times for Hughes and Alliant Techsystems. However, no controlled experimental parameter or combination of parameters could be identified. HPLC and ion chromatography analyses were also conducted on PWAs with high rise times as well as on PWAs with low rise times. These analyses showed all chloride extractions were less than 2.5 µg /in^2 (see Section 4.15 for further explanation) and therefore, were also not helpful in identifying the source of the higher rise times.

4.9 High Speed Digital - Analysis of Anomalies

Rise and fall time measurements were made before ESS and after 1, 2, and 3 weeks of ESS. Measurements were made on the output pulse from the HSD circuits as explained in Section 2.4. Information on data sheets from the IC supplier indicated that the rise and fall times of these pulses should not exceed 7 ns.

Two types of anomalies were noted in the HSD Section: damaged ICs and rise and fall times exceeding 7 ns. In addition, no output was recorded for some ICs at pre-test, but they all produced output at later stages of testing. These ICs were included with those having rise or fall times greater than 7 ns. The anomalies are now considered in detail.

Damaged ICs

Six ICs were damaged from high-voltage flashovers (zaps) during electrical testing that were due to the design problem discussed in Section 4.7. Two of these ICs sustained massive damage and did not have any output during at least one of the electrical tests. The first IC was on an Alliant Techsystems board in the SMT subsection (FR-4 substrate, cleaned, and conformally coated - rack position 46). This IC met all criteria before conformal coating was applied, but sustained damage during the post-conformal coat electrical tests. (Boards were not repaired after receiving conformal coating.) At the completion of the tests, the IC package was de-lidded and found to have extensive damage from an electrical over-stress. The second badly damaged IC was on a Hughes board in the PTH subsection (polyimide, cleaned, with no conformal coating - rack position 90). The failure was discovered during the week 2 electrical tests. The last gate in the IC had no output, but the first gate was functional. Analysis revealed that the VCC line on the IC chip was burned open.

Four of the six damaged ICs sustained minor damage that affected their performance. The first two appeared during the week 2 tests. Both ICs were on a Texas Instruments board (FR-4, not cleaned, and conformally coated - rack position 64). One IC was from the PTH subsection and the other from the SMT subsection. The circuits did not have any output, but performed satisfactorily when the VCC power supply was replaced with one that could supply more current. The VCC to ground semiconductor junctions were verified to be degraded and therefore the ICs required a larger power supply to produce an output. The third and fourth of these damaged ICs appeared during the week 3 tests. Both ICs were on an AlliedSignal board (PTH subsection, FR-4, not cleaned, and no conformal coat - rack position 134). Again, one IC was from the PTH subsection and the other from the SMT subsection. The performance and damage sustained by these two ICs was similar to the two found to be damaged during the week 2 test. This board also had a high-voltage via that was shorted to the ground plane as discussed in the previous section of this report.

Because of low output voltages, four additional ICs were suspected to have sustained a lesser degree of damage from high-voltage zaps. However, their power supply currents were within the normal range and the VCC to ground semiconductor junctions appeared normal. Three of the four circuits had long rise and fall times and were included in the long rise and fall time category since the current-voltage characteristics of the IC semiconductor

junctions were not degraded. The fourth suspected damaged IC, from an RMA board, met the rise and fall time criterion and therefore, was not analyzed further.

No Output or Long Rise and Fall Times

The boxplots in Figures 4.16 to 4.19 show longer rise and fall times with a higher degree of variability for SMT circuits than for PTH circuits, even though they contain the same type of silicon chip. Therefore, the six SMT circuits with long rise times at the conclusion of the third week of ESS were selected for further analysis. Electrical testing showed that only the last gates of these six ICs had long rise times. Two other SMT subsections that had long rise times earlier in the ESS, but not at the end, were also selected for further analysis. The output traces of the last gate of all eight SMT ICs were cut open at the IC output pin to remove any possible capacitive loading. The subsequent rise and fall times of all eight circuits met the 7ns criterion. The capacitive loading on the opposite side of the cut was found to be excessive on all eight circuits (47pF to 177pF). Most of the capacitive loading was determined to be due to the parasitic capacitance at the location where the output trace passes under the two VCC filter capacitors as shown in Figure 4.20. The capacitive loading was checked on a few SMT circuits that always had rise times less than 7ns and was found to be about 70pF in all cases. The capacitive loading for PTH circuits is estimated to be less than 25 pF. It is concluded that the output traces passing under the two VCC filter capacitors introduced excessive capacitive loading to the SMT ICs, thereby increasing their rise and fall times.

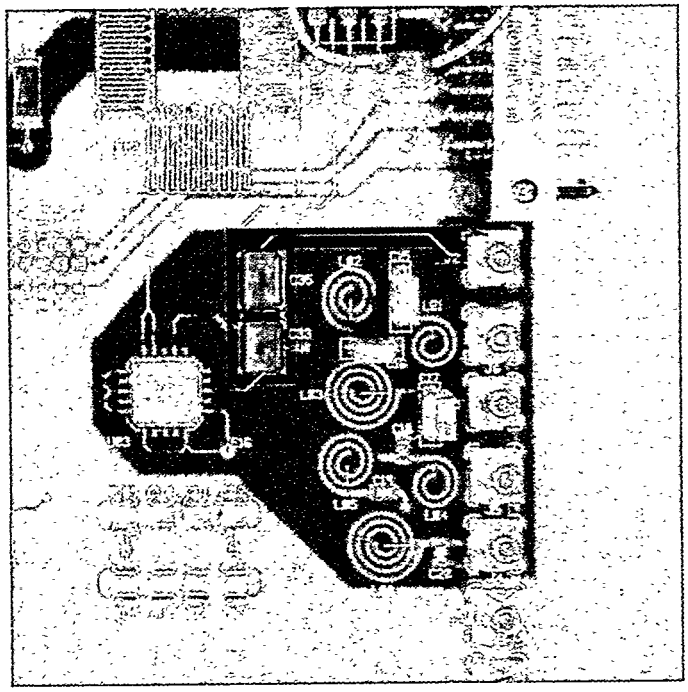

Figure 4.20 Parasitic Capacitance in the HSD/SMT Section of the PWA

4.10 High Frequency Low Pass Filter - Statistical Modeling

Pre-test high frequency transfer function response measurements were recorded for the low pass filters (LPFs) on the LRSTF functional boards for both PTH and SMT. Additional measurements were taken after 1, 2, and 3 weeks of ESS (see Figure 4.21). The transfer function response was measured at 50 MHz and the frequency was measured at -3 dB and -40 dB. The transfer response at 50 MHz is displayed in boxplots by test time and site in Figures 4.22 and 4.23 for PTH and SMT, respectively. These boxplots show very little variability for all measurements. In fact, the total spread in these measurements was less than 0.2 dB for all sites.

Therefore, the change from the pre-test must also be quite small. The test plan criterion was ± 5 dB change in response from the pre-test measurements. Since the observed change in response is well within this criterion, these data were not analyzed further.

Figure 4.21 The LRSTF Assembly is Subjected to High Frequency Testing between Segments of ESS

The frequency at -40 dB for PTH and SMT are displayed in boxplots by test time and site in Figures 4.24 and 4.25, respectively. The test plan criterion for change in frequency from the pre-test measurements was ± 50 MHz. The changes were all within this criterion, so these data were not subjected to further analyses. The frequency data at -3 dB were similar to those at -40 dB.

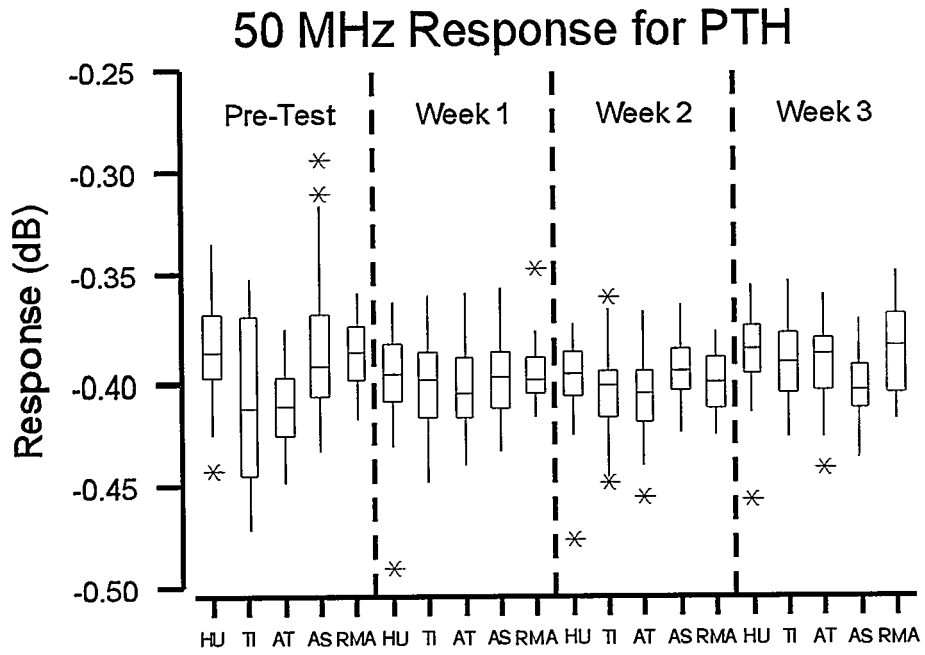

Figure 4.22 Boxplots of the 50 MHZ Response for PTH by Test Time and Site

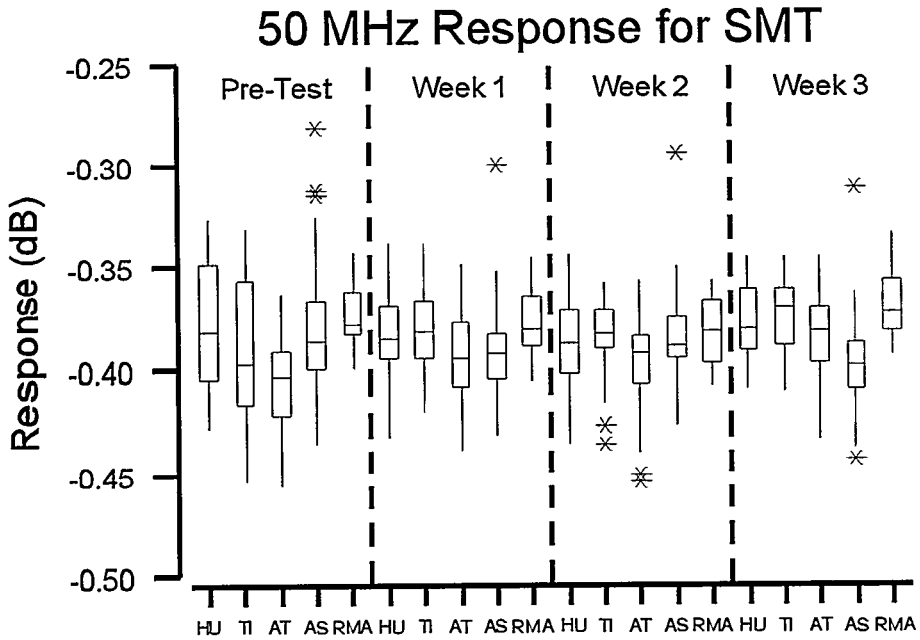

Figure 4.23 Boxplots of the 50 MHZ Response for SMT by Test Time and Site

4.11 High Frequency Transmission Line Coupler - Statistical Modeling

Pre-test high frequency measurements were recorded for the transmission line coupler (TLC) on the LRSTF functional boards and additional measurements were taken after 1, 2, and 3 weeks of ESS. Forward coupling measurements were made at 50 MHz, 500 MHz, and 1 GHz. Reverse coupling frequency and response measure-

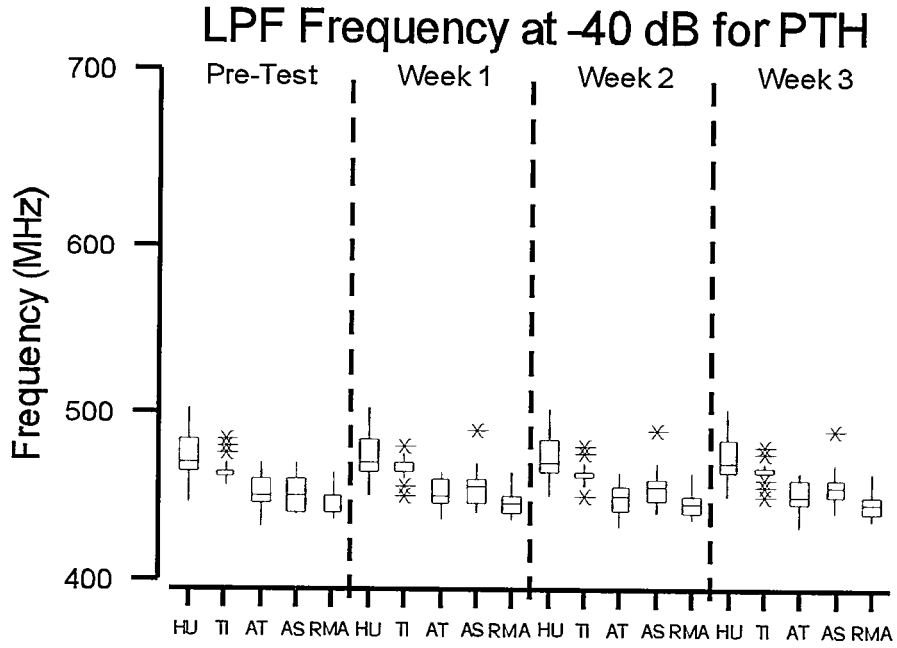

Figure 4.24 Boxplots of LPF Frequency at -40 dB for PTH

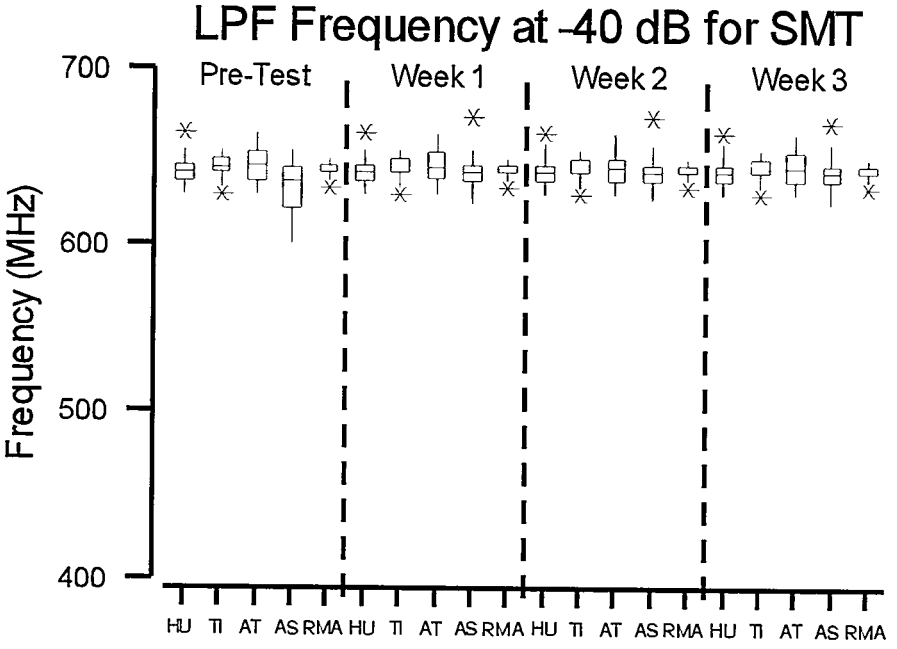

Figure 4.25 Boxplots of LPF Frequency at -40 dB for SMT

ments were taken at the null point (see the minimum point on the dashed line in Figure 2.17). The 50 MHz forward coupling measurements are displayed in boxplots by test time and site in Figure 4.26. These boxplots show that the measurements for Hughes, Texas Instruments, and Alliant Techsystems are similar at each test time. In addition, the measurements for AlliedSignal low-residue are very similar to those for RMA and are less variable

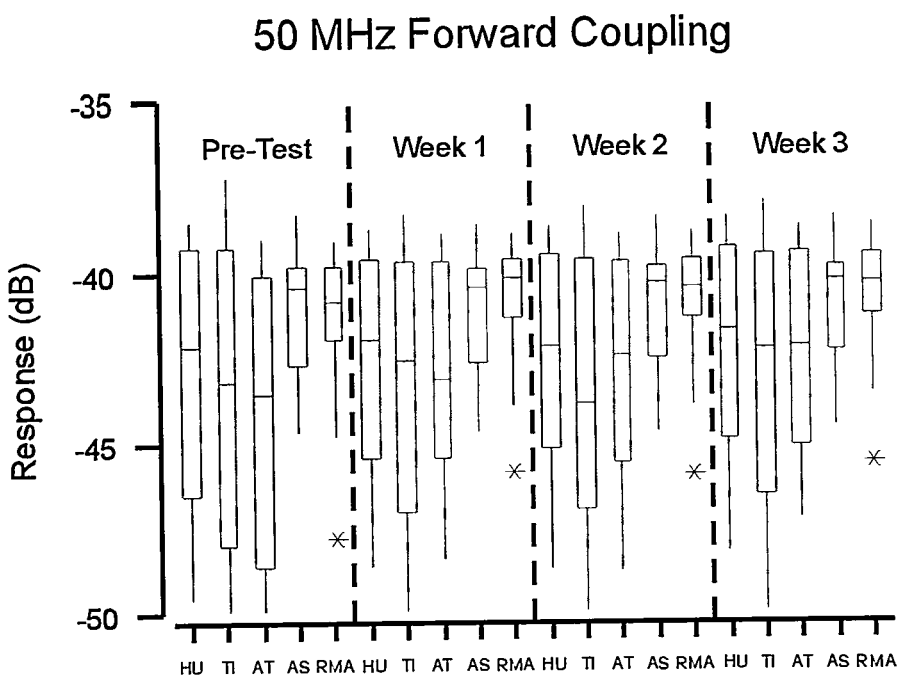

Figure 4.26 Boxplots for 50 MHZ Forward Coupling Measurements by Test Time and Site

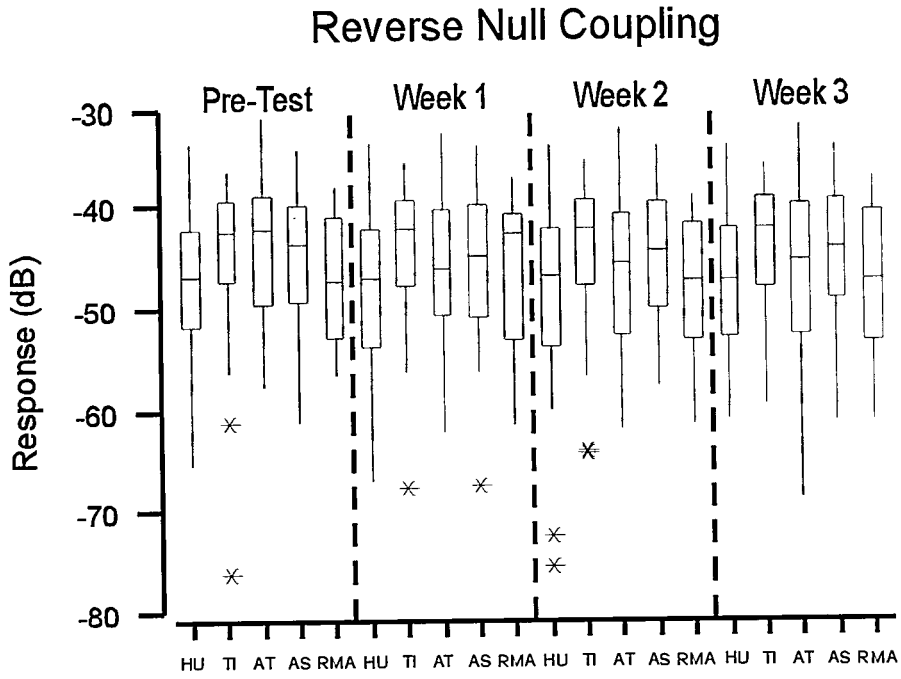

Figure 4.27 Boxplots for Reverse Null Coupling Measurements by Test Time and Site

than for the other sites. The 50 MHz forward coupling measurements were subjected to GLM analyses and gave similar results for each test time. The models for the pre-test (R^2 = 88.4%, s = 1.29) and week 3 (R^2 = 87.7%, s = 1.07) measurements are as follows:

$$Y_{Pre\text{-}test} = -39.80 - 3.06\ \text{Conformal Coat} - 5.19\ \text{Alliant Techsystems} * \text{Conformal Coat} - 5.24\ \text{Texas Instruments} * \text{Conformal Coat} - 3.65\ \text{Hughes} * \text{Conformal Coat} + 0.86\ \text{Texas Instruments} * \text{Polyimide} + 1.21\ \text{Allied Signal} * \text{Not Cleaned} * \text{Conformal Coat} \quad (4.7)$$

$$Y_{Week\ 3} = -39.44 - 2.33\ \text{Conformal Coat} + 3.03\ \text{AlliedSignal} * \text{Conformal Coat} - 2.34\ \text{Texas Instruments} * \text{Conformal Coat} - 3.67\ \text{Cleaned} * \text{Conformal Coat} - 2.99\ \text{Not Cleaned} * \text{Conformal Coat} + 1.58\ \text{Texas Instruments} * \text{Cleaned} * \text{Conformal Coat} \quad (4.8)$$

These models clearly identify conformal coating and its application at specific sites as significant processing parameters. The conformal coating applied by AlliedSignal (both low-residue and RMA boards) was observed to be more sparse than those at the other sites. As mentioned previously, the AlliedSignal low-residue measurements were very similar to those for RMA (see Figure 4.26). Given the influence attributed to conformal coating in the GLMs, this similarity is most likely due to both sets of boards being conformally coated at AlliedSignal.

The reverse coupling null measurements are displayed in boxplots by test time and site in Figure 4.27. These boxplots show that the measurements are very similar for all sites and RMA throughout the tests. During pre-test, it was observed that measurements below -50 dB were not repeatable from one test time to the next. This issue is addressed in more detail in the next section. In addition, the measurements above -50 dB for RMA and Alliant Techsystems were not as repeatable as the other sites. This lack of repeatability above -50 dB may be a reliability issue for high frequency circuit designs.

4.12 High Frequency Transmission Line Coupler - Analysis of Anomalies

Computer simulations were used to predict a value of -39dB as the ideal null frequency response of the TLC. The criterion for the upper limit for the pre-test frequency response incorporates this ideal response, the measurement resolution, and the circuit tolerance:

Upper limit for pretest frequency response
= -39dB + 5dB + 1dB = -33dB

The criterion for the upper limit following ESS incorporates one additional term to account for aging:

Upper limit for the frequency response following ESS
= -33dB + 2dB = -31dB

The circuit tolerance (1dB) and aging (2dB) are based upon engineering judgment. Only one TLC null response did not meet the pre-test criterion, an Alliant Techsystems board (polyimide substrate, cleaned, and not conformally coated - rack position 113) with a pretest reading of -31dB (just above the -33dB criterion). This board passed all subsequent tests so it was not analyzed further.

Investigation of the measuring instrument (a network analyzer) revealed that its resolution for the sharp null characteristics was only within 10dB for frequency responses less than -50dB and within 5dB for frequency responses greater than -50dB. It was concluded that the ± 5 dB criterion in the test plan was not reasonable.

Additional testing revealed that reverse null measurements less than -50 dB did not correlate from one test time to the next. To illustrate this point, pairs of successive measurements (Pre-test and Week 1, Week 1and Week 2, and Week 2 and Week 3) for each site were divided into two sets: (1) both measurements greater than or equal to -50 dB and (2) the remainder. Sample correlation coefficients were computed on these sets for each of the pairs of test times and are summarized in Figure 4.28. Note that in all cases but one, the correlations below -50 dB are less than the corresponding correlations above -50 dB. In fact, several of the correlations below -50 dB are negative, indicating a complete lack of repeatability. On the other hand, the correlations for Hughes, Texas Instruments, and AlliedSignal above -50 dB are all close to 1, indicating a high degree of repeatability. The correlations above -50 dB for Alliant Techsystems and RMA are all lower than the corresponding correlations for the other sites, with some quite lower, indicating a lower degree of repeatability.

4.13 PGA, 10-Mil Pads, and Stranded Wires - Statistical Modeling

The layout for the PGA socket was previously shown in Figure 2.19. Leakage measurements were made between the two inner squares (PGA-A) shown in this figure and also between the two outer squares (PGA-B). The two outer squares were covered with solder mask to provide a direct comparison with a similar pattern without solder mask. Measurements were made at pre-test and after 1 week, 2 weeks, and 3 weeks of ESS. Measurements

Test Time Pair	Response Frequency	Low-Residue Site				
		HE	TI	AT	AS	RMA
Pre-Test and Week 1	< -50dB	.531 (15)	.975 (8)	-.546 (15)	.324 (11)	-.412 (9)
	≥ -50dB	.982 (25)	.963 (32)	.674 (25)	.983 (29)	.654 (10)
Week 1 and Week 2	< -50dB	.022 (17)	.702 (8)	-.066 (15)	-.411 (11)	.472 (9)
	≥ -50dB	.983 (23)	.977 (32)	.858 (25)	.994 (29)	.919 (10)
Week 2 and Week 3	< -50dB	-.170 (15)	.092 (7)	.036 (14)	-.138 (11)	.434 (8)
	≥ -50dB	.977 (25)	.982 (33)	.971 (26)	.994 (29)	.950 (11)

Figure 4.28 Correlations of Pairs of Successive Reverse Null Frequency Response Measurements by Site and Range of Response Frequency. (The numbers in parentheses indicate the number of measurements.)

for PGA-A and PGA-B are shown in boxplots by test time and site in Figures 4.29 and 4.30, respectively. Since these two figures are very similar, the solder mask does not appear to influence leakage. The upper limit for the change in current in the test plan was 10 μA. Currents (nA) shown in Figures 4.29 and 4.30 are too small to support a change as large as 10μA, hence these data were not subjected to further analyses. However, it is worth noting that although the RMA pre-test leakage measurements without solder mask met the test criterion, they exhibited greater variability as noted by the elongated boxplot in Figure 4.29.

The 10-mil pads were laid out in two rows of five pads each and the pads within each row were connected on the bottom layer of the board. The leakage between the two rows was measured at pre-test and after 1 week, 2 weeks, and 3 weeks of ESS. These measurements are shown in boxplots by test time and site in Figure 4.31. The upper limit for the change in current in the test plan was also 10 μA for the pads. Currents shown in Figure 4.31 are lower than those in Figures 4.29 and 4.30, hence these data were not subjected to further analyses. As was noted for the PGA pre-test RMA leakage measurements without solder mask, the RMA pre-test leakage measurements for the 10-mil pads met the test criterion, but they exhibited far more variability as indicated by the elongated boxplot in Figure 4.31.

Two 22-gauge stranded wires were hand soldered as previously shown in Figure 2.20. One wire was soldered directly into plated through holes and the other was soldered to two terminals. The wires on two boards from each assembly site, including two RMA boards, were visually inspected after week 3 of ESS. The wire insulation was removed to inspect for flux residues and corrosion. All wires appeared normal with no corrosion and very little remaining residues. The RMA control boards did have slight brown colored residues on the wires just beyond the solder joints. This residue was considered normal for RMA processes by the task force.

The primary mode of evaluating the stranded wires was visual inspection, however electrical measurements‡ were also made in an attempt to gain further insight. These measurements displayed large variation for all sites and processes and increased significantly with time. The probe point where each measurement was taken was scraped to remove oxidized metal. Results improved, but the basic problem was not resolved. Hence, these measurements are not reported.

‡ The stranded wires were electrically tested by applying a 5A pulse from a constant current source and measuring the resulting voltage with an oscilloscope. An oscilloscope probe was connected to a test point close to the stranded wires. A laboratory pulse generator was used to command the constant current source when to supply the pulse. A ground loop was created by the oscilloscope's 115VAC input power ground being common with that of the pulse generator. This common ground connection continued from the pulse generator's signal ground to the constant current source's ground, from there to the stranded wire's ground, and finally on to the oscilloscope probe's ground return. The 5A return from the stranded wires to the constant current source generated noise in the ground loop that appeared on the oscilloscope signal lines as "common-mode" noise. The 60Hz AC power noise probably added to the common mode noise to some degree. The resulting noise was decreased by capacitively de-coupling the 5A constant current ground from the pulse generator's signal ground. After this modification, the stranded wires measured close to the resistance indicated by handbook tables on the characteristics of copper wire.

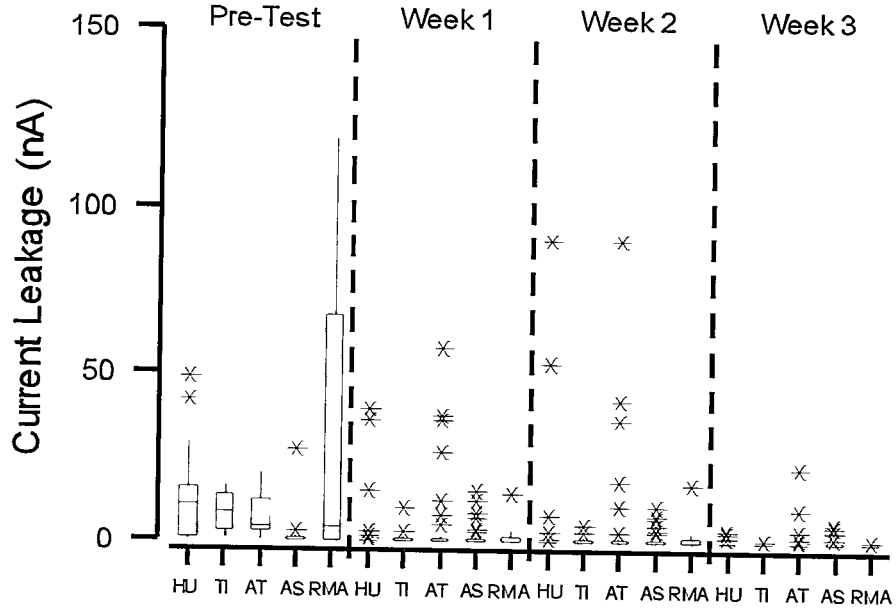

Figure 4.29 Boxplots of PGA-A Current Leakage by Test Time and Site (No solder mask)

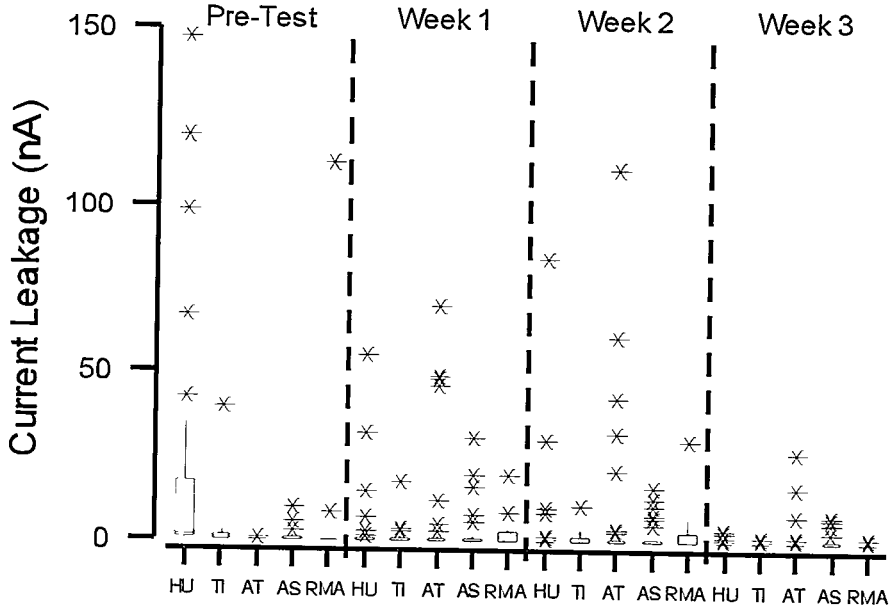

Figure 4.30 Boxplots of PGA-B Current Leakage by Test Time and Site (Solder mask)

4.14 Ionic Cleanliness Test Results

Each test site shipped functional assemblies in clean bags to the EMPF for ionic conductivity testing. Ionic conductivity tests were performed using an Ionograph 500M - an unheated, dynamic test system commonly used in industry. This system was chemically calibrated daily once the system had reached its stabilized, ambient temperature.

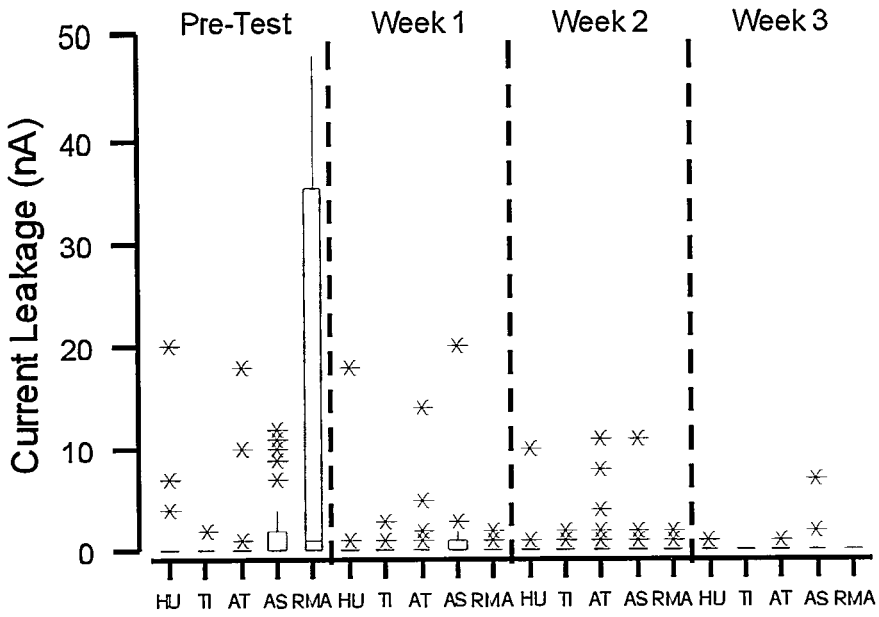

Figure 4.31 Boxplots of 10-Mil Pads Current Leakage by Test Time and Site

		Low-Residue Site				
Substrate	**Cleaned**	**TI**	**AT**	**AS**	**HE**	**RMA**
Polyimide	**Yes**	0.22	0.74	24.58	0.87	4.77
	No	7.46	16.22	55.37	182.35	
FR-4	**Yes**	0.55	0.78	35.47	13.91	14.91
	No	7.75	14.91	77.81	184.67	

Figure 4.32 Mean Ionic Cleanliness in µg/in^2 NaCl Equivalence for LRSTF Boards after Processing

The temperature and flow rate were recorded for each test to ensure consistency of results (within measurement error). Testing was performed with 75% (±2%) isopropyl alcohol in a DI water test solution. The system was operated using the automatic end-point algorithm, and the actual test time was recorded for each test. Test results averages are reported in µg/in^2 NaCl equivalence in Figure 4.32.

In general, the ionic conductivity test results covered a wide range, reflecting the material and process differences between test sites. Texas Instruments and Alliant Techsystems both used spray fluxing for wave soldering, and both sites had relatively low ionic conductivity levels (5-20 µg/in^2 NaCl equivalence for uncleaned assemblies). AlliedSignal used foam fluxing and had higher readings (50-100 µg/in^2 NaCl equivalence for uncleaned assemblies). Hughes Electronics applied the most flux with wave fluxing and had the highest readings (150-210 µg/in^2 NaCl equivalence for uncleaned assemblies).

In addition, ionic conductivity results indicated the relative effectiveness of the various cleaning processes used by the test sites. Texas Instruments (using DI water cleaning) and Alliant Techsystems (using IPA/DI water cleaning) achieved cleanliness levels less than 2.5 µg/in^2 NaCl equivalence after cleaning. Hughes Electronics (using Oakite OkemClean cleaning) achieved mixed results, with three assemblies testing less than 4.5 µg/in^2 NaCl equivalence and with two other assemblies testing between

24 and 45 µg/in^2 NaCl equivalence. Test results indicate that AlliedSignal (using IPA cleaning) had the least effective cleaning process, with typical remaining residue levels between 20-35 µg/in^2 NaCl equivalence.

As shown in Figure 4.32, three of the four low-residue sites with cleaning had lower ionics (0.22 to 0.87 µg/in^2) than RMA cleaned (4.77 µg/in^2) for the polyimide substrate. Three of the four low-residue sites with cleaning also had lower ionics (0.55 to 13.91 µg/in^2) than RMA cleaned (14.91 µg/in^2) for the FR-4 substrate. In addition, the Texas Instruments boards with an FR-4 substrate *without cleaning* had lower ionics (7.75 µg/in^2) than the RMA FR-4 cleaned boards (14.91 µg/in^2), and Alliant Techsystems without cleaning had the same level as RMA.

4.15 High Pressure Liquid Chromatography / Ion Chromatography Test Results

The LRSTF PWAs (partially functional) were analyzed by CSL Inc. for process residues using ion chromatography to detect ionic residues and using high pressure liquid chromatography (HPLC) to detect organic residues. The same extract solution used for ion chromatography was also used for HPLC.

The ion chromatography analysis detected three residues: chloride, bromide, and weak organic acids (WOAs). The HPLC analysis detected two residues: rosin and WOAs. The mean residues (µg/in^2 of extracted surface) from these two analyses are shown in Figure 4.33. The rosin column in Figure 4.33 represents a combination of detected isomers: abietic acid, dehydro-abietic acid, and neo-abietic acid. The WOA residues detected by HPLC are similar to those detected by ion chromatography. The difference is due to a different type of detector used on the HPLC system.

Chloride

Chloride is one of the more detrimental materials found on printed circuit assemblies, and one of the first materials that is examined when assessing board cleanliness. Chlorides can come from a variety of sources, but are most often attributable to flux residues. Chlorides will generally initiate and propagate electrochemical failure mechanisms, such as metal migration and electrolytic corrosion, when combined with water and an electrical potential. These characteristics are generally well known. The amount of chloride that can be tolerated on an assembly depends on the flux chemistry being used, the design, and the end use environment. Assemblies processed with high-solids rosin fluxes (RA, RMA) can tolerate higher levels of chloride due to the encapsulating nature of the rosin. Water soluble fluxes and low-residue fluxes are generally based on resins or very low levels of rosin, and so do not have this encapsulating protection, therefore they require lower levels of flux on final assemblies. Note that the recorded levels of chloride and bromide shown in Figure 4.33 for RMA boards (1.32 µg/in^2 for polyimide and 3.02 µg/in^2 for FR-4) exceed that of the corresponding low-residue boards (0.18 to 0.63 µg/in^2 for polyimide and 0.80 to 1.94 µg/in^2 for FR-4) in all cases.

Rosin / Resin

The HPLC testing showed residual rosin on all processed assemblies. The source of the residual rosin was the Kester 245 solder paste and from the hand soldering operations. The levels exhibited are fairly low for sites except AlliedSignal and are not believed to be a cause for concern. The values for HPLC rosin for AlliedSignal were significantly higher than any other test site. This is most likely caused by residual rosin flux in the foam fluxer stone (see Wave Soldering Flux Application in Section 3.5), although no additional testing was done to confirm or deny this theory. High rosin content was not characteristic of the low-residue fluxes used by Allied-Signal.

HPLC testing also detected the WOAs contained in the extract solution. In general, the levels of WOAs detected by IC and those detected by HPLC are very close, with the difference attributable to the difference in the detectors in the two systems.

Bromide

Bromide is generally attributable to the bromide fire retardant added to laminates to give fire resistance, and which is subsequently extracted in the ion chromatography analytical procedure. Bromide can also sometimes come from solder masks. Bromide is not a material considered to degrade long term reliability of electronic assemblies. The level of bromide can vary depending on the porosity of the laminate and/or mask, or the degree of over/under cure of the laminate or mask. Levels of bromide noted on the FR-4 LRSTF assemblies were consistent with FR-4 laminate. A lesser amount of bromide was noted for the polyimide boards, due to the lower amounts of added bromide in polyimide laminate, however, these levels are consistent with polyimide laminate. The cleaning operations do not have a great impact on the levels of bromide.

			Ion Chromatography			HPLC	
		Substrate	Chloride	Bromide	WOA	Rosin/ Resin	WOA
Bare Boards		Polyimide	0.63	0.22	0.00	0	0
		FR-4	1.23	0.68	0.00	0	0
Site	**Cleaned**						
AS RMA	Freon Cleaning	Polyimide	1.32	1.64	0.00	2.43	0
		FR-4	3.02	3.77	0.00	3.67	0
TI	No	Polyimide	0.34	0.42	7.78	1.18	7.09
		FR-4	0.97	1.27	14.40	1.52	13.96
	Yes	Polyimide	0.19	0.25	2.70	1.04	3.12
		FR-4	0.80	1.03	5.86	1.35	6.54
AT	No	Polyimide	0.36	0.48	6.76	0.90	7.24
		FR-4	1.23	1.29	18.26	1.03	20.24
	Yes	Polyimide	0.18	0.22	2.41	0.18	1.31
		FR-4	0.89	0.93	5.29	0.39	5.67
HE	No	Polyimide	0.63	0.54	126.49	1.13	139.45
		FR-4	1.94	1.15	240.85	1.73	246.14
	Yes	Polyimide	0.24	0.16	2.13	0.33	3.76
		FR-4	1.09	1.39	7.41	0.41	10.17
AS	No	Polyimide	0.49	0.48	17.52	24.16	16.79
		FR-4	1.42	1.21	25.55	48.71	23.99
	Yes	Polyimide	0.19	0.26	6.69	15.94	7.23
		FR-4	1.10	0.99	10.33	21.60	11.16

Figure 4.33 Mean Ionic and Organic Data (µg/in^2) from Ion Chromatography and HPLC on LRSTF Boards after Processing

Weak Organic Acids

Weak organic acids, such as adipic or succinic acid, are used as activator compounds in many fluxes, especially low-residue fluxes. WOAs are considered benign materials and are not considered a threat to long term reliability. All detected weak organic acid species were grouped collectively as WOAs to avoid disclosing formulations used by flux manufacturers. The WOAs in this evaluation were blends of multiple WOAs including adipic acid, succinic acid, and malic acid. The standard test method, used in this evaluation, did not separate and quantify the WOAs into the individual acids. Such a quantification is possible, but was outside the scope of this investigation.

The levels of WOAs are highly variable among the four manufacturing sites. The levels of WOAs noted for Texas Instruments and Alliant Techsystems were considered typical of low-solids flux manufacturing processes and did not have any adverse impact. The levels of WOAs noted for AlliedSignal (for FR-4) and Hughes were very high with respect to WOAs as expected for a foam and wave fluxing operation, respectively. In spite of these high levels of WOAs, SIR and functional electrical testing showed that the performance of the AlliedSignal and Hughes assemblies was comparable to the RMA assemblies. The levels of WOAs for polyimides were quite low compared to the values observed for the FR-4 assemblies for each of the processing sites.

The cleaning operations are effective in reducing the concentration of WOAs. A baseline of 3-5 $\mu g/in^2$ seems to be the lowest level achievable for this study. Based on the processes used in this study, detectable concentrations of WOAs ranging from 2.13 $\mu g/in^2$ to 240.85 $\mu g/in^2$ on the LRSTF board produced results comparable to those of RMA.

Conclusions

1. The assemblies tested do not contain residues outside of those typically found on low-solids flux processed assemblies, namely: chloride, bromide, weak organic acids (WOAs) and rosin.
2. The levels of WOAs were variable among the four processing sites and were attributable to the amount of flux applied in those individual processes. The AlliedSignal and Hughes assemblies had high levels of applied flux, and so had correspondingly higher levels of WOAs. The levels of WOAs detected on the polyimide assemblies were dramatically lower than those seen on the FR-4 laminates.
3. The bromide levels noted for FR-4 were typical for epoxy glass laminate. The amount of bromide found on the polyimide assemblies was significantly lower than that found on the FR-4.
4. The chloride levels were fairly low for the uncleaned assemblies. The cleaning operations were effective at reducing the chloride levels. The levels of chloride are much lower for polyimide than those noted for comparable FR-4 assemblies.
5. HPLC and ion chromatography analyses agreed on the levels of WOAs detected. Differences in readings were attributed to the difference in conductivity detectors used.
6. HPLC was able to detect low levels of residual rosin in the form of abietic acid.

5. Surface Insulation Resistance Test Results

5.1 Processing of the IPC-B-24s at the Four Test Sites

Each of the four test sites processed 30 IPC-B-24 boards for surface insulation resistance (SIR) testing. Twelve of these boards were soldered with a reflow process and 12 with a wave process. The remaining six boards served as controls. None of the control boards were soldered, but three of them received conformal coating. The experimental design specified processing three low-residue boards at each site for each of the following cases:

1. Apply paste to comb pattern using stencil for IPC-B-24, reflow, clean and conformal coat
2. Apply paste to comb pattern using stencil for IPC-B-24, reflow, conformal coat
3. Apply paste to comb pattern using stencil for IPC-B-24, reflow, clean
4. Apply paste to comb pattern using stencil for IPC-B-24, reflow
5. Flux with comb pattern down, wave solder with comb pattern down, clean and conformal coat
6. Flux with comb pattern down, wave solder with comb pattern down, conformal coat
7. Flux with comb pattern down, wave solder with comb pattern down, clean
8. Flux with comb pattern down, wave solder with comb pattern down
9. Unsoldered with conformal coating
10. Unsoldered without conformal coating

All boards used in the LRSTF evaluations were procured with a specification of less than 5 $\mu g/in^2$ NaCl equivalent. Incoming LRSTF boards with the FR-4 epoxy substrate exceeded this requirement as did the MIL-I-46058C Y-coupons used for evaluating coating adhesion. All boards were sent to the EMPF and cleaned with a Westek in-line aqueous cleaner. DI water was used in the wash and rinse sections of the cleaner, with wash and rinse temperatures of 120°*F*, and pressures in the 80-90 psi range. This aqueous cleaning was sufficient to bring ionic contamination levels below 1 $\mu g/in^2$ NaCl equivalence. The IPC-B-24 boards processed by Hughes were not cleaned, as they were processed before the cleanliness issue was discovered.

The IPC-B-24 boards were soldered by each site using the same fluxes, pastes, and soldering and cleaning processes used with the functional assemblies (see Figures 3.2 and 3.3). However, it was necessary to use different solder machine parameter settings since the IPC-B-24 differs in design from the functional assembly. Due to an operator misunderstanding, AlliedSignal did not change the parameter settings for the wave soldering machine as was done at the other sites. Visual inspection of AlliedSignal's wave soldered boards identified a processing problem and several boards from cases 6 and 8 in the above list fell somewhat short of established SIR test criteria. AlliedSignal reprocessed cases 6 and 8 with proper parameter settings, which eliminated the processing problem. These replacement boards underwent SIR testing and these results have been used in all analyses presented in this section.

After processing the 30 boards in cases 1 to 10, each test site sealed individual boards in clean Kapak bags and shipped them to the EMPF for SIR testing. In addition, AlliedSignal processed three RMA boards to serve as controls for each of the following conditions:

1. Apply RMA paste to comb pattern using stencil for IPC-B-24; reflow; conformal coat
2. Apply RMA paste to comb pattern using stencil for IPC-B-24; reflow
3. RMA flux with comb pattern down; wave solder with comb pattern down; conformal coat
4. RMA flux with comb pattern down; wave solder with comb pattern down
5. Unsoldered with conformal coating
6. Unsoldered without conformal coating

Figure 5.1 gives a summary of the number of boards processed.

5.2 SIR Test Conditions

All SIR tests were performed by the EMPF at the Naval Air Warfare Center, Indianapolis using a single Despatch temperature/humidity chamber and a Keithley measurement system. SIR readings were obtained at the following times:

Initial reading:	After 2 hr at 25°*C* / 50%RH
24-hr reading:	24 hr after ramp to 85°*C* / 85%RH
96-hr reading:	96 hr after ramp to 85°*C* / 85%RH
168-hr reading:	168 hr after ramp to 85°*C* / 85%RH
Final reading:	2 hr after return to 25°*C* / 50%RH

Process	Conformal Coat	Cleaned*	Low-Residue Site				
			TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	3	3	3	3	3
		No	3	3	3	3	
	No	Yes	3	3	3	3	3
		No	3	3	3	3	
Wave	Yes	Yes	3	3	3	3	3
		No	3	3	3	3	
	No	Yes	3	3	3	3	3
		No	3	3	3	3	
Unsoldered	Yes		3	3	3	3	3
	No		3	3	3	3	3

Figure 5.1 Number of IPC-B-24 Boards Processed for SIR Testing. (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

A 50V reverse bias was applied to all assemblies during the 85°C / 85%RH environmental exposure. However, this reverse bias was not applied when readings were taken with a 100V test voltage.

Due to the large number of SIR test boards, five consecutive tests were conducted in the same chamber using identical conditions. Boards were randomly stratified among the five runs and randomly placed in the chamber test slots to minimize the possible effect of run number and slot location. Statistical modeling later showed that run number and slot location did not affect the test results.

A nonfunctional gold-plated ceramic substrate was used to measure for possible cross-contamination within the SIR chamber. The substrate was placed in the chamber with the test boards. Following completion of the test, the substrate was extracted and evaluated using ion chromatography. No cross-contamination was indicated.

The cabling and Keithley measurement system were tested before and after each run using a standard resistor assembly (13 log ohms). The measurement system was also validated across the range of expected resistance values using a test assembly with multiple resistors of varying resistance provided by Texas Instruments.

After testing, the boards were inspected at 10X magnification (30X used for referee) using backlighting to look for evidence of electrochemical migration (ECM) and/or corrosion.

All assemblies with final readings less than 10 log ohms were placed in the chamber and retested at 25°C / 50%RH to verify the readings. Re-verification for assemblies with conformal coating showed that a 2-hour hold at ambient conditions was not sufficient to stabilize the readings, since the readings increased over time.

A significant change to the test, as compared with the method specified in the test plan, involved the ramp-up from 25°C / 50%RH to 85° C / 85%RH. The plan called for a staggered ramp of temperature followed by humidity. However, due to communication problems, a simultaneous ramp of both temperature and humidity was used for all SIR tests. IPC Cleaning and Cleanliness Phase 3 Test Programs have examined both the simultaneous and non-condensing ramp methods. The simultaneous method, used in the Phase 3 Water Soluble Flux evaluation (IPC-TP-1043), was an inherently less controllable ramp method than the non-condensing method, and could lead to condensation within the chamber. Condensation may be more of a chamber-specific phenomenon than a ramp method related problem. When condensation occurs, ECM is generally observed on uncoated test samples. Figure 5.2 gives a summary of ECM cases observed on the LRTSF boards. The unsoldered blanks showed evidence of ECM, indicative of condensation in the chamber. No ECM was observed for conformally coated boards, as expected. All low-residue boards performed as good as or better than the unsoldered controls. ECM was also observed on an RMA board.

Process	Conformal Coat	Cleaned*	Low-Residue Site				
			TI	AT	AS	Hu	RMA
Reflow	Yes	Yes					
		No					
	No	Yes		1			1
		No					
Wave	Yes	Yes					
		No					
	No	Yes	2	1		1	
		No	1	1	2		
Unsoldered	Yes						
	No		2	1		1	3

Figure 5.2 Number of Occurrences of Electrochemical Migration Observed for the Three IPC-B-24 Boards in Each Cell after SIR Testing.

5.3 Statistical Modeling Results for SIR Testing

All SIR test results are available on disk, as are all the other data associated with this study. A general linear model (see Section 4.4 for a detailed explanation) was used to determine if the SIR readings were influenced by process site, soldering process (wave versus reflow soldering), cleaning process, and conformal coating. The base case model represents the unsoldered, uncoated RMA controls. The following models (based on $\log_{10}$ Ohms) were obtained for initial, 24-hr, 96-hr, 168-hr, and final SIR results:

$$\begin{aligned} SIR_{Initial} = {} & 12.22 + 1.35\ \text{Conformal Coat} + 1.09\ \text{TI*Wave} - 4.71\ \text{AT*Reflow*Cleaned} \\ & + 5.17\ \text{AT*Reflow*Cleaned*Conformal Coat} + 2.33\ \text{Reflow*Cleaned} \\ & - 1.75\ \text{AS*Wave*Not Cleaned} + 1.19\ \text{Wave} + 1.95\ \text{TI*Reflow*Not Cleaned} \\ & + 1.01\ \text{AT*Reflow*Not Cleaned} - 1.02\ \text{AT*Reflow*Conformal Coat} \\ & - 3.51\ \text{AT*Wave*Cleaned*Conformal Coat} - 2.17\ \text{AT*Wave*Not Cleaned} \\ & - 1.27\ \text{HU} - 1.03\ \text{AS} + 3.24\ \text{AT*Wave*Conformal Coat} - 1.26\ \text{Wave*Conformal Coat} \\ & - 1.89\ \text{Reflow*Cleaned*Conformal Coat} + 0.94\ \text{Hu*Wave*Not Cleaned*Conformal Coat} \\ & - 0.86\ \text{TI} - 1.51\ \text{TI*Reflow*Not Cleaned*Conformal Coat} + 0.79\ \text{Hu*Conformal Coat} \\ & + 0.84\ \text{AS*Reflow*Conformal Coat} + 0.71\ \text{AS*Wave*Conformal Coat} \end{aligned} \quad (5.1)$$

$$\begin{aligned} SIR_{24\ hr} = {} & 7.57 + 0.91\ \text{Conformal Coat} - 0.42\ \text{AS*Conformal Coat} \\ & - 0.52\ \text{Hu*Reflow*Conformal Coat} - 0.41\ \text{Cleaned} - 1.63\ \text{AT*Reflow*Cleaned} \\ & + 1.47\ \text{AT*Reflow*Conformal Coat} + 1.44\ \text{Reflow} + 1.36\ \text{Wave} \\ & - 0.95\ \text{Not Cleaned} - 1.26\ \text{Wave*Conformal Coat} - 1.21\ \text{Reflow*Conformal Coat} \\ & + 0.36\ \text{TI*Not Cleaned} + 0.78\ \text{Not Cleaned*Conformal Coat} \\ & - 1.14\ \text{AT*Reflow*Not Cleaned*Conformal Coat} + 0.26\ \text{AT} \\ & + 0.45\ \text{Cleaned*Conformal Coat} \end{aligned} \quad (5.2)$$

$$SIR_{96\ hr} = 8.68 - 1.58\ AT*Reflow*Cleaned + 1.20\ AT*Reflow*Conformal\ Coat - 0.85\ Hu*Reflow*Not\ Cleaned + 0.36\ Hu*Wave*Conformal\ Coat + 0.37\ TI*Conformal\ Coat + 0.30\ AT - 0.58\ Not\ Cleaned - 0.74\ AT*Reflow*Not\ Cleaned*Conformal\ Coat + 0.53\ Hu*Reflow - 0.63\ Hu*Reflow*Cleaned*Conformal\ Coat + 0.46\ Hu*Wave*Not\ Cleaned*Conformal\ Coat + 0.57\ Reflow*Not\ Cleaned + 0.41\ Wave - 0.36\ Wave*Cleaned \quad (5.3)$$

$$SIR_{168\ hr} = 8.69 - 1.31\ AT*Reflow*Cleaned + 0.64\ AT*Reflow*Conformal\ Coat + 0.37\ Hu*Cleaned + 0.50\ TI*Conformal\ Coat - 0.79\ TI*Reflow*Cleaned + 0.29\ AT + 0.74\ Hu*Wave*Not\ Cleaned*Conformal\ Coat - 0.17\ Not\ Cleaned*Conformal\ Coat + 0.52\ TI*Reflow*Cleaned*Conformal\ Coat - 0.41\ Hu*Reflow*Not\ Cleaned + 0.18\ Hu - 0.37\ Hu*Reflow*Cleaned*Conformal\ Coat \quad (5.4)$$

$$SIR_{Final} = 12.66 - 1.23\ Reflow*Cleaned - 2.62\ TI*Reflow - 2.14\ AT*Reflow*Cleaned + 2.07\ TI*Reflow*Conformal\ Coat + 1.02\ Reflow*Cleaned*Conformal\ Coat + 0.70\ HU*Cleaned - 0.38\ Reflow*Not\ Cleaned + 0.29\ Conformal\ Coat - 0.47\ AS*Wave*Not\ Cleaned + 0.47\ Hu*Wave*Not\ Cleaned \quad (5.5)$$

The first term (constant) in each model represents the predicted SIR value (in $\log_{10}$ Ohms) for the unsoldered RMA controls without conformal coating. This term is 8.69 in the 168-hr model. The coefficients of the other terms in the model quantify the magnitude of site-process combinations that have a significant impact on SIR results. The models can be easily interpreted by following a simple rule: If a particular site or process is involved, then replace the corresponding words in the model with 1, otherwise replace them with 0.

To illustrate use of this rule, consider the second term in the 168-hr model: -1.31 AT*Reflow*Cleaned. This term only refers to the Alliant Techsystems reflow process with cleaning. When this particular site-process combination is of interest, the second term in the model becomes -1.31 x 1 x 1 x 1 = -1.31. Since the coefficient is negative, the constant term, 8.69, is reduced by 1.31 for Alliant Techsystems' reflow processes with cleaning.

The third term in the 168-hr model is 0.64 AT*Reflow*Conformal Coat. The positive coefficient for this term represents an increase of 0.64 in SIR readings for Alliant Techsystems' low-residue reflow process with conformal coating. The seventh term in the model shows an increase of 0.29 in SIR readings for all Alliant Techsystems' low-residue processes. Thus, an Alliant Techsystems board that was reflowed, cleaned, and conformally coated deviates from the unsoldered, uncoated rosin control (8.69 $\log_{10}$ Ohms) by -1.31 + 0.64 + 0.29 = -0.38.

The models in Equations 5.1 to 5.5 all account for a significant amount of the variation in SIR measurements, with the respective R^2 and s values for the models being: 52.8% and .97, 41.1% and .53, 36.7% and .42, 34.9% and .46, 52.2% and .96. Note that the Initial and Final models exhibit about twice the variability as the other models.

These models are highly statistically significant and do a good job of modeling the variability. A pair of tables has been created to summarize the results for each model. Figure 5.3 gives a table with the predicted SIR values for each site-process combination based on the initial model given in Equation 5.1. The table in Figure 5.3 also contains the actual mean SIR values and their deviations from the predicted values. Note that these deviations are quite small, which underscores the adequacy of the model in Equation 5.1. Figure 5.4 provides a convenient table summary of the deviations of the initial SIR results from the unsoldered, uncoated RMA controls for each site-process combination. As explained in the preceding paragraphs, these deviations are derived from the coefficients in Equation 5.1. Figures 5.5-5.12 give similar summaries for the 24-hr, 96-hr, 168-hr, and final SIR results.

The SIR averages in Figures 5.3, 5.5, 5.7, 5.9, and 5.11 are compared with RMA averages in graphs for each site-process combination in Figures 5.13-5.22. The 168-hr readings are used to assess SIR performance. Figure 5.9 gives a table summary of the means at 168 hr. All values in this table are quite close, with a range from 7.57 to 9.38. Eight of the 9 values exceeding 9.00 are associated with low-residue processing (unsoldered cases are not included in this count). Only two values are less than 8.00 (both low-residue cases). These means show that the low-residue processes had slightly higher readings than the corresponding RMA processes in 5 of the 8 con-

Initial SIR Test Results

Process	Conformal Coat	Cleaned*	Low-Residue Site				
			TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	13.15	13.45	13.82	13.53	13.57
			13.48	13.45	13.80	13.07	13.38
			-0.33	0.00	0.02	0.46	0.19
		No	13.16	13.56	13.38	13.09	
			13.16	13.56	13.40	12.98	
			0.00	0.00	-0.02	0.11	
	No	Yes	13.69	9.84	13.52	13.28	12.22
			13.78	9.84	13.22	13.51	11.75
			-0.09	0.00	0.30	-0.23	0.47
		No	13.31	13.22	11.19	10.95	
			13.31	13.22	11.20	11.67	
			0.00	0.00	-0.01	-0.73	
Wave	Yes	Yes	13.73	13.23	13.18	13.02	13.50
			13.53	13.23	13.18	13.37	13.29
			0.20	0.00	0.00	-0.35	0.21
		No	13.73	14.57	11.75	13.96	
			13.78	14.57	12.01	13.39	
			-0.05	0.00	-0.26	0.56	
	No	Yes	13.64	13.41	12.37	12.13	13.41
			13.81	13.23	12.22	12.82	13.44
			-0.17	0.18	0.16	-0.68	-0.03
		No	13.64	11.24	11.66	12.13	
			13.63	11.24	11.40	12.15	
			0.02	0.00	0.26	-0.01	
Unsoldered	Yes		12.71	13.57	12.54	13.09	13.57
			12.51	13.90	12.35	13.43	13.59
			0.21	-0.33	0.19	-0.34	-0.02
	No		11.36	12.22	11.19	10.95	12.22
			11.11	11.87	11.82	9.84	13.26
			0.25	0.35	-0.63	1.11	-1.04

Figure 5.3 Predicted SIR, Actual SIR Mean, and their Difference (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

Initial SIR Test Results

Process	Conformal Coat	Cleaned*	Low-Residue Site TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	0.94	1.23	1.60	1.32	1.35
		No	0.94	1.34	1.16	0.88	
	No	Yes	1.48	-2.38	1.30	1.06	0.00
		No	1.09	1.01	-1.03	-1.27	
Wave	Yes	Yes	1.52	1.01	0.96	0.80	1.28
		No	1.52	2.35	-0.47	1.74	
	No	Yes	1.42	1.19	0.16	-0.08	1.19
		No	1.42	-0.98	-0.56	-0.08	
Unsoldered	Yes		0.50	1.35	0.32	0.88	1.35
	No		-0.86	0.00	-1.03	-1.27	0.00

Figure 5.4 Predicted Deviations from Unsoldered, Uncoated RMAs (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

formally coated cases for reflow and in 7 of the 8 conformally coated cases for wave. On the other hand, only 1 of the 16 low-residue cases exceeded the corresponding RMA process without conformal coating, although all readings were quite close. It is interesting to note that the Hughes boards had the highest average performance over all processing groups, although they were processed with excessive levels of incoming ionics (see comments in Section 5.1).

5.4 Lessons Learned and Conclusions

The following lessons were learned in the SIR testing.

- SIR test results indicate areas where process optimization is required
- Overall SIR test results for low-residue processes were comparable to RMA (even though the low-residue processes were not optimized)
- A simultaneous ramp of temperature and humidity was used in the SIR testing. ECM was observed due to condensation in the chamber, which may be a chamber specific problem. A non-condensing profile, as a more controllable method, should be used wherever possible.
- A 2-hr delay between the ramp down from 85°C / 85%RH to 25°C / 85%RH and final readings is probably not sufficient for conformally coated boards due to water retention by the conformal coating
- In some cases, cleaning had a detrimental effect on SIR test results
- The boards processed by Hughes had the highest average performance over all processing groups, although they had excessive levels of ionics
- ECM was observed on all boards: unsoldered, low-residue, and RMA
- Evidence of corrosion was noted on 1 of 3 wave soldered, not cleaned, coated boards and 3 of 3 wave soldered, not cleaned, and not coated boards processed by AlliedSignal. Discolored, corroded conductors were noted on 2 of 3 reflow soldered, conformally coated boards processed by Hughes. No evidence of corrosion was noted on any other boards.

24-Hour SIR Test Results

			Low-Residue Site				
Process	Conformal Coat	Cleaned*	TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	8.76	8.86	8.34	8.23	8.71
			8.85	8.86	8.26	8.17	8.61
			-0.09	0.00	0.08	0.06	0.10
		No	8.90	9.14	8.13	8.02	
			8.88	9.14	8.26	8.07	
			0.02	0.00	-0.13	-0.05	
	No	Yes	8.61	7.24	8.61	8.61	9.01
			8.60	7.24	8.56	8.84	8.71
			0.01	0.00	0.04	-0.24	0.30
		No	8.42	8.32	8.06	8.06	
			8.33	8.36	8.29	8.03	
			0.09	-0.04	-0.22	0.04	
Wave	Yes	Yes	8.63	8.89	8.21	8.63	8.58
			8.68	8.80	8.21	8.76	8.68
			-0.05	0.09	0.00	-0.13	-0.10
		No	8.77	8.68	8.42	8.42	
			8.76	8.56	8.24	8.59	
			0.01	0.12	0.18	-0.17	
	No	Yes	8.53	8.79	8.53	8.53	8.93
			8.47	8.85	8.42	8.40	9.23
			0.05	-0.06	0.11	0.12	-0.30
		No	8.34	8.24	7.98	7.98	
			8.45	8.23	7.89	7.84	
			-0.11	0.02	0.09	0.14	
Unsoldered	Yes		8.47	8.73	8.06	8.47	8.47
			8.66	9.01	8.03	8.30	8.26
			-0.18	-0.28	0.03	0.17	0.22
	No		7.57	7.83	7.57	7.57	7.57
			7.70	7.70	7.73	7.39	7.57
			-0.14	0.13	-0.16	0.18	0.00

Figure 5.5 Predicted SIR, Actual SIR Mean, and their Difference (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

24-Hour SIR Test Results

			Low-Residue Site				
Process	Conformal Coat	Cleaned*	TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	1.19	1.29	0.77	0.67	1.14
		No	1.34	1.57	0.56	0.46	
	No	Yes	1.04	-0.33	1.04	1.04	1.44
		No	0.85	0.75	0.49	0.49	
Wave	Yes	Yes	1.06	1.32	0.64	1.06	1.01
		No	1.20	1.11	0.85	0.85	
	No	Yes	0.96	1.22	0.96	0.96	1.37
		No	0.77	0.68	0.42	0.42	
Unsoldered	Yes		0.91	1.17	0.49	0.91	0.91
	No		0.00	0.26	0.00	0.00	0.00

Figure 5.6 Predicted Deviations from Unsoldered RMAs (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

96-Hour SIR Test Results

			Low-Residue Site				
Process	Conformal Coat	Cleaned*	TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	9.06	8.60	8.68	8.58	8.68
			8.98	8.60	8.76	8.59	8.87
			0.08	0.00	-0.08	0.00	-0.19
		No	9.05	9.43	8.67	8.35	
			8.98	9.43	8.68	8.46	
			0.07	0.00	0.00	-0.11	
	No	Yes	8.68	7.40	8.68	9.21	8.68
			8.60	7.40	8.64	9.21	8.82
			0.08	0.00	0.04	0.00	-0.13
		No	8.67	8.98	8.67	8.35	
			8.66	8.94	8.80	8.20	
			0.02	0.04	-0.13	0.15	
Wave	Yes	Yes	9.11	9.04	8.74	9.10	9.10
			9.04	8.93	8.66	9.17	8.77
			0.07	0.11	0.08	-0.07	0.32
		No	8.89	8.82	8.52	9.35	
			9.05	8.76	8.66	9.20	
			-0.16	0.06	-0.14	0.15	
	No	Yes	8.74	9.04	8.74	8.74	9.10
			8.61	9.11	8.93	8.95	9.42
			0.13	-0.07	-0.19	-0.22	-0.32
		No	8.52	8.82	8.52	8.52	
			8.59	8.77	8.25	8.53	
			-0.07	0.05	0.27	-0.02	
Unsoldered	Yes		9.06	8.99	8.68	8.68	8.68
			9.12	9.38	8.52	8.66	8.52
			-0.07	-0.39	0.16	0.02	0.16
	No		8.68	8.99	8.68	8.68	8.68
			8.70	8.82	8.88	8.75	8.32
			-0.01	0.17	-0.19	-0.07	0.36

Figure 5.7 Predicted SIR, Actual SIR Mean, and their Difference (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

96-Hour SIR Test Results

			Low-Residue Site				
Process	Conformal Coat	Cleaned*	TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	0.37	-0.08	0.00	-0.10	0.00
		No	0.36	0.75	-0.01	-0.34	
	No	Yes	0.00	-10.28	0.00	0.53	0.00
		No	-0.01	0.29	-0.01	-0.34	
Wave	Yes	Yes	0.42	0.36	0.05	0.42	0.41
		No	0.21	0.14	-0.17	0.66	
	No	Yes	0.05	0.36	0.05	0.05	0.41
		No	-0.17	0.14	-0.17	-0.17	
Unsoldered	Yes		0.37	0.30	0.00	0.00	0.00
	No		0.00	0.30	0.00	0.00	0.00

Figure 5.8 Predicted Deviations from Unsoldered RMAs (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

168-Hour SIR Test Results

			Low-Residue Site				
Process	Conformal Coat	Cleaned*	TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	8.93	8.32	8.69	8.87	8.69
			8.93	8.43	8.75	8.87	8.72
			0.00	-0.11	-0.06	0.00	-0.03
		No	9.03	9.46	8.52	8.29	
			8.92	9.35	8.57	8.35	
			0.10	0.11	-0.05	-0.06	
	No	Yes	7.91	7.67	8.69	9.25	8.69
			7.91	7.57	8.63	9.38	8.95
			0.00	0.11	0.07	-0.13	-0.26
		No	8.69	8.98	8.69	8.46	
			8.74	8.86	8.74	8.37	
			-0.05	0.12	-0.05	0.09	
Wave	Yes	Yes	9.20	8.98	8.69	9.25	8.69
			9.13	8.91	8.68	9.34	8.59
			0.06	0.07	0.02	-0.09	0.10
		No	9.03	8.81	8.52	9.44	
			9.14	8.81	8.53	9.27	
			-0.11	0.00	0.00	0.18	
	No	Yes	8.69	8.98	8.69	9.25	8.69
			8.61	9.15	9.02	9.08	9.37
			0.08	-0.17	-0.33	0.17	-0.68
		No	8.69	8.98	8.69	8.87	
			8.62	8.89	8.43	8.79	
			0.07	0.09	0.26	0.08	
Unsoldered	Yes		9.20	8.98	8.69	8.87	8.69
			9.27	9.26	8.52	8.86	8.40
			-0.07	-0.28	0.17	0.01	0.30
	No		8.69	8.98	8.69	8.87	8.69
			8.87	8.94	9.00	8.96	7.80
			-0.17	0.04	-0.30	-0.09	0.89

Figure 5.9 Predicted SIR, Actual SIR Mean, and their Difference (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

168-Hour SIR Test Results

			Low-Residue Site				
Process	Conformal Coat	Cleaned*	TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	0.23	-0.38	0.00	0.18	0.00
		No	0.33	0.76	-0.17	-0.40	
	No	Yes	-0.79	-1.02	0.00	0.55	0.00
		No	0.00	0.29	0.00	-0.23	
Wave	Yes	Yes	0.50	0.29	0.00	0.55	0.00
		No	0.33	0.12	-0.17	0.75	
	No	Yes	0.00	0.29	0.00	0.55	0.00
		No	0.00	0.29	0.00	0.18	
Unsoldered	Yes		0.50	0.29	0.00	0.18	0.00
	No		0.00	0.29	0.00	0.18	0.00

Figure 5.10 Predicted Deviations from Unsoldered RMAs (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

Final SIR Test Results

Process	Conformal Coat	Cleaned*	Low-Residue Site TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	12.18	10.59	12.74	13.44	12.94
			12.33	10.69	12.62	13.25	12.75
			-0.15	-0.10	0.12	0.19	0.19
		No	12.01	12.56	12.56	12.56	
			11.86	12.83	12.43	12.37	
			0.15	-0.27	0.13	0.20	
	No	Yes	8.81	9.28	11.43	12.13	12.66
			8.66	9.19	11.12	12.72	13.52
			0.14	0.10	0.31	-0.59	-0.86
		No	9.65	12.28	12.28	12.28	
			9.81	12.09	12.87	11.79	
			-0.15	0.19	-0.59	0.48	
Wave	Yes	Yes	12.94	12.94	12.94	13.65	12.94
			13.28	12.96	12.83	13.09	12.96
			-0.34	-0.02	0.12	0.56	-0.02
		No	12.94	12.94	12.47	13.41	
			13.13	12.83	12.82	13.74	
			-0.19	0.11	-0.34	-0.33	
	No	Yes	12.66	12.66	12.66	13.36	12.66
			11.99	12.78	12.84	13.35	12.97
			0.66	-0.13	-0.18	0.02	-0.31
		No	12.66	12.66	12.19	13.12	
			12.70	12.94	11.85	13.02	
			-0.04	-0.28	0.34	0.10	
Unsoldered	Yes		12.94	12.94	12.94	12.94	12.94
			12.51	12.84	12.70	13.13	13.47
			0.44	0.10	0.25	-0.19	-0.53
	No		12.66	12.66	12.66	12.66	12.66
			12.60	12.36	12.87	12.66	11.94
			0.06	0.30	-0.21	-0.01	0.72

Figure 5.11 Predicted SIR, Actual SIR Mean, and their Difference (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

Final SIR Test Results

			Low-Residue Site				
Process	Conformal Coat	Cleaned*	TI	AT	AS	Hu	RMA
Reflow	Yes	Yes	-0.48	-2.07	0.08	0.78	0.29
		No	-0.65	-0.10	-0.10	-0.10	
	No	Yes	-3.85	-3.37	-1.23	-0.53	0.00
		No	-3.00	-0.38	-0.38	-0.38	
Wave	Yes	Yes	0.29	0.29	0.29	0.99	0.29
		No	0.29	0.29	-0.18	0.75	
	No	Yes	0.00	0.00	0.00	0.70	0.00
		No	0.00	0.00	-0.47	0.47	
Unsoldered	Yes		0.29	0.29	0.29	0.29	0.29
	No		0.00	0.00	0.00	0.00	0.00

Figure 5.12 Predicted Deviations from Unsoldered RMAs (in Log_{10} Ohms). (*The Cleaning Process Used with Low-Residue Differs from that Used with the Standard RMA Process.)

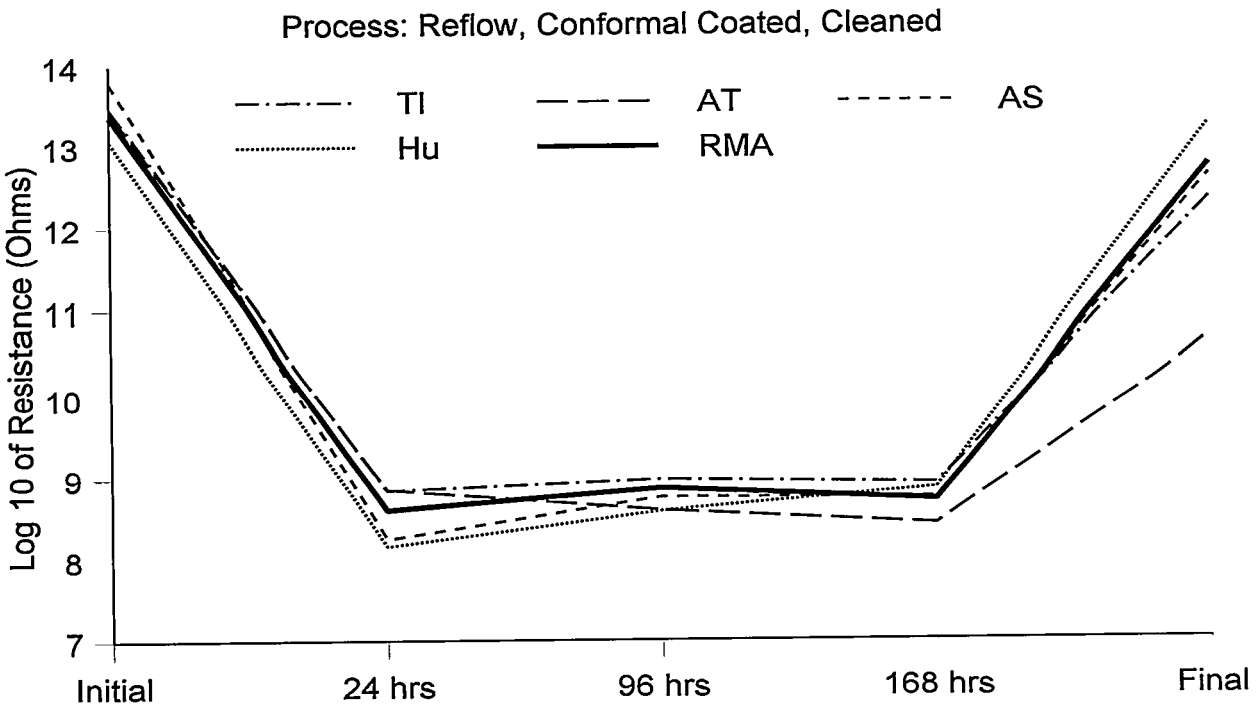

Figure 5.13 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

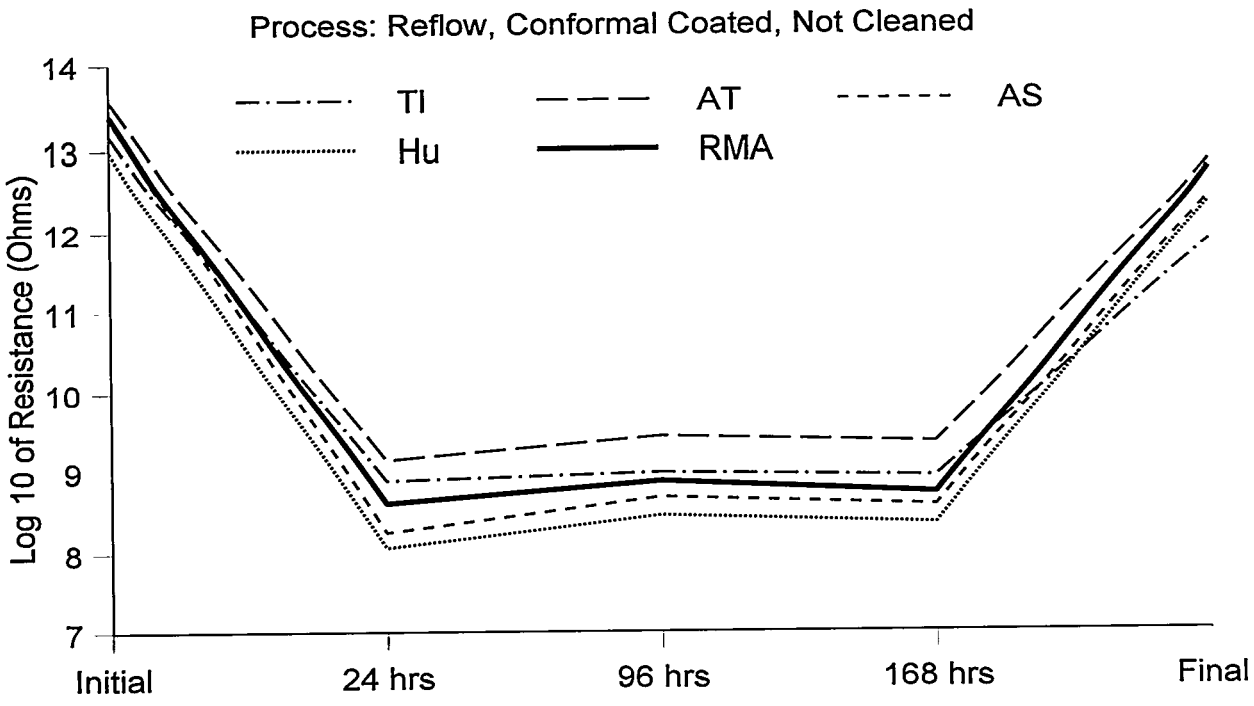

Figure 5.14 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

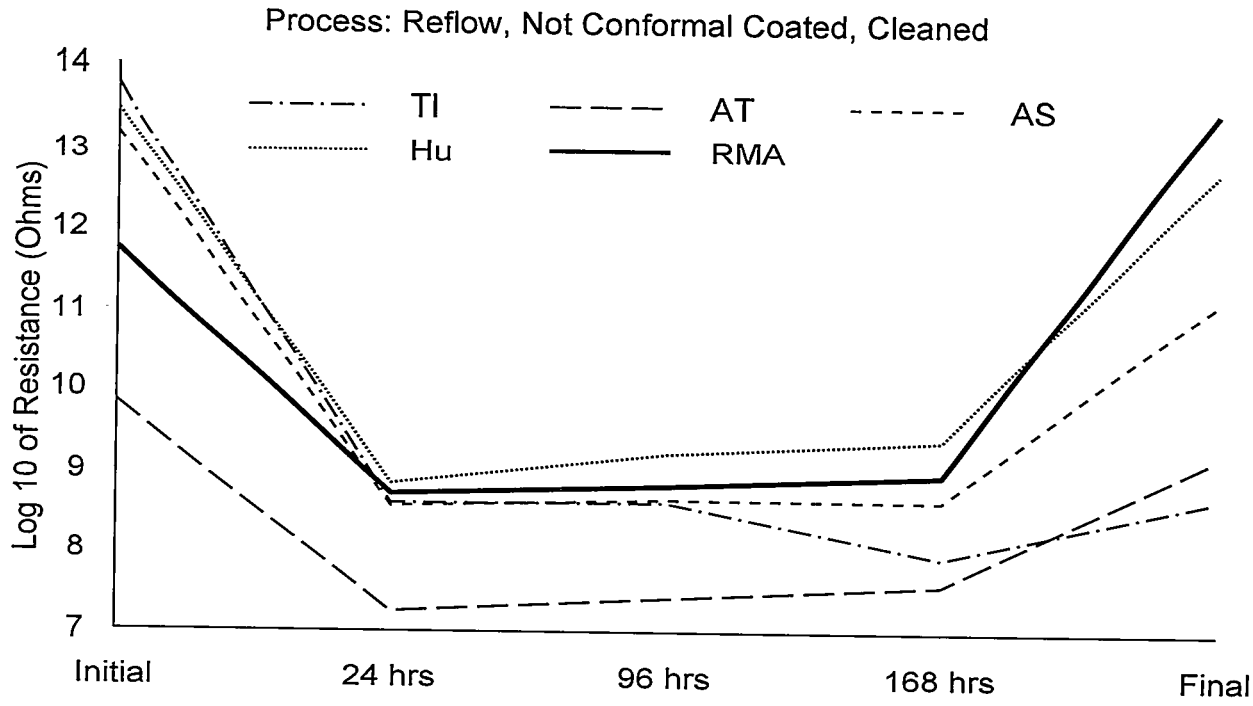

Figure 5.15 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

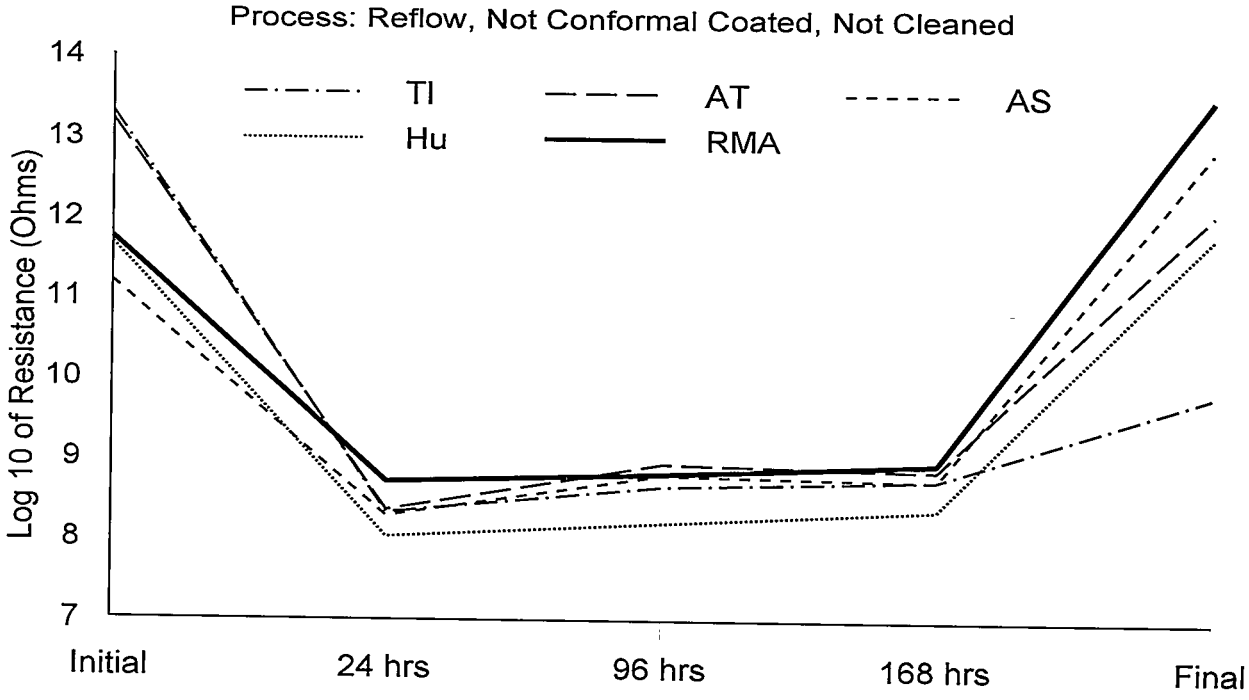

Figure 5.16 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

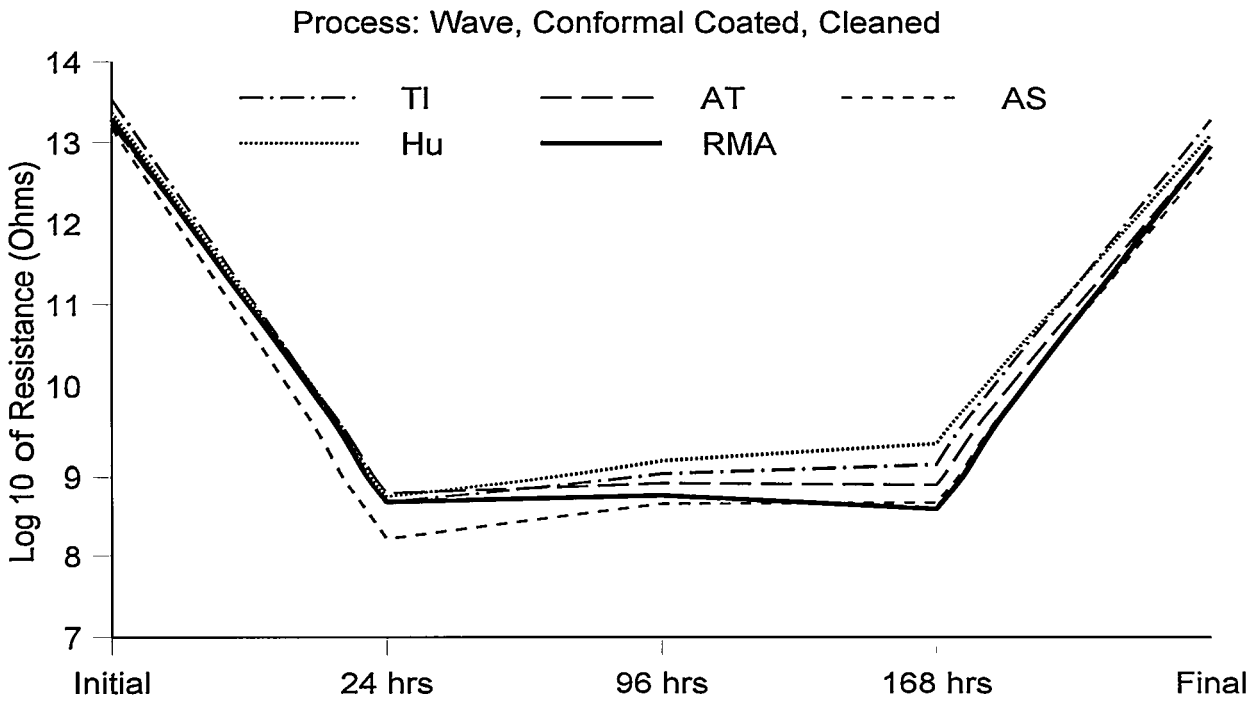

Figure 5.17 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

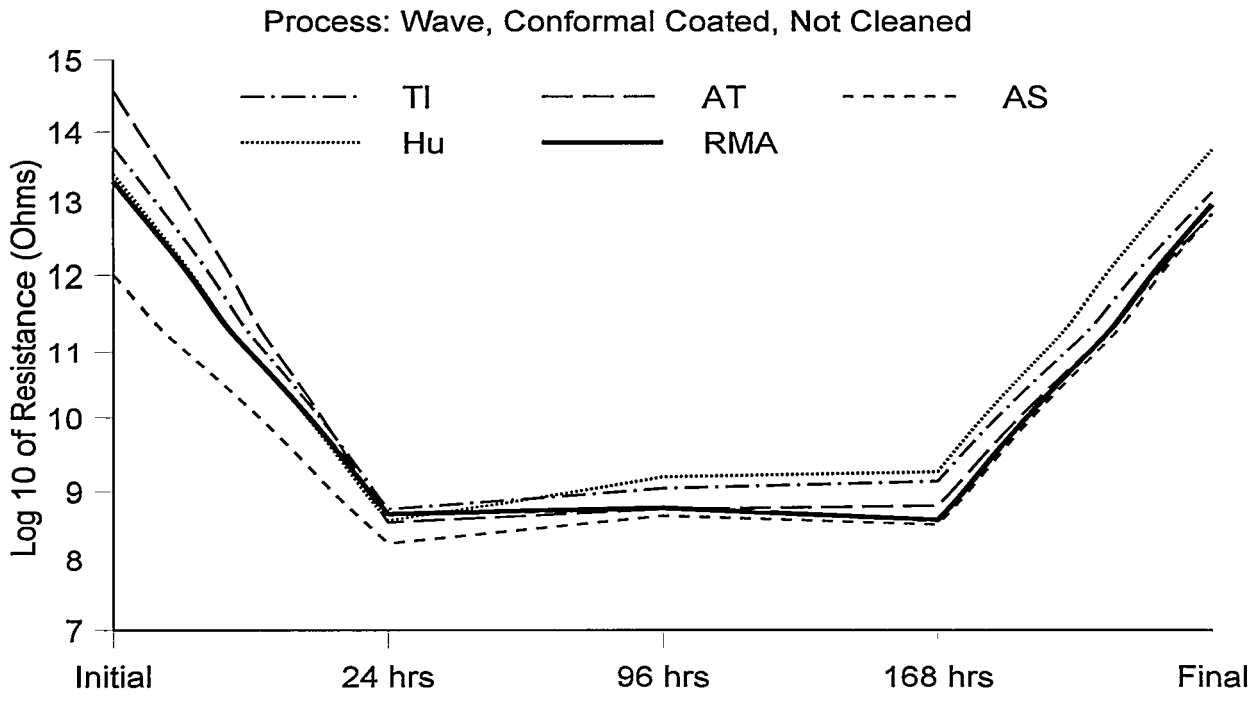

Figure 5.18 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

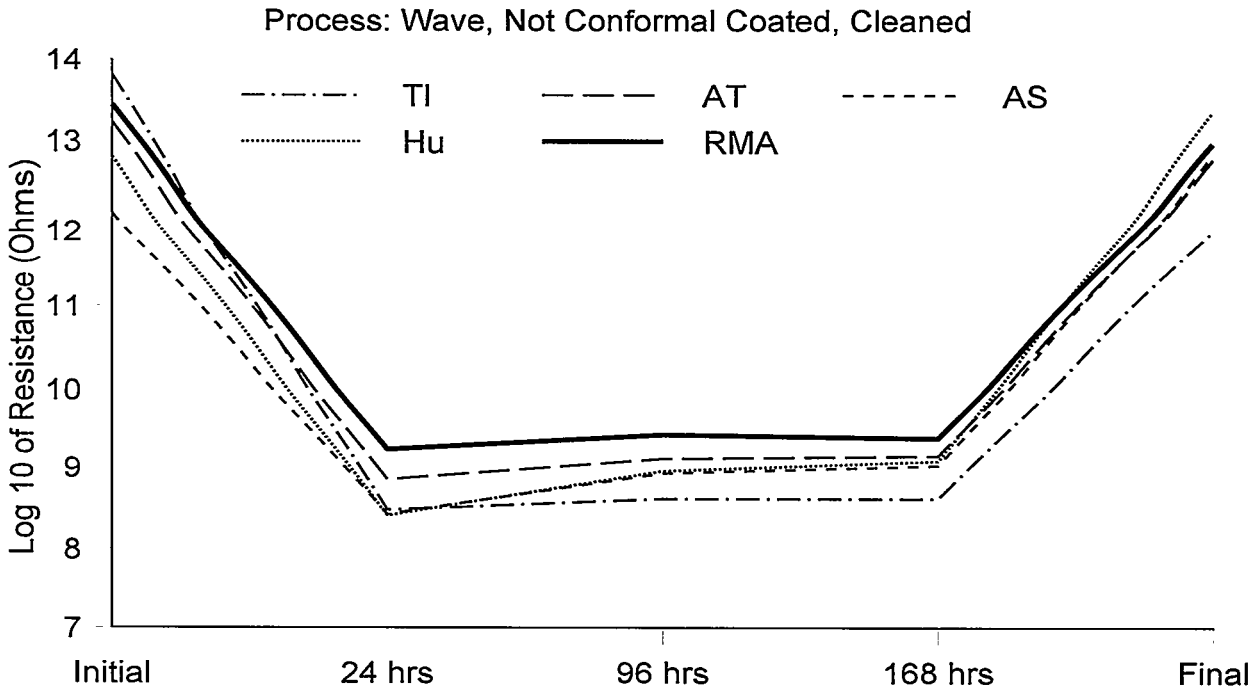

Figure 5.19 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

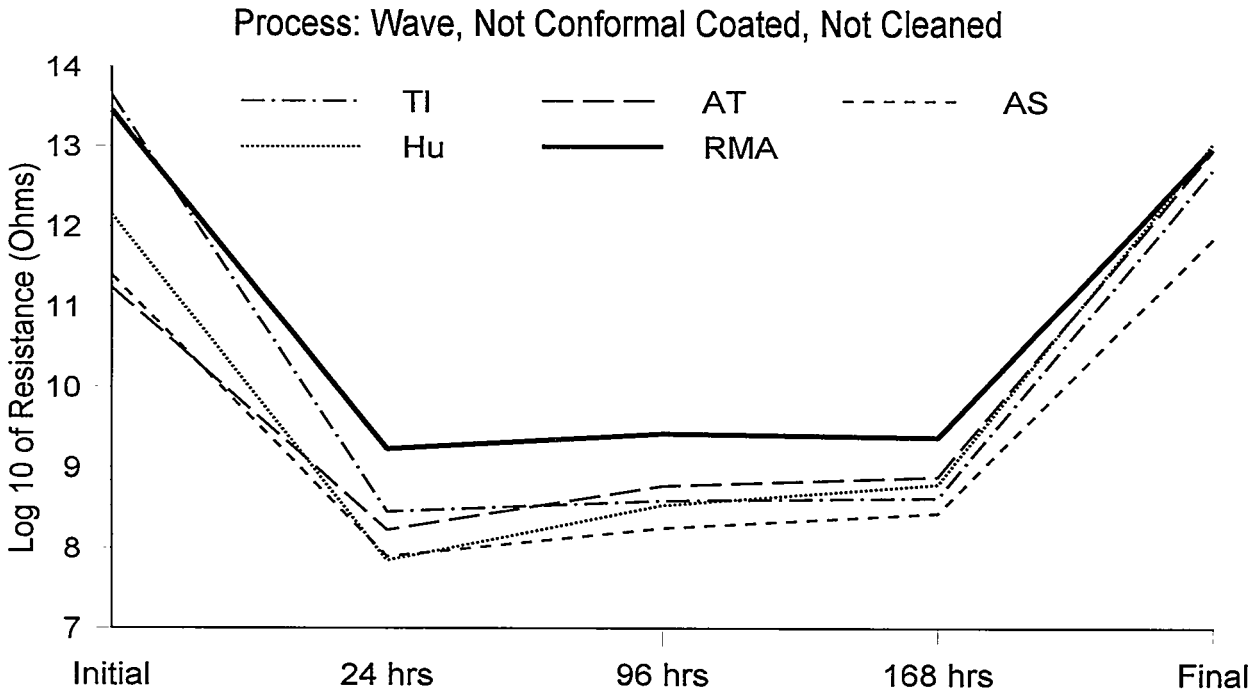

Figure 5.20 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

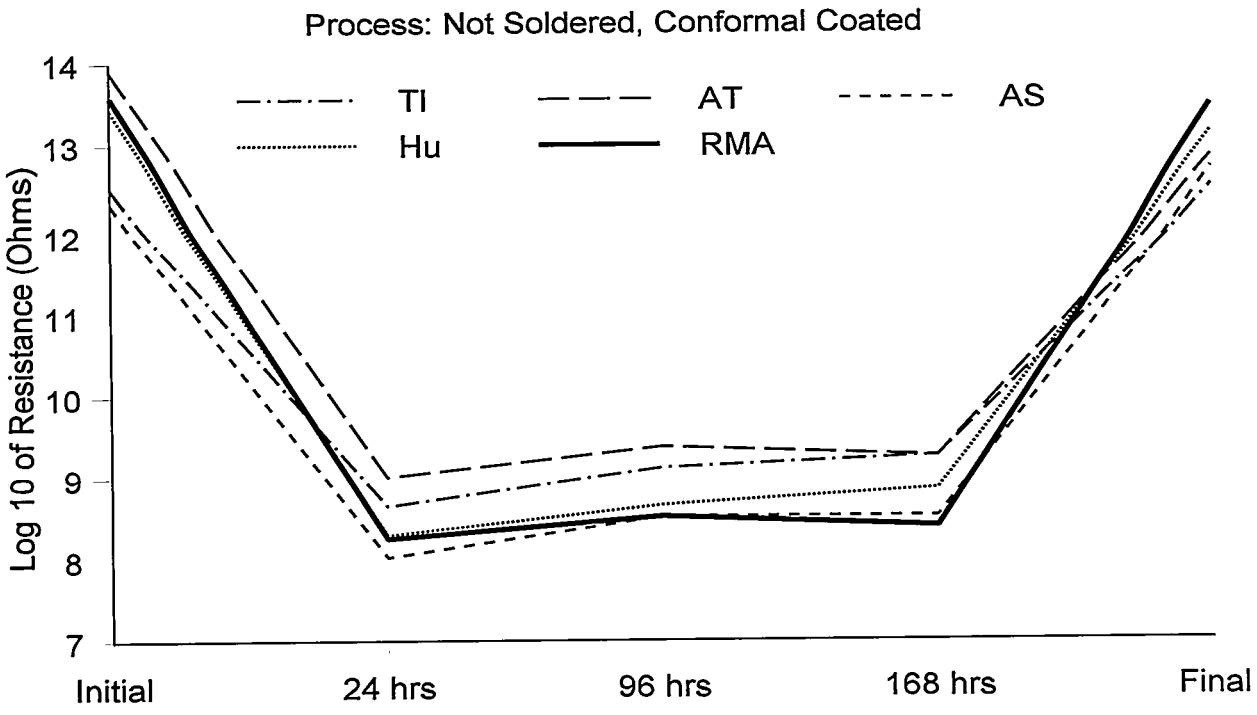

Figure 5.21 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

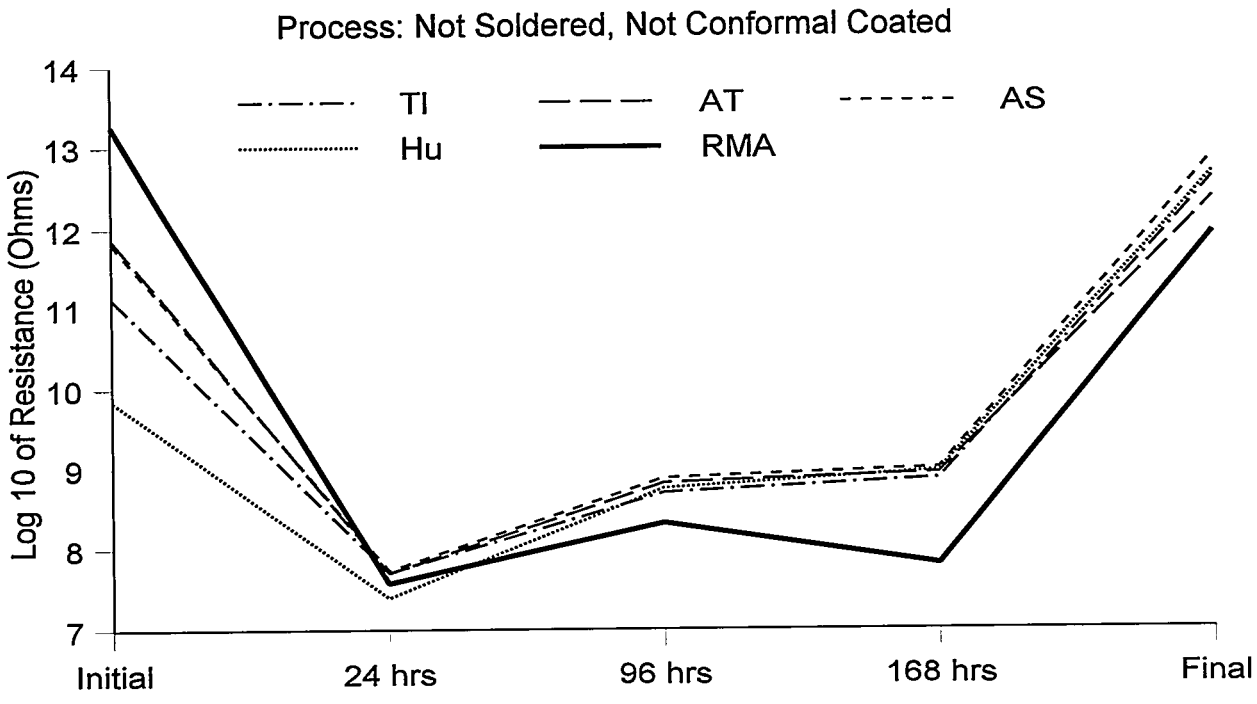

Figure 5.22 Average SIR over Time by Site (Note: the X-axis is not on a linear scale.)

6. Coating Adhesion Test Results

6.1 Coating Adhesion

Tests were conducted at AlliedSignal to evaluate the possible effects of low-residue fluxes on adhesion of conformal coating. These tests were conducted with single-sided, FR-4 laminate, MIL-I-46058C Y-coupons. Adhesion properties were evaluated using peel-by-tape tests and inspections for mealing. Peel-by-tape tests subjectively quantify the adhesion of conformal coating. These tests were conducted according to ASTM D 3359, Method B (Standard Test Methods for Measuring Adhesion by Tape Test). Peel-by-tape tests were done before and after environmental conditioning using the environmental conditions specified in MIL-STD-202, Method 106, Moisture Resistance. Mealing inspections to evaluate appearance and coating integrity were also made before and after environmental conditioning.

A total of forty-four panels were processed by the manufacturing sites using low-residue soldering processes, either reflow, wave, or hand. Half of these panels were cleaned before application of conformal coating. Standard RMA processed Y-coupons were manufactured to serve as controls for the test.

6.2 Processing of the MIL-I-46058C Coupons

Each panel contained five Y-coupons as shown in Figure 6.1. The sites processed the panels with the same materials, equipment, and processes used for the LRSTF assembly (see Figures 3.2 and 3.3), except Texas Instruments dispensed paste for their reflow process. Two panels were processed at each site for each of the following conditions, except hand solder at Hughes (panels lost in transit) and the RMA control panels (processed only at AlliedSignal).

1. Low-residue wave solder
2. Low-residue wave solder with cleaning
3. Low-residue paste and reflow
4. Low-residue paste and reflow with cleaning
5. Low-residue hand solder
6. Low-residue hand solder with cleaning
7. RMA wave solder (cleaned)
8. RMA reflow (cleaned)
9. RMA hand solder (cleaned)

All panels were conformal coated after processing, individually packaged, and shipped to AlliedSignal for testing. Figure 6.2 gives a summary of the number of panels processed by for each site-process combination.

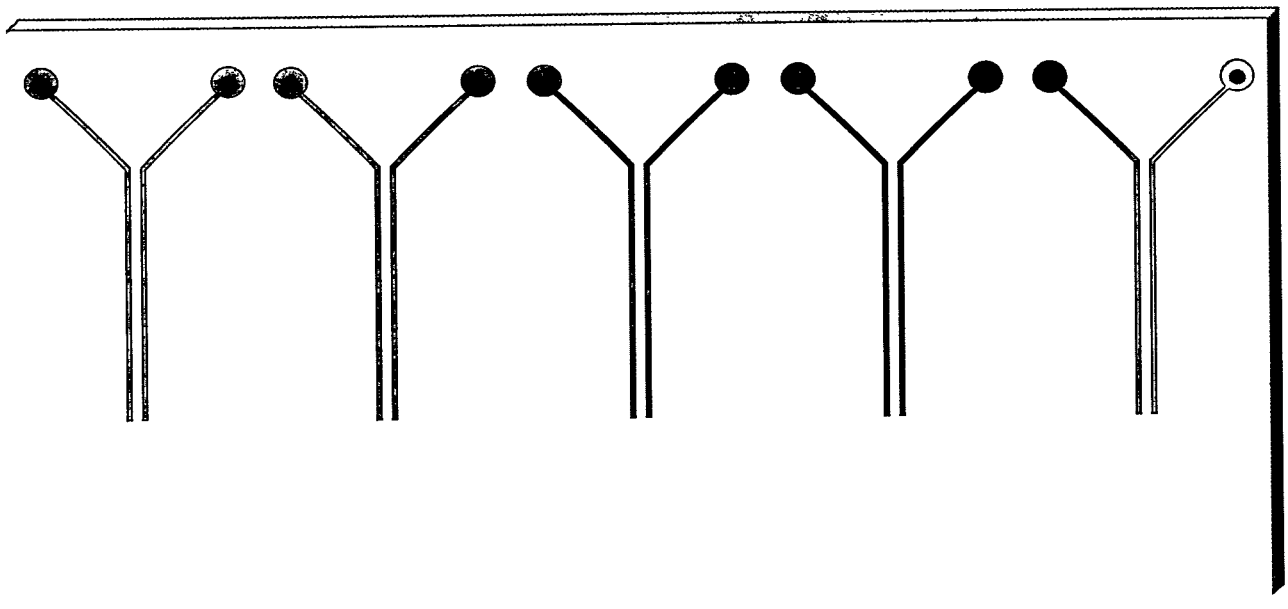

Figure 6.1 An Unprocessed MIL-I-46058C Panel with Five Y-Coupons

Soldering Process Prior to Conformal Coating	Processing Site	Process: Wave Solder	Process: Paste & Reflow	Process: Hand Solder
Low Residue Flux	TI	2	2	2
	Hughes	2	2	0
	Alliant	2	2	2
	AS	2	2	2
Low Residue Flux (Cleaned)	TI	2	2	2
	Hughes	2	2	0
	Alliant	2	2	2
	AS	2	2	2
RMA (Cleaned)	AS	2	2	2
	Totals:	18	18	14

Figure 6.2 Panels Processed for Peel-by-Tape Coating Adhesion Tests and Mealing Inspections

6.3 Moisture Resistance / Accelerated Aging

The test protocol utilized the first six steps of the temperature cycle described in MIL-STD-202, Method 106 (without electrical biasing and vibration). All test panels were initially conditioned in a dry oven for 24 hours at 55°C with the relative humidity uncontrolled. The temperature was lowered to 25°C for 2.5 hours prior to the start of temperature cycling. The relative humidity was between 90% and 100% during a 2.5-hour ramp up from 25°C and 65° C. Temperature was maintained at 65°C for 3 hours, with relative humidity between 90% and 100%. During the 2.5- hour ramp down, the relative humidity was between 80% and 100%. One complete cycle lasted eight hours. Figure 6.3 shows the temperature cycling profile for two cycles. The panels were subjected to 10 cycles of temperature and humidity conditioning.

6.4 Peel-by-Tape Test

In peel-by-tape tests, pressure-sensitive tape is applied over a lattice pattern that is cut into the conformal coating with a hand-held eight-bladed knife. This tape is rapidly peeled and the adhesion of the conformal coating is subjectively quantified by assigning an integer rating from 0 to 5 based on the following scale:

Rating	Interpretation
5	No noticeable removal of the coating
4	Less than 5% of the coating is removed
3	5%-15% of the coating is removed
2	15%-35% of the coating is removed
1	35%-65% of the coating is removed
0	More than 65% of the coating is removed

A lattice pattern was cut on the laminate portion of the panel beneath the rightmost Y-pattern, as shown in Figure 6.4, before ESS and a second pattern was cut beneath the leftmost Y-pattern after ESS. These patterns produced 100 ratings (25 site-processing combinations × 2 panels per combination × 2 tests per panel) for coating adhesion on the laminate. A rating of 5 was recorded for all 100 tests.

Lattice patterns were also cut across the base of the two rightmost Y-patterns before ESS (see Figure 6.4). One set of 100 (25X2X2) ratings was produced from these patterns before ESS. Two additional patterns were cut across the base of the two leftmost Y-patterns, as presented in Figure 6.4, following ESS, which produced

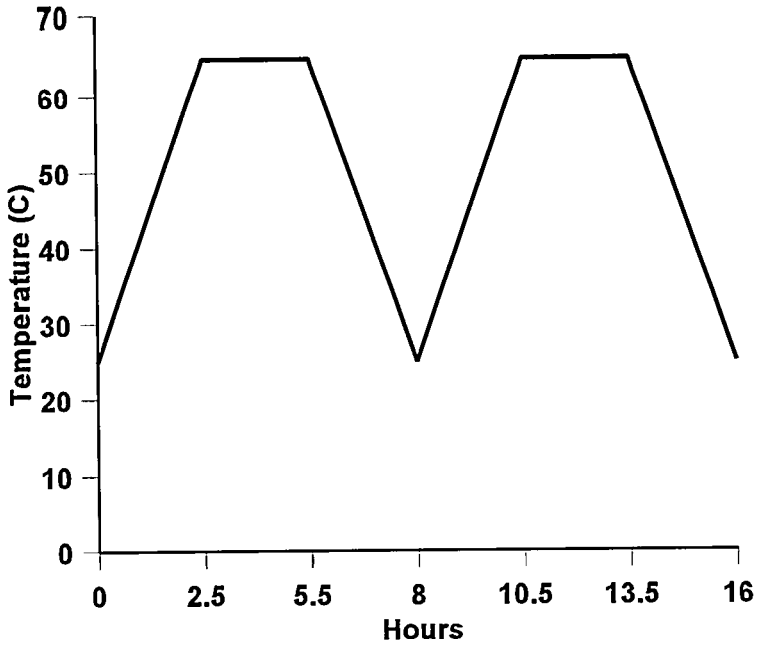

Figure 6.3 Temperature Cycle Profile for Environmental Conditioning

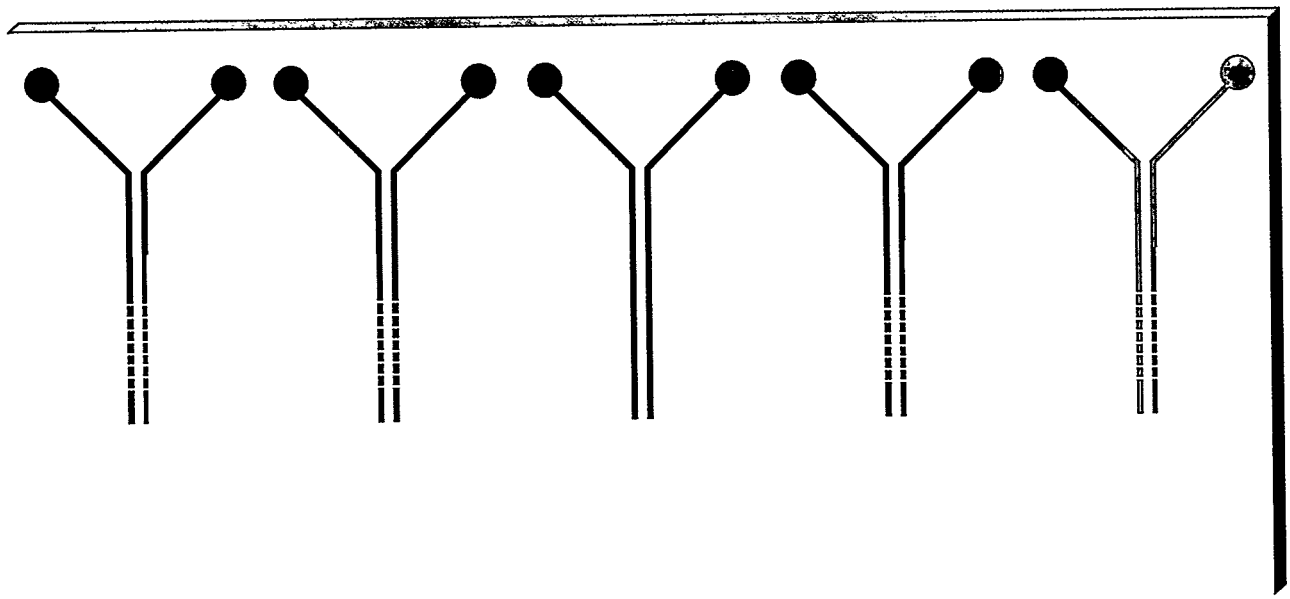

Figure 6.4 Lattice Patterns Cut on the Y-Coupons and Laminate of a MIL-I-46058C Panel

a second set of 100 ratings. Both sets of ratings are summarized in Figure 6.5, which shows a rating of 5 recorded for 143 of these 200 peel-by-tape tests (71.5%).

The Y-pattern in the middle of the panel was not used in the peel-by-tapes tests.

Site	Cleaned	Process	Ratings Before	Ratings After
Hughes Electronics	Yes	Reflow	5, 5, 5, 5	4, 5, 5, 5
		Wave	5, 5, 5, 5	5, 5, 5, 5
		Hand	*	*
	No	Reflow	2, 4, 2, 3	5, 4, 4, 3
		Wave	5, 5, 5, 5	5, 5, 5, 5
		Hand	*	*
Texas Instruments	Yes	Reflow	3, 3, 2, 3	2, 3, 2, 2
		Wave	5, 5, 5, 5	5, 5, 5, 5
		Hand	4, 5, 5, 5	5, 5, 5, 5
	No	Reflow	3, 3, 3, 3	2, 3, 2, 2
		Wave	4, 4, 4, 5	5, 5, 5, 5
		Hand	4, 5, 5, 5	5, 5, 5, 5
Alliant Techsystems	Yes	Reflow	5, 5, 5, 5	5, 5, 5, 5
		Wave	5, 5, 5, 5	5, 5, 5, 5
		Hand	5, 5, 5, 5	5, 5, 5, 5
	No	Reflow	3, 3, 3, 3	3, 3, 3, 3
		Wave	5, 5, 5, 5	5, 5, 5, 5
		Hand	4, 4, 5, 5	5, 4, 5, 4
AlliedSignal	Yes	Reflow	3, 4, 5, 5	4, 4, 5, 5
		Wave	5, 5, 4, 5	5, 5, 5, 5
		Hand	5, 5, 5, 5	5, 5, 5, 5
	No	Reflow	5, 4, 4, 4	5, 5, 5, 5
		Wave	5, 5, 5, 5	4, 5, 5, 5
		Hand	3, 4, 5, 5	5, 4, 4, 5
AlliedSignal	RMA	Reflow	5, 5, 5, 5	5, 5, 5, 5
		Wave	5, 5, 4, 4	5, 5, 5, 5
		Hand	5, 5, 5, 5	5, 5, 5, 5

Figure 6.5 Ratings from the Peel-by-Tape Test Before and After Environmental Conditioning

6.5 Statistical Modeling Results for the Peel-by-Tape Test

A GLM was used to determine the influence of site, process, and cleaning on the ratings in Figure 6.5. The base case model represents RMA processing. The model (R^2 = 73.9%, s = .44) for the "before" ratings is:

$$\begin{aligned} Y_{before} = {} & 4.86 - 1.94\ \text{Reflow*Not Cleaned} \\ & - 2.11\ \text{Reflow*TI*Cleaned} \\ & + 1.33\ \text{Reflow*AS*Not Cleaned} \\ & - 0.61\ \text{Reflow*AS*Cleaned} \\ & - 0.61\ \text{Wave*TI*Not Cleaned} \end{aligned} \quad (6.1)$$

The first term (constant) in this model, 4.86, represents the predicted "before" rating for all RMA processes and all but seven of 22 low-residue processes. That is, the RMA processes (reflow, wave, and hand) did not differ significantly from one another. In addition, 15 of the 22 low-residue cases did not differ significantly from RMA. The coefficients of the remaining terms in the model quantify the impact of site, process, and cleaning parameters for those seven low-residue processes that the model identifies as significantly different from RMA. The use of these coefficients to make adjustments to the RMA base case is now discussed.

The second term in the model is *-1.94 Reflow*Not Cleaned.* Since the coefficient is negative, the ratings for all low-residue reflow processes without cleaning (four cases) are reduced by 1.94. However, the fourth term in the model shows that the ratings for the low-residue reflow process without cleaning at AlliedSignal are also increased by 1.33, for a net reduction of -1.94 + 1.33 = 0.61 at AlliedSignal. The third term in the model shows that ratings for the low-residue reflow process with cleaning at Texas Instruments (one case) are also reduced by 2.11. The TI reflow process is responsible for the decrease in their ratings and not their low-residue process, since cleaning did not improve their ratings (in fact, cleaning slightly lowered their ratings). Ratings for the low-residue wave process without cleaning at TI (one case) decreased by 0.61. The ratings for the low-residue reflow process with cleaning at Alliant Techsystems (one case) also decreased by 0.61. The coefficients in Equation 6.1 are summarized in Figure 6.6 for ease of reference.

The "after" ratings model (R^2 = 87.1%, s = .32) is:

$$\begin{aligned} Y_{after} = {} & 4.96 - 2.71\ \text{Reflow*TI} \\ & - 1.96\ \text{Reflow*AT*Not Cleaned} \\ & - 0.96\ \text{Reflow*Hu*Not Cleaned} \\ & - 0.46\ \text{Reflow*AS*Cleaned} \\ & - 0.21\ \text{AS*Not Cleaned} \end{aligned} \quad (6.2)$$

The first term (constant) in this model is 4.96 (nearly 5.00). This term represents the predicted "after" rating for all RMA processes and all but eight of the low-residue processes. The eight low-residue cases that differ from RMA are now discussed.

The second term in the model shows that the ratings for the low-residue reflow process (with and without cleaning) at TI (two cases) are reduced by 2.71. As with the "before" ratings, the low-residue reflow process at TI received lower ratings. Ratings for low-residue processes without cleaning at AlliedSignal (three cases) are decreased by only 0.21 and ratings for their reflow process with cleaning (one case) are reduced by 0.46. Ratings for the low-residue reflow processes without cleaning at Alliant Techsystems (one case) and at Hughes (one case) are decreased by 1.96 and 0.96, respectively. The coefficients in Equation 6.2 are summarized in Figure 6.6 for ease of reference.

Means for the four observations in each cell in Figure 6.5 are given in Figure 6.7 and displayed in a series of graphs in Figure 6.8. These graphs aid understanding of the results of the general linear models in Equations 6.1 and 6.2 and show the following:

- 16 of the 22 low-residue cases with cleaning had ratings greater than or equal to RMA
- 8 of the 22 low-residue cases without cleaning had ratings greater than or equal to RMA
- Hughes lowest rating was associated with reflow without cleaning; however, this reading improved after environmental conditioning
- TI's reflow ratings were lower than the reflow ratings for the other sites for both cleaned and not cleaned
- AS reflow ratings were approximately the same for cleaned and not cleaned
- Cleaning improved the ratings for Hughes and AT reflow processes
- AT ratings for all processes with cleaning were greater than or equal to RMA
- All low-residue wave processes with cleaning had higher ratings than RMA before environmental conditioning and the same as RMA after environmental conditioning
- All low-residue wave processes (cleaned and not cleaned) had ratings greater than or equal to RMA, except two cases that were slightly lower

		Before Ratings (Constant = 4.86)		After Ratings (Constant = 4.96)		Mean Difference (Constant = 0)	
Site	Process	Cleaned	Not Cleaned	Cleaned	Not Cleaned	Cleaned	Not Cleaned
Hughes Electronics	Reflow		-1.94		-0.96		+1.25
	Wave						
	Hand						
Texas Instruments	Reflow	-2.11	-1.94	-2.71	-2.71	-0.63	-0.63
	Wave		-0.61				+0.75
	Hand						
Alliant Techsystems	Reflow		-1.94		-1.96		
	Wave						
	Hand						
AlliedSignal	Reflow	-0.61	-0.61	-0.46	-0.21		+0.75
	Wave				-0.21		
	Hand				-0.21		
AlliedSignal (RMA)	Reflow						
	Wave						
	Hand						

Figure 6.6 Changes in Ratings from the Base Case in the General Linear Model by Site and Process for the Peel-by-Tape Test

- All low-residue processes for hand soldering were equivalent to RMA before and after environmental conditioning except TI before, which was slightly lower
- All ratings for wave and hand were greater than 4, with many equal to or close to 5

The differences in the means in Figure 6.7 ("after" minus "before") are also shown in that figure. A general linear model was developed for these mean differences to determine how site, process, and cleaning parameters influence the mean change in ratings. The intercept (constant term) in the fitted GLM did not differ significantly from zero, so the GLM was refit with the constant term set equal to zero. The coefficients in the subsequent model show the change from zero for a given set of conditions.

The model is:

$$Y_{\text{mean difference}} = 1.25\ \text{Reflow*Hu*Not Cleaned} - 0.63\ \text{Reflow*TI} + 0.75\ \text{Reflow*AS*Not Cleaned} + 0.75\ \text{Wave*TI*Not Cleaned} \quad (6.3)$$

This model shows that the mean "after" ratings increase by 1.25 and 0.75 for the low-residue reflow processes without cleaning at Hughes and AlliedSignal, respectively. The mean "after" ratings also increase by 0.75 for the low-residue wave process without cleaning at Texas Instruments. On the other hand, the mean "after" ratings decrease by 0.63 for the low-residue reflow process (with and without cleaning) at Texas Instruments. The coefficients in Equation 6.3 are also summarized in Figure 6.6.

		Mean Before Ratings		Mean After Ratings		Mean Difference (After - Before)	
Site	Process	Cleaned	Not Cleaned	Cleaned	Not Cleaned	Cleaned	Not Cleaned
Hughes Electronics	Reflow	5.00	2.75	4.75	4.00	-0.25	1.25
	Wave	5.00	5.00	5.00	5.00	0	0
	Hand	*	*	*	*		
Texas Instruments	Reflow	2.75	3.00	2.25	2.25	-0.50	-0.75
	Wave	5.00	4.25	5.00	5.00	0	0.75
	Hand	4.75	4.75	5.00	5.00	0.25	0.25
Alliant Techsystems	Reflow	5.00	3.00	5.00	3.00	0	0
	Wave	5.00	5.00	5.00	5.00	0	0
	Hand	5.00	4.50	5.00	4.50	0	0
AlliedSignal	Reflow	4.25	4.25	4.50	5.00	0.25	0.75
	Wave	4.75	5.00	5.00	4.75	0.25	-0.25
	Hand	5.00	4.25	5.00	4.50	0	0.25
AlliedSignal (RMA)	Reflow	5.00		5.00		0	
	Wave	4.50		5.00		0.50	
	Hand	5.00		5.00		0	

Figure 6.7 Means from the Cells in Figure 6.5 and their Corresponding Differences

6.6 The Mealing Test

The conformal coating on each coupon was inspected for mealing before and after environmental conditioning. Inspection was visual and nondestructive. Panels were examined for mealing when they were received from the sites and again after at least eight hours of completion of the temperature cycles as shown in Figure 6.3. Visual inspection (10X magnification) checked for the presence of blisters, delaminations, peeling, discoloration, and tackiness.

Visual inspection conducted before temperature cycling showed no obvious defects. An "orange-peel" surface texture was observed on the low-residue wave and hand soldered Y-coupons manufactured by AlliedSignal. No mealing, discoloration, chalking, cracking, or tackiness was noted following the completion of the temperature/humidity test. A wrinkled undercoating was observed on the low-residue reflow Y-coupons produced by AlliedSignal and Texas Instruments (over the metallization).

6.7 Lessons Learned and Conclusions

Though subjective, peel-by-tape and mealing inspections do provide quick and inexpensive evaluations of coating adhesion. Sharp blades must be used to cut the lattice grid for the peel-by-tape test. Solder and conformal coating mounds can affect the cutting action and care needs to be taken when cutting the lattice pattern.

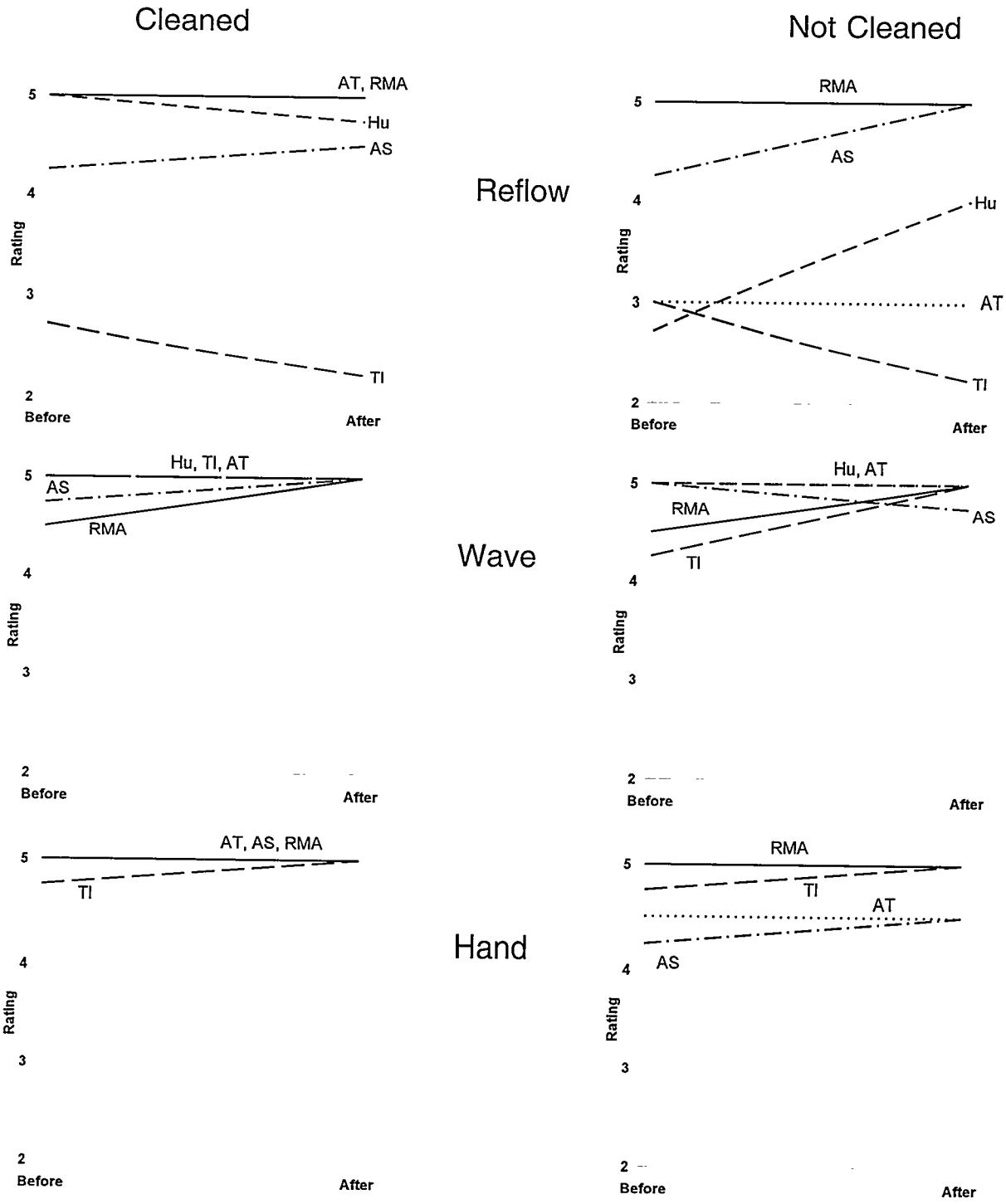

Figure 6.8 Graphs of Before and After Means in Figure 6.7 by Site and Process

Ratings for low-residue wave and hand soldering processes were essentially the same as RMA processes. More than half the low-residue cases (both cleaned and not cleaned) had average ratings greater than or equal to the corresponding RMA processes. The lowest ratings for the peel-by-tape adhesion test were for low-residue reflow processes, although some were equivalent to RMA.

Cleaning improved the ratings for some low-residue reflow processes; however, the ratings for AlliedSignal's reflow process without cleaning were close to those for RMA. Reflow process development should resolve this issue, since the sites had limited experience with low-residue reflow processes.

Distribution List

Lt. Col. David Abati - USAF ASC/VXC
Ahmad Abnoosi - SAN-O Industrial Corp.
J. W. Abouchar - Unit Design
Mike Abowd - Packard Electric Div., GM
Robert D. Acosta - Industrial Electronic Engr. Inc.
Craig Adams - USAF ASC/VLLX
David Adams - Harris Corporation
David C. Adams - ITT Aerospace
E. Kay Adams - UnIPEG
Jack Adams - Concurrent Technologies Corp.
Lt. Col. Paul Adams - USAF MSG/SMR
Sean M. Adams - Airco Gases
Carol Adkins - Sandia National Laboratories
Paul Adler - Metcal
John W. Agopovich - Draper Lab
David R. Ahlberg - Seika Corp.
Lt. Michael L. Ahmann - USAF ESC/SRG
Kola Akinade - UDS-Motorola
Capt. Ernest Albritton - USAF ESC/JS-2JD
Michael Alderete - Loral
Benjamin D. Alexander - DCMD
Robert L. Alexander - United Technologies
Richard Aliviado - Sonatech, Inc.
Yater Allen - USAF M-ALC/LHH
Chris Alter - Honeywell, Inc.
John Althouse - Fairchild Space and Def. Corp.
Stuart Altman - US Department of Energy
James Altpeter - Ford Motor Co.
W. E. Alzheimer - Sandia National Laboratories
Ken-ichi Amano - Tenkoh-doh Intl.
Lawrence L. Ambs - Univerity of Massachusetts
Stephen O. Andersen - US/EPA
Dennis Anderson - Sandia National Laboratories
Edward A. Anderson - Hughes Aircraft Co.
Gene Anderson - USAF ESC/AVJ
Gerry Anderson - USAF AGMC/MAE
James R. Anderson - US Department of Energy
Kari Anderson - Naval Air Warfare Center
Ralph Anderson - General Technology
Ron Andreas - Sandia National Laboratories
Raqib Anwar - Sorensen
Gad Arbel - IAI
Dorothy Arbiter - USAF HSC/YAQ
Harry Armen - Grumman Corp.
Maria E. Armendariz - Sandia National Laboratories
Sam Armstrong - Alpha Metals, Inc.
Wayne Armstrong - Loral Control Systems
Bernard Aronson - Electronic Industries Assoc.
David Artus - BF Goodrich Aerospace
S. Arun - Sargam Metals Private Ltd.
Dan Arvizu - Sandia National Laboratories
Kelly Asada - Hughes Aircraft Co.
Bob Asanuma - Hewlett Packard
Lt. Col. B. Ashcraft - USAF ESC/AVB
David Asher - Vanguard Electronics Co.
Eileen Ashmore - Argo Systems
David Asiello - Office of the Chief of Naval Oper.
Daniel F. Askey - Capco, Inc.
Arvind Atreya - University of Michigan
Bob Atwood - Viatrain
Jim Aubert - Sandia National Laboratories
Craig R. Auletti - Litton/Amecom
Bob M. Axline - Sandia National Laboratories
Milt Axton - Motorola Corp.
Jim Ayers - Ingersoll Engineers
Niles Baba - Hughes Aircraft Co.
Adra Baca - Sandia National Laboratories
Louis Baca - ARCRD-E
Jeff Baechler - DMG
Anne Baic - AlliedSignal Aerospace Co.
Roger Bail - Calculex, Inc.
Ken Bair - USAF ESC/AV
Craig Baker - ST. Microwave Corp.
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Col. Terry R. Talbot - USAF/Pentagon
Amori Tanganadhan - Developed Technology Resource
Steve Tavan - Mitre
Carl J. Tauscher
Jerry Tavores - Unicor Federal Industries
Col. Edward Taylor - USAF ESC/AW
June Taylor - USAF ESC/SR(SSG/LSC) (CMC)
John E. Taylor - Delphax Systems
Kathleen C. Taylor - General Motors Corporation
Phil Taylor - DuPont Electronics
Mo Tazi - Chemtronics, Inc.
Mark Tebbano
Les Teel - Aerojet
Karen Tellefsen - Alpha Metals
Dick Tello - The MITRE Corporation
Paul Templin - BEI-Systron Donner
D. Morgan Tench - Rockwell International Science Center
George Terrell - USAF AMCRD-E
Ray Terry - NAVAIRWARCENWPNDIV
Saujanya Thakker - The Morey Corporation
Warren Thausand
S. R. Thery - FMC Corp.
Duane Thexton - Northop Corp.
Jim Thiry - Cincinnati Electronics
Christopher Thoben - Systron Donner
Paul Thomas - Naval Undersea Warfare Center
Sean Thomas - OTA/EOEA
David Thomas-Greaves - GLMTC Manufacturing Outreach Program
Larry H. Thompson - St. Microwave Corp.
Norm Thompson - NWS
Richard T. Thompson - Loctite Corporation
Robert A. Thompson - NUWC - Division Newport
Sheila Thompson - BEI-Systron Donner
Capt. Bob Thomson - USAF AFMC/DRMP
Jeff Thurston - USAF ESC/IS
Glenn Tibbett - Marine Corps Logistics
Charles Edwin Tibble - AlliedSignal Aerospace Company
Jim Tira - AlliedSignal Aerospace Company
Leo Tober, Jr. - ITT
Audie R. Todd - USAF OL-AA PL/SE
Tom Todd - ToddCo General, Inc.
Joseph S. Tomaszek - GEC Marconi
John V. Tomczak - Hi-Grade Alloy Corp.
John H. Topalian - GenCorp Aerojet
David Torp - Rockwell International
Jerry Tovares - Union Federal Industries
Kevin Townsend - Christopher Associates
Dzoan Q. Tran - Hughes Aircraft Co.
Chuck Treadway - Square O Co.
Richard Tremblay - USAF ESC/AVD
Anita Trenholm - Naval Air Warfare Center
Stuart G. Tribble - Boeing
John Tribou - US Department of Energy
Hem Tripathi - Defense General Supply Center

Roger Trovato - Dover Seltec
Shirnell Troxtell - Texas Instruments
George Trujillo - Hughes Aircraft Co.
Thang D. Truong - AT&T MicroElectronics
Laura J. Turbini - Georgia Institute of Technology
Wayne Turnacliff - Ball Aerospace & Communcations Group
Robert Turner - University of Nevada-Reno
Tom Turner - Trace Laboratories
Wayne C. Turner - Oklahoma State University
Victor A. Twadell - Lockheed Sanders, Inc.
Rodney R. Tyler - NUWC
Trent Uehling - Motorola, GEG
Keith Valecko - Powcon, Inc.
Phil VanBuren - Sandia National Laboratories
Bob Van Hoomissen - Boeing Defense & Space Group
Hubert Vander Plas - Hewlett-Packard
Ralph Vaughan - Rockwell International
Robert Vaughn - R. L. Vaughn & Assoc.
Laura Vedra - General Inst. Videocipher Div.
Angel Venegas - AIL Systems, Inc.
Sharon T. Ventress - USA MICOM
Gary Vest - Pollution Prevention
Lawrence G. Vettraino - USAF SM-ALC/TIELC
Steve Vincent - Ohmtek, Inc.
Wayne Vine - Sandia National Laboratories
Mark Vininski - Intel Corp.
Clare Vinton - NCMS
John Vinyard - Bekaert Assoc., Inc.
Rus Voigt - Aeorjet Ordance
Sandy Voigt - Minnesota Technology Inc.
Paul Vu - Qualcomm, Inc.
Joe Wade - INTERMRC
Howard W. Wagenblast - Metalworking Technology, Inc.
Dilip Waghray - Northern Telecom
Charles E. Wagner - Wright Laboratoriesoratory
James Wagner - Northern Telecom
Krishan Wahi - GRAM, Inc.
Fred Wahl - E-Systems, Inc.
Ralph Walker - Draper Laboratories
S. Walker - Smith Industries
James Wall - Litton Industries
Barbara Waller - Texas Instruments
Micheal D. Walley - Hughes Aircraft Co.
Col. Peter Walsh, AF/CEV - The Pentagon
Don K. Walter - US Department of Energy
James C. Walters - University of Louisville
D. J. Walukas - Concurrent Technology Corp.
Bill Wangard - WMAC
Cory D. Ward - NAVCOM Defense
Paula Warnock - Rockwell International
John L. Warren - Research Triangle Institute
Robert F. Warren - Teledyne Systems Co.
James Washington - Hughes Aircraft Co.
Sig Wathne - Sikama International, Inc.
Danny Watson - General Dynamics
Katherine Webb - Praxair, Inc.
Gary L. Weed - Teledyne Systems Company
Ed Weinbrecht - Sandia National Laboratories
Ronald J. Weis - Naval Air Warfare Center
Courtney Weiss - Boeing Defense & Space
Joel Weldon - IBM-Canada, Ltd.
Dick Wells - Interfux, USA
Duwayne Wells - TRW
Steven Welsh - Hughes Missile Systems Co.
Lt. Col. Gil Wendt - USAF AFMC/ENSE
Dale Werner - EG&G Power Systems
Betty West - USAF HSC/EMP
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Sandra Wheeler - GDE Systems, Inc.
R. M. Whitcomb - Raytheon Co.
Eddie White - USAF WL/MLSA
George D. White - Harris Corp.
Col. Charles Whited - USAF SMC/EN
Cliff Whited - Loral Defense Systems
Lt. Col. Thomas Whittemore - USAF ASC/VXG
Col. Robert Wickert - USAF ASC/EF
Capt. Andrew Widger - USAF ESC/SES
John Wilder - USAF ESC/PKC
Keith Wilkes - Department of the Navy
Brad Williams - Harris Corporation
J. D. (Jim) Williams - Praxair, Inc.
John Williams - Draper Laboratories
Kim Williams - Space Systems Loral
George Williamson - Sandia National Laboratories
Perry Wilson - Ludlum Measurements, Inc.
Richard Wilson - Smiths Industries
C. Byron Winn - Colorado State University
Julie Winter - Heath Electronics Mfg. Corp.
Don Wippel - Metro
Ben Wiseman - General Dynamics
Katy Wolf - Inst. for Res. & Tech. Asst.
Norm Wolstein - Teledyne Systems Co.
Mike Wolverton - Texas Instruments, Inc.
Byard D. Wood - Arizona State University
Periann Wood - US Environmental Protection Agency
J. B. Woodard -Sandia National Laboratories
Jim Woodford - Secretary of Defense OASD
Phillip Woodring - USAF SM-ALC/LHV
Ted Woods - Motorola, Inc.
Adrian Woodward - Meaurement Technology Limited
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Thomas Workman - Pentex Engerprises, Inc.
John Wos - Loral Aerospace
Michael J. Wozny - NIST
James A. Wrezel - Motorola, Inc.
Conrad Wright - Hewlett Packard
Mark E. Wright - Asheville-Buncombe Technical Community
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Jimmy H. Yarbrough - Tracor Aerospace
Col. C. Kevin Yard - USAF SA-ALC/LDI
Shelgon Yee - Solectron
Graham Yelton - Sandia National Laboratories
John Ykema - SPD Technologies
Fred Yost - Sandia National Laboratories
Peter You - Solectron
Dean E. Young - Production Engineering
John Young - Pacific Environmental Consultants, Inc.
Don Youngblood - Honeywell
Andy Yuen - Alpha Metals, Ltd.
Peter K. Yuen - Titan Electronics
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Zun Zhu - Delco Electronics
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