Marine High Voltage Power Conditioning and Transmission System with Integrated Storage DE-EE0003640

Final Report

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Glossary

AC	*Alternating Current*
ANSI	*American National Standards Association*
BOM	*Bill of Materials*
BOS	*Balance Of System*
CEC	*California Energy Commission*
COGS	*Cost of Goods Sold*
COTS	*Commercial off the Shelf*
CRL	*Central Resonant Link*
DC	*Direct Current*
DNP	*Distributed Network Protocol*
DR	*Distributed Resources*
FDR	*Final Design Review*
GUI	*Graphical User Interface*
HF	*High Frequency*
HVDC	*High Voltage Direct Current*
HMI	*Human Machine Interface*
IEC	*International Electrotechnical Commission*
IEEE	*Institute for Electrical and Electronics Engineers*
IGBT	*Insulated Gate Bi-polar Transistor*
LVAC	*Low Voltage Alternating Current*
MTBF	*Mean Time Between Failures*
NEMA	*National Electronics Manufacturers Association*
NESC	*National Electric Safety Code*
PE	*Power Electronics*
PDR	*Preliminary Design Review*
PPS	*Princeton Power Systems*
PWM	*Pulse Width Modulation*
RLC	*Resistor Inductor Capacitor*
SWER	*Single Wire Earth Return*
THD	*Total Harmonic Distortion*
UART	*Universal Asynchronous Receiver/Transmitter*
UL	*Underwriters Laboratories*
VAC	*Volts Alternating Current*
VAR	*Reactive Volt Amperes*
VDC	*Volts Direct Current*

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Project Summary

Chapter 1: **Project Summary**

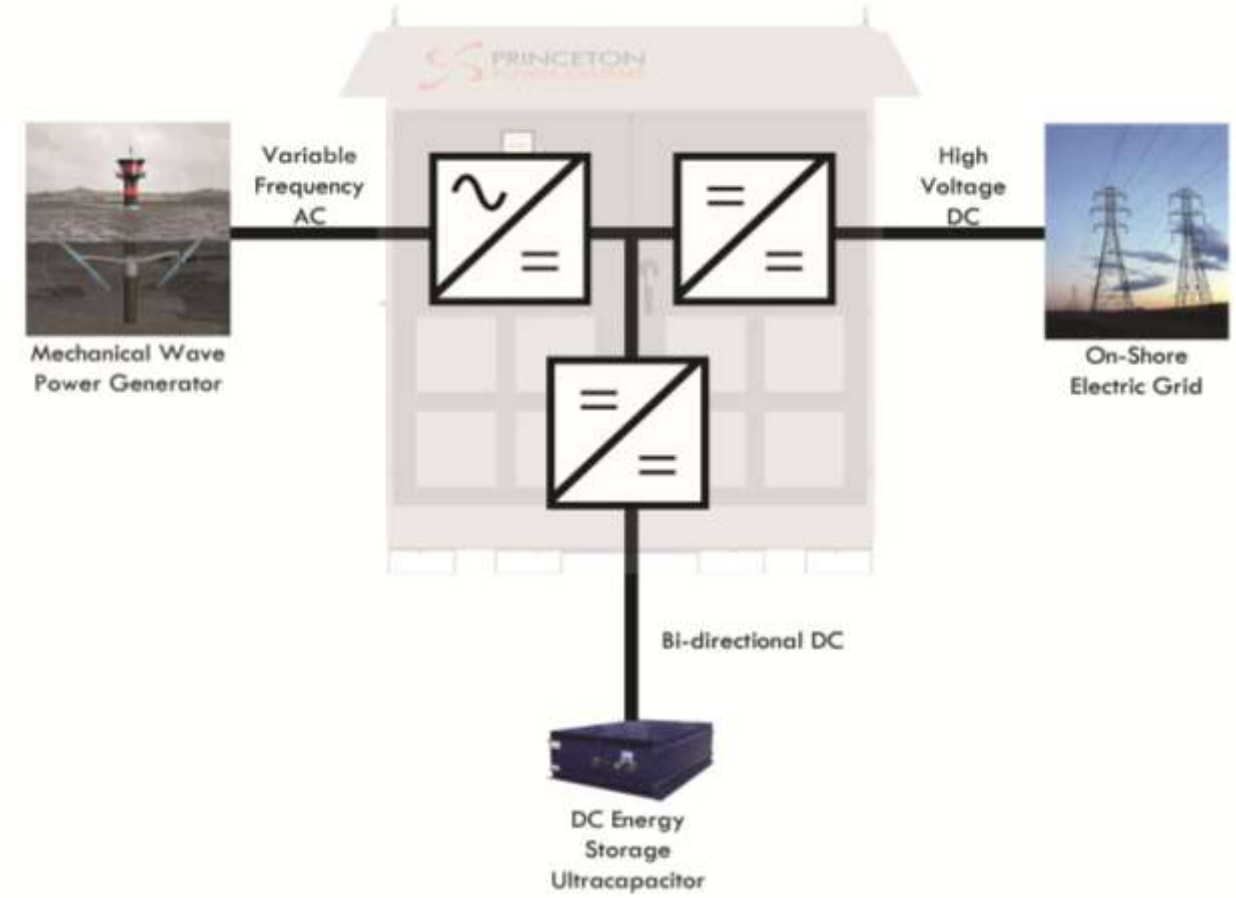

FIGURE 1: POWER CONVERTER CONCEPT.

PPS has designed, developed and tested a 3 port power converter system for Marine Hydro-Kinetic power transmission as part of the Department of Energy's (DoE's) Technological Readiness Level (TRL) Advancement Initiative.
Much progress has been made towards key project goals. A base cost of $0.32/Watt is well within the system cost of $0.50/Watt, even when $0.10/Watt is added in for advanced energy storage such as Lithium-Ion batteries. The converter has successfully generated up to 40.2kV DC which, using Princeton Power System's high voltage test load, provided 32kW of output power. The goal of 10 year design lifetime is also within reach, with the current projected MTBF of 5.34 years. This will be revised as the design is improved. The goal of 97% efficiency is also within reach, with 95.4% measured without significant investment into tuning system parameters to optimize this performance. HV ripple was measured as 1.3% maximum, far exceeding the specified goal of 2%. Output regulation under steady state conditions was 0.2% far exceeding the 5% baseline goal.

The converter, while capable of power generation, was also intended to be bi-directional so that the power generation was able to be re-converted at the shore to usable system voltage. During testing it was realized that this was not going to be possible with the current IGBT component. The design for the high voltage IGBT switches was realized as being inadequate, and so focus was put instead on developing the system and delivering many of the key goals. For this reason, the third goal of field testing the unit has been put on hold as power receiving functionality is developed. PPS is confident that limited testing of this functionality will be successfully achieved within the next six months. The corrective action has been designed and procurement is underway. PPS then intends to develop this functionality to demonstrate a two port variant of the technology (without energy storage) in rural Alaska within a year. It is hoped that this will allow entry into further opportunities in Alaska, some of which may include the energy storage component.

Technical Progress

Chapter 2: **Task 1: Final Hardware Design of Prototype System**

2.1 Overview of Progress

The task to design the required hardware for the MHK prototype, namely the three port converter proposed was successfully completed by April 2012.

The design leverages work performed in conjunction with another product that PPS is developing, namely that of a 1MW system for HVDC transmission without energy storage, which is comprised of 2 parallel 500kW systems. One system was used for the MHK project. Each system is comprised of a high voltage oil tank that contains the transformer and high voltage switching stack, and a low voltage cabinet containing the low voltage switching stacks and balance of system.

For prototyping, the energy storage component was implemented using a separate product that PPS offers, namely its 100kW Grid-Tied Inverter (GTI) which interfaces DC energy storage such as batteries and ultra-capacitors to the electrical grid. The final product would therefore use the same hardware as the GTI, but at the 500kW power level. It would use the same power bridge as the AC side, except it would be configured for DC power by bussing the three individual phases together. The low voltage enclosure contains space for such a bridge to be installed, although it was not installed and instead the connection was made to the GTI product.

Figure 2 shows an overview of the final prototype system used for the majority of the tests. The GTI component providing the ports for energy storage (battery) and AC port for hydrokinetic power is visible on the top of the drawing. The bottom of the drawing shows the equipment providing the generation of high voltage DC from an internal low voltage bus voltage.

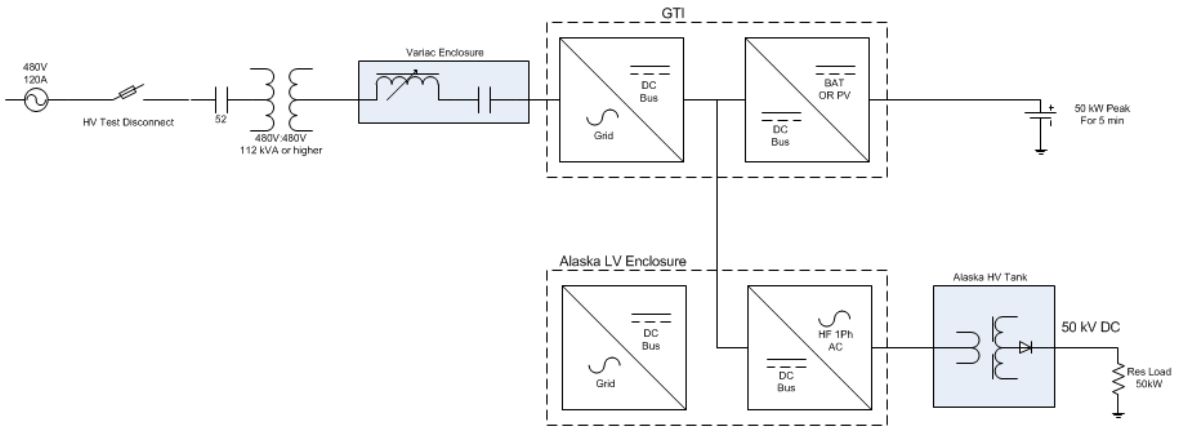

FIGURE 2: PROTOTYPE SYSTEM OVERVIEW

2.2 System Power & Control Architecture

The system is designed using two separate sections because of size, weight, maintenance and transport concerns.

The High Voltage Section consists of a step-up transformer with one low voltage primary and 16 high voltage secondary windings, as well as 16 "HV Stage Bridges". In order to meet voltage spacing requirements, as well as for cooling purposes, these components are placed entirely in an oil filled "HV Tank". A block diagram of this section is shown in Figure 3.

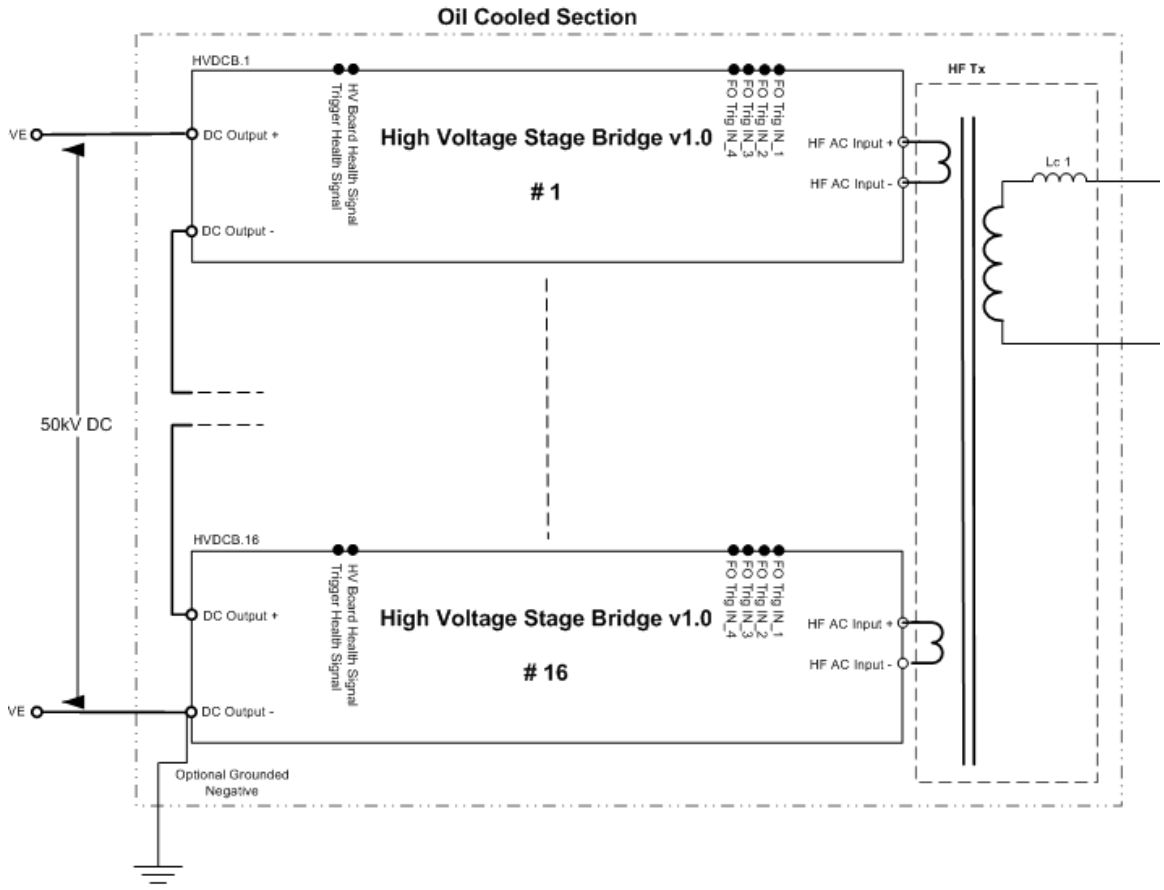

FIGURE 3: HVDC TRANSFORMER TANK: POWER BLOCK SCHEMATIC

Figure 4 shows the accompanying "Low Voltage Section", which is air-cooled and installed in a standard industrial enclosure that can be designed to meet any environmental specification. The low voltage section contains a bidirectional 3-phase AC-DC inverter, including the necessary filtering on the grid side, as well as an H-bridge to generate the low voltage HF input for the step-up transformer, forming a low voltage to high voltage DC-DC converter.

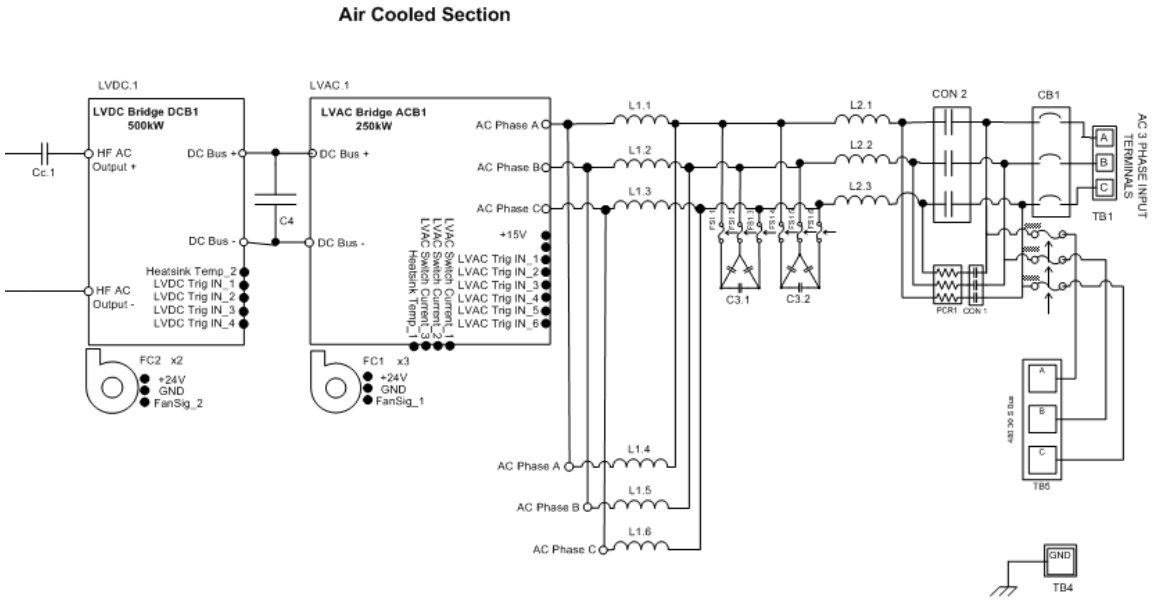

FIGURE 4: LVAC ENCLOSURE: POWER BLOCK SCHEMATIC

Figure 5 shows the overall control topology of the complete system, The diagram is simplified to illustrate the control signals that are sent to each bridge, and the voltage and current sensors which provide feedback information for closed loop control and fault detection.

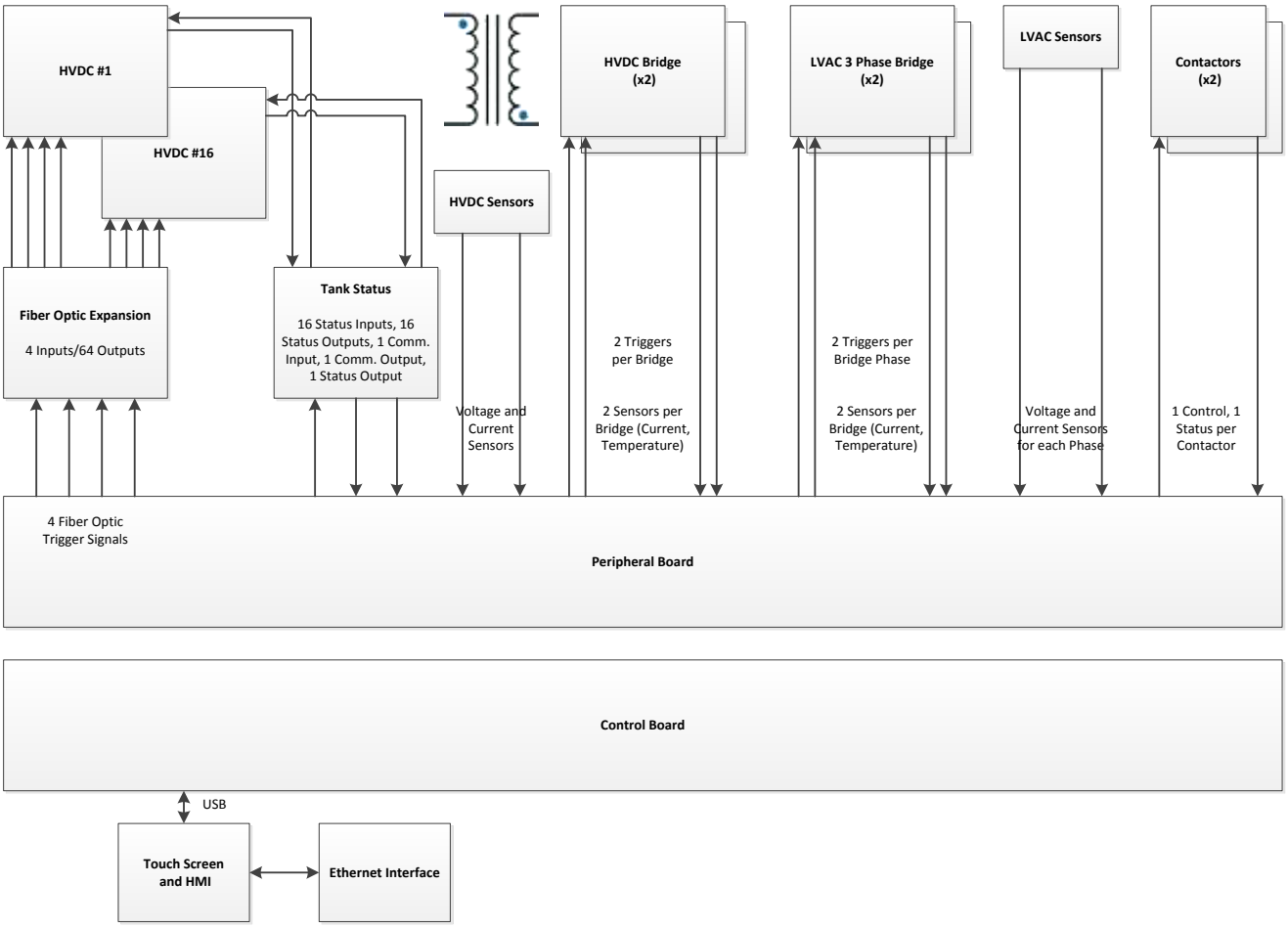

FIGURE 5: CONTROL SYSTEM: BLOCK SCHEMATIC (SIMPLIFIED)

2.3 Mechanical Design

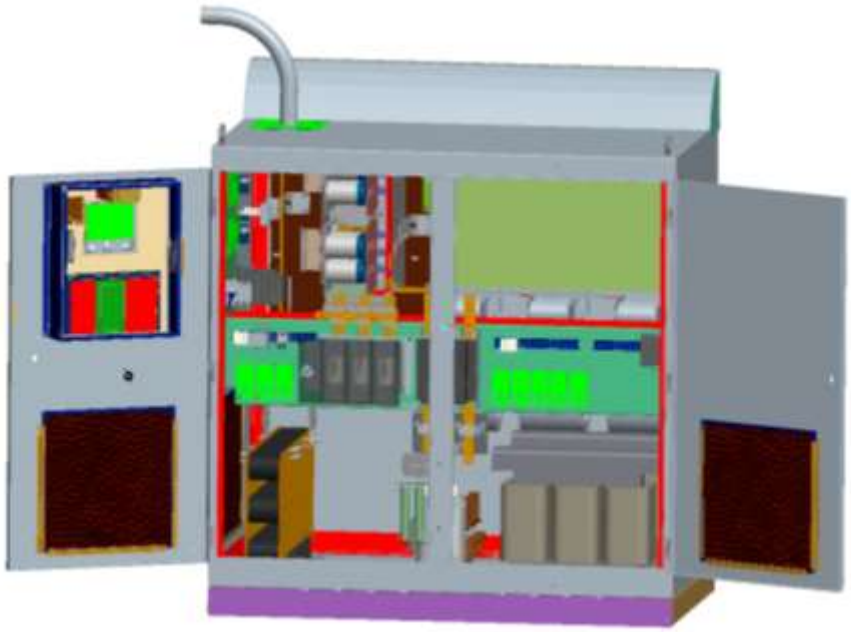

FIGURE 6: LVAC ENCLOSURE: MECHANICAL LAYOUT

Figure 6 shows the power converter's LVAC enclosure with its doors open and the control compartment cover removed. This enclosure is designed for outdoor installations using a NEMA 3R rated cabinet. It is anticipated that the unit will be installed inside a power plant or other enclosure with semi-controlled operating conditions. The LVAC enclosure is made from 14 gauge low carbon steel and painted ANSI 61 gray to withstand the weather for a service life of up to 50 years. The cabinet design includes a structural frame and back panel to support the weight of components and to handle any excessive stress encountered during shipping. The layout of the components inside is optimized for even weight distribution and for establishment of the lowest possible center of gravity. It was also optimized for even air flow through the cabinet to maintain thermal stability. The cabinet is provided with a reinforced steel base that has (12) mounting holes. There are also (4) lifting eyehooks at the top of the cabinet for loading & unloading during transportation. The lifting eyehooks are removable to reduce the overall height of the cabinet and clear doorways. The enclosure exhaust plenum and wiring conduit are also removed during transportation. There are (12) "bolt down" mounting holes in the base for the permanent installation of the enclosure onto a concrete foundation to meet requirements of seismic risk zone 4, as tested per ICC-ES-AC 156.

Cabinet size: 66"W x 42"D x 66"H;

Cabinet weight: Approximately 2200 lbs.

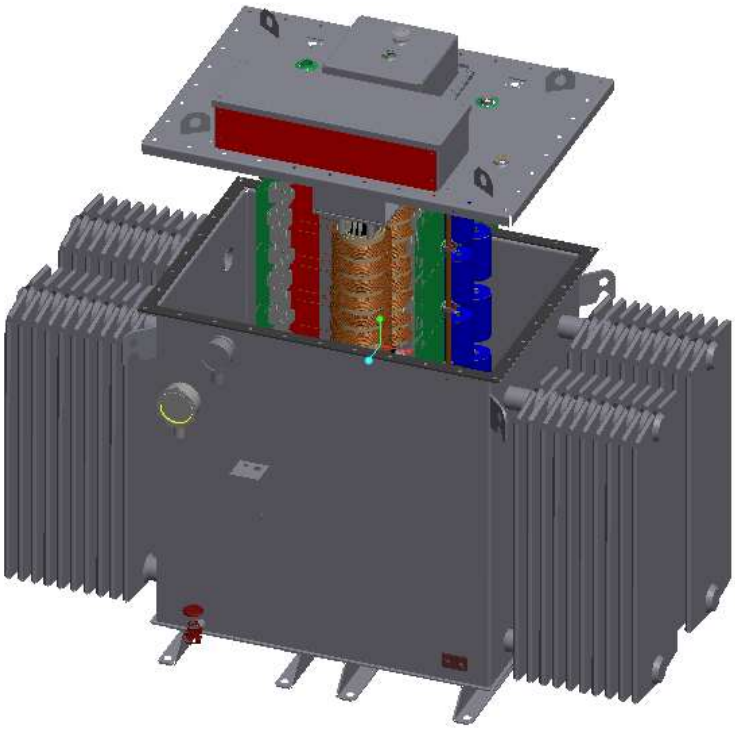

FIGURE 7: HVDC TRANSFORMER TANK: MECHANICAL LAYOUT

Figure 7 shows the HVDC Transformer tank assembly with the tank lid and attached transformer and power electronic components lifted for clear view. The tank assembly consists of High Voltage IGBT switching stacks combined with a power transformer in the same oil-filled tank. The Transformer tank is made of welded construction 12 gauge low carbon steel sheets and painted ANSI 61 gray. The tank lid has a supporting structure to mount power electronic components and the HVDC transformer onto it. The lid has hooks for lifting. The transformer tank has separate lifting hooks and (8) mounting holes in the base to meet the requirements of seismic risk zone 4.

Tank size: 88”W x 39”D x 59.25”H;

Tank weight with oil: 4200 lbs.

Transformer oil: Mineral Oil, Cross Trans 206.

Figure 8 and Figure 9 show mechanical drawings with dimensions of the LVAC enclosure and the HV tank.

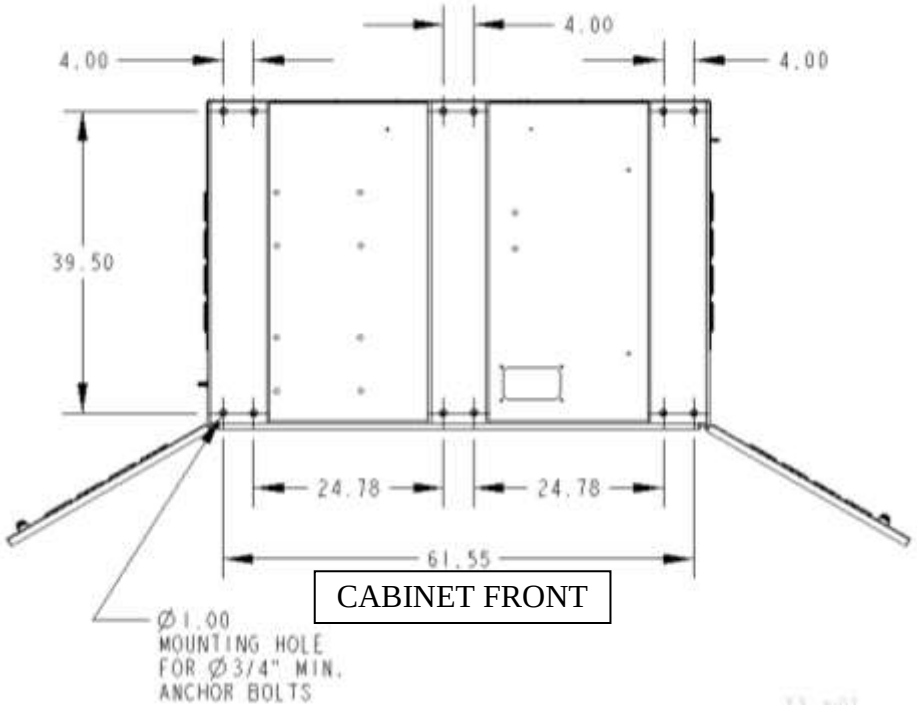

FIGURE 8: LVAC ENCLOSURE: INSTALLATION DRAWING (BOTTOM VIEW)

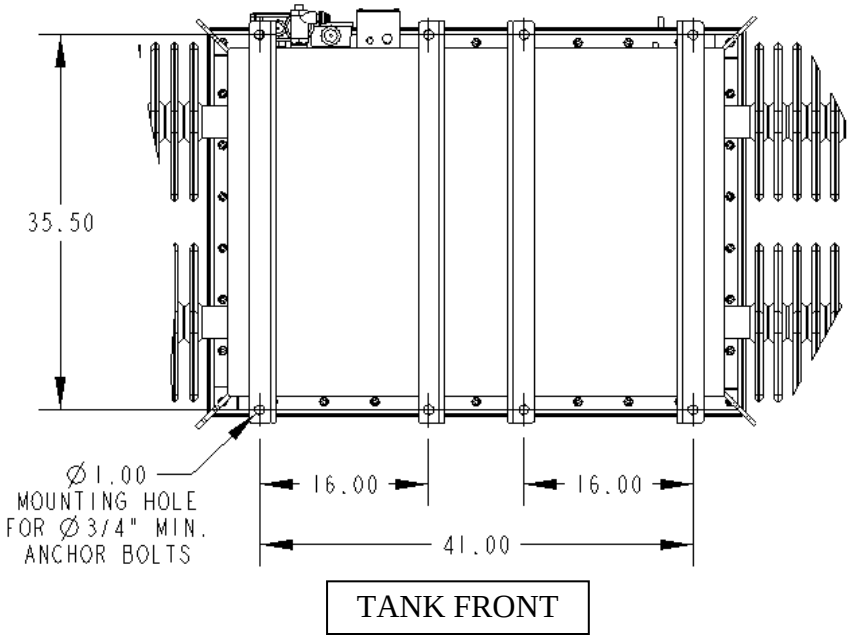

FIGURE 9: HVDC TRANSFORMER TANK: INSTALLATION DRAWING (BOTTOM VIEW)

2.4 Thermal Design

2.4.1 LVAC Enclosure

In the power converter's LVAC enclosure, forced air cooling by blowers that are part of the AC/DC bridge modules and air flow patterns (see Figure 10) were used to determine optimal placement of power electronic components. The number of fans/blowers was minimized, due to the concern that fans are typically the most unreliable components in the system because of their rotating parts. Since each bridge module with blower was installed high or midway on the back panel, ducting of the bridge modules is relatively short. Hot air is exhausted directly out of the cabinet at the top towards the rear and negative internal pressure is created, which in turn draws outside air through the front and side lower intake vents without use of additional intake fans.

It has been determined that (4) sets of intake louvers are needed for adequate air flow, (2) on the doors and (2) on side walls. (4) air filters are to be installed inside the cabinet, one at each louver set, to ensure intake air quality.

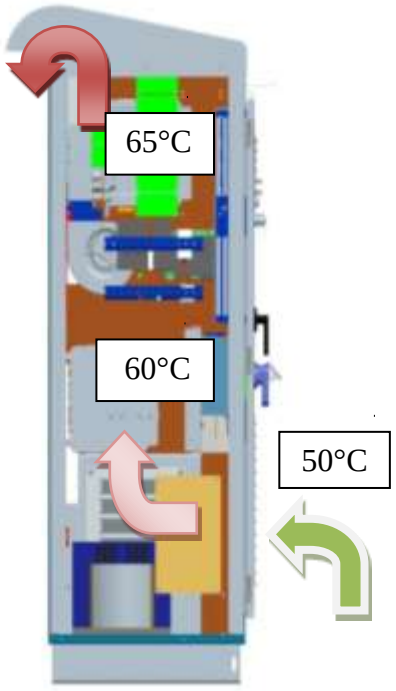

FIGURE 10: LVAC ENCLOSURE: AIRFLOW PATTERN

Over-temperature protection of the LVAC enclosure is provided by temperature sensors on critical components like the bridges and critical electronics. In the transformer tank temperature sensors are placed on each HV stack board and the transformer itself. The controls will have a threshold setting to send an over-temp warning and then, when a higher threshold is reached, send an over-temp trip.

2.4.2 HVDC Transformer Tank

Two studies were done for the HVDC transformer oil tank. The first using 12-plate radiators, the second comparing the 12-plate radiator design with an 8-plate radiator design. Based on the studies and consultation with NWL Inc., the transformer tank manufacturer, PPS has concluded

that a 10-plate radiator design will maintain the top oil temperature below 75°C.

Oil Temperature Goals:

1) Maximum oil temperature of the top oil in the tank:
    a. 72.6°C for 100% radiator efficiency,
    b. 73.7°C for 68% radiator efficiency.
2) Maximum oil temperature in the entire system will be near the transformer core material:
    a. 107.5°C for 100% radiator efficiency,
    b. 112.2°C for 68% radiator efficiency.

	Factor	Case	3a	3b	4a	4b
Model Inputs	Radiator Efficiency		100%	100%	68%	68%
	Number of Plates		12	8	12	8
	Model Heat Load	Watt	1411	1411	1411	1411
	Inlet Temperature	C	50	50	58	58
	Outlet Mass Flow	kg/sec	0.0	0.0	0.0	0.0
		lb/min	4.356	3.168	6.336	4.62
	Outlet Average Velocity	ft/min	1.3	1	1.9	1.4
	Radiator Design Loss @ 75 C	Watt	1820	1330	1820	1330
	Thermal Conductivity of Core	W/M-K	9	9	9	9
Calculated	Tank Converter Losses	Watt	120	156	137	166
	Net Radiator Heat Load	Watt	1291	1255	1274	1245
	Oil Temperature Rise	C	1770.0%	2260.0%	1200.0%	1570.0%
	Actual Radiator Loss	Watt	1288.56	1202.32	1284.71	1228.29
	Energy Balance Discrepancy		0.2%	3.7%	-0.8%	1.2%
	Outlet Oil Temperature	C	67.7	72.6	70	73.7
	Maximum Oil Temperature	C	103.6	108.5	103	106.8
	Maximum Solid Temperature	C	107.5	112.2	103.7	107.5
	Average Oil Temperature	C	66.3	71.5	68.7	72.5

Table 1: Thermal Study of 8-Plate vs 12-Plate Design.

The temperature simulation images shown in Figure 11 through Figure 15 assume 68% efficiency and K_{CORE} = 9 W/MK.

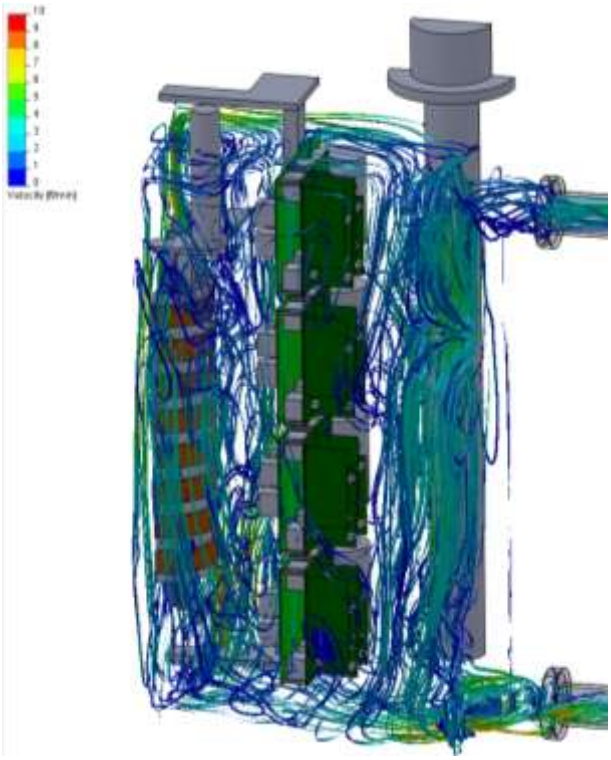

FIGURE 11: HVDC TRANSFORMER TANK: FLOW STREAMLINES

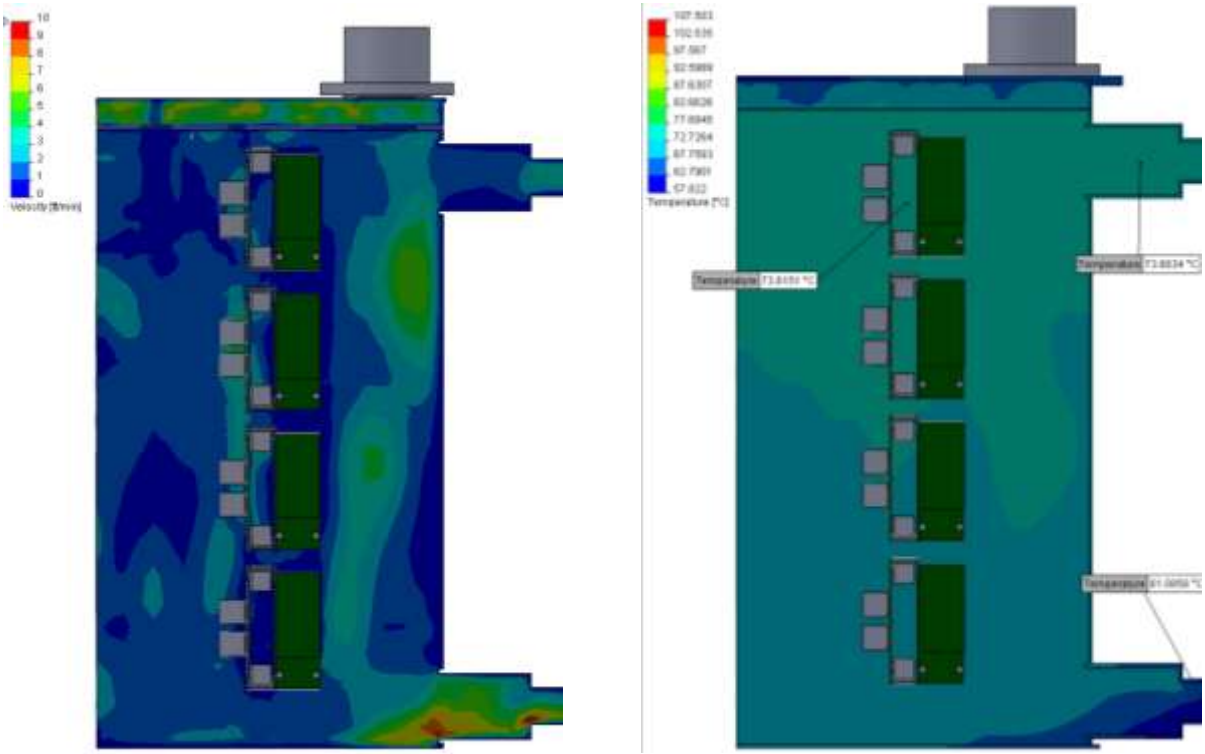

FIGURE 12: HVDC TRANSFORMER TANK: VELOCITY AND TEMP OF SECTION THROUGH INLET AND OUTLET

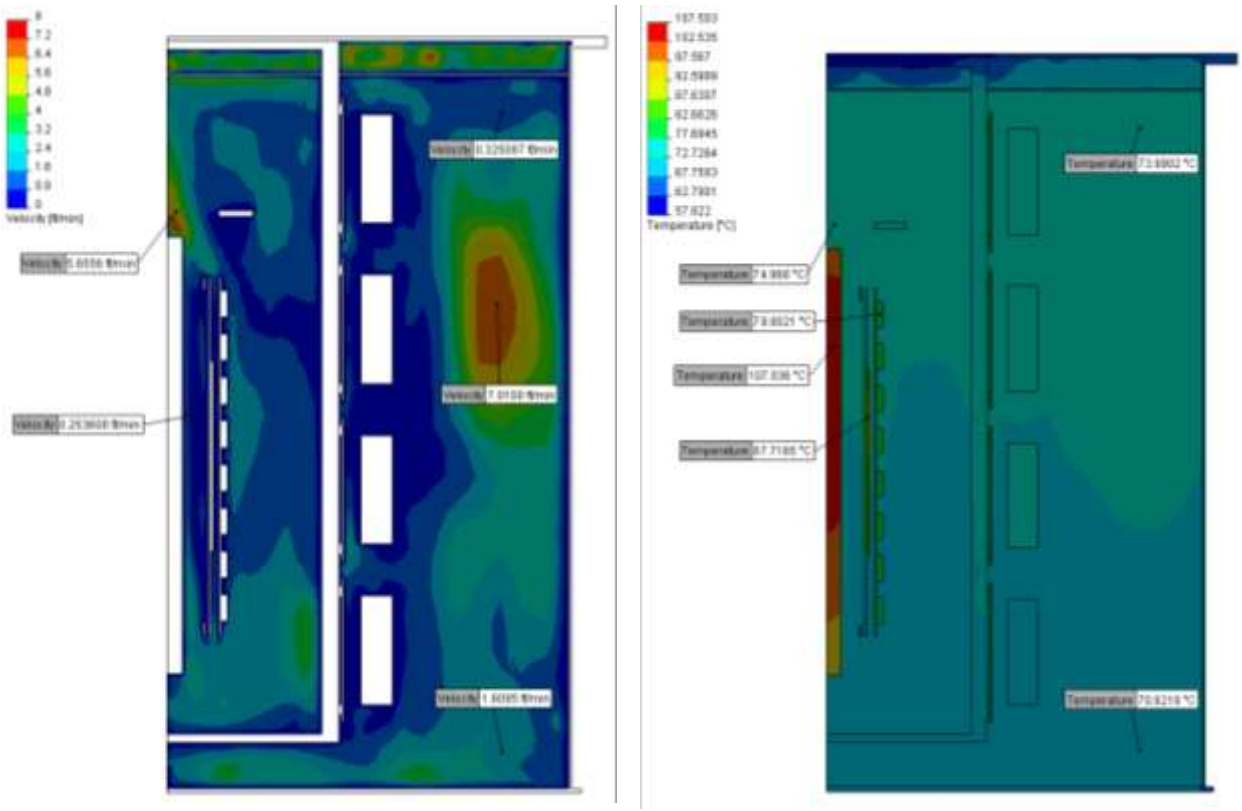

FIGURE 13: HVDC TRANSFORMER TANK: VELOCITY AND TEMP OF SECTION THROUGH CORE

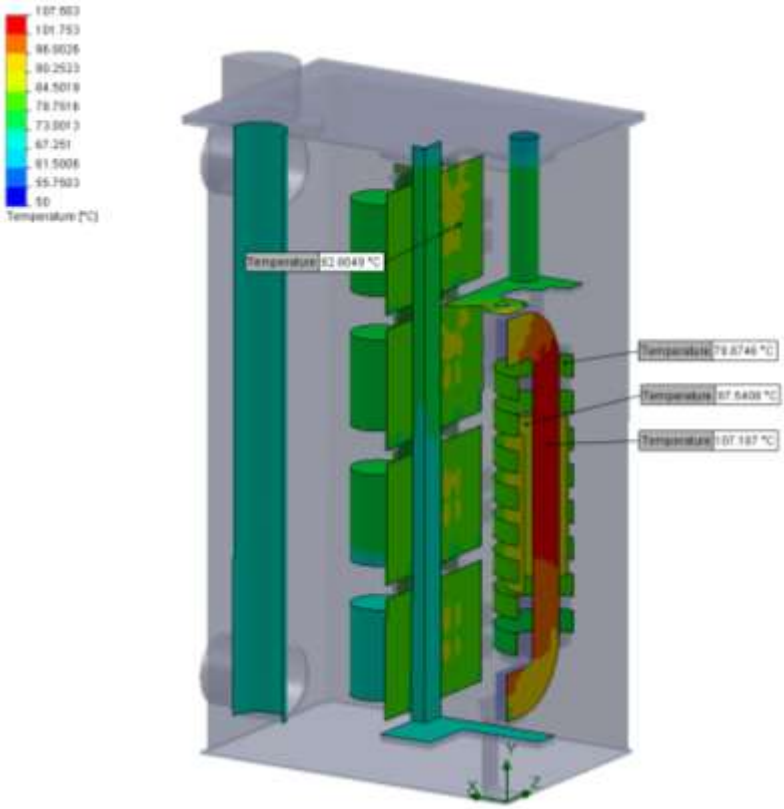

FIGURE 14: HVDC TRANSFORMER TANK: SURFACE TEMPERATURES

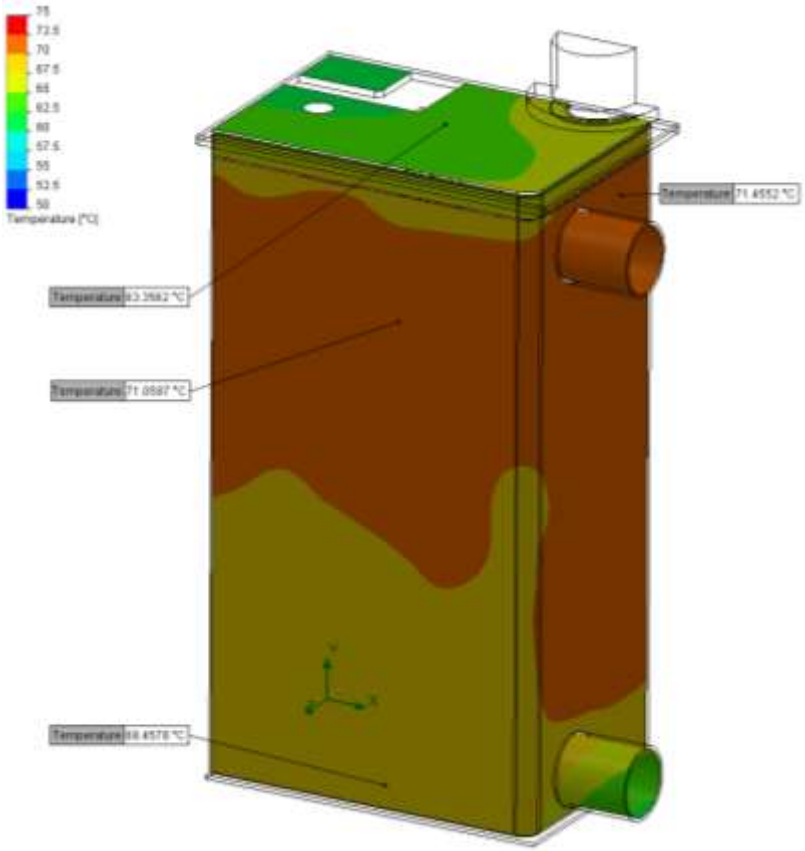

FIGURE 15: HVDC TRANSFORMER TANK: TANK WALL TEMPERATURES

2.5 Packaging

The packaging design attempts to place heavy, dense components near the base of the cabinet to keep the center of gravity as low as possible. This will increase stability during shipping and installation, and will result in a safer unit. Keeping the weight near the base also reduces the amount of load the walls must support, which can reduce structural cost and weight. The image below shows the approximate weight distribution of the major components and approximate location of center of gravity of the cabinet.

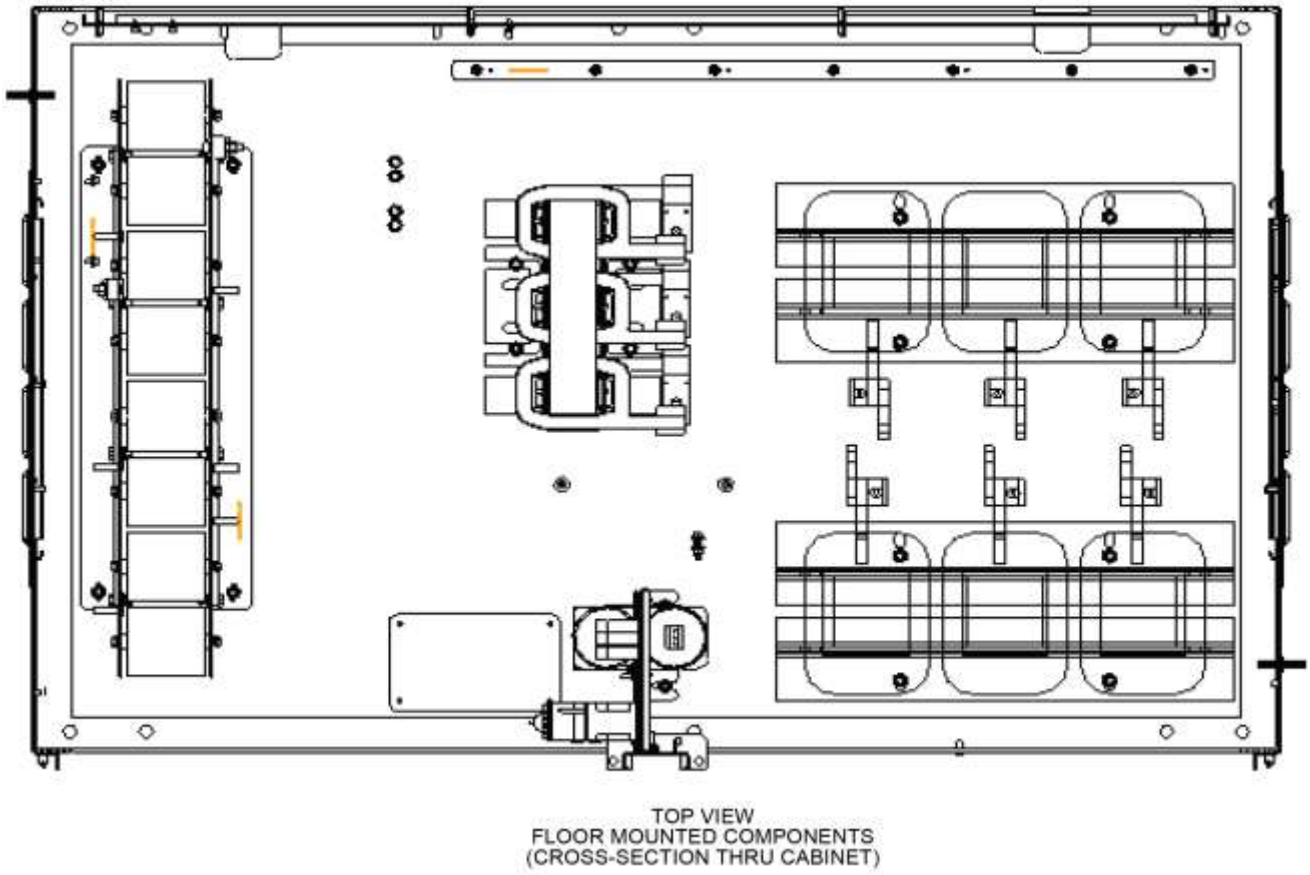

FIGURE 16: LVAC ENCLOSURE: APPROXIMATE WEIGHT DISTRIBUTION

2.6 Control Design

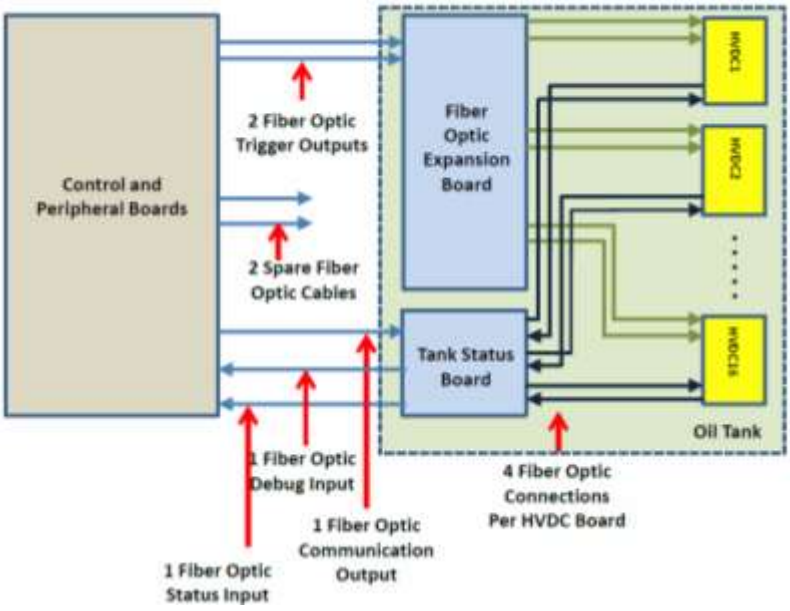

FIGURE 17: CONTROL SYSTEM: HVDC CONTROL ARCHITECTURE

The HVDC section for the control system consists of the following:

- Stack Board Triggers originate on the Control/Peripheral board in the LVAC Enclosure.
- Trigger expansion occurs inside the HVDC tank
  - Each trigger is duplicated 16 times (one for each HVDC stack board)
- Status is passed back to the Control system via the Tank Status board
  - Each HVDC board reports status based on:
    - 4 IGBT Status signals
    - HVDC value within the acceptable “window”
    - IGBT heat sink temperature within the acceptable “window”
- Fiber Optic communication from Control/Peripheral to Tank Status
  - Used to set “window” values for HV and Temperature monitoring
  - “Window” values are communicated to individual stack boards via the Tank Status board
- Debugging:
  - Each stack board has debug reporting capability (not used for normal system operation)
  - Tank Status can request debug info from stack board
  - Stack board can bypass “normal” status chain and use UART instead when in debug

mode

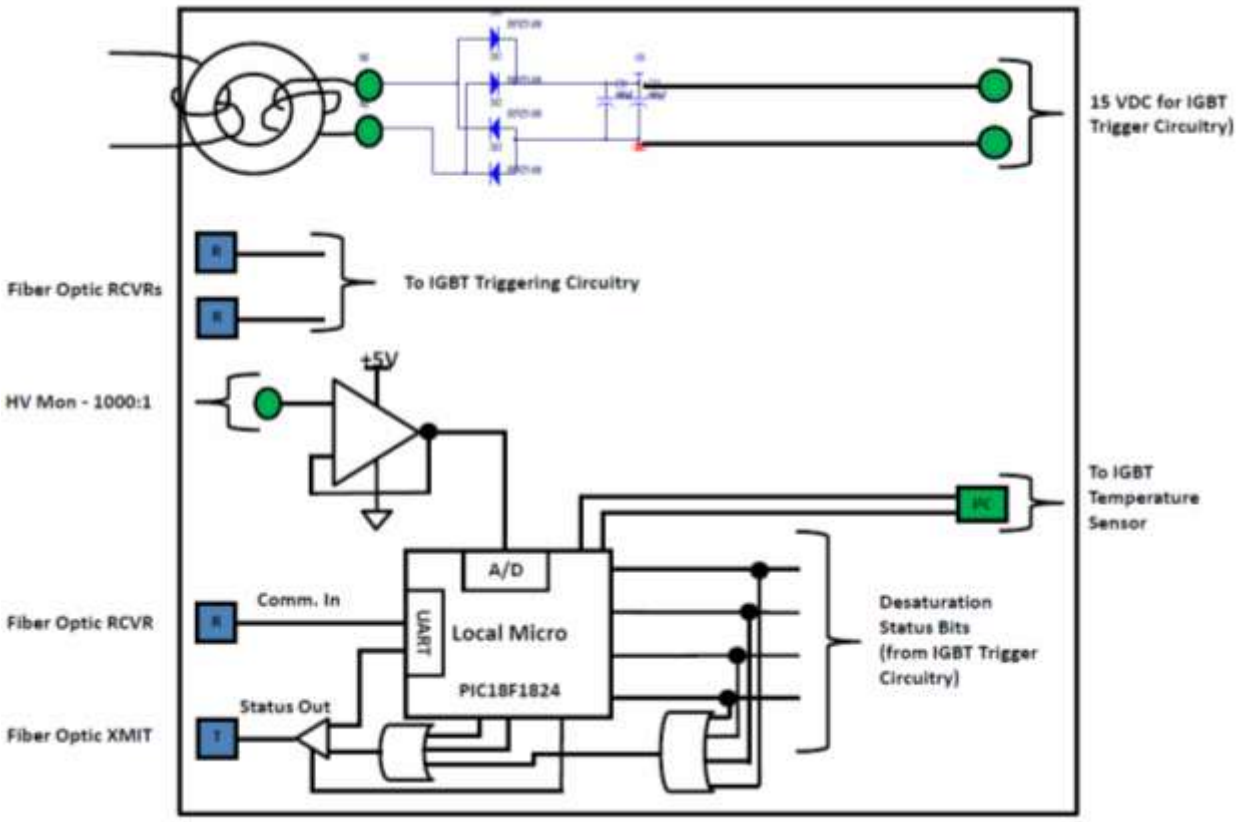

FIGURE 18: CONTROL SYSTEM: HVDC TRIGGER BOARD DIAGRAM

- Optical Triggering signals are received from the Fiber Optic Expansion Board
- Using either 2 or 4 triggers
  - Legacy design required 4 triggers (due to OEM trigger board requirements)
  - Existing design optimizes this down to 2 triggers (one for each “H Bridge Diagonal”)
- Additional Fiber Optic Input for communication
  - Used to set “windows” for HV and Temperature monitoring
  - On board micro monitors HV via 1000:1 test point and A/D converter
  - On board micro monitors one IGBT heat sink temperature via I^2C interface
- Desaturation status for each IGBT
- Status Output via Fiber Optic (to Tank Status board)
  - Status is single-bit based on 4 Desaturation Statuses, HVDC value and IGBT temperature
- Status Output can also be used to send debug data
  - Data path is changed to the microcontroller UART via a 2 input MUX

- 3 Byte Status
  - 4 bits for IGBT Desaturation
  - 1 bit for HVDC status
  - 1 bit for IGBT Temperature status
  - 10 bits HVDC
  - 8 bits Temperature

- Fiber Optic Expansion Provides 16 up to Optical Inputs
- Provides 64 up to Optical Outputs
- Outputs are Connected in Groups of 4
- Up to 4 Output Groups per Input
- Can Connect up to 16 Outputs to Each Input
- Only Required Outputs Need be Populated
- Input/ Output Mapping Achieved via 0Ω resistors
- Design split into Base Board/Plug-In Boards
- Plug-In provides 2 inputs/8 outputs
- Each Plug-In connects to all 16 receiver inputs
- Receiver Inputs from Plug-In are routed to Base Board

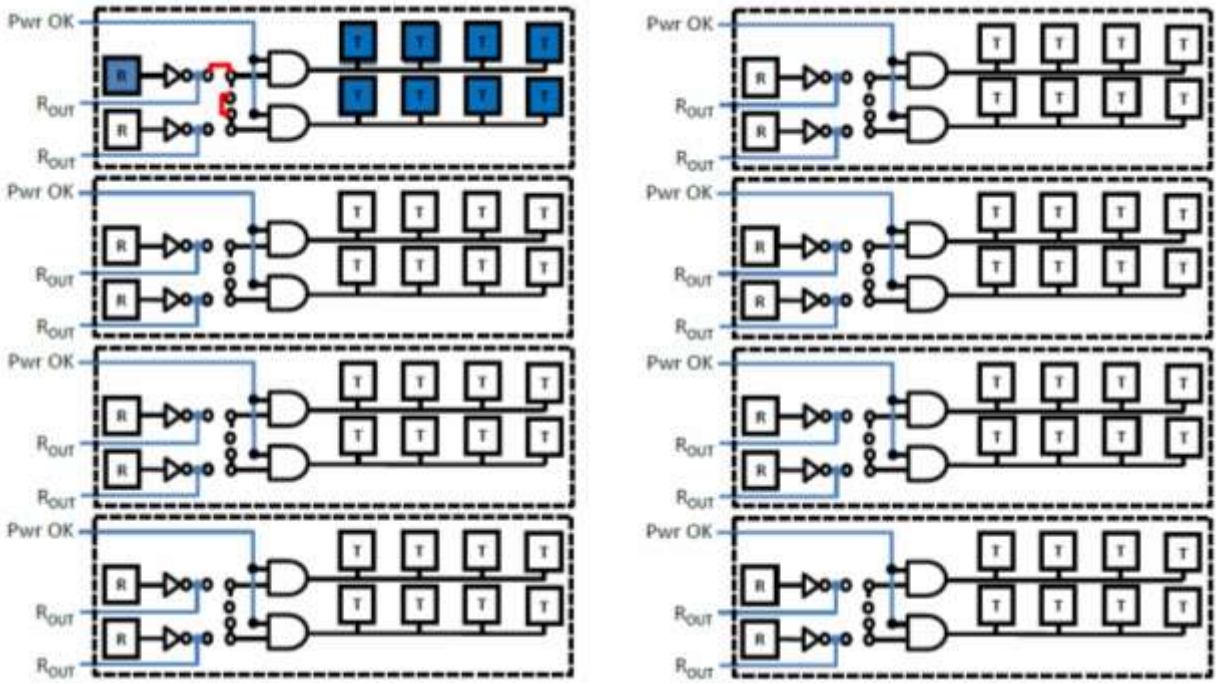

FIGURE 19: CONTROL SYSTEM: FIBER OPTIC EXPANSION BLOCK DIAGRAM

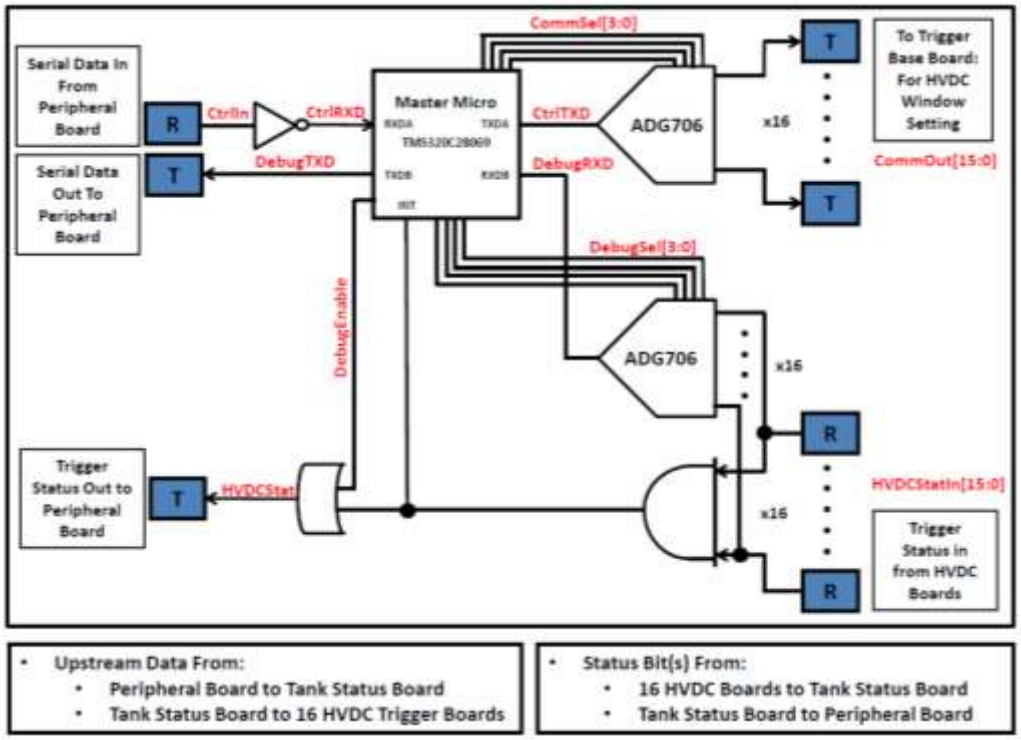

FIGURE 20: CONTROL SYSTEM: TANK STATUS BLOCK DIAGRAM

FIGURE 21: TANK STATUS AND FIBER OPTIC EXPANSION BOARDS

Chapter 3: **Task 2: Develop and Test HVDC Switching Bridge**

3.1 Overview of Progress

HVDC development began with testing the components and will be considered complete when full voltage, full power HV transmission has been successfully demonstrated in both directions. To that end, the goal is not yet complete. The current state of development is such that the system is functional in the DC rectification mode. The inverter mode (from HVDC to 480VAC) is not functional. Although it passed preliminary tests for power electronics, two problems have been identified.

The first, and most significant problem, is a thermal issue related to the high frequency switching of the IGBT's used to switch the high voltage DC. Although the IGBT components used in the HV bridge stacks passed thermal preliminary tests, they overheated when operating at higher voltage (during a 33kV bring-up test). The corrective action is to redesign the HV board and use more heavily de-rated components. This action requires significant future investment to re-design and replace the 16 HVDC stages.

The second problem is that the fiber optic system was unreliable, leading to non-simultaneous triggering of the high-voltage stack. This causes unnecessary heating within the IGBT as it switches off against non-zero current and thus exaggerates the first problem. This was corrected and bench-top tested, it has yet to be evaluated in full system operation.

This technical setback has led to the subsequent change of scope to first prove system operation in generation of HVDC only.

We anticipate the work will be performed soon following this project to begin testing the redesign work. It is anticipated that if the corrective actions are successful, bi-directional power can be demonstrated within 6 months.

Nevertheless, the HVDC switching development can be considered successful in the rectification mode, having reached 50kV open circuit in that mode of operation.

3.2 Theory of Operation

The converter is based on a zero-current resonant switching H-Bridge topology. It is intended to be bidirectional, such that the converter can be used both at the transmitting and receiving stations of the transmission line.

The general principle of operation will be explained using Figure 22 and Figure 23 below. In these figures power flows from left to right, with current always flowing out of the low voltage (LV) bus capacitor (C_{LV}) and always into the high voltage (HV) DC bus capacitor (C_{HV}).

The path the current takes is a key aspect of understanding the operation of the converter. In short, a single phase AC square wave is generated by the LV bridge alternately connecting the bridge output terminals (measured with a voltmeter as V_{AC}) to the top and bottom of the LV bridge (see Figure 22). This square wave is applied to the resonant capacitor (C_{CC}) in series with the transformer primary terminals (measured with a voltmeter as V_{XL}).

The transformer performs two main functions. First, and most obviously, it passes power from the primary to secondary, stepping up the voltage in a ratio of 63.5:1 and at the same time isolating the circuits galvanically. The second function is that its impedance limits the inrush into

the resonant capacitor, and in particular its leakage inductance forms a series resonant RLC circuit. The resulting resonant pulse is sinusoidal and the resulting power-transferring current only flows in one direction (i.e. the current is a half sine wave rather than a fully oscillatory one). This behavior is desirable because the switches can be turned off when the current is zero, and so the power dissipated in the switches (line current x switch voltage) is theoretically zero. The current pulse travels through the transformer to the HV bridge (acting as a full wave rectifier) and charges the HV bus capacitor, which is then discharged by the load (here represented as a resistance).

No more power will be transferred until the polarity of the LV bus capacitor is reversed, an action performed by triggering the alternative complementary pair of LV IGBT switches (see Figure 23). The voltages and current flows in the resonant section are opposite to the first pulse; however, because the HV bridge is a full wave rectifier, the pulse also results in power being transferred to charge the HV capacitor in the same direction. This toggling action of the LV bridge switching the LV bus capacitor defines a *switching* frequency (f_s). This is not to be confused with the *resonant* frequency (f_r) (see Figure 24), which is the frequency of the sine wave of the resonant current. Since the switches should not be turned off against current, it follows that f_s must be less than f_r for efficient (and safe) operation.

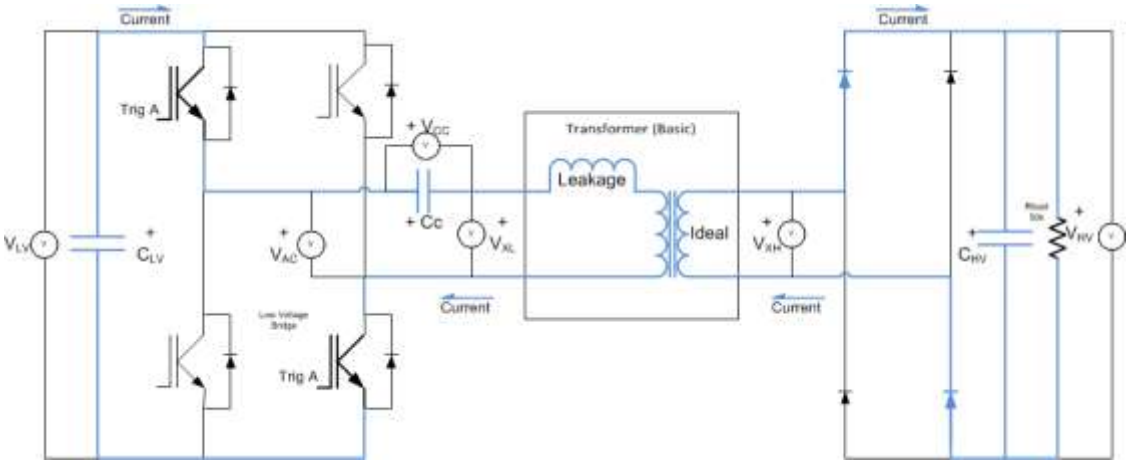

FIGURE 22: POSITIVE PULSE

SHOWING MAIN CURRENT TRANSFERRING POWER FROM LEVT TO RIGHT (BLUE PATH) DUE TO TRIIGER A SIGNAL BEING TURNED ON.

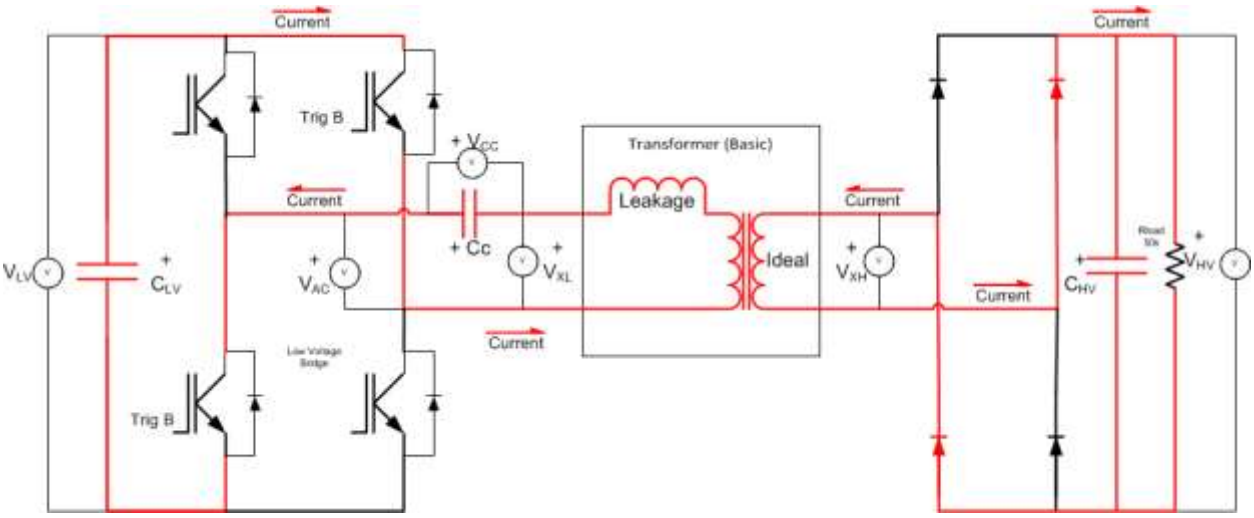

FIGURE 23: NEGATIVE PULSE.

MAIN POWER IS STILL TRANSFERRED IN SAME DIRECTION, BUT TRANSFORMER AND RESONANT CAP VOLTAGES, AND RESONANT CURRENT POLARITY ARE REVERSED DUE TO TRIGGER B.

The basic voltage balance equations are expressed in terms of the voltmeters which are shown later in scope shots of actual operation. Note that the diagram shows sign convention, which is important.

1) $V_{AC} = \pm|V_{LV} - 2xV_{IGBT}|$, namely that the bridge applies the LV bus voltage to the terminals, minus a small voltage drop ~0.3V of the IGBT, which can be ignored in the pedagogy. The polarity will change depending on which switching pair are operating.
2) $V_{AC} = V_{CC} + V_{XL}$. The exact nature of the transformer will be elaborated on, but this equation will always be true and the lumped effect of the transformer can be measured using a voltmeter at the terminals.
3) $V_{XH} = R\ (V_{XL}-V_{Leakage})$, where R is the effective transformer ratio. As designed it is 10 primary turns: 16 x 39-turn secondaries, or 62.5:1, but the apparent value of this will change slightly depending on running conditions.
4) Under open circuit conditions, at the end of a pulse during steady state operation (having charged the output capacitor up to operating voltage, $V_{HV} = |V_{XH} - 2xV_{DIODE}|$.

The duty cycle of switch operation is defined below. As noted before, the switch must stay on at least as long as the resonant switching period. There must also be a minimum time between switching events, known as dead time, between the complementary pairs. It is usually taken to be 3us, and ensures that both the A and B switches are not on at the same time, which would result in a short circuit of the DC bus. The overall switching period, the reciprocal of f_s, is defined as 2x (On Time + Dead Time).

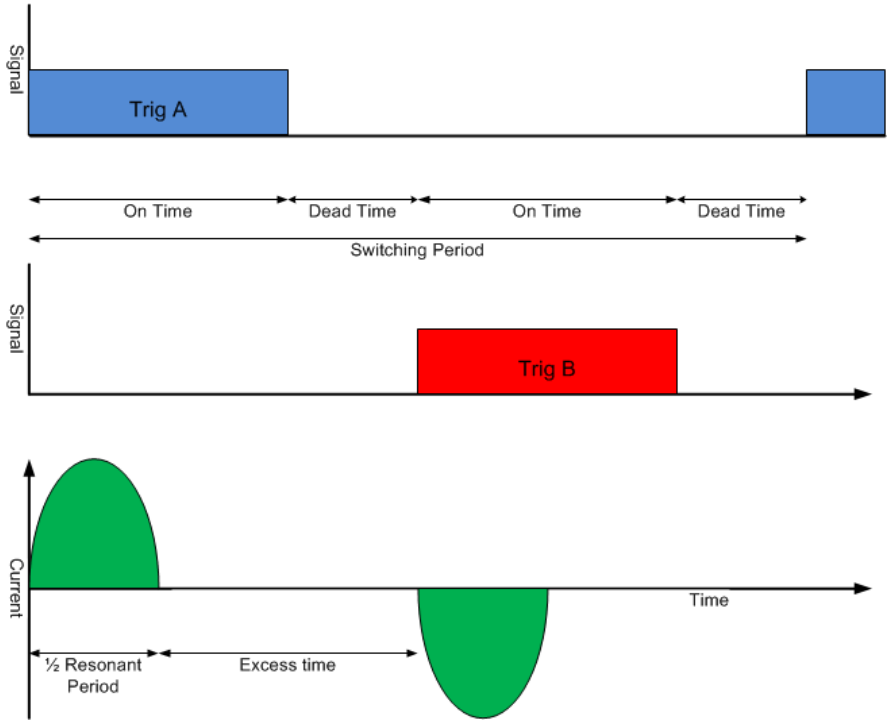

FIGURE 24: TRIGGER SIGNALS RELATING TO POWER FLOW DIAGRAMS (SEE ALSO FIGURE 22 AND FIGURE 23)

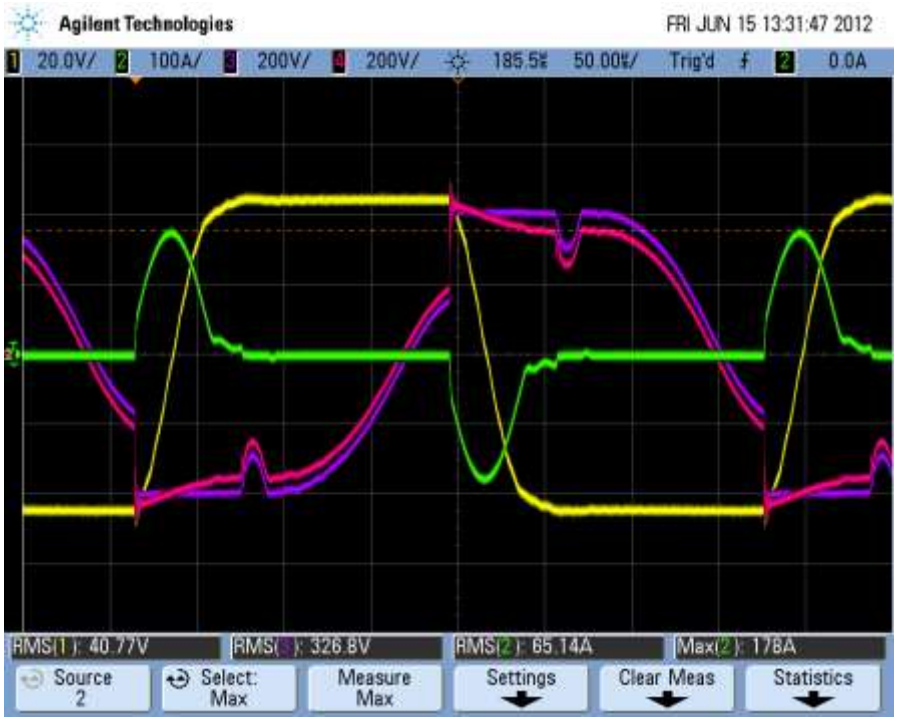

FIGURE 25: TYPICAL PULSE WAVEFORM.

RESONANT CAP VOLTAGE (VCC, YELLOW), CURRENT (ICC, GREEN), AC OUTPUT (VAC, PURPLE) AND TRANSFORMER VOLTAGE (VXL, PINK) ARE SHOWN.

The most important trends that can be gleaned from observing operation are the following:

1) $\mathbf{V_{HV} = V_{LV}*R}$, namely that overall the circuit behaves like a DC transformer, that steps up the LV bus voltage by the (effective) transformer ratio. It follows that since the converter is a voltage controlled source, regulation of the LV bus voltage leads to the regulation of the HV bus voltage.
2) For a given power output, the higher the switching frequency f_s, the lower the resonant current. This can be seen that the average power delivered to the load is made up of individual packets of charge delivered from the LV bus to the HV bus. The more frequently the packets are transferred, the smaller each packet can be.
3) The resonant cap voltage, V_{cc}, will alternate in polarity with each pulse, but have a magnitude $|V_{cc}|$ proportional to the power throughput of the system. The resonant capacitor can be thought of integrating the current according to the capacitor circuit equation: $V = 1/C \int I(t)dt$. Note that charge $Q = \int I(t)\, dt$. So the voltage swing is proportional to the charge passed per pulse. When higher power is put through, more charge must be transferred to the output to give the higher average current. This is a corollary of (2), since it is the same charge transfer being discussed except we assume here increased power and fixed frequency.

3.3 Component Tests

The component tests were limited to the areas of highest technical risk. The following tests were performed and passed:

1) IGBT
    a. Voltage withstand
    b. Conduction loss/thermal test
2) Diode
    a. Voltage withstand
    b. Conduction loss/thermal test
3) HV Bridge resonance test
    a. Rectification mode
    b. Inversion mode
4) Transformer
    a. 20 kV AC Hi-pot (dry)

Both the IGBTs and the diodes on the HV stack board were tested as components. The tests are to be considered successful since both conduction losses and voltage hold-off were successfully on both the IGBTs and the diodes. In hindsight, there were deficiencies in the plan for component testing, since the IGBT switching issue was not identified at this stage.

3.3.1 IGBT Voltage Test

The purpose of this test was to confirm that the IGBTs used could withstand the nominal operating DC input voltage of 3.125 kV. The test was performed with a single HV stack board that had a high voltage DC input and a resistive load, as per the test schematic (Figure 26). The

DC input as measured was 3.312 kV (the green trace in Figure 27), 200 V higher than the typical stack voltage. The test was run for an hour into a 0.2A (2%) load with no adverse effects or degradation observed. This can be seen in the purple trace.

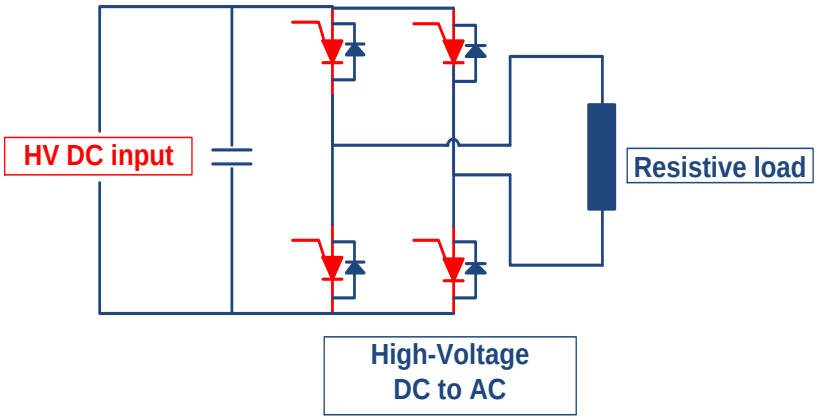

FIGURE 26: HIGH VOLTAGE DC TO AC @ 1 KHZ

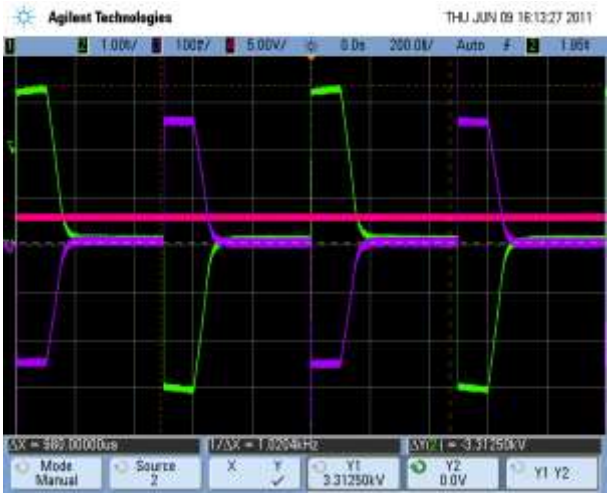

FIGURE 27: TEST DATA EXAMPLE SHOWING 3.312 KV, 1 KHZ SWITCHING

3.3.2 IGBT Thermal Test

The design power and thermal simulations indicate that each of the IGBTs need to handle **5.5 A average current** and dissipate at least **12.5 W** below rated temperature at 120°C. A similar test setup was used as per the Section 3.3.1 Voltage Test, but with an increased load. The IGBTs were not switched but left on to ensure that all losses were conductive. A DC current of 7 A was measured. Thermal readings were made and are shown in Figure 29 and Figure 30. 13 W of power losses were measured on each device. PPS concluded that the IGBT jacket temperature and heatsink temperature were below the rated design temperature which is 120°C at 7 A/13 W in air. Further, the air temperature should be higher than that recorded in oil.

The IGBT and high voltage board passed the thermal test.

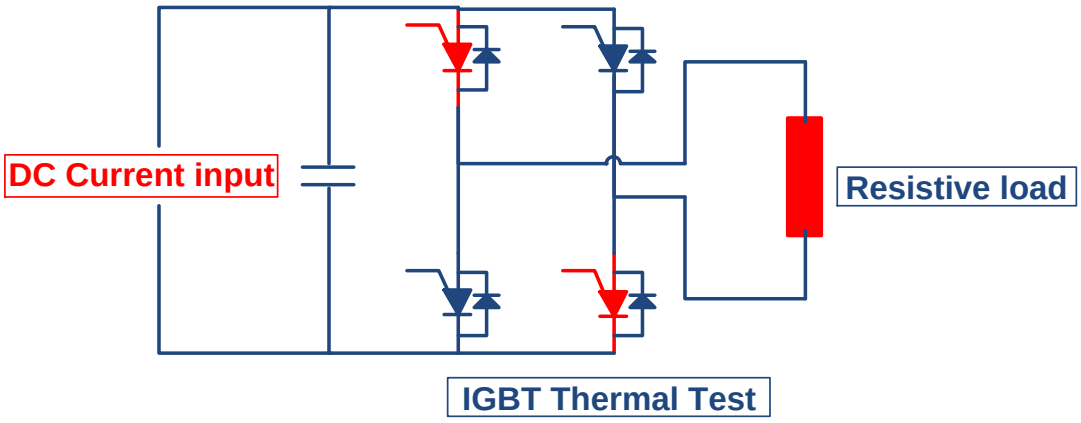

FIGURE 28: IGBT THERMAL TEST SETUP

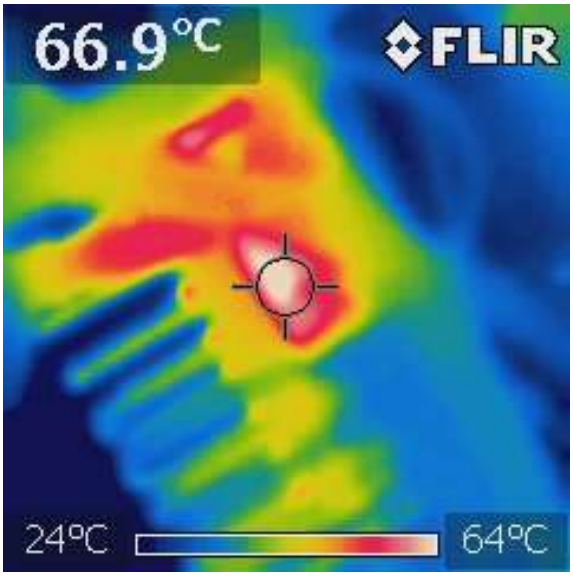

FIGURE 29: IGBT JACKET TEMPERATURE WAS MEASURED AS 67°C IN AIR

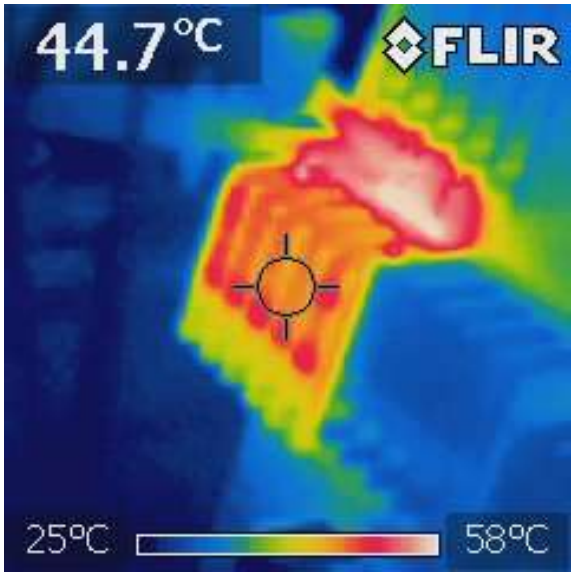

FIGURE 30: IGBT HEATSINK WAS MEASURED AS 45°C IN AIR

3.3.3 Diode Voltage Test

Unlike the IGBT DC to AC test, the diode test is an AC to DC rectifying test. Like the IGBT, the diode and high voltage board also have to pass the voltage and thermal test to make sure the low voltage AC resonant can be rectified to 50 kV DC. The test schematic is shown in Figure 31, using a high voltage AC source and the same resistive load bank. The AC was input was 60 Hz. The rectified output voltage was measured as 3200 V, higher than the nominal operating voltage. The diode and HV stack board therefore passed thermal testing.

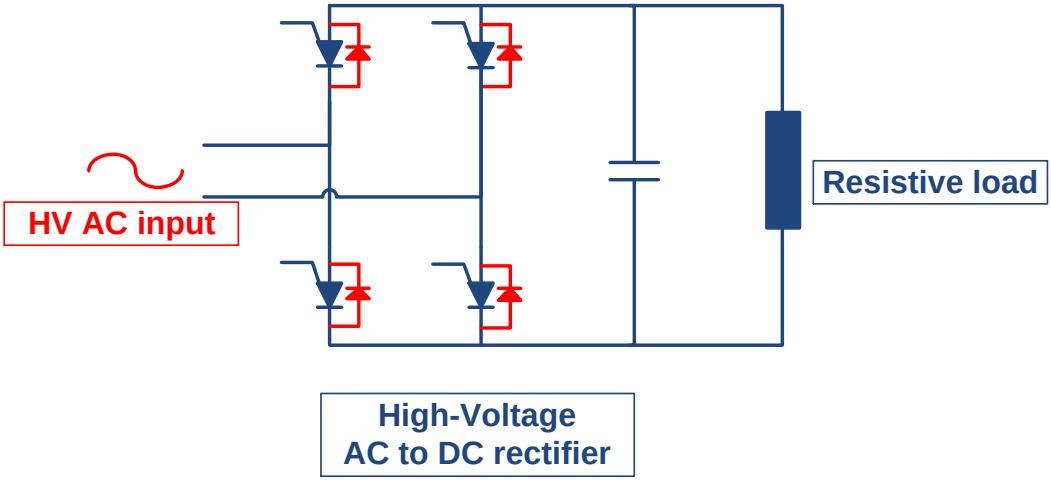

FIGURE 31: DIODE VOLTAGE TEST SCHEMATIC

3.3.4 Diode Current Test

The design power and thermal simulations indicate that each of the diodes needs to handle **5.5A average current** and dissipate at least **18W** below rated temperature at 120°C. A similar test setup was used as per Section 3.3.3 Diode Voltage Test but with an increased load and is shown in Figure 32.

The diodes were conducting for half cycle as per the real application. A DC current of 10 A was measured. Thermal readings were made, and are shown in Figure 33 and Figure 34. 18 W power loss was measured on each device. The diode jacket temperature and heatsink temperature are at least 30°C below the rated design temperature which is 120°C at 7 A/13 W in air. Further, the recorded air temperature should be higher than that recorded in oil.

The diode and HV stack board passed thermal testing.

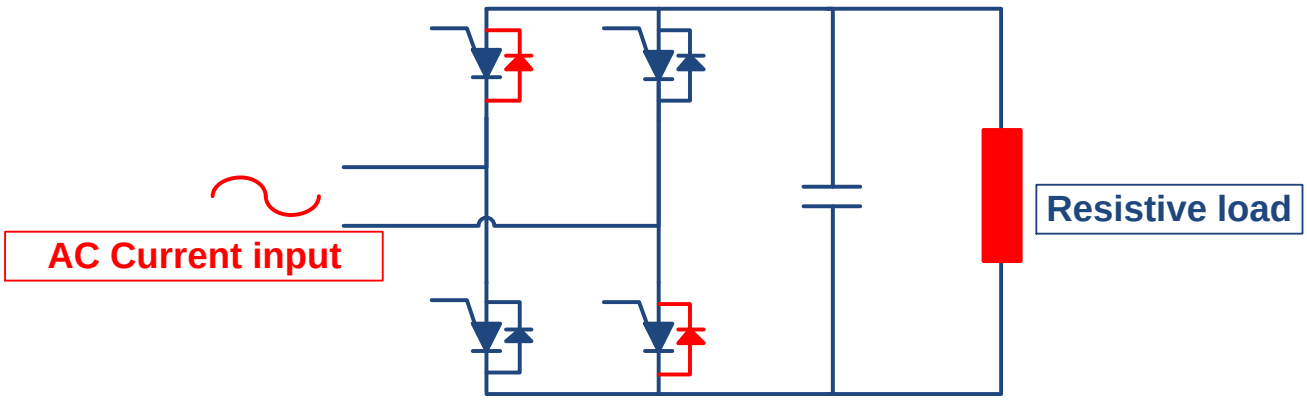

FIGURE 32: DIODE THERMAL TEST SCHEMATIC

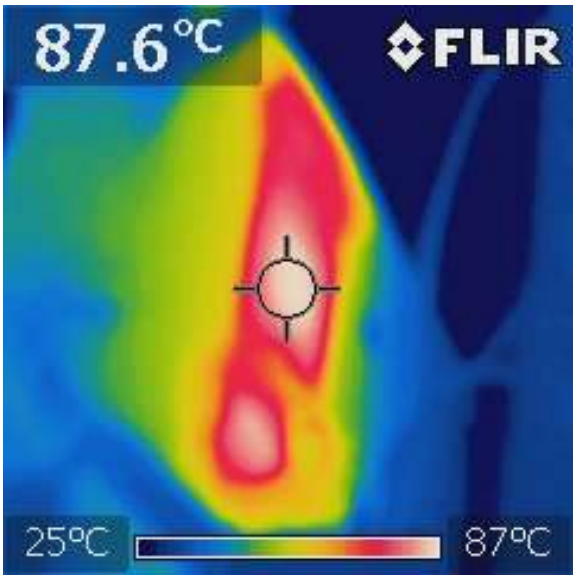

FIGURE 33: DIODE JACKET TEMPERATURE WAS MEASURED AS 88°C IN AIR

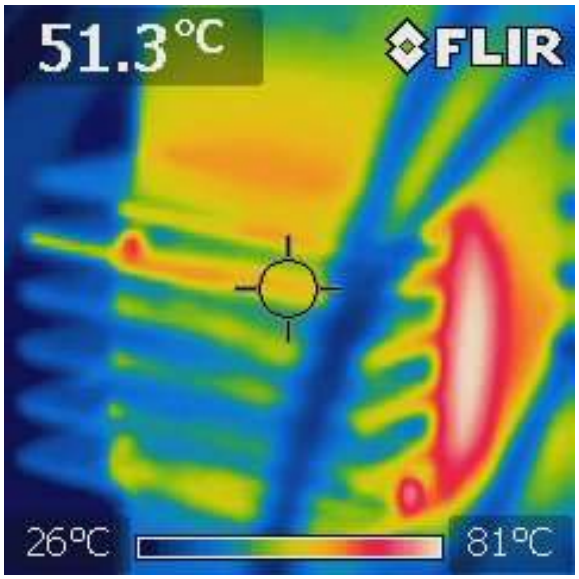

FIGURE 34: DIODE HEATSINK TEMPERATURE WAS MEASURED AS 52°C IN AIR

3.3.5 Transformer Hi-pot Test

This test, while not the final hi-pot test, was to ensure that the transformer looked like it would pass the final test. In air, the voltage hold-off was estimated as 20 kV AC, as opposed to the 50 kV in oil. The test identified insulation deficiencies between the primary and the secondary windings and was performed until the current observed was sufficiently low and no arcing could be seen.

Hi-pot (in air)	Hi-pot Voltage	Leakage Current	State
Transformer Secondary to High Voltage Tank	*20,000 V*	*1.8 mA @ 1min*	*PASS*
Transformer Primary to High Voltage Tank	*3,000 V*	*0.8 mA @ 1min*	*PASS*
Transformer Primary to Low Voltage Cabinet	*1,700 V*	*30 mA @1 min*	*PASS*

Table 2: Transformer Hi-pot in Air Test Results

FIGURE 35: HI-POT TEST SETUP SHOWING TRANSFORMER (LEFT) AND HI-POT EQUIPMENT (RIGHT)

3.4 Preliminary Operation Tests

A single HV Bridge PCB was paired with an LV Bridge and LV resonant capacitor and operated in both directions (see Figure 36). Transforming LV DC to HV DC is the key mechanism for the system to rectify HVDC (rectification mode) and transforming from HV DC to LV DC is that for AC generation (inverter mode). Both operations were tested, and passed.

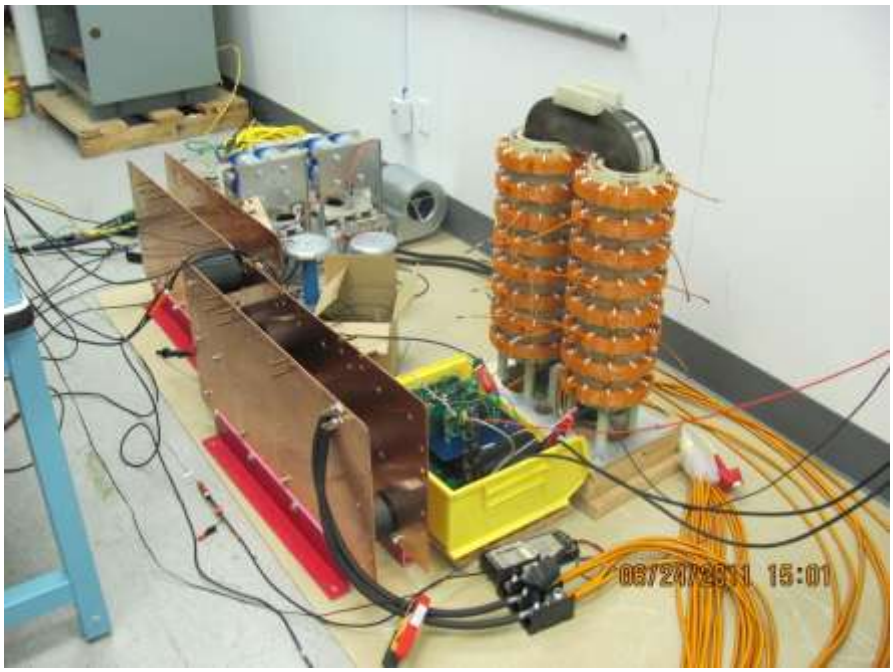

FIGURE 36: CENTRAL RESONANT LINK TEST SETUP
SHOWING (L TO R) RESONANT CAPACITOR, HV STAGE, AND TRANSFORMER.

3.4.1 Rectification Mode

The schematic is shown in Figure 37. The test was operated with the LVDC increased until the output was at 500 V in air. By switching the LVDC Bridge, a single-phase AC square wave voltage was applied across the resonant circuit with 50% duty cycle. This pulse had sinusoidal current as determined by the leakage inductance of the transformer and the capacitor in the circuit. This pulse was transferred to the transformer secondary and stepped up by its turns-ratio. It is then rectified and the DC output is loaded with a resistor. Soft switching and high frequency resonance (22 kHz) were observed, and the test is therefore considered a success. The operation was monitored using an oscilloscope, from which a typical capture can be seen in Figure 38. The pink and purple curve represent to the current for both primary and secondary side, respectively. The green curve is the output voltage, showing 500 VDC with low ripple.

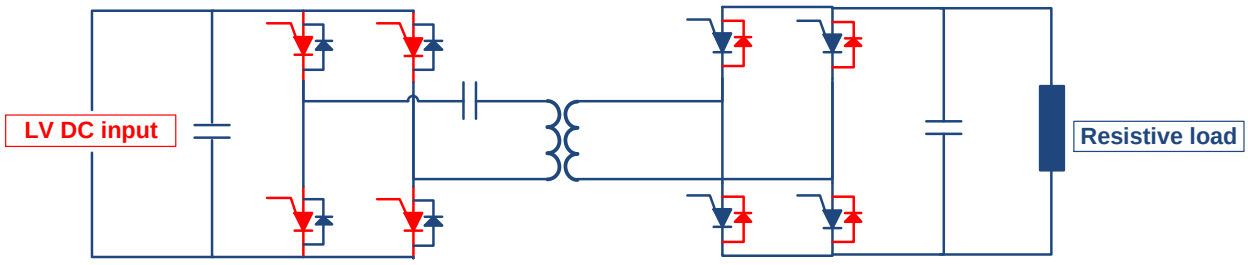

FIGURE 37: CENTRAL RESONANT LINK TEST SETUP SCHEMATIC (LV TO HV)

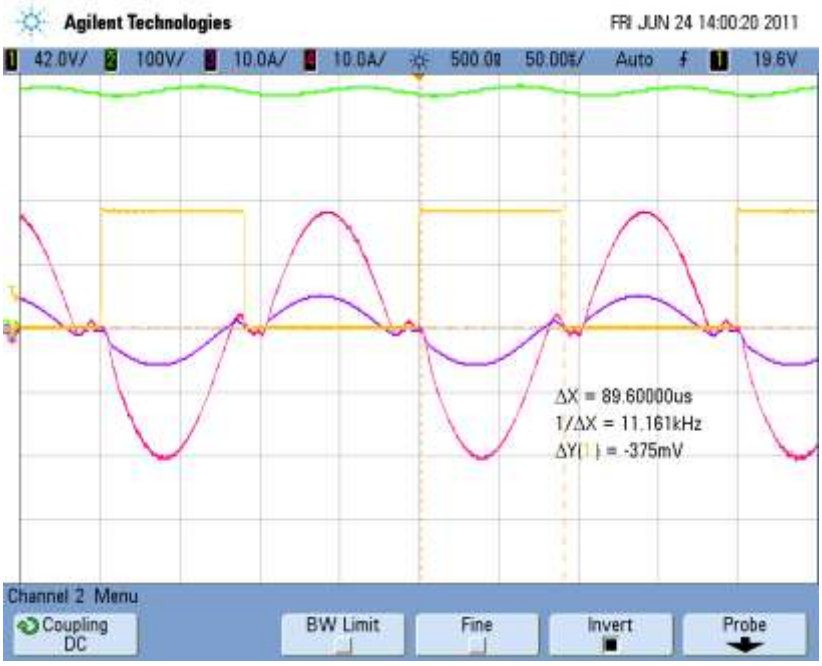

FIGURE 38: RECTIFICATION MODE RESONANT LINK TEST RESULT

3.4.2 Inversion Mode

This test was similar to that described in 3.4.1 Rectification Mode, with the source changed to the HV side and the load connected to the LV side. The HV side achieved 800 V in air, about ¼ of normal operating voltage, which was sufficient to prove the resonant mechanism. The results are illustrated in Figure 40. The pink and purple curve represent to the current for both primary and secondary side, respectively. The green curve is the output voltage, while the yellow signal is the trigger driver signal. The ratio of purple to pink traces shows the transformer action upon the current. The observation that the pink current is zero when the trigger is applied shows soft-switching, which is a necessary action for reduced switching losses.

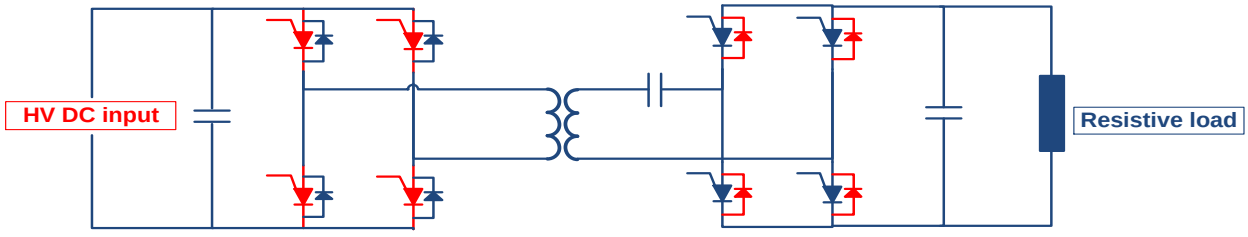

FIGURE 39: CENTRAL RESONANT LINK TEST SETUP SCHEMATIC (HV TO LV)

FIGURE 40: CENTRAL RESONANT LINK TEST RESULT

3.5 Trigger Improvement Testing

3.5.1 Summary

The triggering system was identified during preliminary operation testing as being unreliable, and suspected of leading to the failure of the HV stack at approximately 33kV while raising the voltage to demonstrate switching at 50kV. The system was investigated and unreliable trigger signals discovered. The design was revised, and this test was performed to confirm the improvements showing:

- All IGBT gates turning on within **0.5us** of each other
- All IGBT gates turning off within **3us** of each other
- All pulses successfully transmitted to all IGBT gates.

Further, the remaining difference in simultaneity was traced to the transmitter circuits, which are not highly tolerant of variation in design, and are dependent upon particular device characteristics.

The turn off can be tuned to 1.5us either side of the zero crossing. The application has 17Apk current at 8 kHz resonant frequency, which results in dI/dt maximum of 0.85 A/us at the zero crossing and therefore potentially turn off against 1.28 A. Any switch used must therefore be tolerant of dissipating the power associated with this current. The devices currently selected are not able to dissipate the heat generated during switching.

3.5.2 Test Setup

The schematics of the setup are very similar to that of the final application, with the exception of the power circuit. The power circuit consisted of the following:

- Magna Power DC supply positive connected to 16 625Ω resistors
- Each resistor connected to AC1 of a HV Stack PCB
- All DC returns of HV Stack PCB connected to DC supply negative

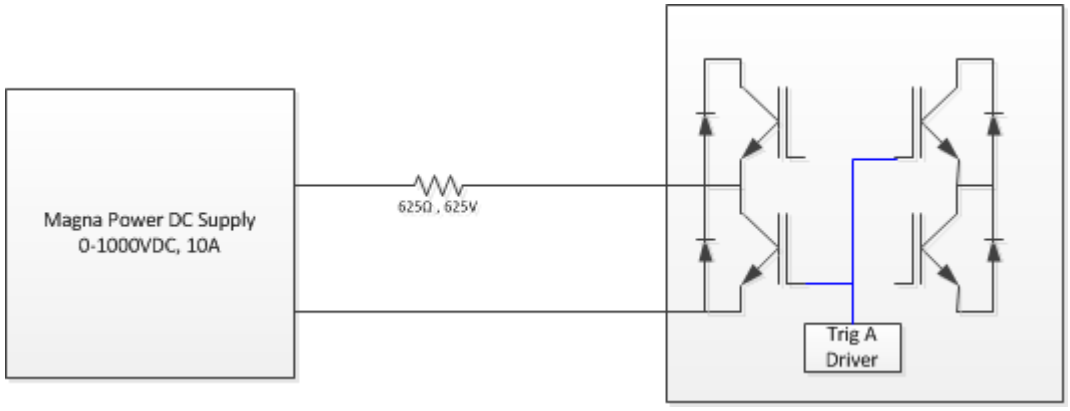

FIGURE 41: POWER SCHEMATIC, WITH ONLY BOTTOM LEFT (Q2) SWITCH IN USE

The control circuit consisted of the following

- TI28069 EVM development card and base board with "Channel A" IR transmitter
- Fiber Optic Expansion Base Board with two Fiber Optic Expansion Daughter Cards in positions 5 and 6.
- 16 Fiber "Signal A", with 4 of 1.3m, 1.6m, 1.9m, 2.2m cables each
- 16 HV Stack PCB's Trigger Board, receiving "Signal A" into D65.

Together, these systems will switch Q2, the bottom switch of AC1 leg of the H-Bridge. The switch is to be triggered at 1 kHz, 10% duty cycle.

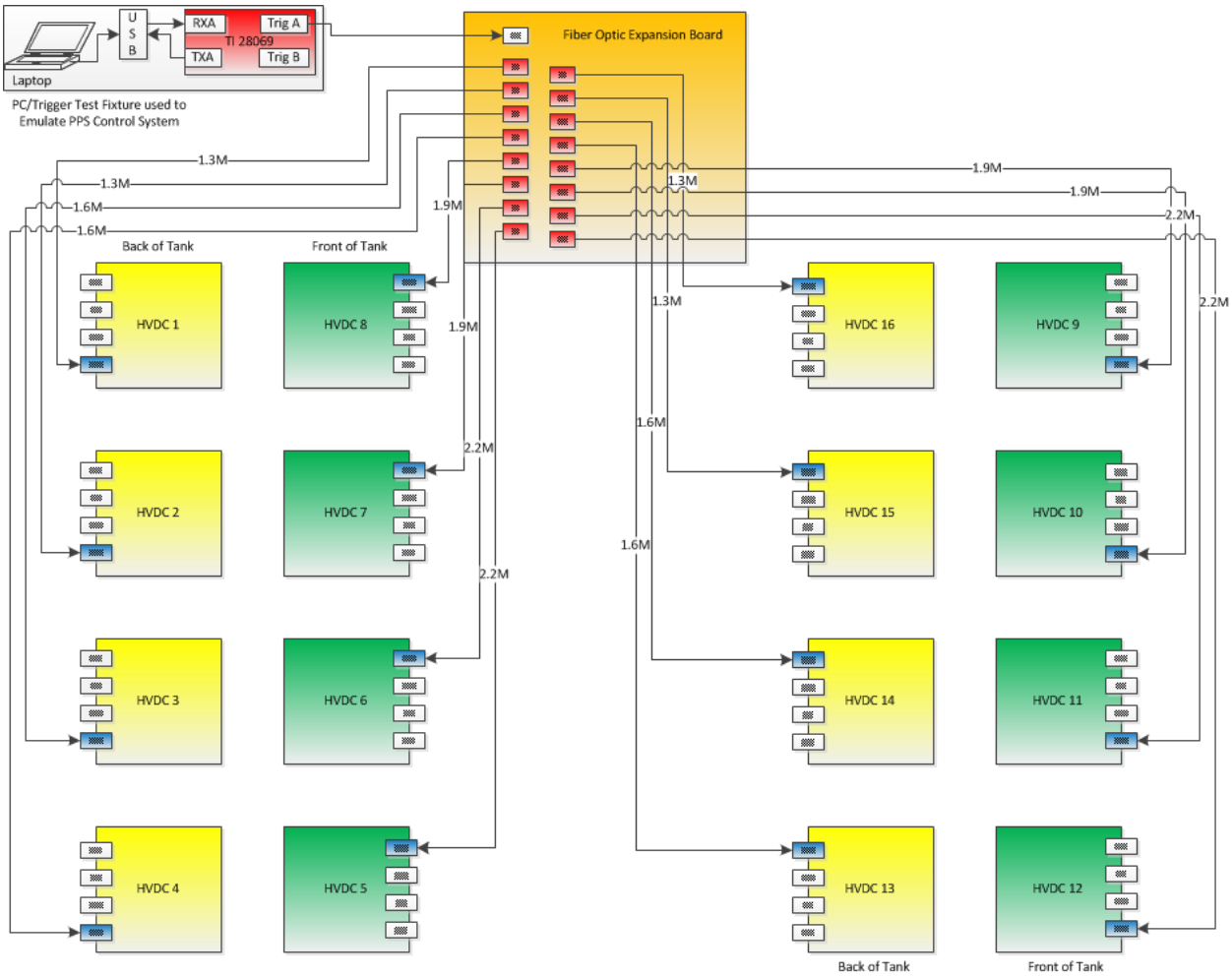

FIGURE 42: CONTROL SCHEMATIC FROM TI TEST FIXTURE TO FIBER OPTIC RECEIVERS ON EACH HIGH VOLTAGE STAGE BOARD

The control power circuits consist of

- 5V USB power from the PC, providing power to the TI28069 card
- 24V power from BK Precision 1550 benchtop supply, providing power to the Fiber Optic Base Board and Expansion Cards
- A 24V, 10A power supply is used to provide power to the Dc To HFAC Power Supply Board
- The DC to HFAC power supply board provides isolated control power to the HV Stack Trigger Boards via a transformer

The monitoring circuits consist of

- 4 scopes measuring 16 signals, with the probe clipped to the gate of Q2 of each HV Stack Board and grounded to the emitter of Q2.
- One signal from GPIO pin 0, the logical output of the TI28069.

Based on the above setup, all signals are monitored and triggered off the GPIO pin 0 signal ("Trigger A"). All times reported are therefore relative to the very start of the signal command chain. The scopes are to use persistence viewing, to generate a history of all pulse edges, and to have the trigger edge delay accounted for and calibrated out accordingly, so that reported times are not affected by the delay.

3.5.3 Test Results

As measured at 300V, the peak current drawn is 0.5A per board. With a 10% duty cycle, this is an average voltage applied to the resistors of 30V, with 50mA average current accordingly drawn. Only 14 boards were switched, due to the failure of HVDC1 and HVDC9, due to the poor regulation of the isolated control power supply.

- All trailing edges at 100V were measured to be between 1.7usec and 4.76usec (see Figure 43)

ALL LEADING EDGES AT 300V WERE MEASURED TO BE BETWEEN 2USEC AND 2.5USEC (SEE

- Figure 44).
- The result time was strongly correlated with the choice of transmitter channel, since switching channels effectively changed the result, while keeping the fiber used and HV Stack Trigger board the same (see Figure 45).
- The result time was not observed to be correlated with voltage applied, at least up to the 300V tested.

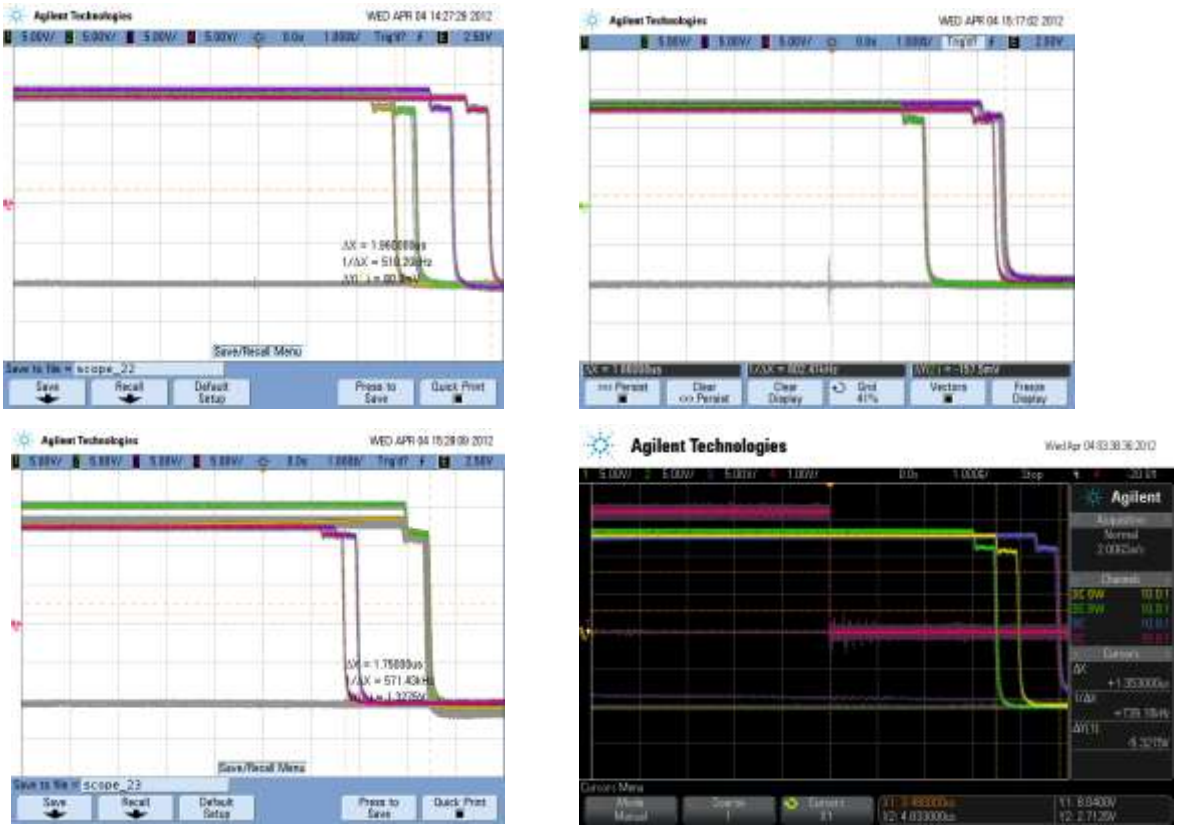

FIGURE 43: DATA FROM 4 SCOPES AT 100V.

BOTTOM RIGHT PINK TRACE IS THE EDGE OF GPIO0, INDICATING THE START OF THE TRIGGER. ALL EDGES ARE WITH 4.83US, AND THE FASTEST IN 1.73, GIVING A SPREAD OF 3.1US (TIME-BASE IS 1US).

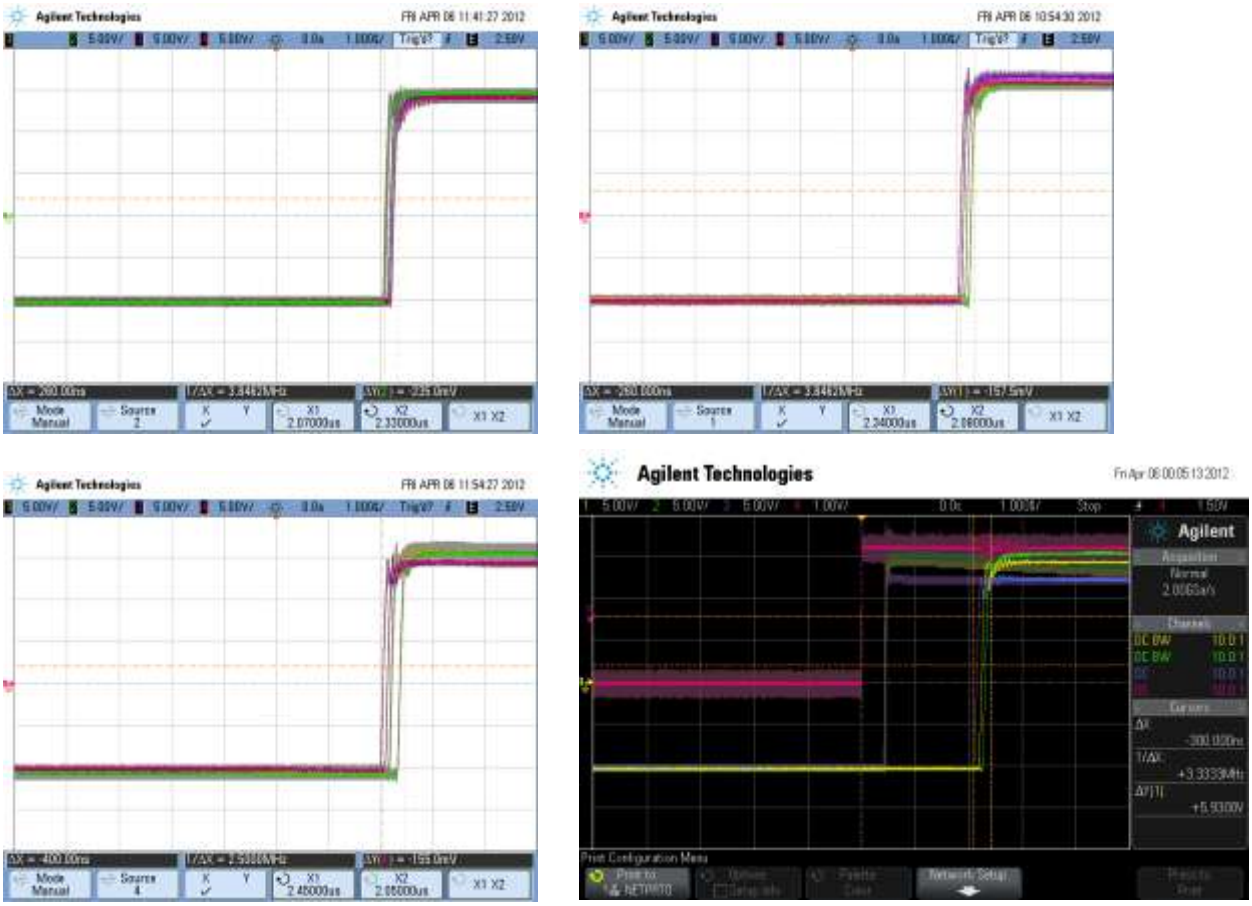

FIGURE 44: LEADING EDGE DATA TAKEN AT 300V

SHOWS SIMULTANEITY WITHIN 500NS, AND OVERALL DELAY BETWEEN 2 AND 2.5US FROM GPIO0 TRIGGER.

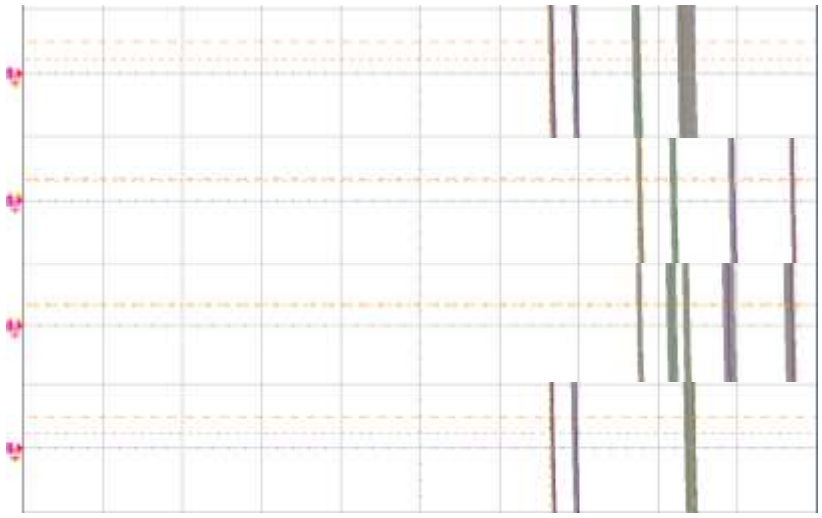

FIGURE 45: TRANSPOSITION OF YELLOW AND GREEN TRANSMITTER CHANNELS.

NOTE THAT FRAMES 1 (TOP) AND 4 (BOTTOM) HAVE IDENTICAL BLUE AND PURPLE LINES, AS DO 2 AND 3. 1 HAS VERY SIMILAR YELLOW AND GREEN TRACES TO 2, WHILE 3 HAS VERY SIMILAR YELLOW AND GREEN TRACES TO 4. THIS INDICATES A STRONG CORRELATION THAT TRANSMITTER CHANNELS AFFECT THE DELAY TIME.

Chapter 4: **Task 3: Design Energy Storage Bank and Controls**

4.1 Overview of Design

The design task is complete. A lead acid based chemistry was chosen and installed in the prototype system. The chemistry was selected based on cost and efficiency. Early on in the project, the idea was proposed of using an ultra-capacitor for storage. During the design phase, it was realized that the benefits offered by ultra-capacitors did not justify the costs. Nevertheless, it was considered during the design phase such that the design would be compatible with an ultra-capacitor should the technology or cost become justifiable in the future.

The remaining options that PPS considers using for energy storage are lead acid and lithium ion based batteries. There is an inherent difficulty in estimating energy storage without very specific information about the power usage profile, which not only depends on the generation source (the profile of available energy throughout the day for that type of source) but also, in the case of wind and perhaps in the case of wave power, very specific preliminary measurements to understand the particulars of the site location. The specifications are therefore liable to change in a specific application, and resizing will certainly be performed. It is simply deemed to be sufficient for demonstration purposes.

There is actually quite a wide range in cost of batteries (the types we surveyed would cost between $20k and $110k) and so another project specific variable is exactly the cost which the project can bear, when compared against the cost of battery renewal and maintenance. Nevertheless, the nominal cost per watt of $0.50 can be met with at least some quantity of the most expensive battery type (Li-Ion) installed, which is very promising.

Another important determining factor in the cost is the number of available cycles before replacement. Battery chemistries are typically optimized for operation in a particular role. For example, Uninterruptible Power Systems (UPSs) will not frequently be exercised but will be expected to output full load power for variable durations. Solar storage batteries will on the other hand undergo one full cycle per day. It seems that this is a high cycle operation (again, pending site-specific details) and cycles can be increased in one of two ways. The first is choosing Li-Ion, which is naturally one of the most capable chemistries in withstanding frequent cycling (see Figure 46). The second way is to install a large quantity of cheap batteries and exercise less of their capacity. The metric for this is Depth of Discharge % (DoD %), which is the percentage of charge (Amp-hour) capacity actually used during a cycle. This number can be reduced by installing multiple strings in parallel or by automatically switching between banks when the bank is considered depleted. All battery technologies benefit from lower discharge, as can be seen in Figure 46 for the case of the Li-Ion battery.

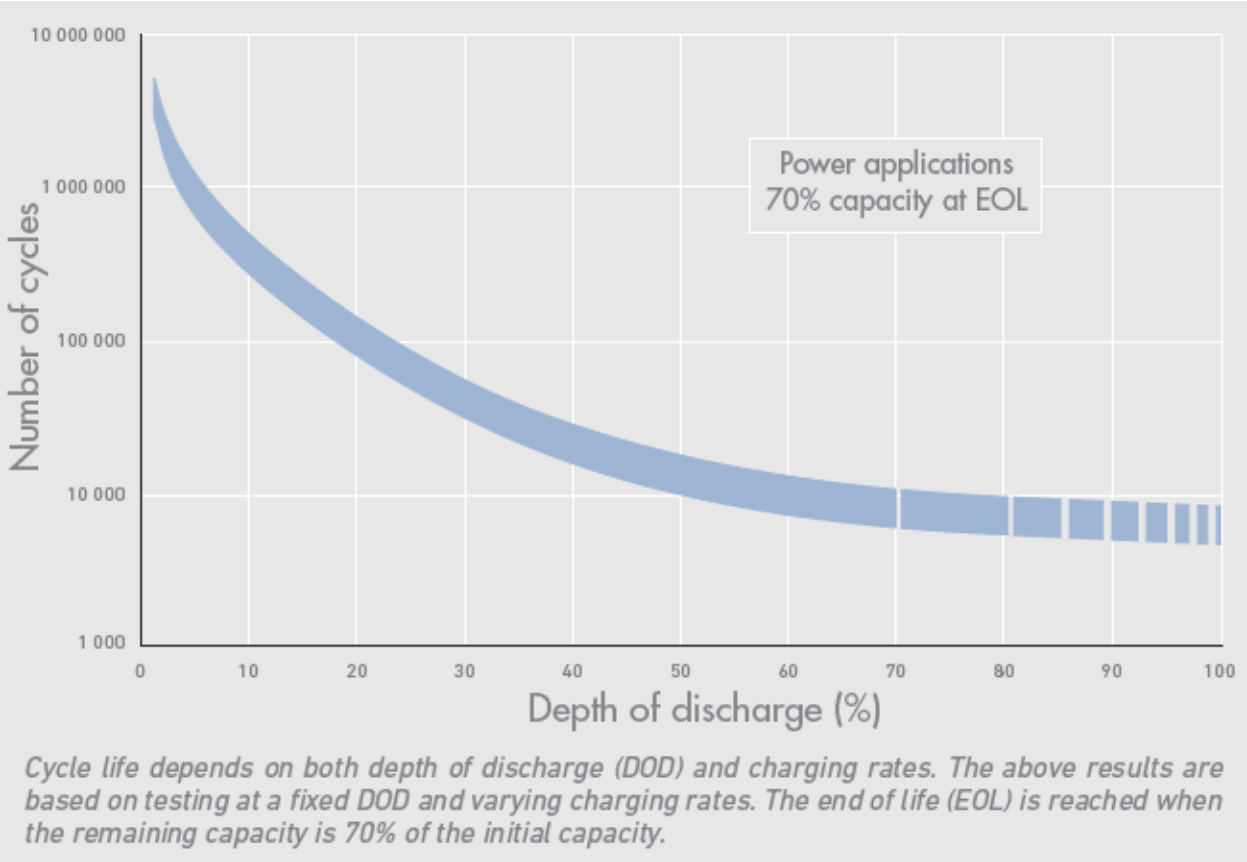

FIGURE 46: SAFT SYNERION 24V/2KWH MODULE LIFETIME

All of the battery technologies discussed can be charged and discharged using the same basic topology, which is a PWM buck-boost converter. While the power electronics of the HVDC converter are sized for 500kW, the present design incorporates the 100kW GTI for interfacing the energy storage component.

One system-wide scenario has a 100kW source which may provide 50kW to the load and 50kW to recharge the batteries during peak production. Another system scenario might have multiple sources interfaced to a common DC bus, to utilize the power capacity of the 500kW converter without re-design – leading to AC input of 1MW peak and battery storage of 500kW peak to serve the 500kW load. But both of these scenarios assume that the project would prefer 50kW or 500kW of power constantly.

A compromise can be made that the resource switches between guaranteed production and variable production. In the guaranteed production mode, the batteries are constantly discharged while in the variable production mode the batteries are constantly charged. In this way, lead acid batteries can be used efficiently because a full charge cycle (see Figure 48) is guaranteed at the expense of variable power to the load. (The converse however is not true. While a full discharge cycle potentially does not make use of excess available power to allow recharge, and thus discharge the most capacity during the next low production period, the charge delivered over the system lifetime is still maximized by taking care of the batteries.)

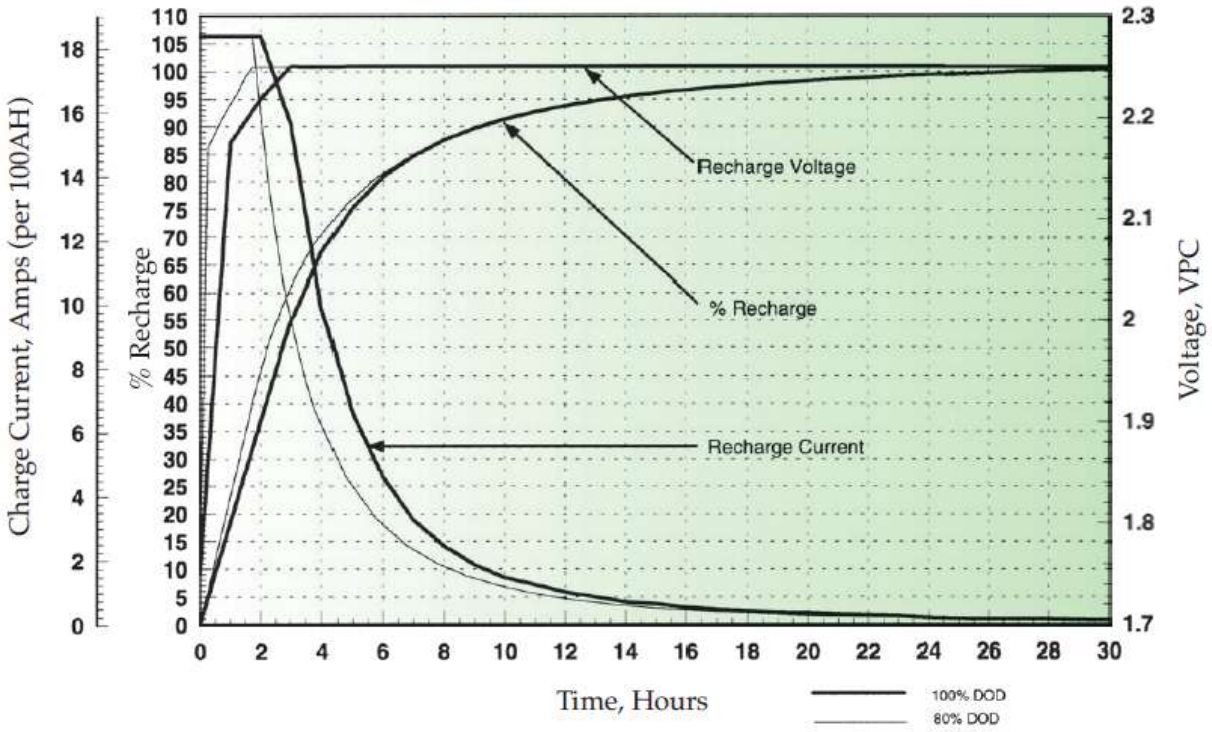

FIGURE 47: CHARGING TIME PROFILE OF ABSOLYTE GP90 LEAD ACID BATTERY

For the power electronics design, therefore, we were satisfied that the 100kW rating of the GTI was sufficient for demonstration purposes. The HVDC low voltage enclosure does, however, have enough spare room for a 500kW bridge to be installed should the decision be made to upgrade the power level of the battery storage.

The consideration was made for using ultra-capacitors. They could be deployed either in place of a battery interfaced by the DC port, or directly connected to the DC bus. They are fundamentally like a capacitor, which means energy is stored via the electrostatic field between separated charges, as opposed to a battery which delivers power via chemical reactions. Thus, as opposed to the complicated charge profile in Figure 47, the profile is that of a capacitors exponential charge and discharge curves of voltage and current.

Ultra-capacitors store a large amount of charge, but at very low voltages. The charge stored in the capacitor is given by Q=CV, and so the useful capacity is given by the maximum and minimum voltage value. Also, each capacitor is rated for about 2.7V, and given sufficient derating, at least 2V. This means that many must be stacked in series, dividing the capacitance by the number in series, and thus making them appear more like a normal capacitor and less like an ultra-capacitor. The ultra-capacitor does also not handle ripple current very well, and hence it must have both voltage sharing devices and also capacitors to handle ripple current.

Based upon the observations above, it would not be particularly useful to use an ultra-capacitor directly on the DC bus. The electrolytic-based bus capacitance would have to be kept, to handle the ripple current of the pulse by pulse operation. The bus voltage range would determine the effective capacity, which might be in the range of 700-8000VDC. The bus voltage would also directly determine the HVDC converter output voltage, which if varied, would have to be

synchronized with other converters on the grid.

The other approach is to use the ultra-capacitor as a replacement battery. This is better, because a much wider voltage swing can be tolerated, so delivering more useful energy. The range might be 500V down to 25V, and with charge cycles numbering hundreds of thousands, energy can be delivered within a second of the renewable resource ceasing production. The design is also better in not having to tolerate high ripple current.

To summarize then, a standard design exists in 100kW form and can easily be scaled to 500kW. The benefit of a DC port is clear whether using ultra-capacitors, Li-Ion or lead acid. The particular details of the quantity of batteries is a site-specific question, with lead acid being the cheapest, Li-Ion probably being the best with today's pricing, and ultra-capacitors the best should the premium for maintenance and power availability be justifiable.

4.2 Battery Design

The battery is designed to meet the following specifications:

- 100kW peak power
- 1 hour capacity
- At least 1000 cycles

This represents a minimum.

4.3 Controls Design

The battery port low-level controls are designed and effectively implemented (and well tested) at the 100kW power level, being already included in the GTI product. The control is a standard PWM buck-boost converter, which operates a single phase bridge at 6 kHz. The control scheme as far as system operation (power flow) is concerned is described in detail in Section 5.3 Software Functionality.

Chapter 5: **Task 4: Final Software Design of Prototype System**

5.1 Overview of progress

The system software has been designed, and evaluated and is functionally correct, using the split control system of the GTI and HVDC control systems. This work was complete as of May 2012. The software needs to be integrated into a single system, which poses little technical risk. The GTI product's control system uses and older generation of control system, while the HVDC converter uses the current generation.

5.2 System Operation

The software control is currently run using two separate control systems which would be integrated in the future. One control system serves to control the AC input and bidirectional DC port, including regulating HVDC output voltage while the other much simpler system is simply controlling the switching action of the H-bridge.

A variable voltage, variable power AC source is connected to the AC port. A DC source, being either a battery or ultra-capacitor, is attached to the LV DC port. The power from both sources is combined into a central DC bus, which provides power to an H-bridge. The H-bridge makes a single phase square wave voltage output, connected to a resonant capacitor in series with the transformer primary terminals. The 16 transformer secondary windings, each with a 3.9:1 step up ratio, have their high voltage AC output rectified and then stacked in series to generate a 50kV HVDC output.

The main software interface uses a Java applet "Web UI" accessible from a standard browser over Ethernet. The H-Bridge control software, for now, uses a serial RS-232 based packet over USB and accessed using a terminal application. It would eventually be combined into the Web UI.

The principle of the control software is to regulate the central DC bus voltage. In doing so, the voltage that the H-Bridge switches gets applied to the transformer and stepped up accordingly. Hence, control of the central bus voltage is controlled over the HV output.

To operate, the HV output must be slowly raised to control inrush current from the HV capacitance (both capacitor components and stray capacitance). To do so presently requires an external pre-charge mechanism, although the ground work has been performed for a novel switching algorithm (called "inversion") which allows the current to be regulated by the H-Bridge.

The slow pre-charge ramp rate presents a technical challenge for the design of the external pre-charge mechanism. Usually, pre-charge is into an unloaded capacitor so that the only energy that must be dissipated by the circuit is the loss in transferring the capacitor's storage energy. However, in our system currently the load is hard wired to the output terminals, which means that the pre-charge must constantly dissipate that much power. In the present 50kV/50kW system, we are fortunate to have a variac which can slowly raise the input voltage to the bus.

It would be possible, in a network of HV converters, to pre-charge by having all other converters not transfer power while the first power source is brought up to voltage, and it would also be possible, although challenging for the system controller, to allow a switch that applies the load after pre-charge. Both options were considered, although the novel inversion algorithm solution

is far superior. Discussed in detail later, it effectively limits the power transferred per switching pulse so that finite, controlled inrush currents are applied to the HV load (of any impedance), and consequently the voltage rise is also controlled.

When operating, the available AC power is assumed to be uncontrolled, such as a renewable resource might be. To simulate limitations in available power, the AC port has a current limit applied independently. The system power control algorithm then takes the available AC power from the AC port and then calculates the required DC output, such that central bus voltage remains stable. This control is implemented using a PI loop on the central voltage, so that the proportional term takes care of small power fluctuations immediately while the integral term offsets the average power output. The integral gain is much smaller than the proportional gain.

The system must also charge the batteries as well as discharge them. Here a decision must be taken further down the road as to whether a 50 kW AC source is to be used or one greater than 50 (the hardware used here would support up to 100kW). Should the maximum 50kW output be required the whole time, a source larger than 50kW would enable the battery to be charged while providing maximum power; otherwise using a 50kW source would require power output to be reduced while the battery is recharged.

To recharge the batteries, the DC port has its own 3 stage charge control algorithm. The algorithm is designed for recharging lead acid batteries, although appropriate for many other chemistries and ultra-capacitors. The profile is defined by a bulk charging voltage, a float charging voltage and a current limit. The first stage, as a current limited voltage source, usually applies the maximum current allowed to charge the batteries up to bulk voltage. The second stage, when that voltage is reached, continues to provide current as needed. The battery draws less current as it becomes more charged, and there is a threshold current from which the voltage is lowered from the bulk voltage to the float voltage. At the new voltage, less current is drawn and continues to decline until a “battery charged” current threshold is reached. The port then switches off, or discharges power again, as determined by the system condition.

A phenomenon known as micro-cycling can occur if the batteries are not fully charged before being required to be discharged again. This can usually be mitigated at a system level by allowing the batteries to be charged on a schedule if a grid connection is present, or by ensuring that when the batteries have started charging, all power is routed to them rather than to the HVDC load. In the present software this action is performed by manually setting the power limits on the battery port to allow zero discharge while charging, but in future it would be mitigated by the inversion algorithm as power to the DC bus would be limited. It would then rely on the HVDC grid controller to either allow the grid voltage to sag or reduce power at the consumption end accordingly to deal with the power output “lost” to battery charging.

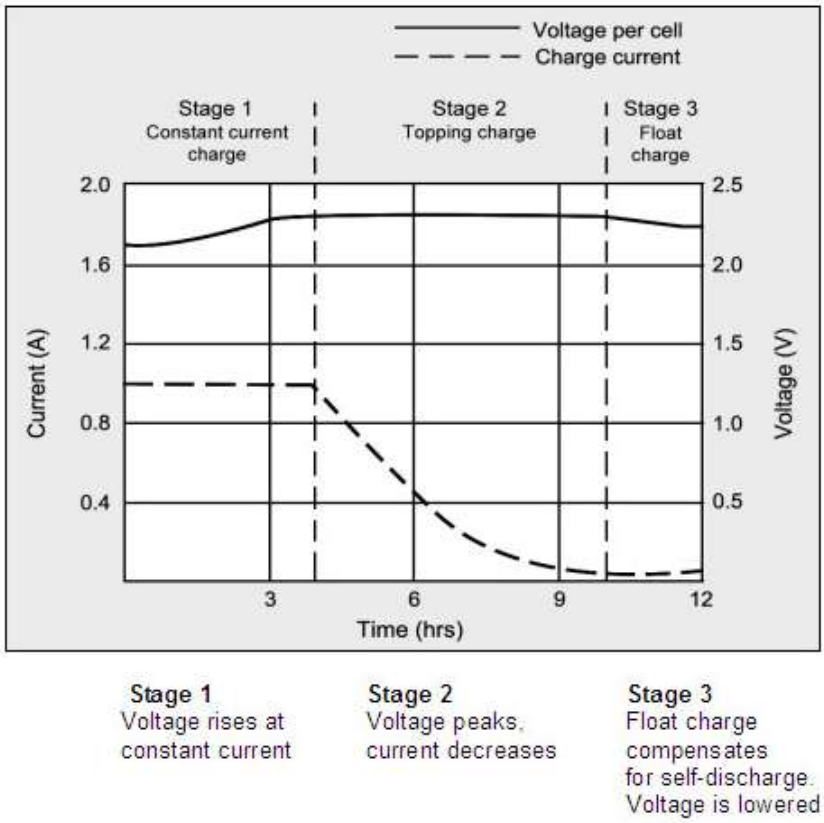

FIGURE 48: BATTERY CHARGING PROFILE

If ultra-capacitors are used, this problem of micro-cycling is mitigated as their lifetime spans 100k+ cycles. This is especially desirable in applications such as MHK where the maintenance of an offshore generator is relatively expensive, especially if new batteries have to be shipped out. The technical design question for using ultra-capacitors over a battery is whether they should be incorporated into the main DC bus or managed on a separate port such as the system we have used so far. Having a DC port allows their power to be controlled, and also as the ultra-capacitor discharges, their voltage decrease to be compensated for.

If ultra-capacitors are placed on the DC bus there is a huge decrease in system response time to step changes in bus power – the charge they hold is so much that the resonant section will never be able to switch that much charge in a single pulse. They are also relatively safe. One risk associated with large capacitors, a large internal fault current, would only occur if the DC bus bars were directly shorted. This behavior, coupled with their low ESR power dissipation due to ripple current and their ability to handle overvoltage means that they are quite suitable for direct placement on the DC bus. The one disadvantage is a penalty in response time to bus voltage change, should the user desire to change the transmission voltage, which would be on the order of tens of seconds rather than milliseconds.

For this project, PPS decided that ultra-capacitors would not be necessary to prove the concept of energy storage and instead chose a traditional lead acid battery configuration for testing. A packaged ultra-capacitor would easily be integrated in the future using the battery port, since it

would look very similar to a lithium-ion battery with an external battery management system (which PPS regularly interface to the GTI).

5.3 Software Functionality

The system consists of three ports: a variable input AC port (0-528V) an energy storage port (500VDC nominal) and a HVDC output port (up to 50kV).

The purpose of the system is to ensure a constant DC output on the HVDC port, assumed to be connected to a grid of similar converters, all of which source onto a shore based power station that converts the HVDC back to utility power.

The variable input AC is not assumed to be constant in power, voltage or frequency, coming from some generalized renewable resource. To ensure that constant voltage is maintained on the HVDC grid, energy storage is incorporated to allow the converter to ride through periods of low power production and to store excess generated power.

To keep the HVDC output constant, the low voltage DC bus voltage must be kept constant. To maximize utility to the user, all available AC power is to be used. Should the power be greater than the user's load, the excess power will be stored in the battery. Should the available power be less than the load, the battery will be discharged to provide the additional power.

The power behavior can be modeled as:

- The AC port will draw power from the source and convert it to a current source which feeds into the DC bus at DC bus voltage.
- The battery port can likewise act as a current source or sink at the DC bus voltage to draw power. The battery port power is controlled such that just the right amount of current is sourced /sunk to maintain the DC bus voltage.
- The HVDC port does not have adaptive control; it generates the voltage "blindly", and so relies upon the correct DC bus voltage for the HVDC output.

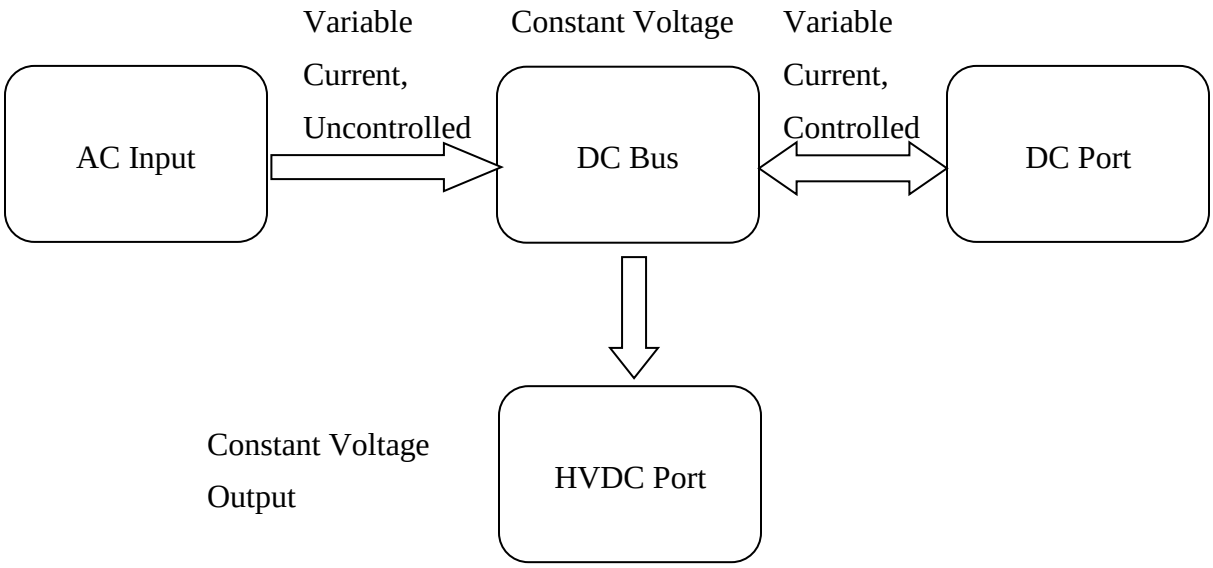

FIGURE 49: POWER FLOW IN SYSTEM

5.4 Software Architecture

The software design, overall, consists of the following modules:

- Grid power module.
  - Controls a 3 phase PWM bridge interfaced to the central DC bus
  - Detects 3 phase voltages and line currents and conditions the signals for good control.
  - It is responsible for:
    - Synchronizing with the input AC
    - Switching so as to draw power with a defined power factor.
    - Announcing the current it is pushing on to the DC bus to the system supervisor
  - It will trip the system offline if it detects:
    - Abnormal current, voltage or voltage frequency
    - An open phase
- Bus power module.
  - Detects the bus voltage and conditions the signal for good control.
  - It is responsible for:
    - Calculating the necessary bus voltage for the HV power module to transmit at 50kV or the user specified transmission voltage.
    - Regulating the central DC bus voltage
    - Using the input current from the grid module to specify whether the battery should charge or discharge, and by how much, to ensure that the bus voltage is constant.
    - Limiting the power flow to user-specified limits if necessary.

- Battery power module.
  - Controls a single phase buck-boost PWM converter interfaced to the central DC bus
  - Detects and the battery voltage and current and conditions the signals for good control.
  - It is responsible for:
    - Calculating and implementing a switching pattern so as to maintain the battery voltage when charging. It has a buck-boost topology
    - Calculating and implementing a switching pattern so as to draw the required power when discharging.
  - It will trip the system offline if it detects:
    - abnormal current or battery voltage
    - reversed battery polarity

- HV power module.
  - Controls an H-Bridge, which applies a high frequency square wave voltage across the HV Transformer at the DC bus voltage, in series with a capacitor.
  - The overall effect of the capacitor and leakage inductance of the transformer is to create a resonant circuit.
  - The HV transformer transforms the resulting current pulse to a high voltage on the secondary, where the pulse is rectified and HVDC is generated.
  - In the test the HV module will operate in a fixed manner because:
    - The pulse must be generated with zero DC component (i.e. the H-bridge switches symmetrically) to ensure the Volt-seconds applied to the transformer average zero.
    - The pulse width is fixed to be the time constant of the tank resonant frequency.
    - The input voltage (i.e. that of the central DC bus voltage) directly corresponds to that of the output HVDC voltage.
    - The power output is related to the number of pulses/second.

Chapter 6: **Task 5: Vendor Selection & Procurement Process**

6.1 Cost

The task was successfully completed by August 2011, as was the assembly of the prototype system. The cost of the system was well within the target of $0.50/W at the 500kW power level.

- Project cost on materials was **$164k**/500 kW
- Variable cost for batteries:
  - Lead-Acid battery cost is **$56k**/100kW backup
  - Li-Ion battery cost is **$105k**/100kW backup

6.2 Mean Time Between Failures (MTBF)

6.2.1 MTBF Measurement Standards and Methodology

MTBF stands for Mean Time Between Failures. It is a statistical prediction of the elapsed time between failures of a system during operation. The value of an MTBF study is nearly axiomatic; it provides consumers with an estimated lifetime for the product they are interested in purchasing, within the environment they intend to use it. In utility scale power electronics, MTBF carries increased value, as the estimated lifetime of grid-level systems catalyze many of the business and technical processes of the companies that utilize such systems. Providing accurate estimations of system life will be of great benefit to the manufacturer of those systems and those who intend to use them over their lifespan.

The MTBF studies performed on the HVDC Converter hardware by MTBF consultant, ARA associates, follow the Telcordia SR332 standard. This standard allows the use of the parts count method; a technique that allows for the development of an estimation of the average life of a whole assembly. The fruit of this exercise is the failure rate, denoted FRx (where x is a number). The MTBF is calculated from the failure rate as follows:

$$MTBF = \frac{1000000000\ hours}{FR1 + FR2 + FR3 + FR4 + \cdots \ldots FRn}$$

The failure rates of the individual components are determined either by referencing manufacturer data or, by using the failure rates provided by MIL-HDBK-217, "Military Handbook, Reliability Prediction of Electronic Equipment". The individual failure rates are then summed to provide the net failure rate of the entire unit.

The test results referenced in this report reflect the predicted life under what is known as Ground, Fixed, Controlled G_B π_E=1.0 conditions. Under these conditions, the parts are assumed to experience nearly no environmental stresses with optimum engineering operation and maintenance. The NEMA 3R standard that the HVDC Converter unit is designed to allows for more strenuous operating conditions. But, on the average, the unit will see conditions that are

similar to those assumed in the Ground, Fixed, Controlled G_B π_E=1.0 standard.

6.2.2 Results of the Study

A preliminary study was made that calculated the MTBF as being 3.67 years, 6.34 years below the desired 10 year lifespan. The work to improve this is ongoing, and the life will only be known when the final design has been studied, but the design has already incorporated some printed circuit board component improvements which have led to an increased value of 46,858 hours or 5.34 years.

Chapter 7: **Task 6: Assembly of the Complete Prototype System**

The prototype system for the HVDC generation (LV enclosure and HV tank) was successfully assembled for full testing by August 2011. For the functional tests these components were combined with an existing GTI unit, to form a three port converter with battery and AC port from the GTI as well as an HVDC port.

FIGURE 50: TRANSFORMER TEST FIXTURE BEFORE FINAL ASSEMBLY

Chapter 8: *Task 7 (Part 1): Test Fixture Assembly and Test Software Development*

The task was successfully completed in April 2012. The main success of the task was developing a high voltage testing facility, complete with full automation so that the equipment under test (EUT) was remotely operated and monitored. The task consisted of designing power distribution and loading for the 1MW power level (the full output power of the HVDC converter system, consisting of 2 500MW units) at 480VAC, and an area capable of safely housing 50kV applied to a 50kW resistive load as well as isolated thermal and electrical monitoring of the internal converter voltages. Equipment was also purchased for evaluating both AC and DC dielectric strength to 70kVDC and 100kVAC.

The task report is divided up into the following section (Chapter 8:) to describe the High Voltage Test Laboratory. Section Chapter 9: refers to the test procedure used.

8.1 Layout of HV Lab

The general floor plan of the HV test area is shown in Figure 51, showing the general location for equipment to power EUTs including protective devices like breakers, the available free area for equipment under test, as well as the monitoring and control station (top right corner) adjacent to, but outside of the HV test area.

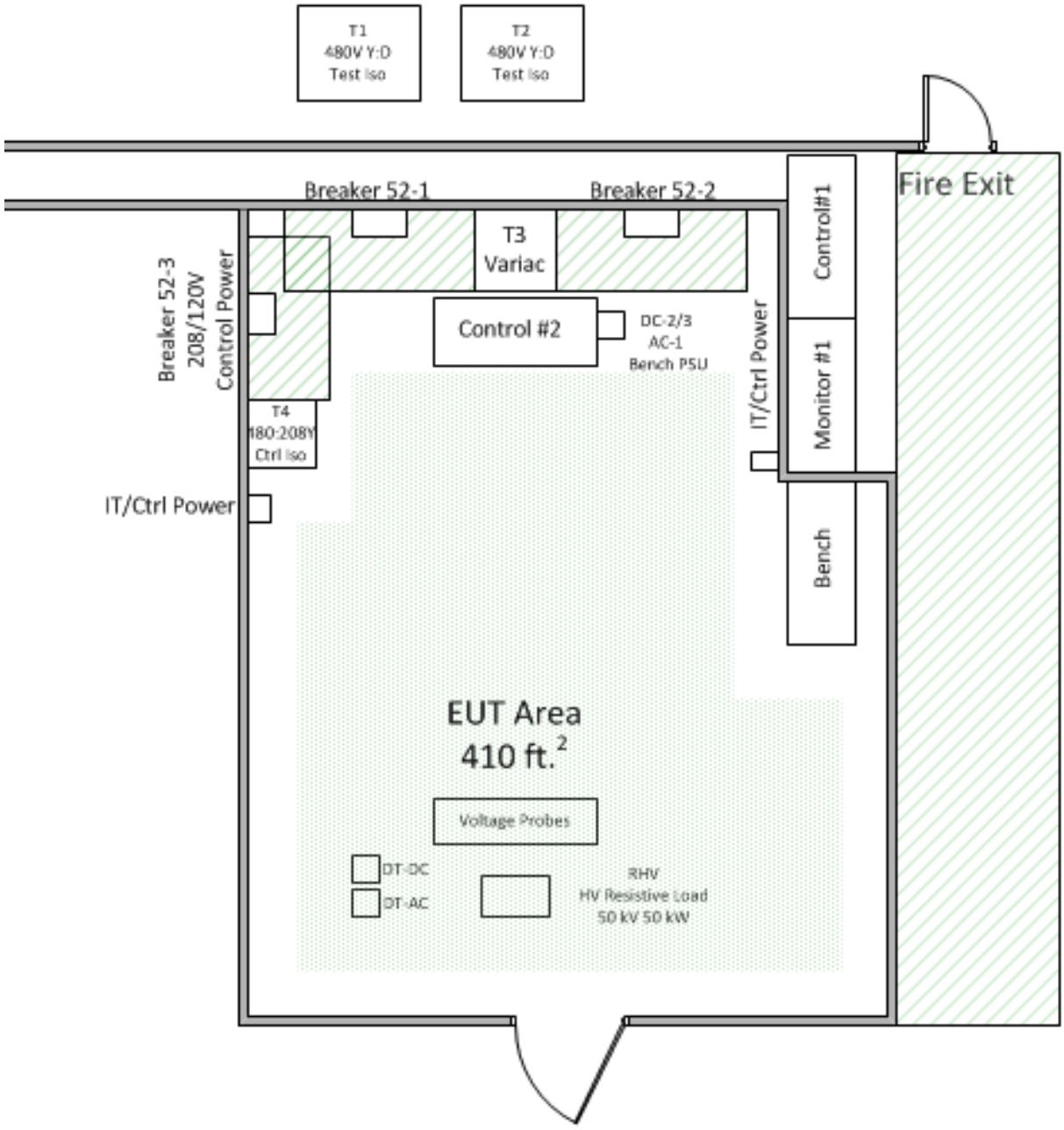

FIGURE 51: PHYSICAL LAYOUT OF LAB, INCLUDING PERMANENT STRUCTURE AND LARGE EQUIPMENT

8.2 Equipment

The following equipment is available to the HV Lab to deliver power to and from the Equipment Under Test (EUT).

8.2.1 Power Sources

The main AC power into the lab consists of:

- 800A 480V service from bus duct
- 2x Programmable 1200A breaker assemblies, each with
  - Schweitzer Electric SEL751 Feeder Protection Relay with advanced monitoring options
    - 10kV withstand 480:120V Potential Transformers
    - Square D CT 1200:5A 74 74-122 600V Current Transformers
  - ABB - MC Switch (KT7MXLDO) with the following options
    - Padlock provision open kit, (KT7MXC6)
    - 110-120V AC/DC closing coil , (KT7XAS2)
    - (2) Form C aux contacts (400VAC) (KT7XS6)
    - Spring charging motor (KT7MXM5)
    - Shunt Trip

In addition there are a number of current/voltage controlled power sources:

- 1000V/1200A DC Power supply (located outside building)
- 2x 6 kVA 0-300V L-N 3 Phase AC Power supply. Variable frequency from 30Hz -5kHz
- 1000V/10A DC Power supply

In addition the following equipment can be connected to the breaker assembly. It has no additional protection, and so the current/voltage controlled sources should be used first to confirm correct operation at low voltage before these are used.

- 6 kV/40A rectifier (requires 480:4160V transformer).
- Variable Transformer:
  - 480VAC Three Phase Wye 60 Hz Input;
  - 0-480VAC L to L or 0-560VAC L to L Output (depending on wiring)
  - 105 Amps Maximum.
  - Motorized version with 120V 60Hz Motor; 60 Second motor travel time (stop to stop).

Item	Characteristics	Manufacturer	Model	Qty.	Schematic Identifier
Feeder Protection Relay	*Programmable trip, voltage deviation*	*Schweitzer*	*SEL 751A 01ABD0X73850300*	*2*	*52-1, 52-2*
Main breakers	*1200A 600V*	*ABB*	*T Max T7 T7MH0B30D000000XX*	*2*	*52-1, 52-2*
Isolation transformer	*480:480 Y:D, 500kVA*	*Hammond*		*2*	*T1,T2*
AC Power Supply	*6 kVA, 45 Hz-5kHz, 0-300V_{L-N}*	*Pacific Power Source*	*AMX-T320*	*2*	*AC-1,AC-2*
DC Power Supply	*1000V/1000A*	*Darrah*		*1*	*DC-1*
DC Power Supply	*1000V/10A*	*Magnapower*			*DC-2*
Variac	*105A, 0-560V, motorized*	*Staco*	*60M6020-9Y*	*1*	*T3*
HV Transformer	*480:4160 Y:D*	*Hammond*		*1*	*T4*
Rectifier	*12kV_{PRR}, 40A*	*HV Component Associates*	*3PHfwb40a12kv*	*1*	*D1*

TABLE 3: POWER SOURCING AND DISTRIBUTION EQUIPMENT

8.2.2 Power Loads

The following are 480V loadbanks (located outside building):

- 962 kVAR/ 1 MVA inductive loadbank with continuous resolution.
- 2 x 500 kVAR capacitive loadbanks with 5 kVAR resolution and automatic PFC correction. (64”H x 47”W x 32”D). Steps 5, 10,15,20, 25,30,30,40,50,60,70,75,100 kVAR.
- 700 kW resistive loadbank with 5 kW resolution
- All loads run into a distribution box in the main lab wall (not HV lab) so that everyone has access to them. They are in elevated raceway from outside to avoid the risk of flooding from groundwater. Other testbays also have access to these loads – they are a shared resource.
- Connections into the distribution box use camloks, to enable one EUT output connection from the Lab to be applied to multiple loads.

There are also DC resistive loads:

- 50 kW/ 50 kW Resistive load (80 x 625Ω). Stainless steel wire, wound around a ceramic core element mounted on glastic end frames separated by 15kV insulators and mounted on 69KV base insulators (69"H x 50"W x 24"D).
- 64x 5.5kW/240V Water load (configurable immersion heating elements) mounted on a

glastic base, and immersed in a water tank with flow control. Outdoor rated.

Item	Characteristics	Manufacturer	Model	Qty.	Schematic Identifier
Resistive Loadbank	*700kW*	*Avtron*		*1*	R_{LOAD}
Inductive Loadbank	*937.5 KVAR at 480 Volts AC, 3 Phase, 60 Hertz, 1127 Amps per Phase, continuously variable*	*Avtron*	*K841B Outdoor*	*1*	L_{LOAD}
Capacitive Loadbank	*500kVA*	*Arteche PQ*		*2*	C_{LOAD}
HV Resistive Loadbank	*80 x 625Ω* *50KV DC, 50KW +-10% @20C, , 1A, continuous duty,*	*Telma & Berger*	*n/a*	*1*	R_{HV}
Water Load	*64x 5500W/240V rated*	*PPS*	*n/a*	*1*	R_{WATER}

TABLE 4: POWER LOADING EQUIPMENT

8.2.3 Test Measurement Equipment

The following are dedicated pieces of equipment:

Item	Characteristics	Manufacturer	Model	Qty.	Schematic Identifier
Dielectric Tester	*100 kV AC/100 mA*	*Hipotronics*	*100HVT*	*1*	*DT-AC*
Dielectric Tester	120V 50/60Hz 10A input, 0-80KV output	*Hipotronics*	880PL-10mA-A	*1*	*DT-DC*
Temperature Logger	*8 Channels*	*Neoptix*	*OmniSense*	*1*	*Temp 1*
Temperature Probe	*Oil-compatible, 100kV*	*Neoptix*	*T2*	*8*	*TS1-8*
HV Voltage Probe	*60 kV, 50 kHz BW*	*North Star*	*VD-60*	*4*	*HVP 1-4*
Oscilloscope	*100 MHz, 2GS/s*	*Agilent*	*6014*	*3*	*Scope 1-3*

TABLE 5: TABLE OF HV-SPECIFIC TEST EQUIPMENT

The following are not exclusively allocated to the HV Lab, but demonstrate typically available equipment that is likely to also be used:

Item	Characteristics	Manufacturer	Model	Qty.	Schematic Identifier
Resonant Current Probe	*50 kHz BW*	*Pearson*	*1330*	*2*	*A8-9*
Differential Voltage Probe	*±7 kV*	*Probe Master*	*4243A*	*2*	*DV 1-2*
Power Meter	*VT and CT scaling*	*Yokogawa*	*WT3000*	*2*	*PQA 1-2*
DC Current Probe	*DC-50 kHz BW*	*Danfysik*	*866R Ultrastab*	*4*	*A4-A7*
AC Current Probe	*1000 A /60 Hz / 600 V*	*AEMC*	*SR1000*	*3*	*A1-A3*
Logic Analyzer	*With 2 Mictor header cables, for debugging only*	*Tektronix*	*TLA612/614*	*1*	*LA*

TABLE 6: TABLE OF AVAILABLE LV TEST EQUIPMENT

8.3 Test Control

This section briefly describes the equipment to safely control and power Devices under Test in the HV test cell.

8.3.1 Control Power

In the testbay:

- 45kVA 208V/120V Isolation transformer
- 120V/20A non-isolated connection for benchtop equipment

In the control room

- 120V/20A non-isolated connection for benchtop equipment

8.3.2 Switchgear Control

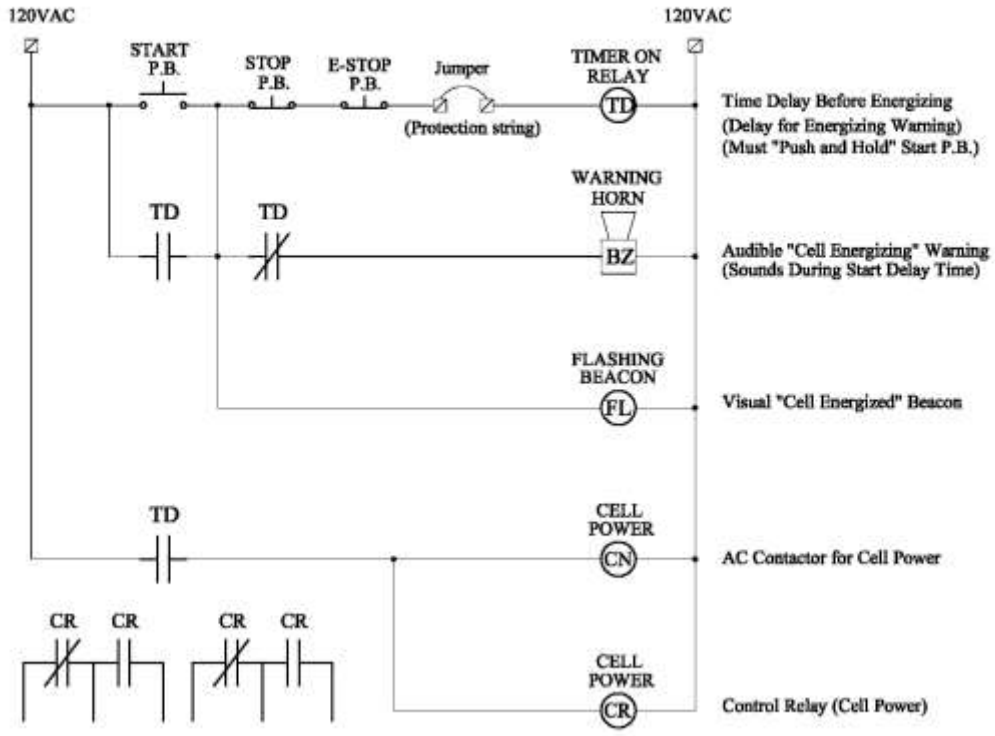

FIGURE 52: START/STOP AND E-STOP CONTROL SCHEME (PPS STANDARD).
NOTE THAT CN SWITCHES IN101 OF THE SCHWEITZER RELAY, AND CR IS NOT USED.

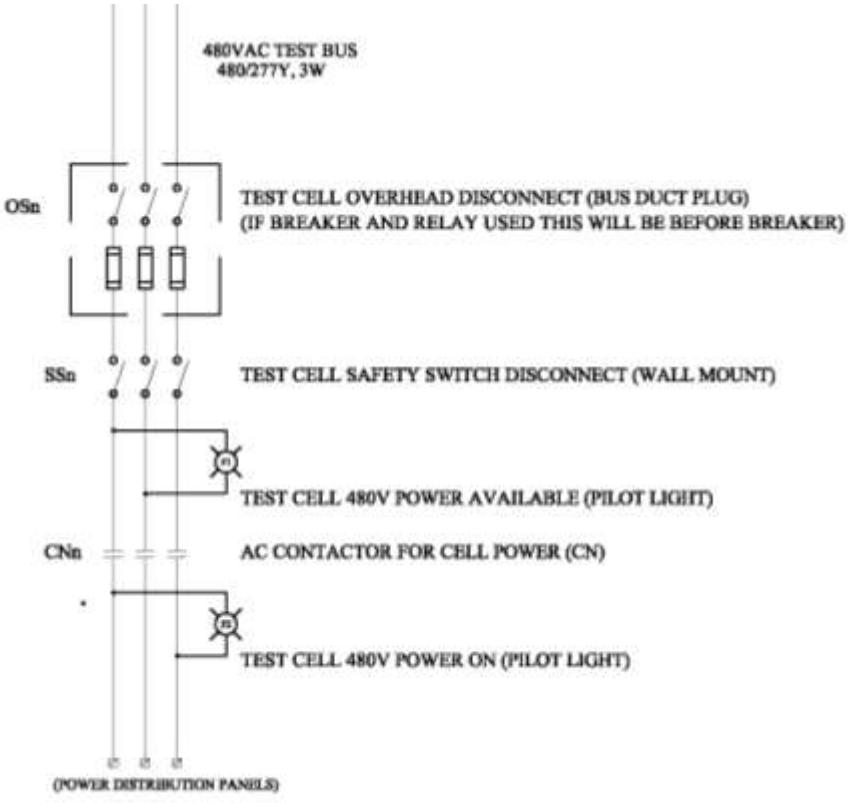

FIGURE 53: UPSTREAM POWER INDICATION (PPS STANDARD).

NOTE THAT THERE ARE TWO POWER AVAILABLE PILOT LIGHTS, ONE FOR 52-1 AND ONE FOR 52-2. THE POWER ON LIGHT IS A STROBE LIGHT MOUNTED ON THE TOP, CENTER, FRONT UNISTRUT SUPPORT. THE CONTACTOR CN IS THE ABB BREAKER CONTROLLED BY THE SCHWEITZER FEEDER PROTECTION RELAY.

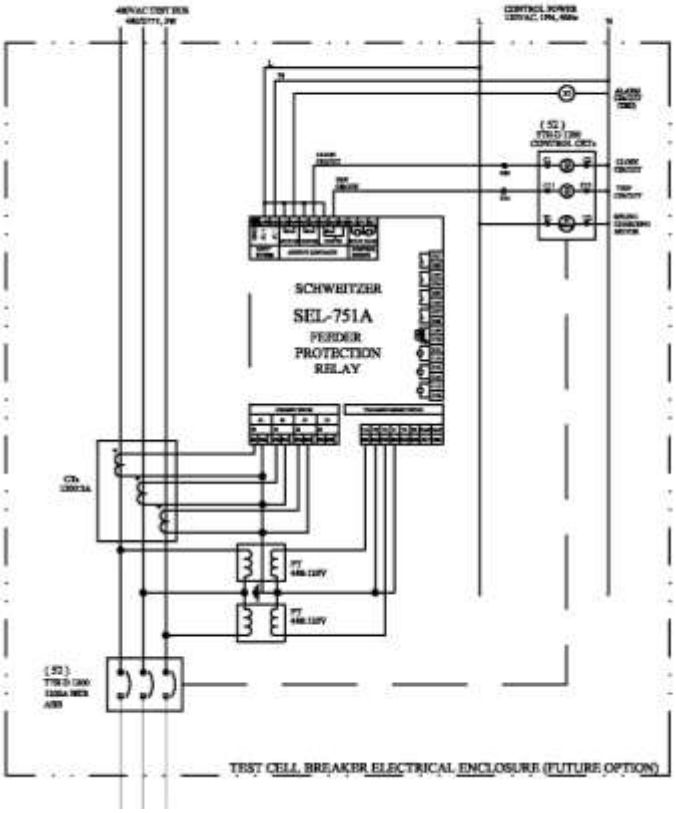

FIGURE 54: SCHWEITZER RELAY CONNECTION DIAGRAM.
THE RELAY IS RESPONSIBLE FOR ENERGIZING AND DE-ENERGIZING THE HV TEST LAB.

8.3.3 Communications Network

The connection between the test equipment and the control room uses isolated fiber optic link between 2x24 port Ethernet switches.

In the control room are two computers:

- One PC for controlling the EUT(s)
- One test control PC with Labview installed for test monitoring and control

In the testbay there are

- One PC for controlling the EUT(s) which is controlled by that in the control room
- Serial to Ethernet server
- GPIB server for collecting data from test equipment using GPIB interface

Table 7 lists the available equipment to provide control and networking of the HV test cell, with the IP addresses for the equipment listed in Table 8. Figure 55 shows a schematic overview of how the test cell equipment is connected.

Item	Characteristics	Manufacturer	Model	Qty.	Schematic Identifier
Fiber Optic Cable	*LC multi-mode (M-M cable, 49 ft, 50 / 125 micron*	*HP*	*AJ837A*	*1*	*n/a*
Fiber Transceiver	*1000BASE-SX SFP Mini GBIC slot*	*Netgear*	*AGM731F*	*2*	*ES1, ES2*
Ethernet switch	*24 Port, Managed*	*Netgear*	*GS724T-300NAS*	*2*	*ES1, ES2*
GPIB LAN Server	*32 Channel*	*National Instruments*	*GPIB-ENET/100*	*1*	*GPIB*
Serial Server	*2 Channel, RS-232/422/485 capable*	*B&B Electronics*	*ESP412*	*2*	*Serial #1, Serial#2*
PC		*Dell*	*Vosotro 260*	*3*	*Control #1, Control #2, Monitoring #1*

TABLE 7: TABLE OF AVAILABLE CONTROL AND NETWORKING TEST EQUIPMENT

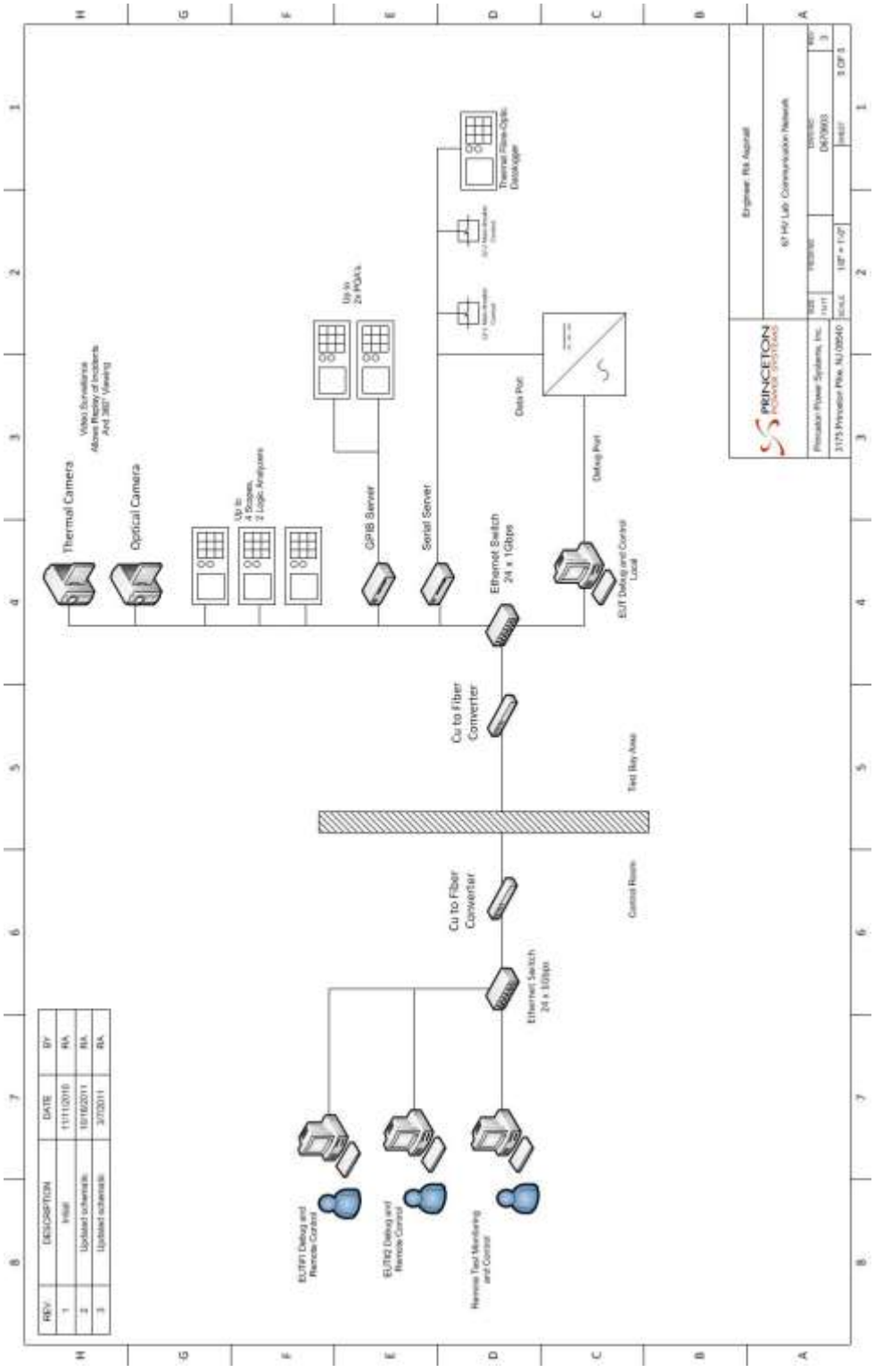

FIGURE 55: TESTBAY COMMUNICATIONS SCHEMATIC

8.3.4 IP Address Table

The IP addresses are to be fixed, and have a block of 20 devices allocated for usage. This will allow a small class C subnet to be made for the entire lab, which should speed up communications by reducing path length. The addresses below begin with 192.168.201.xxx. The block 32-39 is for roving devices (such as scopes and other equipment which will be shared with other projects). The block 40-50 is for fixed equipment which will never change.

Item	Characteristics
40	Breaker 52-1
41	Breaker 52-2
42	PC-1
43	PC-2
44	PC-3
45	PC-4 (if used)
46	GPIB
47	Serial 1
48	Serial 2
49	Spare
50	Spare

TABLE 8: IP ADDRESS ALLOCATION

8.4 Electrical Installation Requirements

All wiring should conform to the NEC unless special exception is made for temporary wiring. Deviations should be recorded. The NESC should also be used when above 600V working voltage. Below are some known requirements for the lab.

8.4.1 HV Wiring

(Article 310.10 E) For permanent installation the following is required (but also good practice)

- Solid dielectric insulated conductors operated above 2 kV shall have ozone-resistant insulation and shall be shielded. All metallic insulation shields shall be connected to [ground].

(Table 310.106(A), Minimum conductor size)

8.4.2 600V Main Power Wiring

(Article 310.10 H, for 1/0 cable and larger. The design specifies 3/0)

- Parallel conductors run in the same raceway need to have the same length, termination type, AWG, conductor material.

(Article 310.15, general notes to tabulated ampacities)

- An ambient temperature correction factor may be applied. I assume that the lab space will be at ambient temperature. 50°C would be the worst case in a climate controlled environment (when the environmental chamber is being used).
- For more than 3 conductors in a raceway, a correction factor may be applied:
    - 4-6: 80% derating
    - 7-9: 70% derating
    - 10-20: 50% derating

A distinction should be made between temporary wiring and permanent wiring.

Permanent wiring:

- From the 400A disconnect to the breaker panels for main power
- From the load distribution panel to the loads
- From the 208V source to the 208V isolation transformer
- From the 208V isolation transformer to the 208V distribution panel

Temporary wiring

- From the main power breaker panels to the EUT, with all variac, transformer and other wiring.
- From the EUT output to the load distribution panel

8.4.3 Distribution Panels

(Article 110.26, ≤ 600V) The following panels should have 30" clearance between adjacent equipment either side, and 3' clearance in front:

- 52-1 Testbay 480V Main Power #1 Panel
- 52-2 Testbay 480V Main Power #2 Panel
- 52-3 Testbay 208/120V Control Power #1 Panel

8.5 Safety Requirements

8.5.1 Clearance

- 6' high fence to keep personnel out of area. 40'x 28' area with 2x 4' wide gates. Based on ~36kV Phase-Phase voltage (50 kV DC)
    - Clearance distances are defined in NFPA 70E Article 130 (10' around hazard for "unrestricted access" down to 2'2" as a no-go zone.
    - Clearance distances are also defined in ANSI C2, the NESC, Table 124.1:
        - 9'6" vertical clearance
        - 4' horizontal clearance of unguarded parts
        - 1' clearance guard of live parts
        - It also states a 200kV BIL level.

8.5.2 Containment

- Polycarbonate shield inside fence reduces noise and contains any debris from catastrophic failure.
- Well-grounded fence keeps personnel clear of area. Serves "to contain" electrical voltage and ionized air.

8.5.3 Indication

- High-visibility red strobe continuously lit from across the 480V input line
- HV warning signs around perimeter stating "Danger! High Voltage".
- Delayed closure of circuit breaker from pressing of "Start" button with warning siren.

8.5.4 De-Energization

- E-stop network which trips main power
    - Keyed door interlock on entrance gates
    - Pull-cord around perimeter fence
    - Dedicated E-stops located at each test control bench and near the gate.

8.5.5 Oil Provisions

- Most insulating mineral oil has a high ignition temperature and low flammability. The main hazard posed by insulating oil is spillage. The location of the 55 Gallon oil cleanup kit is recorded on the door to the lab.
- Drums of oil should not be kept in the lab. The only oil should be that of the EUT.
- MSDS should be kept with other MSDS' and OSHA documents.

8.5.6 Personal Protective Equipment

- While in the Lab, all personnel should wear protective footwear with EH testing to ASTM or CUL standards ("Omega mark")
- Re-entry procedure will require grounding all surfaces with a discharge stick. The operator should be trained, and wear HV gloves while holding the stick. Standard eye and hearing protection should also be used, as discharging high voltage with a grounding stick will flash.
- Hearing protection should be worn when operating noise is present, regardless of whether originating from inside or outside the lab.

8.5.7 Fire Provisions

- The fire provisions are subject to that of the whole building, including sprinkler systems and fire extinguishers.
- The nearest fire exit is immediately to the right of the control operating station (less than 10').
- Note that oil and electrical hazards are present in the lab, and so if a hand extinguisher is used, it should be of the appropriate type. Lab entry procedure should still be followed as after de-energization the electrical hazard of built up surface charge may exist.
- On the whole it would be much safer to de-energize the main bus's disconnect, activate the fire alarm, and exit the building than to try to contain a fire.

8.5.8 Operating Procedure

- The operating procedure is a separate document and is subject to document control. It should be posted on the door to the lab and also near each control station.

8.5.9 Protection Co-Ordination

The Schweitzer SEL-751 requires programming to operate effectively as a breaker. Before each project is installed, the protection requirements must be coordinated with the facility.

- The duct busway from which the power is derived is 1000A rated.
- The facility available short circuit current is 30 kA

A small number of people should be trained as per the restricted operation & maintenance procedure to fulfill the role of programming the limits of the breaker. While there are many quantities that the breaker is able to detect and trip in response to, the following trips must always be set:

- E-Stop control signal
- 50PnP Phase instantaneous Over Current
- 51AP Phase Time Over Current

8.6 Cooling & Environmental Provisions

- High power loads and transformers located outside to minimize excess heating
- Intended to remove an anticipated 100kW maximum loss heat from units (1MW EUT, 10 % losses).
- Thermal chamber can be constructed (if needed in future) around EUT to create thermally controlled environment
    - Roof of chamber traps heat, mounted 9’ above floor.
    - Walls of chamber are the 8’ polycarbonate shields.
    - Fans are then used to deliver required cooling by blowing air out of space between 7’ polycarbonate shields and chamber roof.
    - Effective (approx.) for 25°C to 50°C ambient temperature control.

Chapter 9: **Task 7 (Part 2): Develop Test Procedure**

9.1 Test Program Overview

This procedure refers specifically to system testing. The system configuration block diagram is shown below in Figure 56.

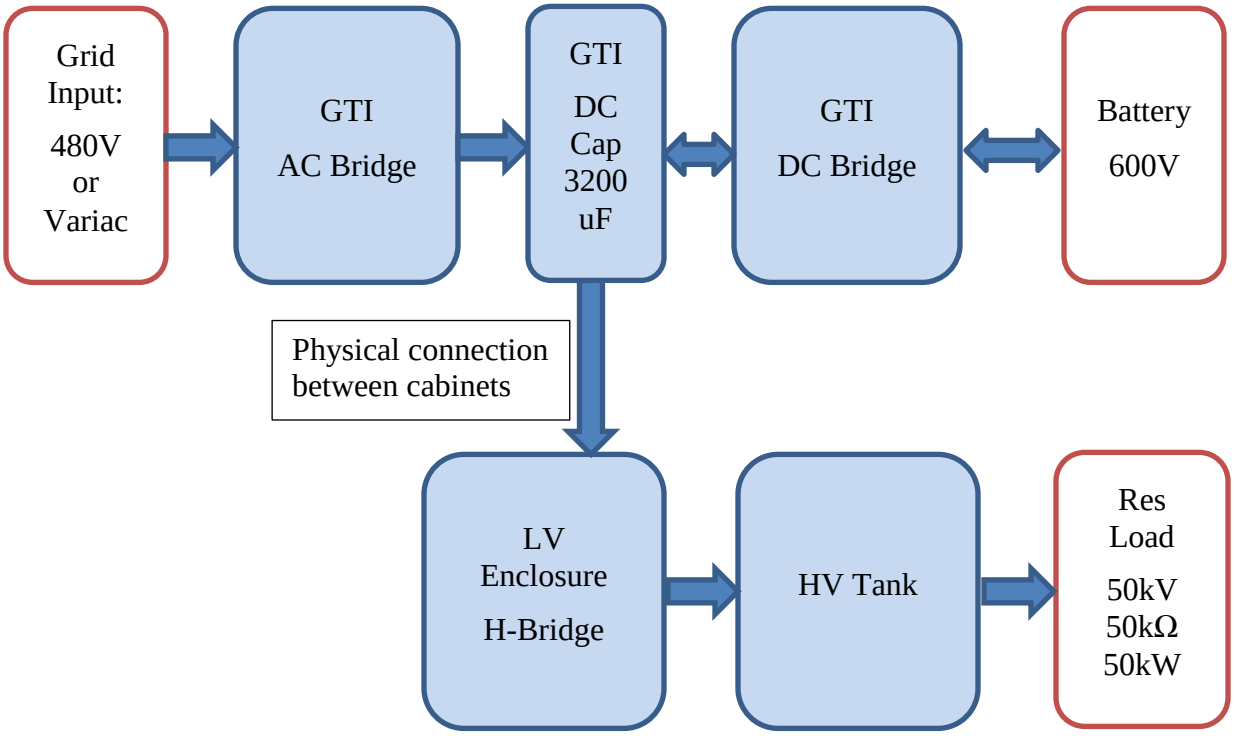

FIGURE 56: SYSTEM CONFIGURATION FOR PROTOTYPE EVALUATION

The outline of the system test is as follows. They will be explained in the following sections.

1) Dielectric tests
    a. 55kVDC, Secondary to ground
    b. 55kVDC, Secondary to primary (primary grounded)
    c. 3.1kVDC, Primary to ground
    d. 2.2kVAC, Primary to ground
2) Preliminary Operation tests
    a. Power control (GTI only)
    b. HV rectification (HVDC converter only)
3) System tests
    a. Steady-state test: 50kV, 50kW (9.5 Steady-State Test)
        i. DC output quality (accuracy/ripple)
        ii. Efficiency measurement
        iii. Thermal measurement
    b. Dynamic response test

i. To varying software power command
ii. To varying AC input voltage

9.2 Preliminary Testing

The purpose of Preliminary Testing is to ensure that the full system test proceeds with as little risk as possible. To that end, the two subsystems (the HVDC converter and the GTI) will be tested separately before being joined together.

9.2.1 GTI Power Control Test Procedure

The GTI has had its software modified and so the primary goal is to ensure that the software, as specified in Task 4, is functional and can achieve its functionality with reasonable performance. To this effect, a resistive load will simulate the HVDC converter reasonably accurately because it acts like a DC: DC voltage converter, and under test, will be loaded with a steady resistance. The resistance therefore must be scaled so that the 50kW load is applied to the central bus, which at 800V will be stepped up to 50kV in the application.

The AC input in the real application is assumed to look like an AC generator, which may be DFIG or synchronous and so have voltage output controlled by field excitation. It is difficult to simulate variable frequency output, but circuit analysis and experience have shown that the AC bridge control can easily handle 1-60Hz (in fact, it has been programmed to operate as a variable speed drive). A variac will therefore be used during testing to simulate the variable voltage component. To simulate variation in available power, the GTI has a current limit programmed into it so that the battery port (which works independently) must compensate for the limited power to maintain the bus voltage.

The DC input will be a battery as described by Table 10. It will be able to source the full power for 5 minutes, and 15kW for 15 minutes. It is of the VRLA AGM (lead acid gel mat) type.

The main criteria are that the DC bus voltage is stable, under static voltage and power and dynamic voltage and power conditions. The unit must be continuously exercised for 15 minutes under a variety of load and voltage conditions as the tester sees fit. The pass criterion is that the EUT does not trip with an allowable control deviation of ±40VDC voltage. This should correlate to ±2.5 kV DC on the HV output, or 5%, which is the specified ripple.

During the test, the DC bus voltage will be monitored using a differential voltage probe. The internal measurements of the GTI will be recorded using a serial output, printing a single line of important parameters and measurements once per second. There is also a high speed data bus which can capture up to 256 internal variables at a rate of up to 6 kHz.

Item	Characteristics	Manufacturer	Model	Qty.	Schematic Identifier
Test bay PC	*RS-232, Matlab, Code composer*	*Any*	*Any*	*1*	*PC*
Oscilloscope	*100 MHz or better*	*Agilent*	*6000 series*	*1*	*Scope 1*

Differential Voltage Probe	*±7 kV*	*Probe Master*	*4243A*	*1*	*DV 1*
Logic Analyzer	*With 2 Mictor header cables, for debugging only*	*Tektronix*	*TLA612/614*	*1*	*LA*

TABLE 9: GTI POWER CONTROL TEST EQUIPMENT LIST

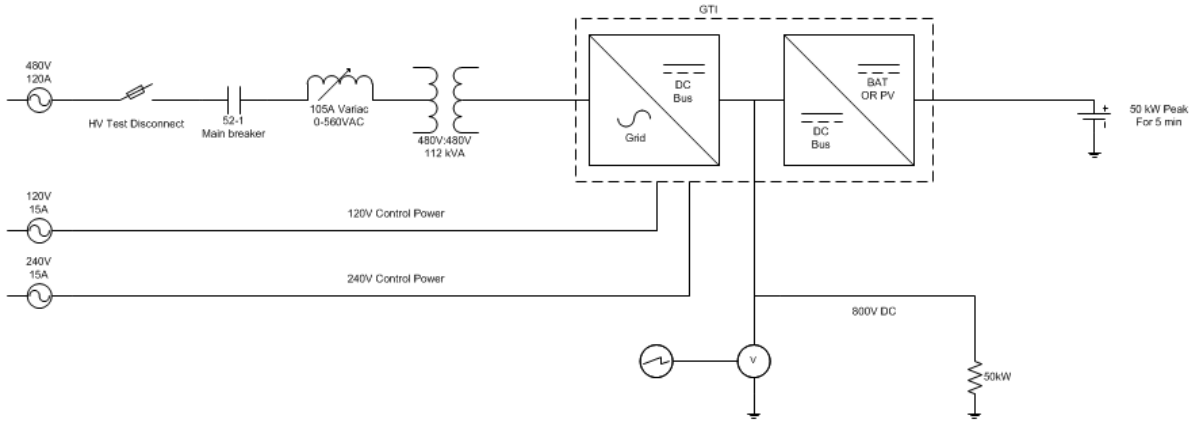

FIGURE 57: GTI POWER CONTROL TEST SCHEMATIC

FIAMM FLX 400	Per cell	Total
V nominal	12	504
V bulk charging	13.8	579.6
V float charging	13.6	571.2
V discharged	10.02	420.8
kW/15 min	0.4	16.8
A/15 min	33.3	33.3

TABLE 10: FIAMM FLX400 BATTERY, 42 CELLS SERIES 1 PARALLEL

9.2.2 HV Rectification Test Procedure

The HVDC converter will be operated by raising the voltage slowly up to 35kV using a current-limited supply. This will ensure that should any fault occur while testing that collateral damage is minimized. The test controls the switching on-time and dead time of the H-bridge that generates the LV resonant voltage, and the current limit to the external power supply. The tester should increment the voltage at no more than 250V increments, and each time look at the internal probes to see that the operation is correct before raising the voltage again. The pass criteria are more complicated since it is unknown exactly what good operation will look like based upon the

internal voltage and current. The minimum is that the converter operates at the maximum available power for 5 minutes with stable output voltage that is shared evenly between the midpoint and the full voltage output. The following waveforms shall be compared where possible to simulation results, and also evaluated by technical staff:

- 4 HV dividers, at ¼ increments of the output voltage, to ensure that stages are sharing power equally (HVP 1-4) Fig. 58
- The LV resonant capacitor voltage, to ensure that voltage swing is within limits. It is also proportional to load (DV1) Fig. 58
- The resonant current, which is to be examined for signs of hard switching and non-sinusoidal phenomena. Two CT's can be used to split the signal, so that the long term current trend is monitored separately from the detailed waveform (A1, A2). Fig. 58
- The LVDC bridge AC output terminals (DV2) Fig. 58
- The transformer primary voltage (DV3) Fig. 58
- The LVDC bridge DC (input) bus voltage and current which must be stable for safe operation (DV4). Fig. 58
- The trigger signals, which should be monitored to ensure that the correct switching period is set and to align observed phenomena with the activation of each trigger. They are located on J14 of the peripheral board.

Item	Characteristics	Manufacturer	Model	Qty.	Schematic Identifier
Test bay PC	*USB*	*Any*	*Any*	*3*	*PC*
DC Power Supply	*600V/ 40A*	*Magnapower*	*TS III Series*	*1*	*PSU 1*
Oscilloscope	*100 MHz or better*	*Agilent*	*6000 series*	*3*	*Scope 1-3*
HV Voltage Probe	*50 kV, 50 kHz BW*	*North Star*	*VD-60*	*4*	*HVP 1-4*
Resonant Current Probe	*50 kHz BW*	*Pearson*	*1330*	*2*	*A1-2*
Differential Voltage Probe	*±7 kV*	*Probe Master*	*4243A*	*4*	*DV 1-4*
Temperature Logger	*8 Channels*	*Neoptix*	*OmniSense*	*1*	*Temp 1*
Temperature Probe	*50 kV Oil-compatible*	*Neoptix*	*T2*	*6*	*TS1-6*

TABLE 11: HV RECTIFICATION TEST EQUIPMENT LIST

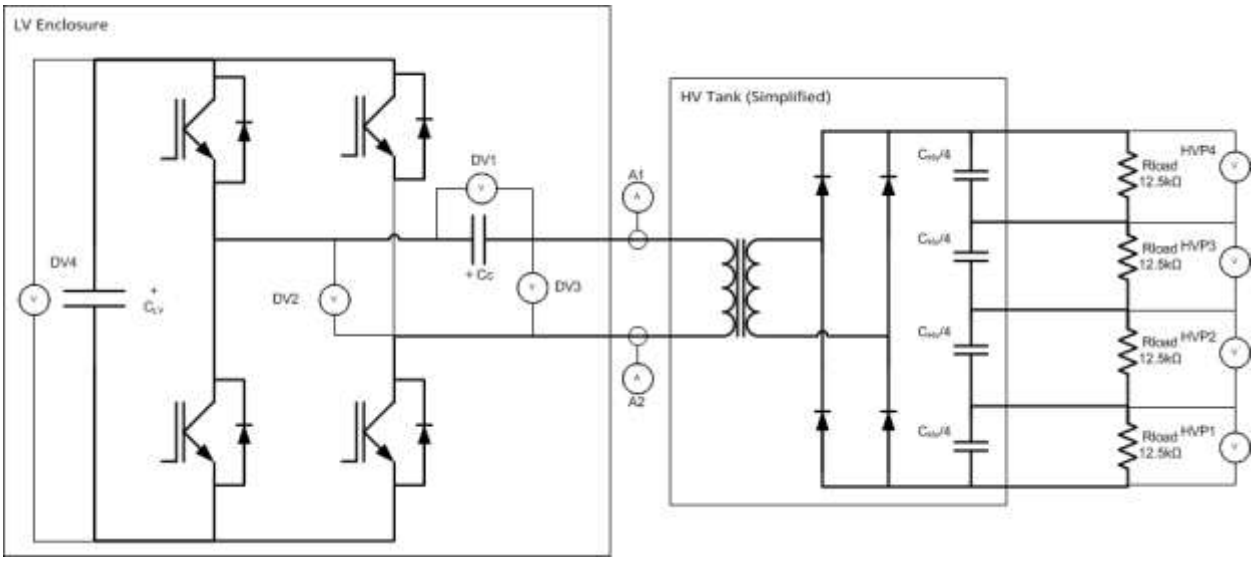

FIGURE 58: HVDC CONVERTER INTERNAL VOLTAGE AND CURRENT PROBE PLACEMENT FOR ALL SYSTEM TESTS.

9.3 Dielectric Test Procedure

The system consists of two chassis, each of which must be tested for leakage between each isolated barrier. The test specimen shall always be chassis grounded, although depending on the equipment used, the ground connection may either flow through an ammeter or be directly grounded. Each chassis itself should be isolated from each other so that all ground current flows through the dedicated ground connection and can be measured accurately. The system shall then be put in its final configuration as for the remainder of testing and then retested.

Each isolation barrier is to be tested to a standard metric of $V_{test} = 2*V_{nominal} +1000V$ for a period of 1 minute at full voltage. The voltage ramp shall be slow and not specifically defined other than to allow diagnosis of any changes in the current and to allow as best possible identification of the source of the change. To aid identification of failures, lighting and noise in the test area shall be kept to a minimum.

The voltage and current shall be recorded at the start and end of the 1 minute of fully applied voltage. The pass criterion is that not more than 10 mA DC shall be observed during the test. Should this threshold be exceeded, attempts shall be made to improve the reading, and then retested. A decision shall be made by the team regarding safety and risk mitigation should the final assembly not pass.

The tests to be performed are:

1) Low voltage cabinet

   480 V terminals to chassis, transformer primary and ground at 2.2 kV AC

2) Low voltage cabinet

   480 V terminals to chassis, transformer primary and ground at 3.1 kV DC

3) High voltage tank

HVDC port to chassis, transformer primary and ground at 55 kV DC

4) System as grounded in test configuration

HVDC to 480 V terminals at 55 kV DC

Item	Characteristics	Manufacturer	Model	Qty.	Schematic Identifier
Dielectric Tester	*100 kV AC/100 mA*	*Hipotronics*	*100HVT*	*1*	*HVT-AC*
Dielectric Tester	120V 50/60Hz 10A input, 0-80KV output	*Hipotronics*	880PL-10mA-A	*1*	*HVT-DC*

TABLE 12: DIELECTRIC TEST EQUIPMENT LIST

9.4 Bring-up Test Procedure

The bring-up test will confirm that the GTI solution and the HVAC cabinets work together. Below the battery voltage, the equipment must be precharged (see Task 4 Operation overview). This will mean that the unit should not be run until 504VDC. When finally engaging the DC voltage, ensure that the peak AC voltage is equal to the DC value to minimize transients. When initiating the power command, DC power should be used by setting the AC power to zero.

The test configuration is shown below in Figure 59: System Test Schematic (All Remaining Tests).The monitoring equipment shall be the same as that of the 9.2.2 HV Rectification Test (Figure 58: HVDC Converter Internal Voltage and Current Probe Placement).

The procedure is the same as 9.2.2 HV Rectification Test, with the goal of raising the HVDC output to 50kV in a steady, controlled manner until full voltage operation is achieved, but this time with active power routing. During the test, the battery will deplete and the AC power command should be moved accordingly upwards until all 50kW is sourced from the AC side. The test will be considered passed when 50kV operation has been stable for 10 minutes.

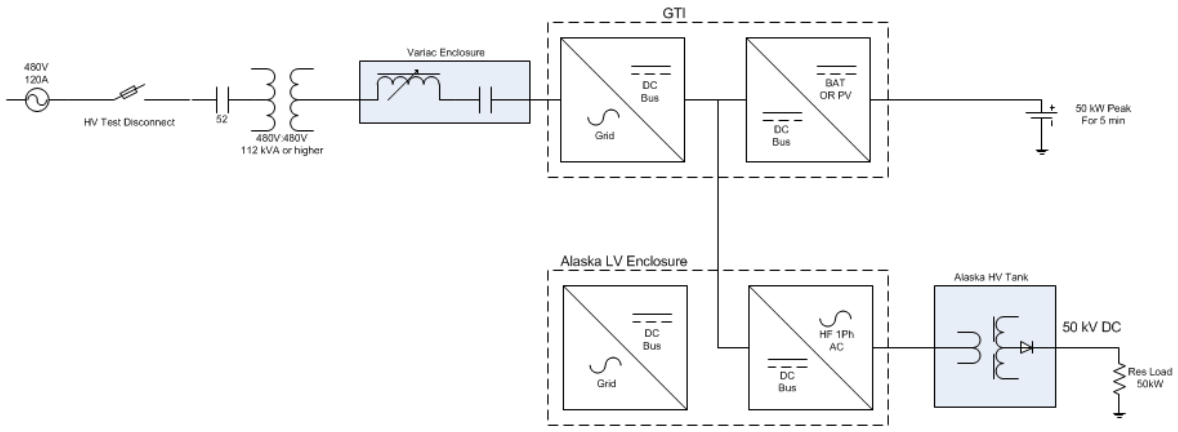

FIGURE 59: SYSTEM TEST SCHEMATIC (ALL REMAINING TESTS).

9.5 Steady-State Test Procedure

The steady state test will operate with 50kW available power at the AC port. It is to confirm that the EUT can operate steadily in increments from 0 to 80kW. At 0kW the HVDC converter will use only DC battery power, and at 80kW it will be charging the battery at 30kW. The battery must be therefore be depleted enough so that the full charging power can be drawn by the battery selected.

The pass criteria will be successful operation for 1 minute at each power level. The internal power command ramp should be set to be slow to avoid any sudden transients. During the test the maximum and minimum HVDC output shall be measured and must be in compliance with the allowed ±5% voltage ripple. In addition, a power analyzer can be used to measure the input power from both sides, with the output power determined by V^2/R applied to the load.

The temperature rise can also be measured since the output power should be constant. When the steady state tests are complete, the unit can continue to be run for up to 8 hours to prove thermal stability. Throughout the test the temperature should be monitored to ensure safe operation. The thermocouple data logger should be configured per Table 13: Thermal Probe Placement below.

Probe SN#	Channel	Location	Placement
443	*0*	*Unit 1 Transformer Core, Top, Front*	*Inside corner of core*
444	*1*	*Unit 1 Transformer Primary, Top, Front,*	*Down primary spacer, adjacent to front wire*
445	*2*	*Unit 1 Stack 8 Transformer Secondary*	*Along ridge of secondary coil, terminating in front secondary support brace*
446	*3*	*Unit 1 Stack 9 Diode*	*On heatsink, near base of fin*
447	*4*	*Unit 1 Stack 9 IGBT*	*Below heatsink base, adjacent to device package*
448	*5*	*Unit 1 Oil, top, between stacks 9 and 16*	*At about 1/3 height of top capacitors*

Table 13: Thermal Probe Placement

9.6 Dynamic Test Procedure

The dynamic test will test operational range with the available power at the AC port varied between 0 and 50kW. It will look at the same performance criteria as the steady state test, but under more challenging conditions. Start the test by going between 0-50kW in 1 kW increments. Following that, move from 50-0 in 2kW increments, followed by 5, 10, 15, 20, 25 kW increments and so on until a single 50kW step is made (the increments do not always add up to 50 – just bump the remainder before increasing the increment). The pass criterion is that the EUT should keep on running. During the change, a scope should capture the entire event, monitoring the resonant current and output voltages, with min/max statistics to look for the severity of the transient. A member of technical staff should observe the test also to ensure that the transients are within expected behavior.

Chapter 10: **Task 8: Testing Program Execution**

The testing program was completed in July 2012. When the constraint had been realized that high voltage to low voltage conversion would not be possible due to the limitation of the IGBT's, the remainder of the tests (and indeed the system test plan as mentioned in Task 7 (Part 2): Develop Test Procedure) focused upon the rectification (generating HVDC power). Within these limited goals, the testing was highly successful:

- Voltage withstand of the system was proven to 55kVDC in the dielectric test
- The unit successfully operated without tripping at 37kV during the steady state and dynamic testing, showing the basic capability for 3 port operation at high voltage.
- A maximum operation voltage of 40.2kV was safely reached at 8.4 kHz switching frequency.
- Withstand against serious events (loss of DC power, loss of AC power) showed resilient, fault tolerant operation.
- A maximum efficiency of 95.6% was recorded for the HVDC converter, which is a promising number given that there are various possibilities for further tuning for performance that were not exercised.
- Dynamic testing showed less than 2.06kV deviation for less than 4 seconds during transients.

10.1 Dielectric Tests

The dielectric test was between a grounded LV side and the HV side. All terminals of each side were shorted together. This negated the need for separate HV to LV and LV to GND DC tests.

The HV port configuration had all four high voltage dividers and both power positive and negative terminals connected to the 50kV load, shorting the entire resistive load as well as all 4 voltage measurement points. The positive DC test voltage was applied to these points.

The LV port configuration had both HF bus bars shorted together, and then connected to the tank. Also connected to the tank was the grounding wire for all 4 voltage probes. The tank was not grounded directly, but through the red return wire to the test set. The leakage current then flowed through an ammeter and the black cable to the single grounding point. This configuration means that the secondary ground path currents were bypassed.

The system test was performed at 55kV DC for 5 minutes and passed with 420 uA DC. This is in comparison to the 55uA recorded at NWL(our supplier) , where the tank was tested alone. During the test, the HV probes were connected to ground. With 800MΩ resistance and 4 in parallel, at 55kV the 200MΩ presented 275 uA of additional load. The residual leakage current was therefore 145uA, considered to be well within the 1mA caution boundary. Crackling was heard, although no visible flashes were seen to define a single point.

The final HV port configuration has HV0 (1) acting as the return path for the DC current, and HV0 (2) grounding the DC return to the tank lid stud. The tank lid stud is bonded to the tank

with braid, and the tank is grounded at the main stud. Also going to the main stud is the HV probe ground.

The final LV port configuration has the HF port floating, and the central cap of the GTI floating. The battery is floating, and the grid side goes through an isolation transformer. The Y point of the grid side was grounded.

All control power and equipment was routed to a control power breaker, through a single ground point.

10.2 Preliminary Test: GTI Power Control

The test was successfully passed in May 2012. The goal of the GTI being able to stably control a DC bus with a 50kW load was met.

A simulation of power flow was first performed, with the main algorithm tested in Code Blocks, a C based IDE and using GCC MinGW compiler. The simulation assumed both ports as current sources, which is true at a system level because their code modules are independent and operate on a current command. The algorithm regulates the DC bus by measuring the voltage and its error, and changing the battery port current command accordingly. It is mentioned comprehensively in Section 5.3 Software Functionality. The provisional tuning values were 0.1Volt/Volt error proportional gain and 1e-5 Volt/Volt-pulse error (each pulse is 6.5 kHz or 153us) integral gain.

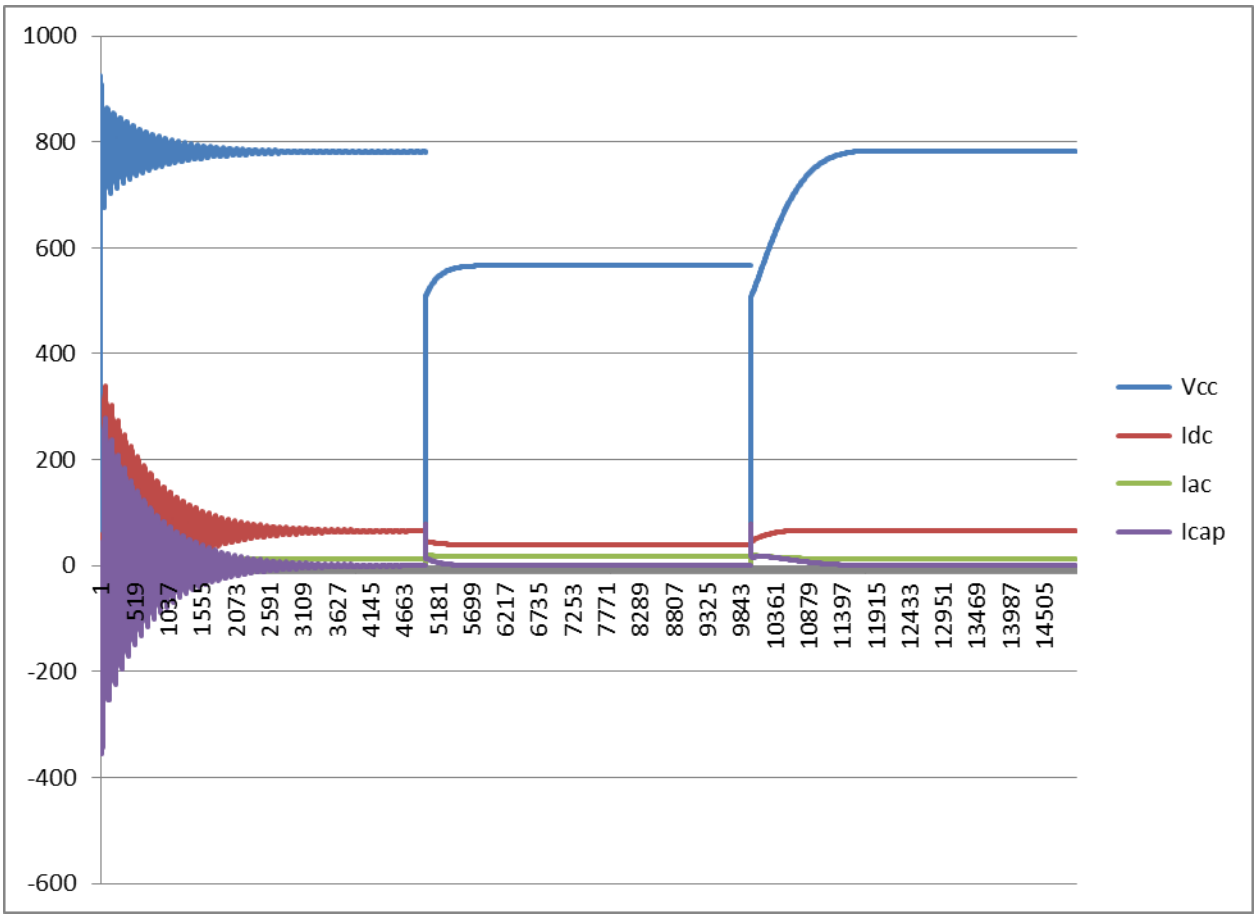

FIGURE 60: VOLTAGE AND CURRENT WAVEFORMS OF FINAL SIMULATION.

NOTE THREE SEPARATE RUNS SHOWING PI LOOP I-GAIN TOO HIGH (0.01), NO I-GAIN, AND GOOD I GAIN (1E-5) SETTINGS RESPECTIVELY.

The test setup was as per Figure 57: GTI Power Control Test Schematic. A logic analyzer monitored an internal data bus on a pulse by pulse basis and this was plotted using Matlab. It is a very powerful tool for close in examination of the code behavior, but will only output data for a limited amount of time (the internal memory is 512 kB).In addition, therefore, a serial RS-232 connection will print data every second, monitored on a PC using a terminal application. A scope with one differential voltage (DV) probe was used to monitor the bus voltage, to confirm that the analyzer was capturing sufficient detail.

The simulation gains were found to be correct when tested on the system. In addition to the control loop which regulates bus voltage directly, a second control loop was implemented. The first loop will command the DC bus to discharge the battery as needed to ensure that the DC bus voltage is constant. However, should excess power be available, the battery may be recharged. To this end, the battery port will limit power based on the charging cycle. It therefore is required to have a second loop which, when charging the battery, will limit the AC input power. This loop was tested and the value of 3.3kW/Volt error proportional gain was found to be sufficient. This loop becomes active when a threshold of +10V error on the central capacitor is detected.

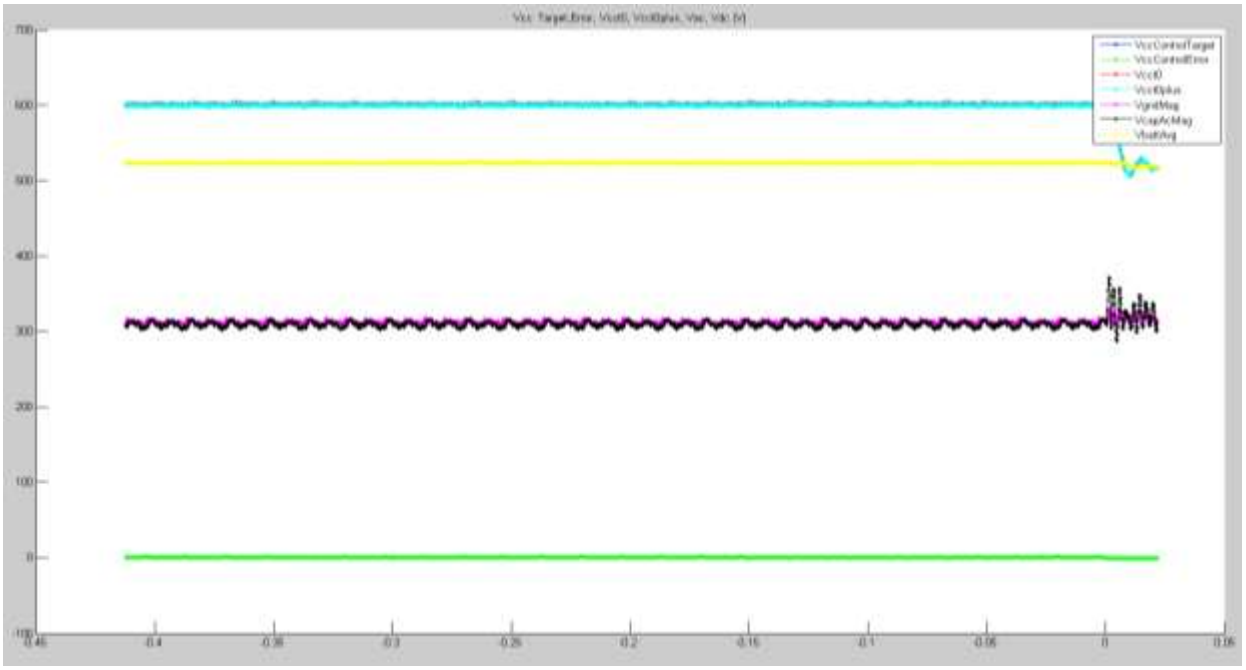

FIGURE 61: EXAMPLE OF TEST DATA SHOWING STABLE OPERATION.

CYAN AND RED ARE THE DC BUS VOLTAGES (600VDC). GREEN IS THE ERROR SIGNAL (APPROXIMATELY ZERO).

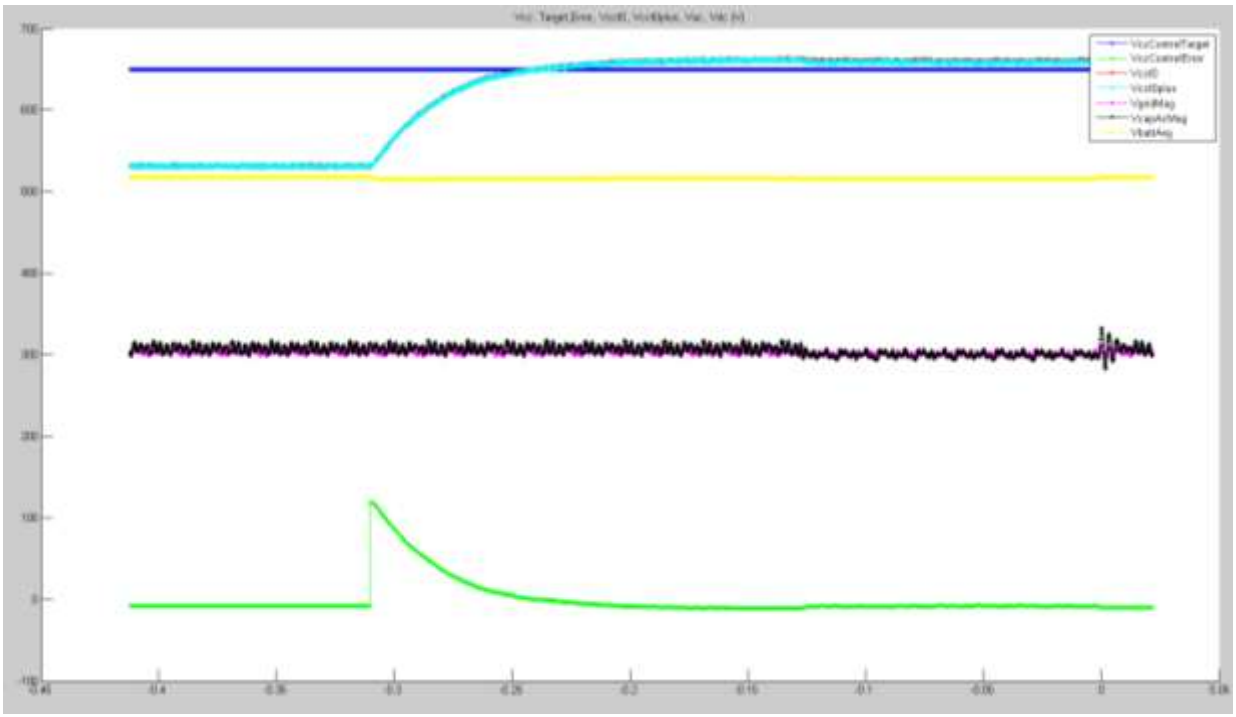

FIGURE 62: EXAMPLE OF DATA SHOWING RESPONSE TIME.

THE RESPONSE TIME IS ~0.1S FROM SYSTEM START.

10.3 Preliminary Test: HV Rectification

The purpose of HV Rectification testing was to ensure that the HVDC converter part of the system was successfully brought up to voltage. Measurements were taken to confirm the system efficiency and that the internal voltage and current waveforms were within specification.

The main variable under test was switching time and dead time (see section 3.2 Theory of Operation for an explanation). Generally, the on-time must be at least long enough for the resonant pulse to complete, which was measured as 50 us. The dead time that follows is ideally as short as possible. Because the energy in each pulse is constant for a given LV bus voltage, generating more pulses/second (the operating frequency) by reducing the dead time is also desirable. However, the system may not be able to support the theoretical maximum frequency of 1/ (50us on –time + 5 us dead time) or 9.09 kHz and indeed this proved true. A "safe" number of 60 us on-time+100 us dead time was chosen (although this was later reduced to 80 us as we became more confident of the system operation as a whole).

The highest achieved voltage was 40.2kV and the highest measured efficiency was 95.6%.

FIGURE 63: HIGHEST RECORDED OPERATION VOLTAGE OF 40.29KV (PINK, X1000), ACHIEVED USING 60US ON-TIME AND 70US DEAD TIME.

FIGURE 64: INTERNAL WAVEFORMS AT HIGHEST OPERATIONAL VOLTAGE

Preliminary Test: HV Rectification														
Nominal Input Vdc	Dead time us	On Time us	Actual Input Vdc	Actual Input Adc	Output Voltage kV	Resonant Cap Vrms	Res. Current Irms	Magnetizing Current A	DC input power W	DC output power W	Vout/ Arms in	VDC ratio	Operating Freq Hz	Overall Efficiency %
200	146	60	195.2	15.86	12.132	24	39.1	41	3095.87	2943.71	310.28	62.15	4854	95.1%
250	146	60	247.9	19.8	15.184	29.54	43.96	51.85	4908.42	4611.08	345.40	61.25	4854	93.9%
300	146	60	296.8	23.7	18.213	35.31	58.22	57.5	7034.16	6634.27	312.83	61.36	4854	94.3%
350	146	60	347.2	27.55	21.28	41.67	61.43	54.35	9565.36	9056.77	346.41	61.29	4854	94.7%
400	121	60	397.7	31.58	24.403	41.37	67.39	65	12559.37	11910.13	362.12	61.36	5525	94.8%
437	121	60	434.8	34.35	26.605	44.6	70.4	38	14935.38	14156.52	377.91	61.19	5525	94.8%
400	100	60	397.4	32.26	24.637	36.68	64.09	100	12820.12	12139.64	384.41	62.00	6250	94.7%
450	100	60	447.6	35.86	27.59	41.09	70	90	16050.94	15224.16	394.14	61.64	6250	94.8%
507	100	60	500.6	39.87	30.88	45.5	75	89	19958.92	19071.49	411.73	61.69	6250	95.6%

TABLE 14: HV RECTIFICATION TEST DATA

10.4 Test Setup for Remainder of Tests

Test Equipment Used:

- Neoptix thermal monitoring system for measuring diode spot temperature and oil temperature
- 3 Agilent scopes with various probes monitoring system behavior as described below
- Terminal capture of GTI second-by-second output
- Logic analyzer of detailed capture of system behavior
- WebUI interface for controlling EUT.

Scope Settings					
Cha-nnel	**ID**	**Name**	**Scaling**	**Probe**	**Notes**
	Scope 1	HV Resonant	100us		Trig on 1.2 falling
1.1	DV1	Vcc	1000: 1 V	DV 7000V	+ to bridge
1.2	A1	Resonant current 1	0.005:1 V/A	Pearson 1330	
1.3	DV3	Transformer	1000: 1 V	DV 7000V	+ to xfmr pos/cc neg
1.4	DV2	AC output	1000: 1 V	DV 7000V	+ to cc pos
	Scope 2	HV System	1 sec		Trig on scope 1
2.1	A2	Resonant current 2	0.005:1 V/A	Pearson 1330	
2.2	DV4	DC Bus voltage	200:1 V	DV 1400V	
2.3	HVP2	HVDC Stage 8	10:1 kV	Northstar VD-60	
2.4	HVP4	HVDC Stage 16	10:1 kV	Northstar VD-60	
	Scope 3	HV Triggers	100us		Trig on scope 1
3.1		Trigger A	Auto (10:1) V	Agilent probe	
3.2		Trigger B	Auto (10:1) V	Agilent probe	
3.3	(DV1)	Vcc	100:1	DV 7000V	Was on GTI DC bus
3.4		DC bus to bus current	0.0001 V/A	Fluke i1010s	

TABLE 15: SETTINGS FOR OSCILLOSCOPES

10.5 Steady State Test

Steady state operation was a successfully measured at 5kW increments from 5kW to 50kW. Operation was smooth, with HVDC ripple voltage less than 1.3%, much lower than specified under constant resistive loading.

The test data is shown in Table 17. Further, the standard deviation of the average voltage taken over the course of a minute was exceptionally low, being less than 0.2%, proving both stable operation and high power quality. Example scope captures from the 50kW AC command are shown in Figure 65 and Figure 66.

Steady State Power Quality						
AC Power kW	**HVDC Power kW**	**LV Average Vdc**	**HV Average kVdc**	**HV Average Std. Dev.**	**Ripple Vdc**	**Voltage Ratio**
5	17.63	464	29.694	16	357	64.0
10	17.67	464	29.724	36	360	64.1
15	17.63	464	29.692	38	340	64.0
20	17.65	463	29.707	27	363	64.2
25	17.65	463	29.711	31	365	64.2
30	17.65	465	29.706	21	367	63.9
35	24.86	552	35.257	30	376	63.9
40	25.10	563	35.426	23	370	62.9
45	25.09	563	35.416	38	370	62.9
50	25.16	565	35.469	36	367	62.8

TABLE 16: STEADY STATE POWER QUALITY DATA

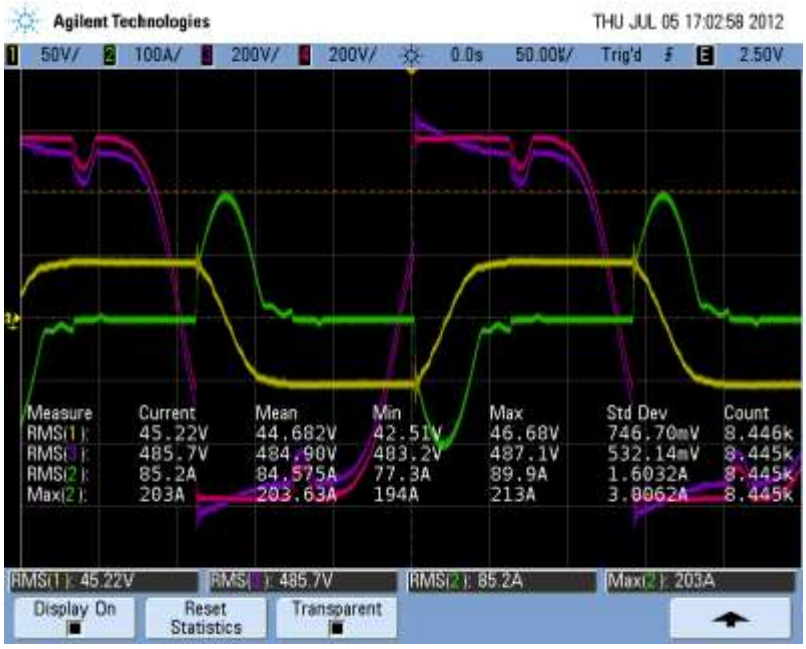

FIGURE 65: RESONANT WAVEFORMS FROM STEADY STATE TEST AT 50KW AVAILABLE AC POWER

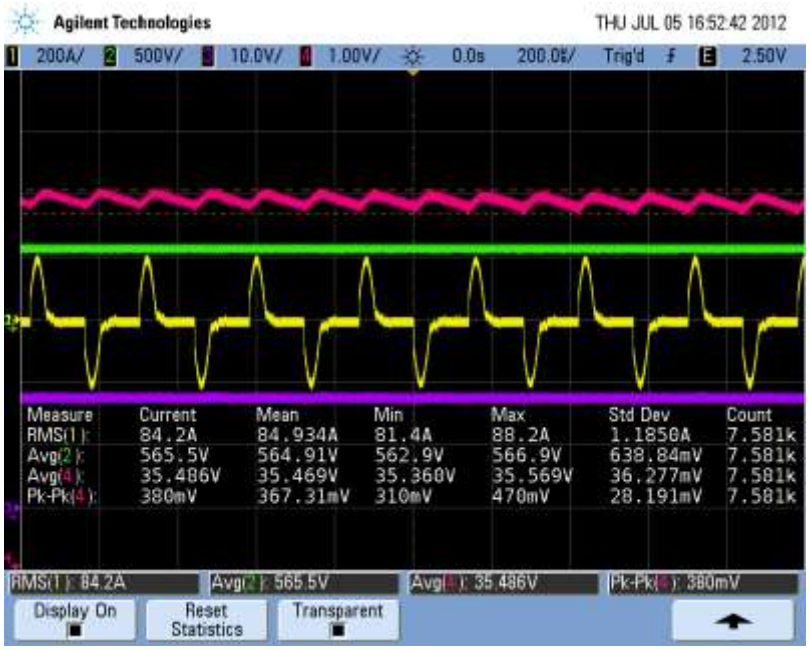

FIGURE 66: HVDC OUTPUT (PINK) AT 50KW AVAILABLE POWER

10.6 Dynamic Test

The dynamic test was designed to show the system's response to transients in available power. The system passed this test. It kept running during the incremental changes in AC power, and the deviation was less than 2.75kV when operating at the same bus voltage. The test was run at a relatively conservative voltage (29kV) in order to ensure headroom should a large transition

voltage occur. Hence two conditions caused the bus voltage to change:

- Above 30kW, the AC power is greater than the load and so the excess power goes to charge the battery. The bus voltage raises due to the higher voltage needed to charge the battery (see Figure 67).
- Above 35kW, the AC power is much greater than both the load and the power needed for AC precharge. If unchecked, the bus voltage will rise indefinitely, but there is a proportional loop that reduces the AC power when the bus voltage deviation exceeds 20V. During the test it was tuned to reduce the AC power (actual, not commanded) and settled at about 100V over the nominal bus voltage (see Figure 68).

The data for the test at the same bus voltage is shown below (Table 17). The test could be repeated at a higher voltage and would likely show similar performance if the AC power algorithm could be improved. It is likely that adding an integral action to the loop (a PI loop) would fix this, in addition to further tuning of the gain.

Dynamic Test Data: 5KW Steps				
Start AC Power kW	**End AC Power kW**	**Min HVDC kV**	**Max HVDC kV**	**Deviation kV**
0	5	28.54	30.73	2.19
5	10	28.6	30.16	1.56
10	15	28.85	30.41	1.56
15	20	28.91	30.91	2
20	25	28.85	30.48	1.63
25	30	28.73	30.41	1.68
5	0	27.04	29.79	2.75
10	5	27.79	29.66	1.87
15	10	27.79	29.48	1.69

TABLE 17: DYNAMIC TESTING RESPONSE TO 5KW STEPS

FIGURE 67:30KW TO 35KW AVAILABLE POWER TRANSITION.

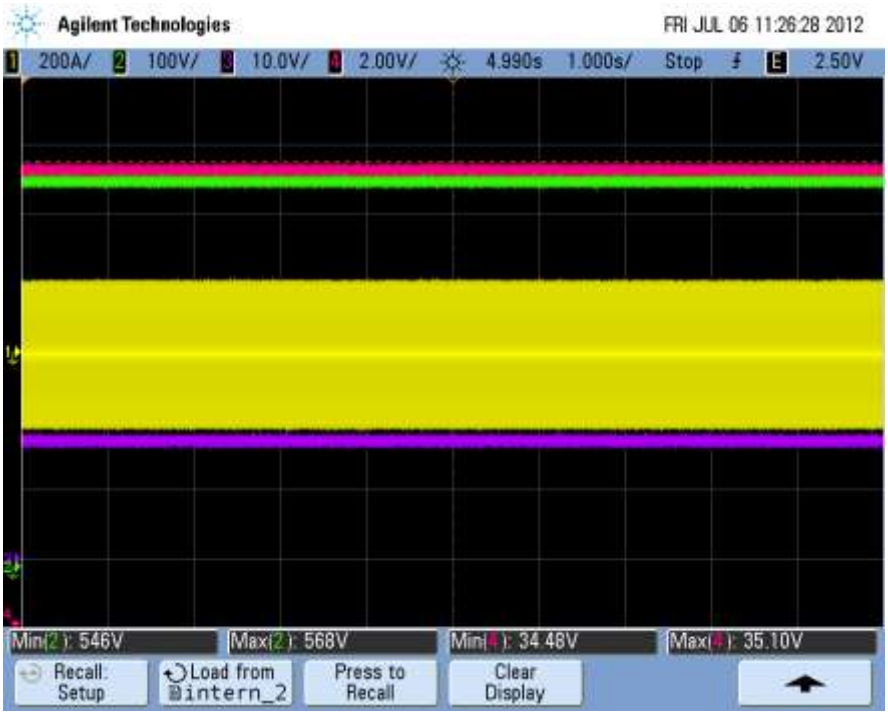

FIGURE 68: 35KW TO 40KW AVAILABLE POWER TRANSITION.

FIGURE 69: TRANSITION FROM 0 TO 25KW.

Above is shown the largest transient in which the start and end bus voltage (green trace) is the same nominal command. The deviation is 2.06kV, which compares favorably to the smaller steps, although the duration of the disruption is longer at 4 seconds. The slower response time may be reduced by further tuning on the system.

In addition to the transient testing, the following transient conditions were demonstrated:

- Precharge from AC rectifier side, starting at 60V (rms, phase-phase) up to where 28 kV DC output is generated through passive rectification (Figure 70).
- Sudden loss of AC voltage, where DC output is generated through passive rectification

Both of these conditions show that the system is tolerant to these fault conditions. It is an important system characteristic to be able to output passively following a partial failure, and thus continue to be productive.

FIGURE 70: AC PRECHARGE

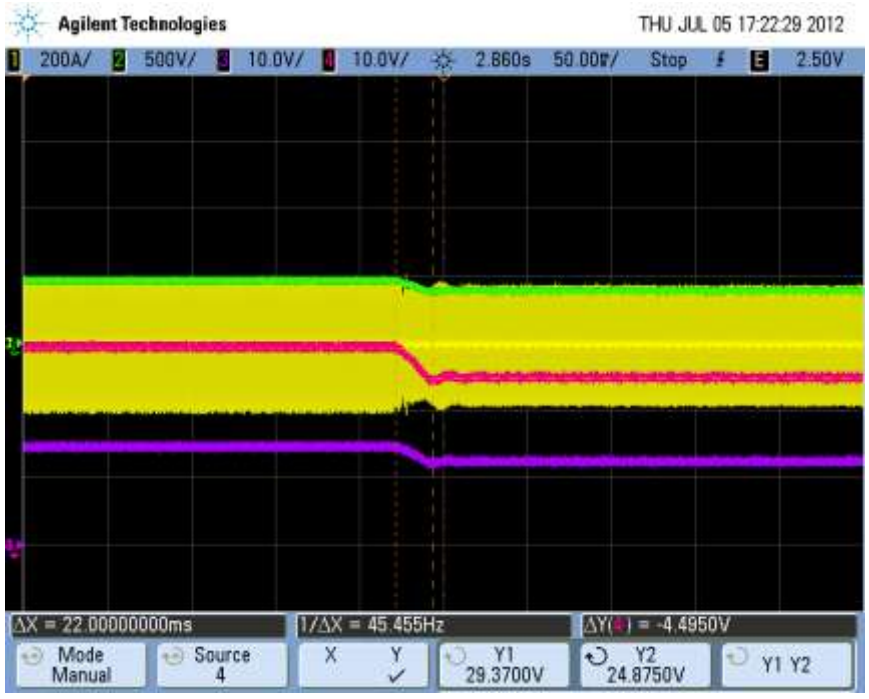

FIGURE 71: SUDDEN LOSS OF AC POWER.

Chapter 11: **Task 9: Identify field testing sites/partners**

Due to the IGBT overheating issue which limited the HVDC to AC functionality, it was recognized that while good technical progress had been made on the system, it would not be feasible in a field test to generate high voltage DC without being able to convert it back to grid-compatible power at the other end of the transmission line.

Currently PPS has been in talks with potential academic and commercial partners evaluating how the results of this project can be integrated in other HVDC projects currently in the proposal stage.

Chapter 12: **Conclusion**

Progress has been made towards the goal of making a commercially viable 3 port converter suitable for marine hydrokinetic applications. Key technical goals have been achieved, including the design and manufacture of a system which meets the key metrics for commercial viability. During this project PPS has:

- Developed equipment for bidirectional power flow to and from a 50kV high-voltage DC port, using a high-efficiency nanocrystalline transformer.
- Shown how this equipment can be combined with existing solutions to provide battery storage and an AC port, forming a three port device as planned.
- Demonstrated algorithms to control and generate 50kV DC output at low power, and up to 30kV at higher output power.
- Demonstrated the ability to control the unit such that the HVDC output power was constant during dynamic conditions (AC input power changes), either charging or discharging the battery as necessary.

A key remaining technical challenge is to implement the corrective action required to allow the HV stage to operate fully bidirectional, by redesigning the HV stages and replacing the IGBT's of the HV stages with IGBT's that will not overheat. The correct IGBT's have been identified and a small quantity have been procured for testing. The HV stack board is currently undergoing redesign. It is anticipated that the prototype solution will have been tested within 6 months, after which it will be able to be applied to the whole design pending fund availability.

A second technical development required for commercial viability is the continued development of an algorithm which enables the resonant section to be power limited, called 'inversion', which will allow the resonant pulse to act in a way similar to a fly-back diode, effectively circulating power within the LV side of the circuit, rather than transferring the energy to the HV side. This modification will allow automatic 'pre-charge' such that the method of manually slowly raising the LV bus voltage used during testing, will no longer be needed. This algorithm development will be a huge benefit, the alternative is to develop a special precharge circuit that can handle the steady state power for the duration of operation until the normal bus voltage is reached.