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Title: List Mode Module Data Acquisition Experience

Author(s): Mayo, Douglas R.

Intended for: LANL/CEA Workshop

List Mode Module Data Acquisition Experience

LANL/CEA Workshop

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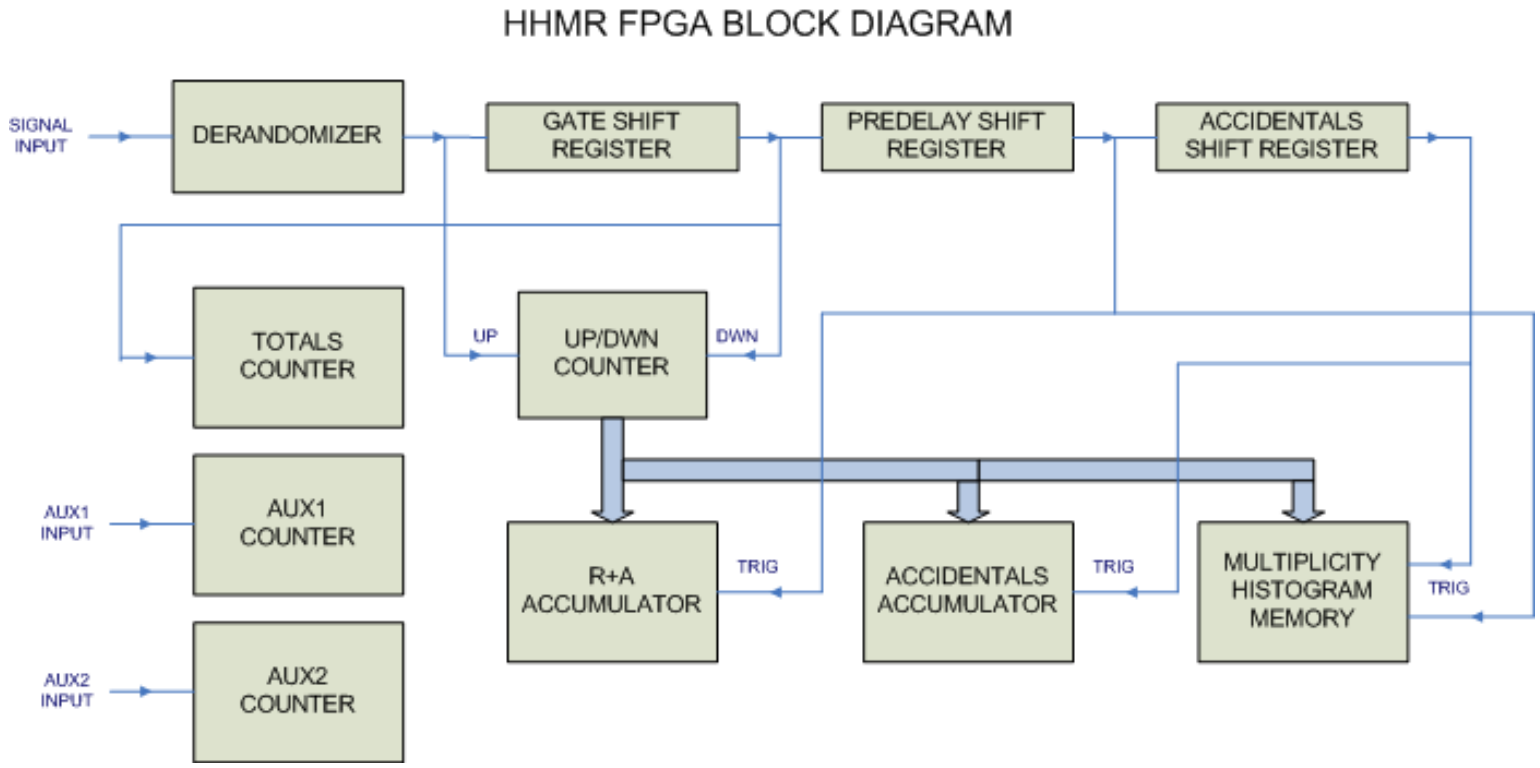
Douglas R. Mayo

EVOLUTION OF DATA ACQUISITION

- **Hardware, Software, and Analysis Techniques are Coupled**
- **Counter/Scalars (NIM)**
  - Totals Counting
- **Shift Registers (NIM - FPGA)**
  - Coincidence Counting
  - Multiplicity Counting
- **Time Tagging (VME/CAMAC)**
  - Expansion of Analysis Capabilities
- **List Mode Data Acquisition (FPGA)**
  - Multiple Channel
  - Can Analyze Data Multiple Ways
- **Waveform Digitization**
  - Non-^{3}He based systems

NEW DEVELOPMENTS



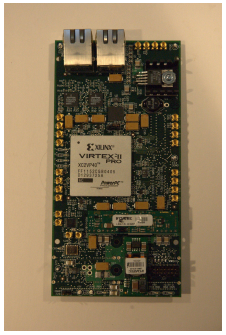
MOTIVATION

- **Existing Data Collection Capabilities (Shift Registers) are very limited.**
  - Changing Gate-width, Pre-delay, and Cycle length requires retaking measurement.
  - Single Channel input
- **List Mode Data Acquisition Allows for Different Processing Capabilities**
  - Timing Experiments Possible
  - Multiple Channel Inputs
  - Improved Passive/Active Data Acquisition
  - Local Coincidence Veto
  - Triggering Levels
  - Continuous Monitoring
  - Other Trigger Inputs
  - Various Analysis Tools
  - Expanded Post-processing capabilities

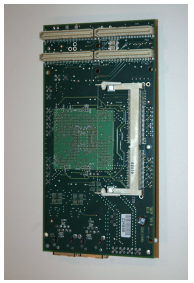
MOTIVATION

- **The NPOD detector system is a fielded neutron detector consisting of 15 ^{3}He tubes embedded in polyethylene, read out by an integrated data acquisition system. The motivation for this project is to modify the electronics to increase functionality and allow use as an active interrogation detector. In particular, high-speed networking capabilities are being added to allow multiple units to operate as single virtual detector.**

▪NPOD Mockup



▪Mezzanine Board Top



▪Mezzanine Board Bottom

MOTIVATION

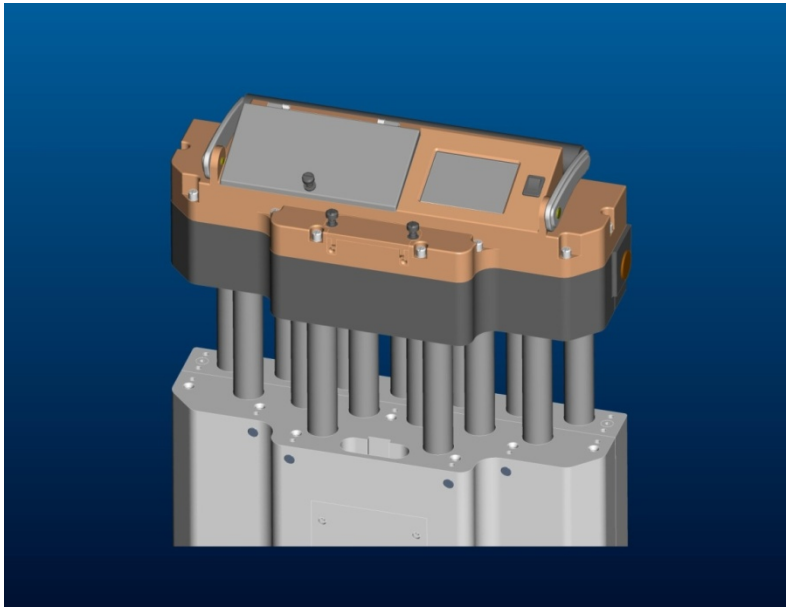
- **Commercially Available Electronics**
  - Not in house built boards
  - Standard Interfaces
  - Embedded PC
  - Flexibility
- **Firmware**
  - VHDL time stamping multiple channel input
  - Ability to accelerate data analysis using custom VHDL
- **Software**
  - Commercial Operating Systems
    - Embedded Linux
    - Windows Operating Systems
  - Real-Time data merging
  - Support for real-time data analysis using multiple algorithms in C++.

LIST MODE DATA ACQUISITION

Development Status

- Use of a commercial component provides a powerful flexible module housing communications, processor, memory, field programmable gate array (FPGA), and interface connectors
- Detector logic is written in very high level description language (VHDL) which is loaded into the FPGA fabric.
- Detector Logic can be reused when faster hardware is required.
- Detector power and interface circuitry is all that is needed to be designed in-house.
- Data transfer rates of 2Mhz are possible with gigahertz Ethernet.

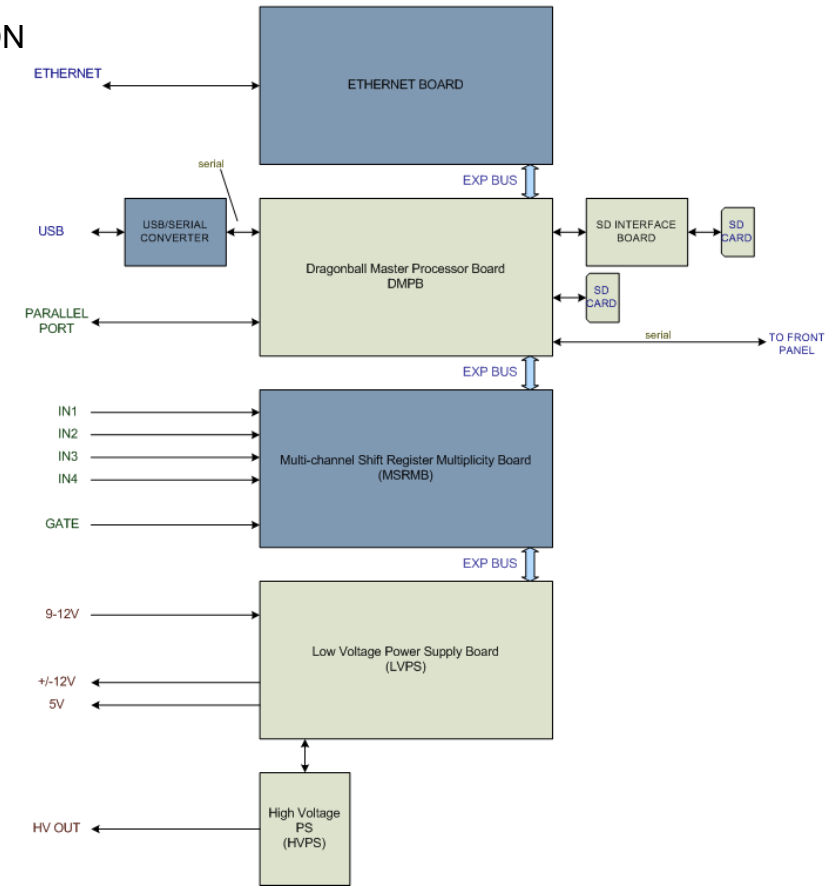
FURTHER DDEVELOPMENTS



NEW DEVELOPMENTS WITH CANBERRA

JSR-16
>50MHZ
UNATTENDED OPERATION
MULTI-CHANNEL

JSR-16
BLOCK DIAGRAM



APPLICATIONS

- Benchmark Subcritical Neutron Measurements
- Safeguards Applications
- Portable Neutron Diagnostics
- Analysis Tools and Techniques Comparisons
- Algorithm Development
- Signature Development

NOT STRAIGHT FORWARD

- **Utilizing Commercial Hardware**
  - Features
  - Unfounded Claims and Capabilities
  - Development Tools
  - Development Lifecycle and Support
- **Clocks**
  - Accuracy is few in 10^{-6}
  - Two system clocks would drift apart 1.3 μs each second
  - How to Synch Clocks or Have Common Clocks
  - Waiting on Atomic Clock Chip few in 10^{-9}

Contributors

- Richard B. Rothrock
- Brian D. Rooney
- Eric B. Sorensen
- Mark Smith-Nelson
- Martyn Swinhoe
- Johnna Marlow
- Edward McKigney
- Matthew R. Newell
- David C. Jones
- Gaetano J. Arnone
- William L. Myers
- Sheila G. Melton