# Final Technical Report

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Project Monitor – Grant Logsdon

# STATUS / ACCOMPLISHMENTS

**Executive Summary:**

A silicon carbide (SiC) based electronic temperature sensor prototype has been demonstrated to operate at 300°C. We showed continuous operation of 1,000 hours with SiC operational amplifier and surface mounted discreet resistors and capacitors on a ceramic circuit board. This feasibility demonstration is a major milestone in the development of high temperature electronics in general and high temperature geothermal exploration and well management tools in particular. SiC technology offers technical advantages that are not found in competing technologies such as silicon-on-insulator (SOI) at high temperatures of 200°C to 300°C and beyond. The SiC integrated circuits and packaging methods can be used in new product introduction by GE Oil and Gas for high temperature down-hole tools. The existing SiC fabrication facility at GE is sufficient to support the quantities currently demanded by the marketplace, and there are other entities in the United States and other countries capable of ramping up SiC technology manufacturing. The ceramic circuit boards are different from traditional organic-based electronics circuit boards, but the fabrication process is compatible with existing ceramic substrate manufacturing.

This project has brought high temperature electronics forward, and brings us closer to commercializing tools that will enable and reduce the cost of enhanced geothermal technology to benefit the public in terms of providing clean renewable energy at lower costs.

**Accomplishments verses Goals and Objectives:**

The main goal of the project is to develop and demonstrate the feasibility of a temperature sensor that can operate at 300°C for at least 1,000 hours. We have shown that the SiC-based oscillator can convert the platinum temperature sensor resistance to a frequency output, proportional to temperature, and the sensor electronics components survive 300°C for at least 1,000 hours. We have integrated the sensor circuit, including passive components, on a ceramic circuit board substrate that is capable of operating at 300°C in excess of 1,000 hours. We have explored alternative ceramic circuit board technologies, different active amplifier designs, various passive component suppliers and parts, and experimented with different packaging process parameters to select a suitable combination of technologies for operation at 300°C.

**Technical Results and Summary:**

The key component of the high temperature sensor system is the active SiC-based operational amplifier, which consists of transistors and resistors on the SiC substrate. The project has focused on the development of SiC lateral MOSFET transistor and linear resistor devices, their simulation models and fabrication processes for the operational amplifier. High temperature passive components have been selected and screened for high temperature functionality in addition to the development of ceramic-based high temperature packaging and die attach methods. The combination of active and passive electronic devices, and packaging material and methods provides a technology platform for high temperature electronics up to 300°C.

**Device Fabrication**

The SiC operational amplifier was improved from previous work done at GE. In the past, the amplifier would work only for a short time and drift out of useful range. Improvements have been made continuously to the transistors such that their stability and reliability have improved dramatically. We know that SiC as an electronic material has much better intrinsic properties than silicon that makes it suitable for higher temperature operation, and the SiC technology has matured to the point that we thought a circuit as complex as an operational amplifier can be made to work.

Three SiC lots were fabricated in this project. The first SiC integrated circuit (IC) lot was intended to demonstrate functioning ICs at 300°C and establish a baseline for device characteristics and to create device models. Design and process variations were included in the lot to identify the optimal conditions to run the second lot. These variations included lateral-MOSFET-based versus JFET-based circuits, different device electrical isolation methods, and different gate materials. Results from the first lot showed that MOSFET-based circuits worked better than JFET-based ones, so the JFET was dropped from subsequent lots. The metal gate was also dropped in favor of poly silicon gate for the MOSFETs. We found that the threshold voltage of the MOSFETs were not optimal for circuit design. The operational amplifiers have high gain, but they cannot be used in closed loop feedback due to mismatch of input and output common mode range.

Single MOSFETs were measured and a new set of simulation device models were created. Circuit design was updated using the new models and new layout was generated for the second lot. Device models based on SPICE level 2 were created for MOSFETs and resistors for room temperature and 300°C.

A number of changes were implemented in the second SiC lot. The second lot was intended to replicate the first lot while making a few key changes to the design and process, and to produce a second set of ICs to function at 300°C. The device design was updated to give a more optimal threshold voltage, and to include some new and modified circuits. The lot contained splits between wafers for two different threshold voltages, different device isolation structures, and one semi-insulating on-axis wafer. The second lot also utilized a modified photolithography alignment scheme that improves alignment between different mask layers.

The third lot contained six SiC wafers: three 4-inch 4H semi-insulating wafers and three 4-inch 4H N+ substrates wafers with p-type epi. The first two lots used contact printing lithography on three inch wafers, whereas the third lot used stepper 5X projection print lithography on four inch wafers. The interconnect metal patterning process was changed from liftoff to subtractive etching in the third lot to provide much improved line definition and also improved metal adhesion to the substrate.

**Device modeling**

Generating high quality simulation models is a critical part in developing integrated circuits. This is even more important for analog designs as the transistors are not merely used as "switches" as in digital circuits. Factors such as subthreshold slope, transconductance, output conductance, back-bias effects etc. can strongly influence the performance of an analog circuitry.

Most MOSFET models have built-in temperature scaling equations that are used to scale the parameters at different temperatures. The equations used to model temperature behavior in these models are based on physical observations in conventional Si transistors. The temperature scaling in SiC lateral MOSFETs are found to be different from their Si counterparts. For example, in Si MOSFETs, as the temperature is increased, the mobility decreases due to the increase in the on-state resistance. This results in an output current drop for the same test conditions with rise in temperature. But in SiC devices, due to the presence of interface states in the SiC-SiO2 interface, the observed temperature behavior is the exact opposite. In other words, as the temperature is increased, the output current is seen to increase. Another interesting observation in SiC lateral FETs is that the threshold voltage stays nearly invariant across the entire temperature range from room temperature to 300°C, while in Si – the threshold voltage decreases with increasing temperature.

Since the above-described effects are not seen in Si MOSFETs, the available FET models do not have temperature scaling functions reflective of what is seen in SiC. Therefore, it would not be possible to directly use these models to design circuits over the entire temperature range. While there are future plans to develop a fully temperature scalable SiC lateral MOSFET, the current technology demonstration phase does not warrant a requirement of the same.

One approach to address this problem is to use a standard model as an iso-thermal model by turning off the temperature-dependent parameters and extracting a parameter set to fit at one single temperature. This may be repeated for different temperatures within the range of interest. This method was then used to create model decks at two different temperatures – room and 300°C. The designer would have to manually switch between the two parameter sets depending on the temperature being simulated.

A wide variety of compact models are available for FET devices – from the simplest SPICE models (Levels 1 and 2) to advanced models such as BSIM4 and PSP, which can accurately predict device behavior over various geometries and temperature. In this project, the MOSFET models were initially developed in SPICE and then as the technology matured, PSP models were generated, because PSP models has additional parameters useful for a tighter fit to our devices. When we moved to generating PSP models, we used the device modeling software IC-CAP from Agilent to help fit the model to the measurement data. Figure 1 shows an example of the fit between model and measurement data. PSP model has physics based parameters such as surface state density that allows us to fit even the subthreshold region fairly well, and the model accuracy is within 1 or 2% of the measurement data.

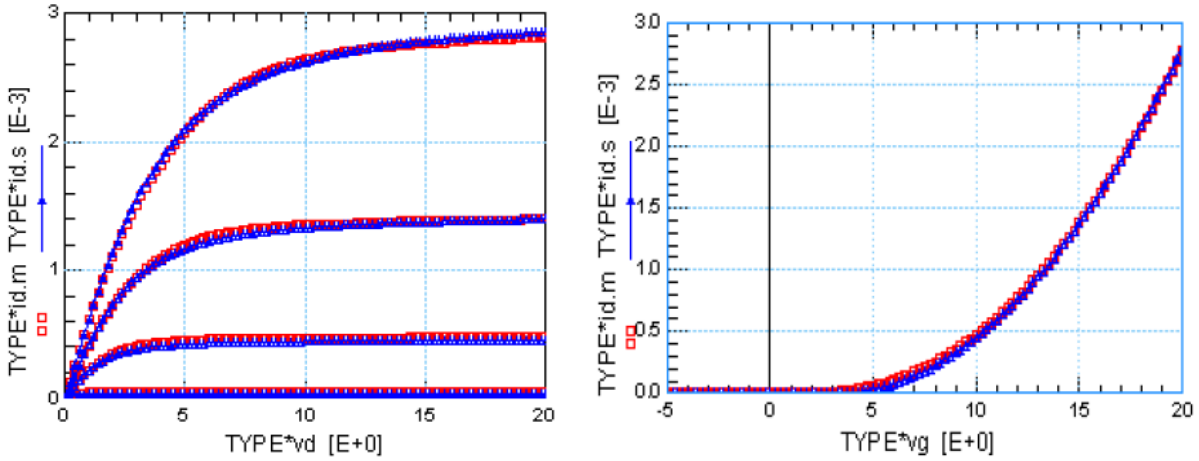



Figure 1. Example of fitting device model to MOSFET measurement data; model in blue line and measurement in red squres. Left plot is a drain family curve fit; right plot is Id vs. Vg curve fit.

To account for process variations, corner models were developed for transistors and resistors. The model set now includes a "nominal", a "low", and a "high" parameters for each temperature. With the help of the "low" and "high" models, designers can be confident that their nominal designs would still work in worst case situations created due to process variations across the wafer and from wafer to wafer.

**Circuit Design and Testing**

In 2009, we fabricated our first lot of devices and operational amplifiers. Operational amplifiers designed with depletion mode MOSFETs achieved 60dB gain at room temperature and 57dB gain at 300°C. Stress test at 300°C shows that operational amplifiers are still operational after 100 hours of continuous operation. The output voltage saw significant drift over this 100 hours, Figure 2. The first lot operational amplifiers were not used in feedback because their output voltage range did not overlap with input voltage range. We modified the design using updated simulation models in the second lot.

In the first lot, we were checking the layout by hand, which proved to be tedious and prone to errors. In the second lot, we started using layout versus schematic (LVS) tool, which is computer software that checks the layout for correctness against the schematic definition. This tool improved our design speed and accuracy. We also check each design with a design rules check (DRC), which ensures that the physical design of the devices and circuits will be within fabrication capability limits. For example, the fabrication process has a minimum line width that we have to comply; otherwise the line may end up disappearing and the design would not be fabricated correctly.

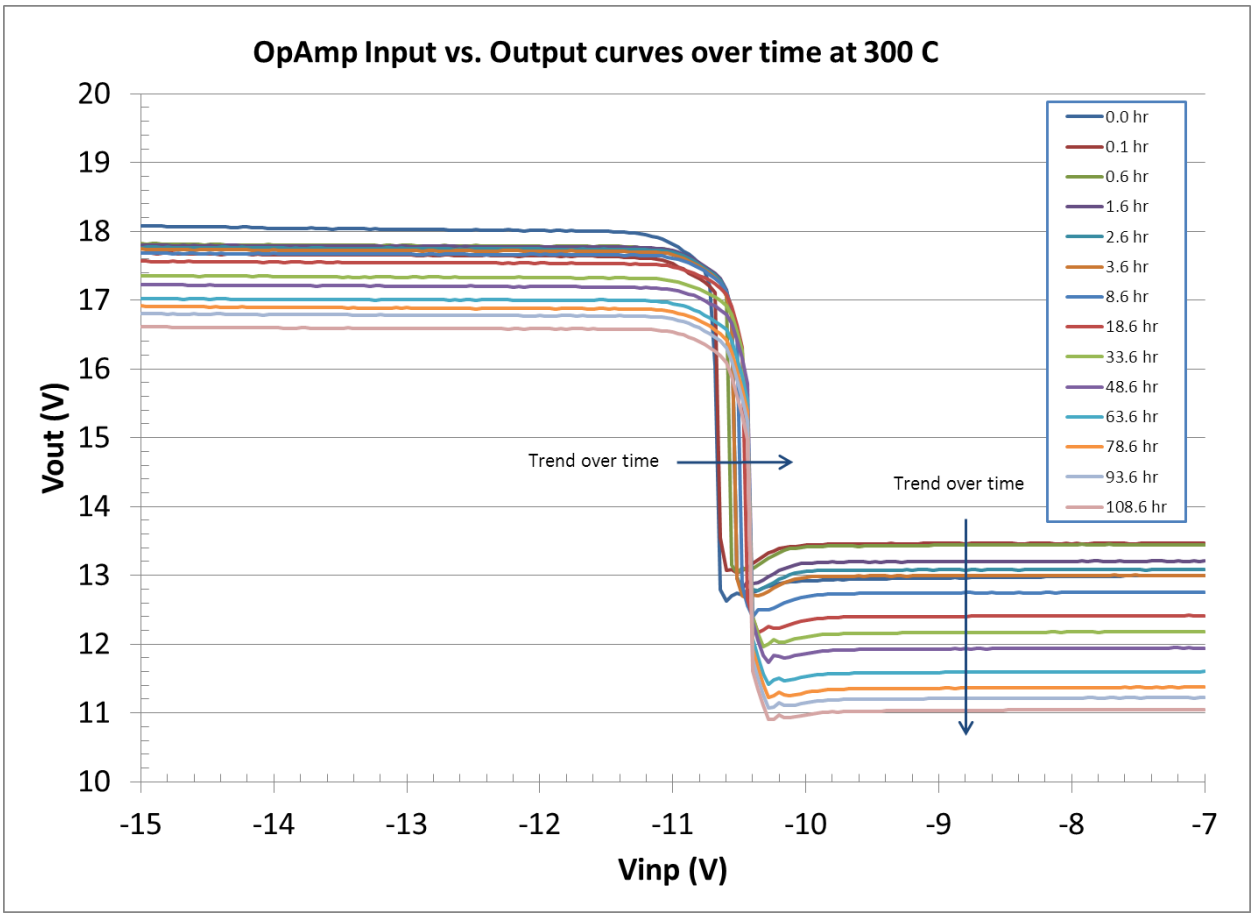



Figure 2. Stress test results from operational amplifier in first lot over 100 hours

In 2010, our second lot of analog circuits yielded working operational amplifiers with lower gain compared to what we expected. We could use these operational amplifiers with closed loop feedback, because their output voltage levels overlapped with input levels. A temperature to frequency conversion circuit using SiC operational amplifiers and off-chip resistors and capacitors was packaged on ceramic circuit boards and stress tested at 300°C and operated for 240 hours. The SiC operational amplifier attached to a dual-inline package (DIP) was operational at 300°C for more than 1000 hours. Figure 3 is a photograph of a SiC operational amplifier.

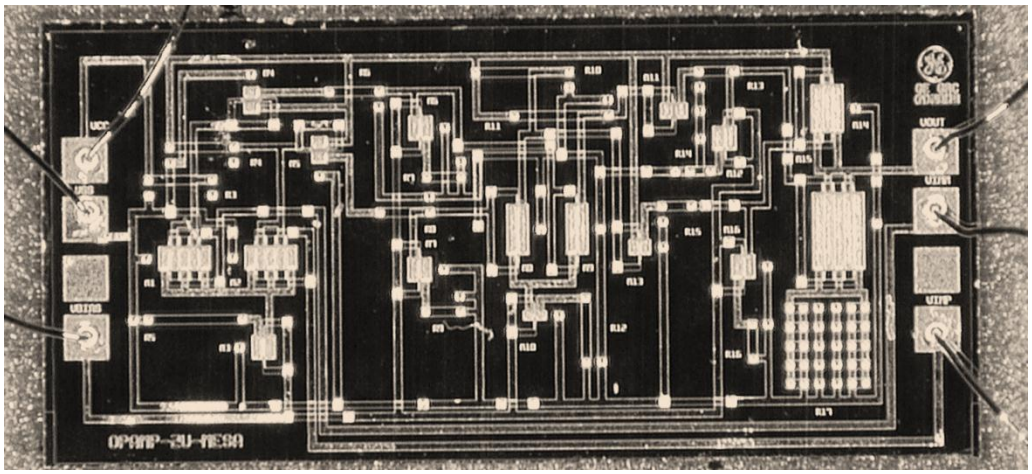



Figure 3. Microphotograph of SiC operational amplifier

In 2011, operational amplifiers were designed using enhancement mode MOSFETs and n-channel resistors. Open loop gain was in the 46dB to 50dB range. This is the first time we build operational amplifiers using enhancement mode MOSFETs. The measured results match well with our simulation models, which give us confidence in the repeatability of future enhancement mode MOSFETs and circuits. At 300°C, the amplifier gain increases to 58dB.

A preliminary datasheet was generated based on available data for the enhancement mode operational amplifier design:

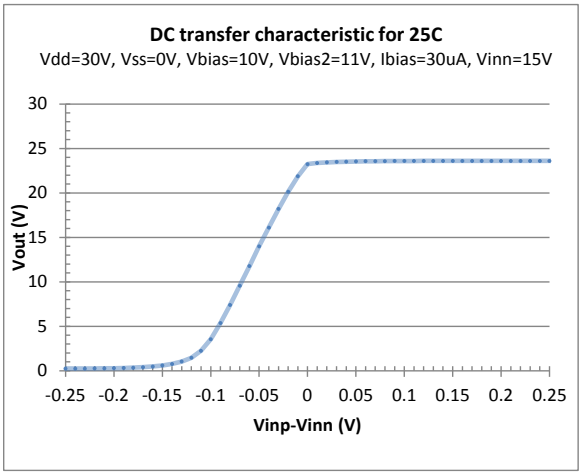
## ABSOLUTE MAXIMUM RATINGS

| | | Value | Unit |
|---|---|---|---|
| $V_S$ = VCC-VSS | Supply Voltage | 50 | V |
| $V_{IN}$ | Input Voltage | VSS to VCC | V |
| | Output Short-Circuit | Continuous | |
| $T_A$ | Operating Temperature | -55 to 300 | °C |
| $T_{STG}$ | Storage Temperature | -55 to 300 | °C |
| $T_J$ | Junction Temperature | 300 | °C |

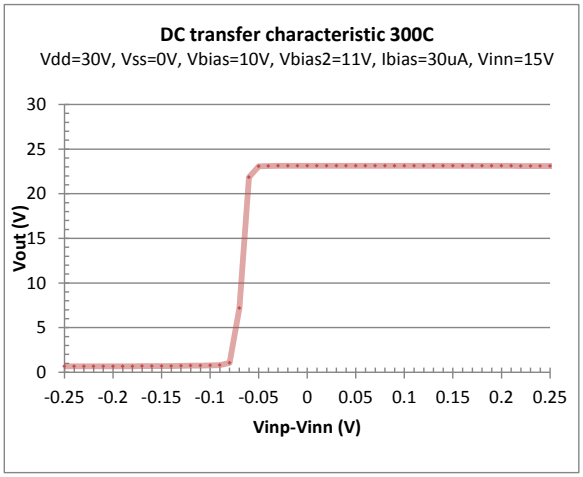
## ELECTRICAL CHARACTERISTICS: $V_S$= ±15 V

$R_L$=10kΩ, $V_{CM}$ = $V_{OUT}$ = midsupply, unless otherwise noted.

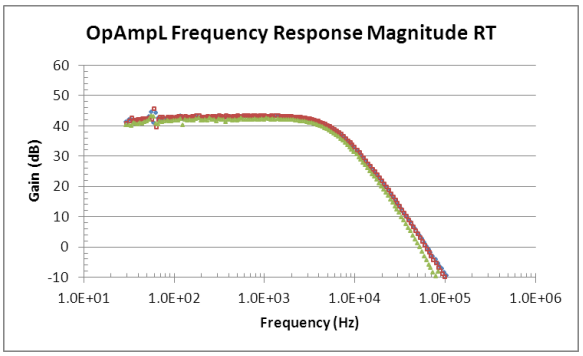
| | | | $T_A$ = 25°C | | | $T_A$ = 300°C | | | |
|---|---|---|---|---|---|---|---|---|---|
| **PARAMERTER** | | **CONDITIONS** | **MIN** | **TYP** | **MAX** | **MIN** | **TYP** | **MAX** | **UNIT** |
| **OFFSET VOLTAGE** | | | | | | | | | |
| Input Offset Voltage | $V_{OS}$ | $V_S$=30V | | ±100 | ±200 | | ±100 | ±200 | mV |
| **INPUT BIAS CURRENT** | | | | | | | | | |
| Input Bias Current | $I_B$ | | | ±0.2 | ±1 | | ±1 | ±10 | pA |
| Offset Current | $I_{OS}$ | | | ±0.1 | ±0.5 | | ±0.5 | ±5 | pA |
| **INPUT VOLTAGE RANGE** | | | | | | | | | |
| Common-Mode Voltage Range | $V_{CM}$ | | VSS+5 | | VCC-10 | VSS+5 | | VCC-14 | V |
| **INPUT IMPEDANCE** | | | | | | | | | |
| Differential | | | | 10M ‖ 1 | | | 10M ‖ 1 | | Ω ‖ pF |
| Common-Mode | | | | 10M ‖ 1 | | | 10M ‖ 1 | | |
| **OPEN-LOOP GAIN** | | | | | | | | | |
| Open-Loop Voltage Gain | $A_{OL}$ | | 40 | 46 | | 49 | 59 | | dB |
| **FREQUENCY RESPONSE** | | | | | | | | | |
| 3-dB Bandwidth | BW | | | 6 | | | 6 | | kHz |
| Unity Gain Bandwidth | GBW | | | 60 | | | 60 | | kHz |
| **OUTPUT** | | | | | | | | | |
| Voltage Output | $V_{OUT}$ | | VSS+1 | | VCC-7 | VSS+1 | | VCC-7 | V |
| Short-Circuit Current | $I_{SC}$ | | | ±2 | | | ±2 | | mA |
| **POWER SUPPLY** | | | | | | | | | |
| Supply Voltage | $V_S$ | | ±15 | | ±25 | ±15 | | ±25 | V |
| Supply Current | Iss | | | 2 | 3 | | 6 | 8 | mA |
| **TEMPERATURE RANGE** | | | | | | | | | |
| Operating Range | | 25°C to 300°C | | | | | | | |



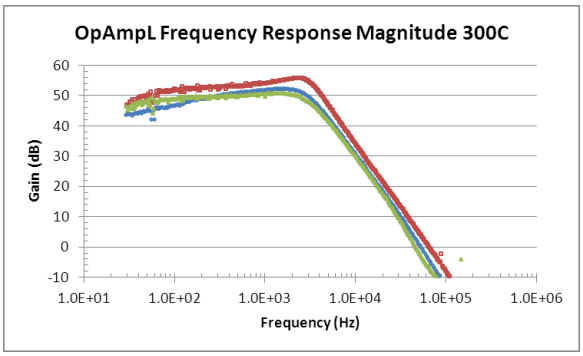

DC Large Signal Output Swing, 25°C




DC Large Signal Output Swing, 300°C




Small Signal Frequency Response, 25°C




Small Signal Frequency Response, 300°C

These amplifiers were packaged to build temperature to frequency conversion circuits and the functionality was verified to be in line with expectations.

Some shortcomings of the enhancement mode operational amplifier include lower gain, lower output current drive capability and lower bandwidth. This is due to the inherent lower transconductance of enhancement mode MOSFETs compare to depletion mode MOSFETs that we have built in previous lots. The gain and drive current disadvantages can be remedies to some extent by increasing transistor sizes, at the expense of larger die area. We also have the ability to use both enhancement mode and depletion mode MOSFETs to take advantage of both types of devices.

**Ceramic Circuit Board Packaging**

To survive and operate at 300°C, we cannot use traditional organic polymer based materials for the circuit board to hold the circuit components. Our first candidate board material is alumina. The substrate is fabricated with a thick film gold metallization and selective dielectric printing is used to allow a second metal to cross over the first. The SiC operational amplifier and surface

mounted capacitors and resistors are attached to the alumina substrate directly. Electrical connections to the SiC die are made with gold wirebonds. The board fabrication and component assembly were done at Auburn University by Dr. Wayne Johnson and his team. A fully assembled temperature to frequency converter board using the alumina substrate is shown in Figure 4.

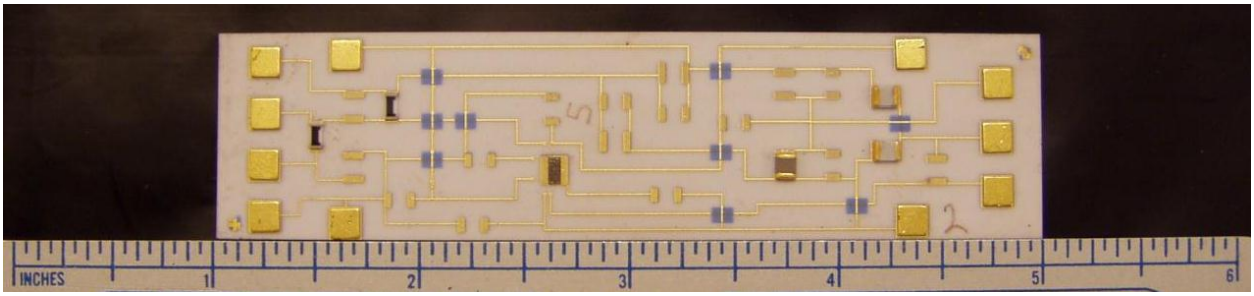



Figure 4. Assembled temperature to frequency converter board on the alumina substrate.

We also studied the use of low temperature co-fired ceramic (LTCC) as board packaging substrate for high temperature operation. This is an alternate to the alumina substrate. The advantage of LTCC is that it can be extended to have multiple conductor layers for high complexity circuits. The down side is its high material cost and needing to account for material shrinkage after firing. The substrates were fabricated by Omega Micro Tech, and component assembly was done at Auburn University. A fully assembled temperature to frequency converter board is shown in Figure 5.

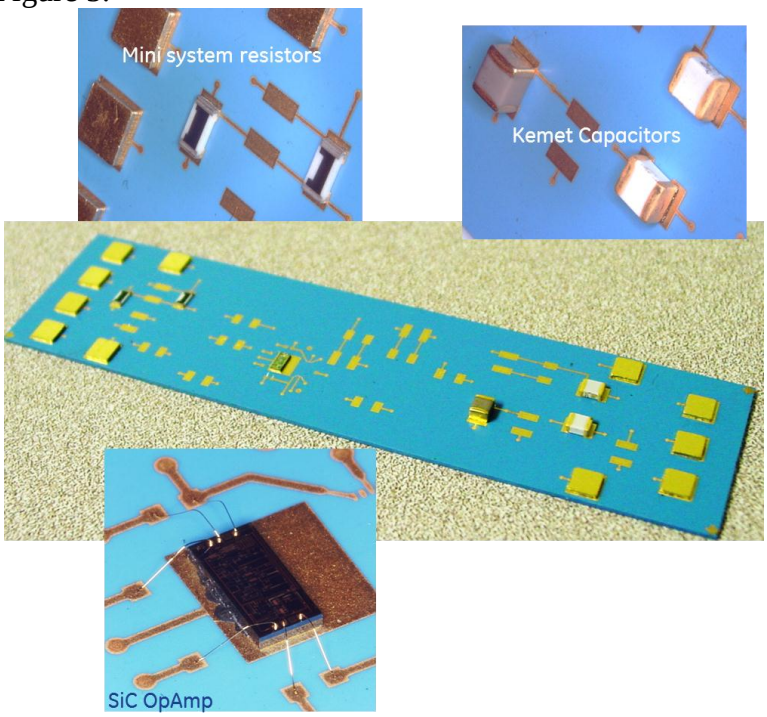



Figure 5. Assembled LTCC temperature to frequency converter board.

## Capacitor Life Testing

We sourced high temperature rated capacitors from TRS, Nova Cap, and Kemet. The detailed parts information is listed in Table 1.

**Table 1. Sourced capacitor list.**

| Component Type | Supplier | Part number | Value | Voltage | Dielectric | Rated Temp |
|---|---|---|---|---|---|---|
| Capacitor | TRS | HT-300 | 0.1 µf | 50 | HT-300 | 300 |
| Capacitor | TRS | HT-300 | 1.0 µf | 50 | HT-300 | 300 |
| Capacitor | Nova cap | 1210H104K100PH | 0.1 µf | 10 | NBT, Class II | 230 |
| Capacitor | Kamet | C1210C104K5GAC | 0.1 µf | 50 | Class I | 250 |
| Capacitor | Kamet | C2220C474K5GAC | 0.47 µf | 50 | Class I | 250 |

We tested the capacitors for their temperature stability across temperature and saw that the Kemet capacitors had the best temperature stability overall. A sample test result is shown in Figure 6.

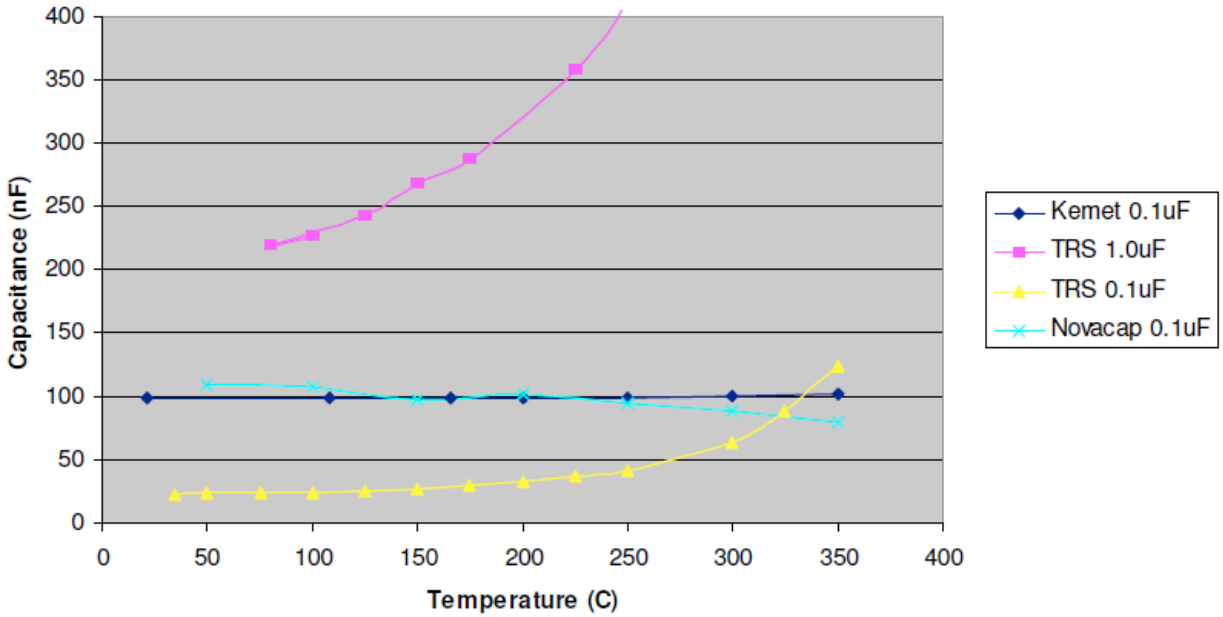



Figure 6. Capacitance versus temperature of commercial surface mount capacitors.

We tested the capacitor stability over time at 300°C with 50V bias for the Novacap and Kemet capacitors. Both show stable capacitance within 3% to 5% over 7000+ hours. Figure 7 shows an example of the test data.

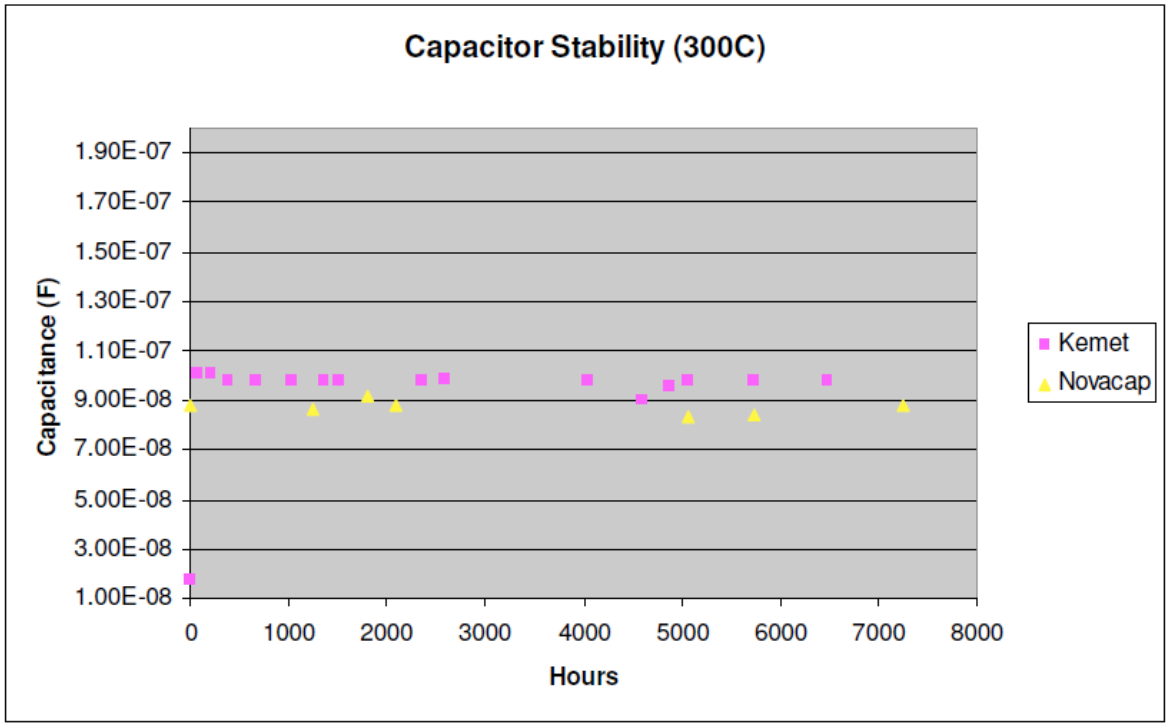



Figure 7. Capacitor stability test at 300°C.

Highly accelerated life test (HALT) of Kemet capacitors found significant differences in life with variations in plating processes. Figure 8 shows the capacitors with different termination metallization. The original Kemet capacitors were offered in either tin (Sn) or AgPd terminations with nickel (Ni) underneath. Because these termination materials were not compatible with our attachment process at 300°C, effort was made to strip the tin and re-plate with gold (Au). Later, Kemet was able to supply capacitors with Au termination, and we compare the test results in Figure 9. The "Immersion Au over Ni" test group (Au plated at GE Research) was found to have a significantly lower life than the "Initial Ni only" group. A repeat of the initial group ("Ni only Stripper#3) shows some improvement toward the initial testing. The sample group that was plated at the supplier ("Kemet Ni/Au") shows some improvement over the initial test group. This improvement indicates that future capacitors can and should be sourced with Ni/Au terminations. For the board assembly, "Kemet Ni/Au" capacitors have been selected with their lifetime estimated at 17,000 hours at 300°C with bias voltage of 30V.

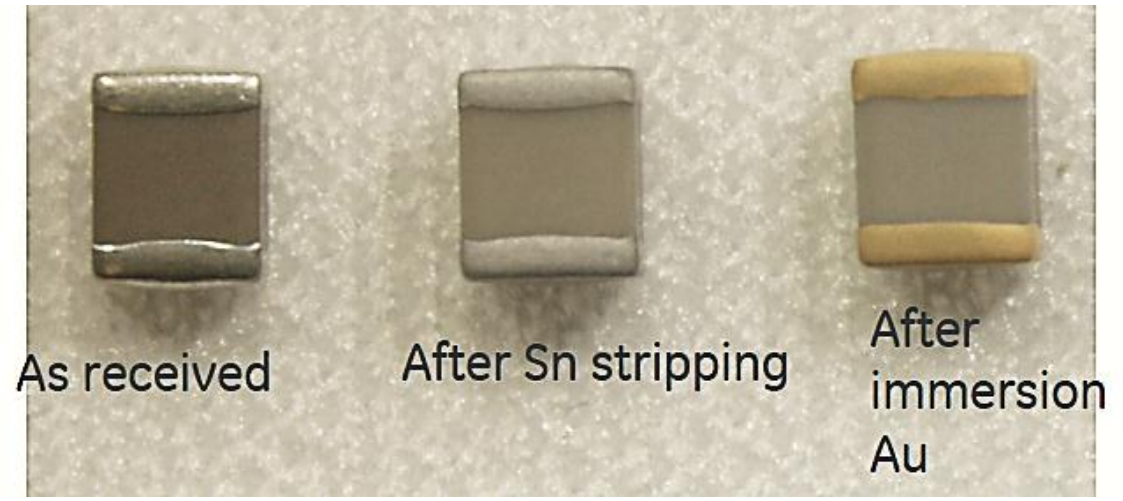



Figure 8. Capacitors with different termination metalizations.

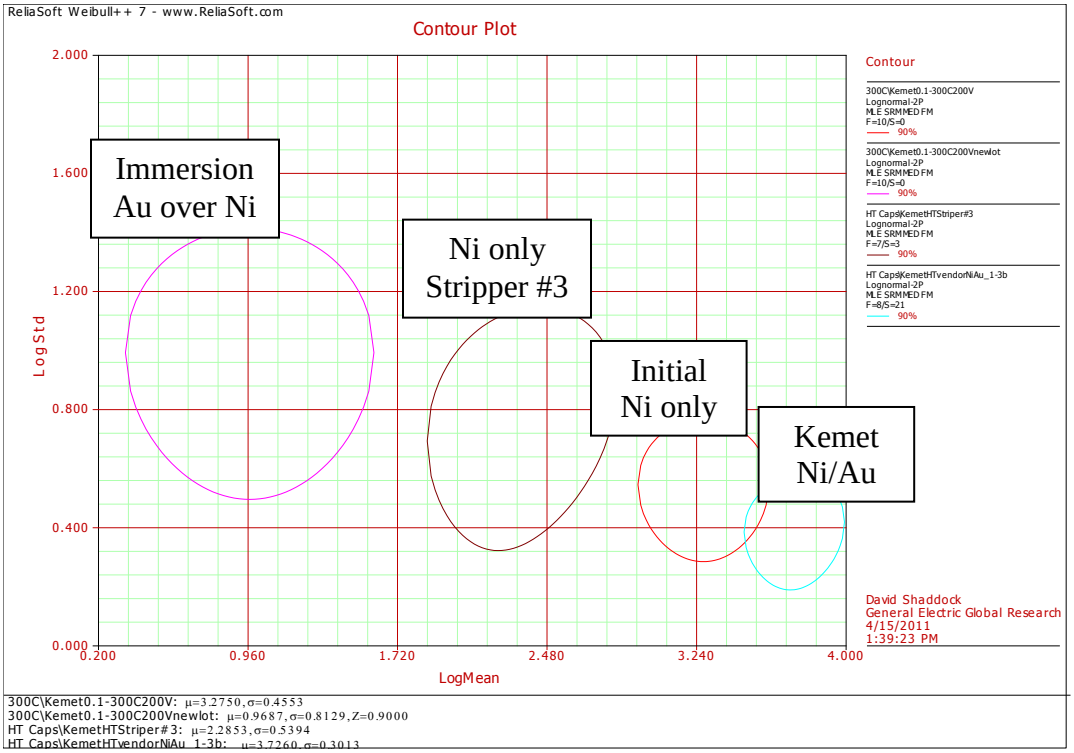



Figure 9. Contour plot of lognormal distribution parameters indicates difference between test groups (lower right is better)

**Resistor Life Testing**

Resistors were sourced from Vishay and Mini-Systems. Vishay resistors were wire-wound and Mini-Systems were thick film resistors. Detailed parts information is listed in table 2.

**Table 2. Sourced resistor list.**

| Component Type | Supplier | Part number | Value | Precision | Wattage | Rated Temp |
|---|---|---|---|---|---|---|
| Wire wound | Vishay | WSC45271K000FEK | 1K | 1% | 2 | 275 |
| Wire wound | Vishay | CW1/21K000HE12 | 1K | 3% | 0.5 | 250 |
| Wire wound | Vishay | CW0021K000HE12 | 1K | 3% | 5.5 | 350 |
| Wire wound | Vishay | CW00210K00HE12 | 10K | 3% | 5.5 | 350 |
| Thick Film | Mini-Systems | D55342K07U1E00C | 1K | 1% | 0.25 | 150 |
| Thick Film | Mini-Systems | D55342K07U10E0C | 10K | 1% | 0.25 | 150 |
| Thick Film | Mini-Systems | D55342K07U100EC | 100K | 1% | 0.25 | 150 |
| Thick Film | Mini-Systems | D55342K07U1P00C | 1M | 10% | 0.25 | 150 |

The Vishay resistors had plastic body that would melt during the attach process, so they were dropped from subsequent high temperature reliability tests.

Resistor HALT testing at 350°C was performed on Mini-Systems resistors. A power law model was generated with the exponent on the power term (n) equal to 3.8. The acceleration model is shown here where the ratio of power under test ($P_T$) and use power ($P_U$) is taken to the power of n.

$$AF = \left( \frac{P_T}{P_U} \right)^n$$

The distribution plot along with a prediction at use condition (1 mW) is shown in Figure 10. The predicted life at 1% failure at use condition is 4.1160E+11 hours.

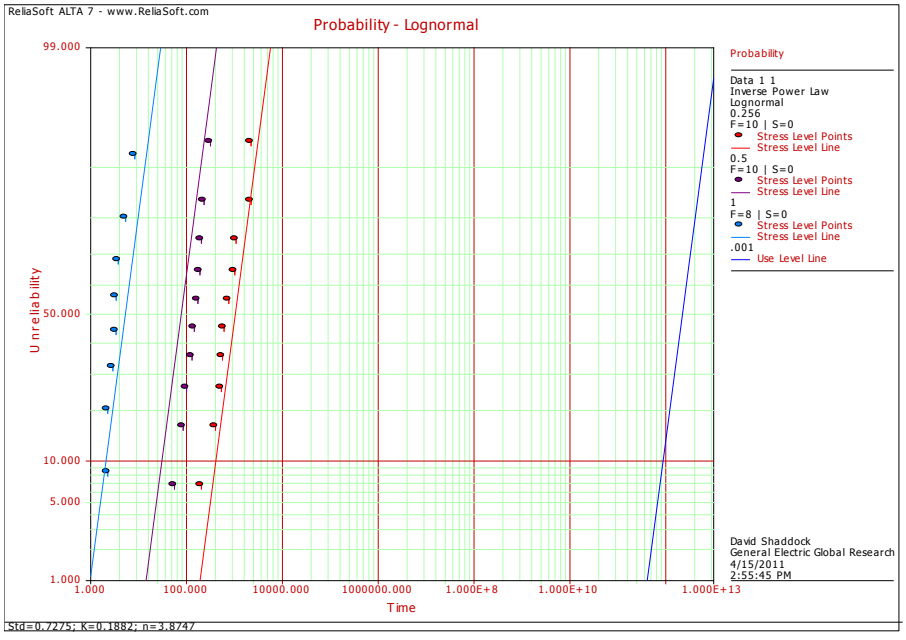



Figure 10 Resistor HALT testing model at 350°C with predicted life at use condition

**Reliability of Temperature to Frequency Converter Board**

A test bed was constructed to enable long-term testing of the high temperature boards at 300°C. The board under test was placed inside the oven maintaining constant temperature environment, while high temperature wiring provides electrical connections to the external power supplies and digital oscilloscope. A Labview-based software code has been developed and implemented to communicate with the measurement equipment and collecting oscillation waveform parameters and bias currents every two minutes. An external resistor placed outside of the oven environment was used to simulate the PT-1000 sensor element. The resistance was switched between 1.0k Ohm and 2.1k Ohm to record data for two different states, simulating high and low temperature sensor resistances.

One of the high temperature boards was tested for 250 hours without test interruptions after the oven temperature was brought up and stabilized at 300°C. The recorded oscillation frequencies at high and low resistance values are shown in Figure 11.

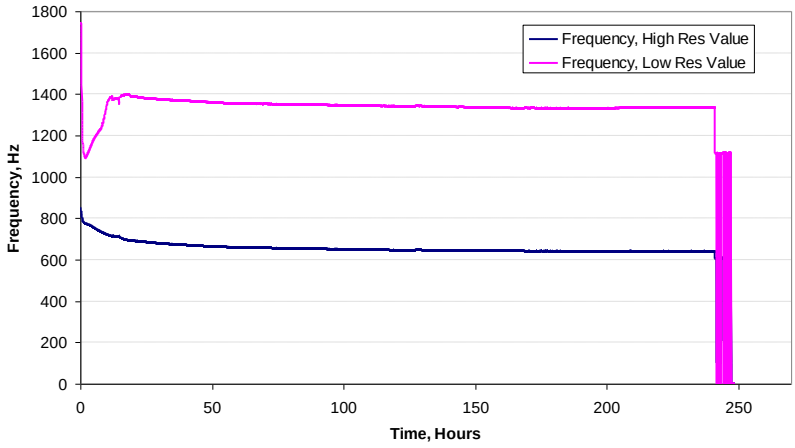



Figure 11. Oscillation frequencies at high and low resistance values

During the first 40 hours, oscillation frequencies were less stable than during the next 200 hours, which is an indication of initial "burn-in". After the initial "burn-in" period, the stability of frequencies was better than 2.5%. An indication of board malfunctioning was noticed at hour 240. The oscillation frequencies showed a step-like change and became unstable.

Another ceramic temperature to frequency converter board was tested in the oven at 225°C for more than 1,000 hours and survived continuous operation, Figure 12.

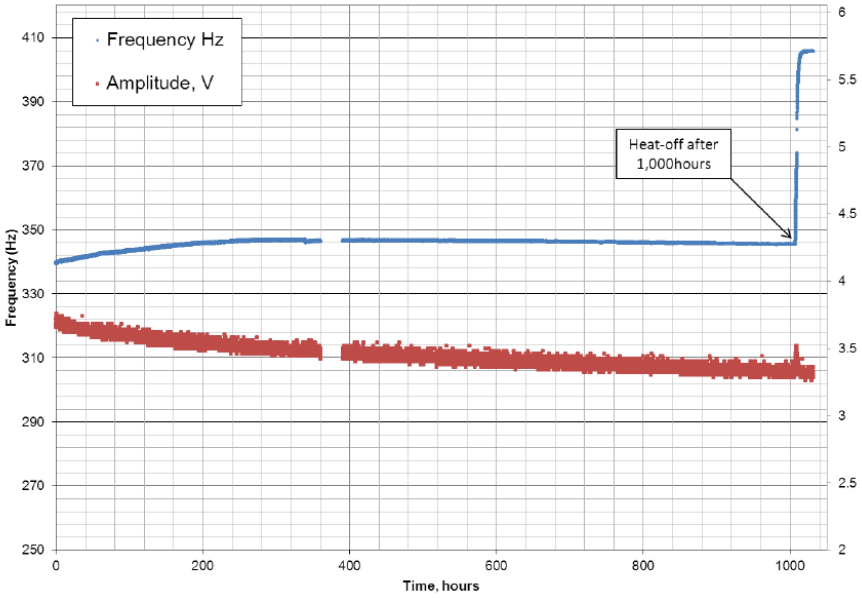



Figure 12. Gen 1 temperature to frequency converter board long term test at 225°C.

Five Gen-1 alumina boards were assembled using SiC components picked from wafers DC-14 and BJ-18, processed in the second lot. Board #5 with DC-14 SiC components has demonstrated continuous operation for more than 400 hours, but output instabilities were seen starting at 170 hours.

Board #2 was tested at a constant resistance value, reducing potentially any issues which could be caused by the resistance switching events and affecting longevity.

The instabilities in the frequency output of board #2 were correlated partially to the light mechanical shock caused by occasional tapping on the test oven, which indicated a potential problem with attachment of some passive components. The most likely failure mechanism was proposed as an electrical open in the capacitor bonding pads due to poor mechanical adhesion. On several boards shipped after the assembly from Auburn University to GE Research, some feedback capacitors were found detached during shipping, which points to the capacitor attach as a likely problem. Besides the attachment, capacitor metallization done at GE Research prior to board assembly is also suspected for introducing poor adhesion of plated Au layer to the Ni capacitor contacts.

Several DIP-packaged op-amps were evaluated at 300°C as part of the oscillator circuit with the rest of components placed outside the oven. The results of the test were quite different from the results of the board testing.

The first op-amp circuit DIP#1 placed in the test has survived 1,000 hours and the test was stopped after that without a failure. The output frequency was observed occasionally, but stability and low drift of the output signal were noted. Several frequency data-points were sampled during the test and are shown in Figure 13 below. We noted an initial burn-in period followed by a slow drift of output frequency and oscillation duty cycle. Several more DIP packaged devices were evaluated to get more statistical data. Most of the long-term tests were stopped after reaching 100 hours, but no failures were detected.

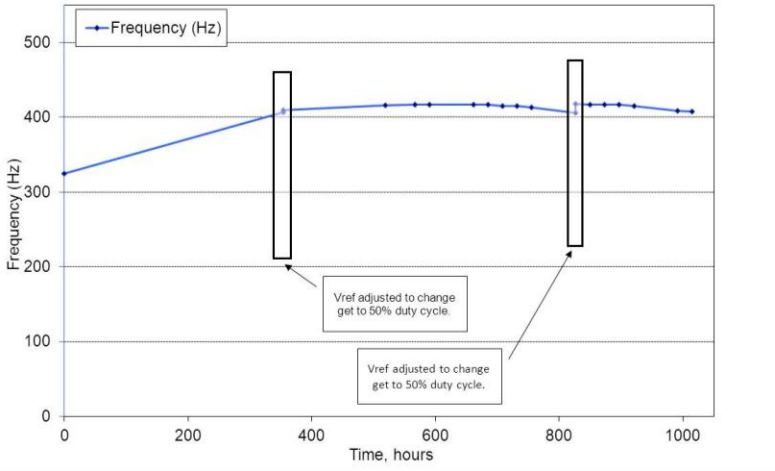



Figure 13. DIP-packaged op-amp: frequency output tested at 300°C with constant feedback resistor.

The total accumulated test time was 740 hours for temperature to frequency boards and 1428 hours for DIP-packaged op-amps. The board mean time to failure was estimated to be 92.5 hours, while DIP-packaged op-amps yielded at least 360 hours or better mean time to failure (some tests were interrupted before failures were observed), see Figure 14 below. The observed difference in the time before failure indicates additional failure mechanisms introduced by the board assembly and passive components attach.

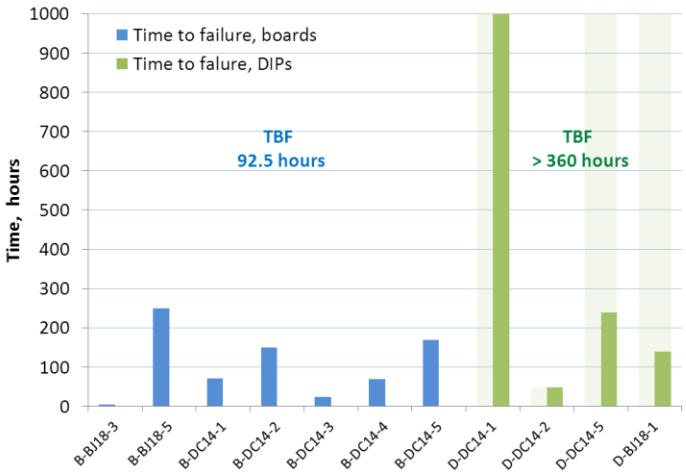



Figure 14. Time to failure of temperature to frequency converter circuits; boards and operational amplifiers in DIPs

A second generation alumina circuit board for the temperature to frequency converter circuit was designed and fabricated at Auburn University. Figure 15 below shows the optimized circuit board with SiC operational amplifier and passive components attached. The board was compacted to fit into a large DIP package, shown in Figure 16.

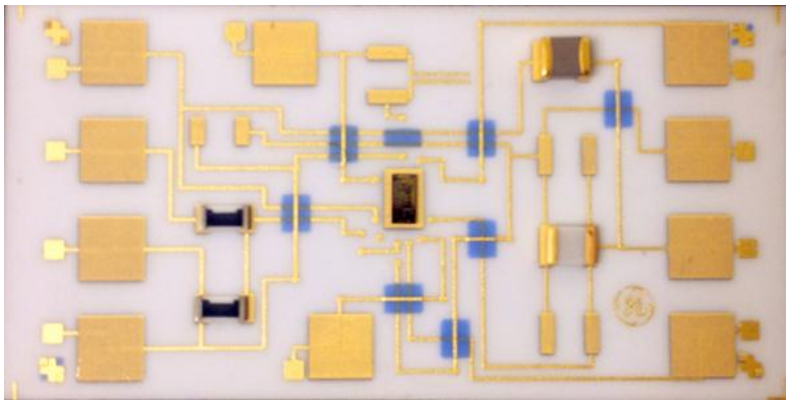


Figure 15. Second generation alumina temperature to frequency converter board.

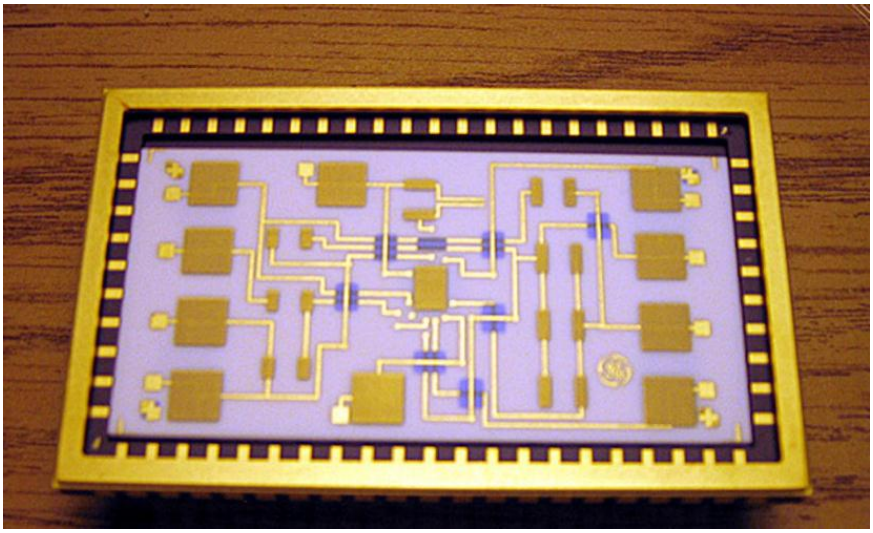


Figure 16. Second generation alumina temperature to frequency converter board fitted inside a DIP.

Temperature to frequency converter circuit built using the enhancement mode operational amplifiers in the third lot was tested and a frequency versus temperature data is shown in Figure 17.

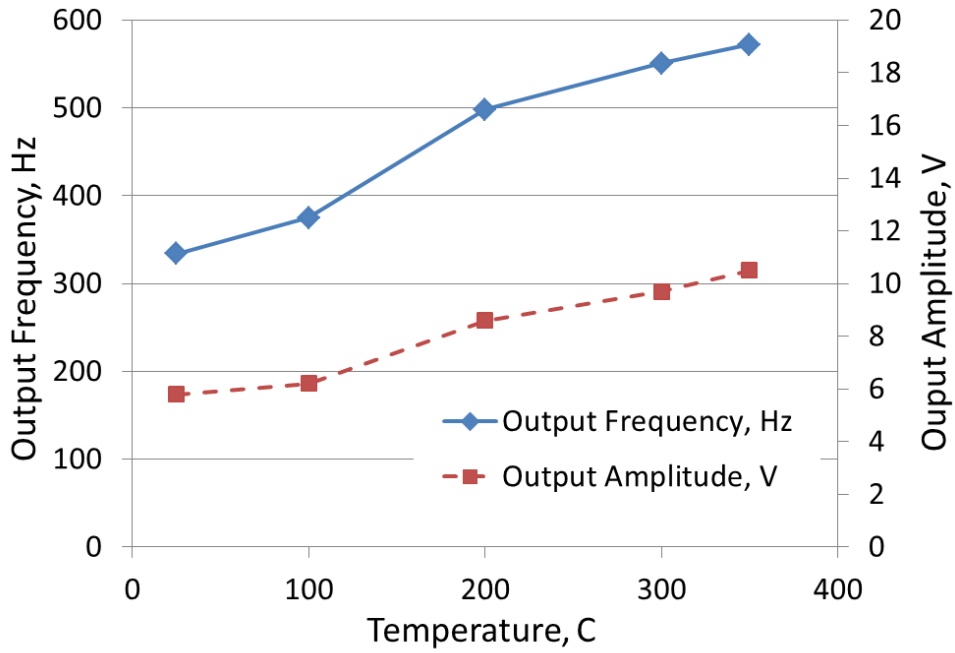
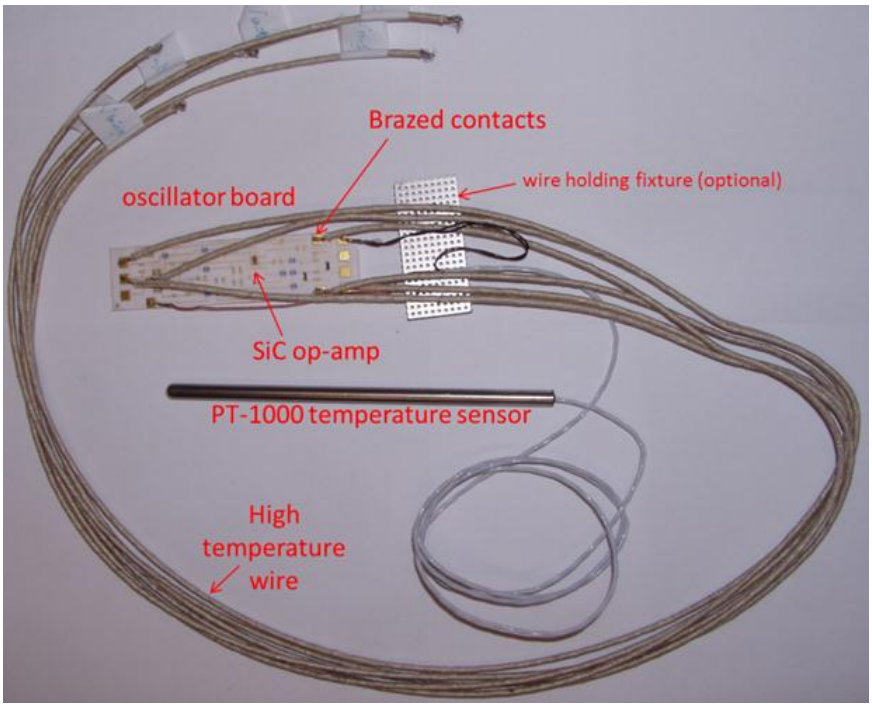



Figure 17. Output frequency vs. temperature of temperature to frequency converter using enhancement mode operational amplifiers in lot 3.

Several operational amplifiers were tested using the same test bed as in the previous temperature to frequency circuit test with the oven at 300°C. Most of the operational amplifiers were failing shortly after 24 hours. Failure analysis indicated that MOSFET gate oxides were damaged due to too high of a supply voltage to the circuit. We expect future enhancement mode circuits will have much longer life when designed with reduced supply voltage. For the final temperature to frequency converter demonstration, we chose to use the Gen 1 board with the depletion mode operational amplifiers from the second lot.

**Temperature to Frequency Sensor Electronics**

In the final task of the project, we built a prototype temperature-to-frequency converter and tested it at 300°C. The lifetime of all system components has been evaluated and shown in the table next to the picture of the prototype, Figure 18.




| Lifetime test summary, 300°C | |
|---|---|
| SiC operational amplifier | >1,000 hours |
| resistors | 1010 hours |
| capacitors | 17,000 hours |
| ceramic board | very little degradation |
| die attach and bonding | >1,500 hours |

Figure 18. Integrated temperature sensor system

The prototype is a resistance to frequency converter (oscillator), where the sensor element is a temperature sensitive resistor (PT-1000). High temperature insulated wires were brazed to the contact pads of the assembled sensor electronic ceramic board. PT-1000 temperature sensor was connected to the resistive feedback loop of the oscillator using the same high temperature brazing process.

The temperature to frequency converter is based on an operational amplifier multivibrator design, Figure 19. An RC circuit sets the frequency of oscillation. A resistor divider network is provided from the output to the non-inverting input of the amplifier. This provides the feedback necessary to set the high-low and low-high transition points. The ratio of the resistors in the divider also sets the hysteresis level of the circuit. In this design, the resistor in the aforementioned RC circuit is a PT-1000.

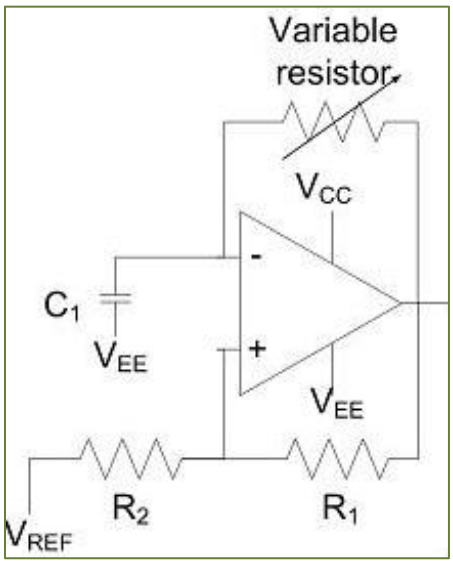



Figure 19. Schematic of a multivibrator-based oscillator as temperature to frequency converter

The PT-1000 has a resistance that is proportional to temperature. At 0°C, it exhibits resistance of 1000 Ohms. As temperature increases, the resistance increases by approximately 3.9 Ohms per °C at lower temperatures, and 3.5 Ohms per °C at 300°C. At 300°C, the PT-1000 exhibits a resistance of 2120 Ohms.

As the resistance of the PT-1000 increases, the RC time constant increases, and the overall frequency of oscillation decreases as a function of resistance. Additionally, as the output signal swing changes, the oscillation frequency also changes. As the output signal swing decreases, the hysteresis band also reduces, thus increasing the operating frequency of the circuit for the same resistance value. The operational amplifiers used in this design do not have rail-to-rail output capability. Additionally, as temperature increases, the output swing reduces causing the oscillation frequency to shift higher. Figure 20 shows an example output waveform from the temperature to frequency converter circuit.

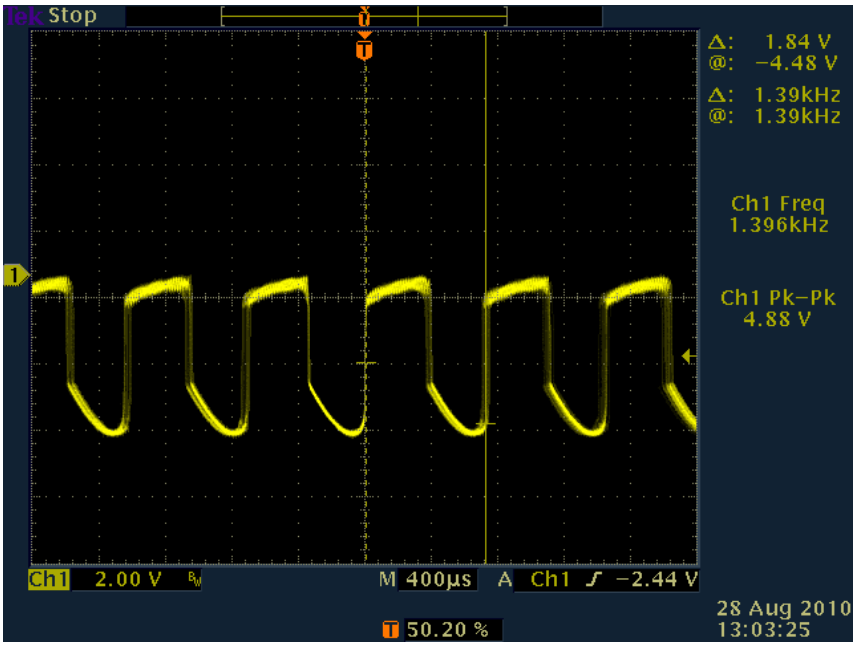



Figure 20. Example output waveform of the temperature to frequency converter circuit.

The temperature sensor system has been tested to obtain calibration curve of oscillation frequency versus temperature, Figure 21. All the components used to assemble temperature sensor system were proved to survive 300°C for at least 1,000 hours.

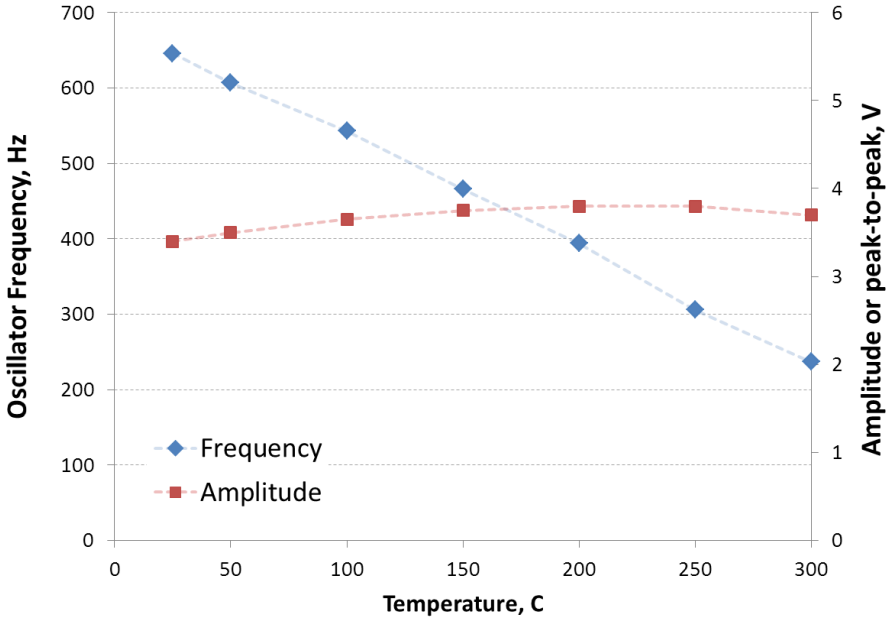



Figure 21. Frequency versus temperature test of SiC-based temperature sensor prototype

The developed prototype is a unique demonstration of SiC technology and high temperature packaging technology that show the feasibility of a packaged sensor electronic system for 300°C operation for extended time. Our studies have shown that active circuit components such as operational amplifiers can be designed and fabricated using SiC MOSFETs and resistors, and they can be used at 300°C continuously. Existing commercial surface mount capacitors and resistors have sufficient lifetime at use condition at 300°C. Ceramic-based circuit boards and component assembly processes are developed and proven to be reliable for high temperature operation. This set of technologies can be used to further the development of down-hole tools for geothermal exploration and well monitoring.

**Publications Generated in this Project:**

V. Tilak, C-P Chen, P. Losee, E. Andarawis and Z. Stum, "Development of a 300°C capable SiC based operational amplifier", Proc. High Temperature Electronics Conf., Albuquerque, NM, May 11-13, 2010.

D. Shaddock, V. Tilak, T. Zhang, R. Zhang and R. Wayne Johnson, "Reliability assessment of passives for 300°C using HALT", Proc. High Temperature Electronics Conf., Albuquerque, NM, May 11-13, 2010.

R. Zhang, R. Wayne Johnson, V. Tilak, T. Zhang and D. Shaddock, "Characterization of Thick Film Technology for 300°C Packaging", Proc. High Temperature Electronics Conf., Albuquerque, NM, May 11-13, 2010.

Z. Stum, V. Tilak, C-P Chen, P. Losee and E. Andarawis, "300°C Silicon Carbide Integrated Circuits", Materials Science Forum Vols. 679-680, pp 730-733, 2011.

A. Kashyap, C. Chen, V. Tilak, "Compact modeling of silicon carbide lateral MOSFETs for extreme environment integrated circuits," International Semiconductor Device Research Symposium (ISDRS), 2011.

D. Shaddock, "Reliability Assessment of Passives for 300°C and 350°C using HALT", High Temperature Electronics Network, Oxford, UK, July 18-21, 2011.

T. Zhang, D. Shaddock, A. Vert, R. Zhang and W. Johnson, "Characterization of LTCC-Thick Film Technology for 300°C Packaging", High Temperature Electronics Network, Oxford, UK, July 18-21, 2011.