

EFFECTS OF RELIABILITY SCREENS ON MOS CHARGE TRAPPING*

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Abstract

The effects of pre-irradiation elevated-temperature bias stresses on the radiation hardness of field-oxide transistors have been investigated as a function of stress temperature, time, and bias. Both the stress temperature and time are found to have a significant impact on radiation-induced charge buildup in these transistors. Specifically, an increase in either the stress temperature or time causes a much larger negative shift (towards depletion) in the I-V characteristics of the n-channel field-oxide transistors. This increased shift in the transistor I-V characteristics with stress temperature and time suggests that the mechanisms responsible for the stress effects are thermally activated. An activation energy of ~ 0.38 eV was measured. The stress bias was found to have no impact on radiation-induced charge buildup in these transistors. The observed stress temperature, time, and bias dependencies appears to be consistent with the diffusion of molecular hydrogen during a given stress period. These results have important implications for the development of hardness assurance test methods.

I. INTRODUCTION

Reliability screens are normally required for electronics in space and military systems. Some types of reliability screens include elevated-temperature biased stresses. For instance, devices are usually subjected to a 150°C one-week "burn-in" for reliability testing, which is considered non-destructive, and is typically performed on IC deliverables to reduce the possibility of "infant mortality." In addition, dynamic screens are often required on all ICs delivered for some system applications. Dynamic screens are often performed at elevated temperatures (125°C) for several days. Thus, during the course of routine reliability testing, devices assembled into a system may have been subjected to several elevated-temperature biased stresses before system application.

*This work performed at Sandia National Laboratories was supported through the Defense Nuclear Agency's Hardness Assurance and Basic Mechanisms Programs and by the Department of Energy under contract No. DE-AC04-94AL85000.

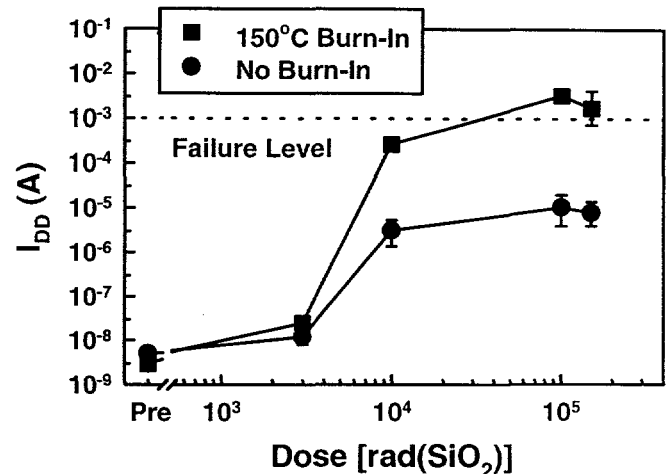


Figure 1: Static power supply leakage current for octal buffer/line drivers with (squares) or without (circles) a pre-irradiation 150°C stress. The dashed line represents a failure level of 1 mA. (After Ref. [10].)

Most previous work on the effects of temperature on MOS radiation response concentrated on the effects of elevated-temperature stresses during [1-3] or after [1,2,4-6] irradiation, rather than prior to irradiation. Previous work [7] using thermally-stimulated-current measurements showed that repeated bias-temperature bakes after an initial stress do not significantly affect the subsequent charge trapping properties of some gate oxides. However, the effects of the "initial" bias-temperature bake on the radiation response of these devices was not examined. Further, for many advanced radiation-hardened and commercial technologies, the radiation response is significantly affected by the response of field-oxide transistors which were not considered in Ref. [7]. The radiation response of field oxides can be considerably different from that of gate oxides [6,8,9].

Recently, we have shown that the radiation response of an MOS device can change dramatically if the device is exposed to a pre-irradiation elevated-temperature biased stress [10]. The effect of a pre-irradiation biased stress on an IC is illustrated in Figure 1. This figure is a plot of the change in standby power supply leakage current, I_{DD} , versus dose for commercial octal

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buffer/line drivers. Note that the maximum value of I_{DD} is 300 times higher for ICs exposed to a 150°C, one-week pre-irradiation stress than for ICs not exposed to a pre-irradiation stress. In addition, a pre-irradiation stress has been shown to affect other IC parameters (e.g., timing). Similar effects were also observed in radiation-hardened technologies, suggesting that these results may be observed in a wide range of technologies (commercial and radiation hardened). Results similar to Ref. [10] have recently been observed by others [11] for ICs packaged in ceramic and plastic packages.

The cause of the differences in radiation response due to a pre-irradiation stress has been attributed to the reduced buildup of radiation-induced interface traps for parasitic field-oxide and gate-oxide transistors exposed to a pre-irradiation stress [10]. For the ICs and irradiation conditions examined in Ref. [10], less interface-trap buildup leads to larger negative n-channel threshold voltage shifts, causing an increase in the standby power supply leakage current and a decrease in timing degradation for ICs.

In order to account for these effects in a hardness assurance program, questions concerning the dependence of radiation response on pre-irradiation stress temperature, bias, and time must be addressed. These questions were not addressed in Refs. [10] or [11]. In this work, we investigate the effects of elevated-temperature biased stresses on the radiation response of field-oxide transistors over a wide range of temperatures, times, and biases. We focus on the radiation response of field-oxide transistors, because they normally play a dominant role in the radiation response of advanced MOS technologies. This is because reductions in oxide thickness have made gate oxides less sensitive to radiation.

II. EXPERIMENTAL DETAILS

We examine field-oxide transistors fabricated in Sandia's CMOS IIIA technology [12]. The CMOS IIIA technology uses radiation-hardened process techniques for both the gate and field oxide. This technology uses 2- μ m design rules. The field-oxide transistors were formed by fabricating transistors with the field oxide as the gate dielectric. The field-oxide thickness was approximately 800 nm.

The design of the field-oxide transistor includes a parasitic gate-oxide transistor in series. This limits threshold-voltage measurements and stress biases to

applied voltages of less than 30 V in order to avoid breakdown of the parasitic gate-oxide transistors. We were unable to measure the post-irradiation response of p-channel field-oxide transistors because irradiation causes an increase in the magnitude of the threshold voltage beyond -30 V. Thus, we can not perform charge separation measurements using the dual-transistor measurement technique on field-oxide transistors. (Recall that, to perform charge separation using the dual-transistor technique [13], one must have irradiation results for both n- and p-channel transistors.) We were also unable to perform single transistor midgap charge separation measurements on field-oxide transistors due to a "ledge" in the I-V characteristics (see Figure 2). We believe that this ledge may be caused by leakage along the field-oxide transistor edge. Because of these limitations we were unable to assess individual contributions of interface-trap and oxide-trapped charge to the total threshold-voltage shift.

I-V measurements were taken at room temperature before and after pre-irradiation stress and irradiation. Because of the I-V ledge, as discussed above, the transistors were characterized by measuring the voltage shift at a current of 10 nA (indicated by the dashed line in Figure 1). This is the current that corresponded to the extrapolated pre-irradiation threshold voltage (no ledge) of the n-channel field-oxide transistors.

For comparison, the radiation response of devices were evaluated with or without pre-irradiation elevated temperature biased stresses. Devices were stressed at various durations up to three weeks at temperatures of 100, 150, and 200°C. The gate-to-source bias, V_{GS} , during stress ranged from -5 to 20 V. The pre-irradiation stresses did not affect the device characteristics (i.e., the I-V characteristics of the transistors were the same before and after stress). This indicates that there were no measurable (classic) bias-temperature instabilities for the devices examined in this work.

Transistors were delidded and irradiated at room temperature using a 10-keV x-ray source at a dose rate of 1.67 krad(SiO_2)/s. The gate-to-source bias on the transistors during irradiation was 5 V. A minimum of two devices was evaluated per test condition.

III. RESULTS AND DISCUSSION

ICs are often exposed to numerous elevated-temperature stresses that vary in temperature, time, and

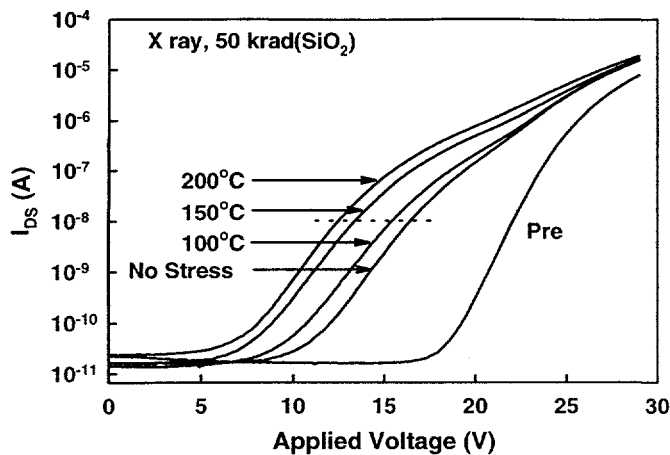


Figure 2: I-V curves for n-channel field-oxide transistors with or without a pre-irradiation one-week stress. The temperature during the stress was 100, 150, or 200°C. The gate-to-source irradiation and stress bias was 5 V.

bias. For example, exposure to elevated temperatures can occur during packaging, qualification, and actual system use. All of these conditions (temperature, time, and bias) are known to affect radiation-induced charge buildup and annealing in MOS devices [1-6]. In this section, we investigate the *pre-irradiation* stress temperature, time, and bias dependence of the radiation response of field-oxide transistors.

A. Temperature Dependence

The temperature dependence of stress on the radiation response of CMOS IIIA field-oxide transistors is illustrated in Figure 2. Figure 2 is a plot of a series of post-irradiation subthreshold current-voltage (I-V) curves measured on different transistors with no stress, or a 100, 150, or 200°C, one-week pre-irradiation stress. In addition to the post-irradiation curves, a typical pre-irradiation I-V curve is shown. The pre-irradiation voltage at 10 nA for all transistors examined in this work is 21.75 ± 0.25 V. The gate-to-source bias during stress was 5 V. The transistors were irradiated to a total dose of 50 krad(SiO₂) at a dose rate of 1.67 krad(SiO₂)/s and were characterized less than one minute following exposure. The I-V curves show that the radiation response of these field-oxide transistors depends on the stress temperature. As the pre-irradiation stress temperature increases, the I-V curves shift further to the left (toward depletion). The increase in the magnitude of the shift in the I-V curves with temperature suggests that the mechanisms causing the pre-irradiation stress effect are thermally activated. Many of the mechanisms responsible for radiation-induced charge buildup in oxides are thermally activated [4,14]. Although we

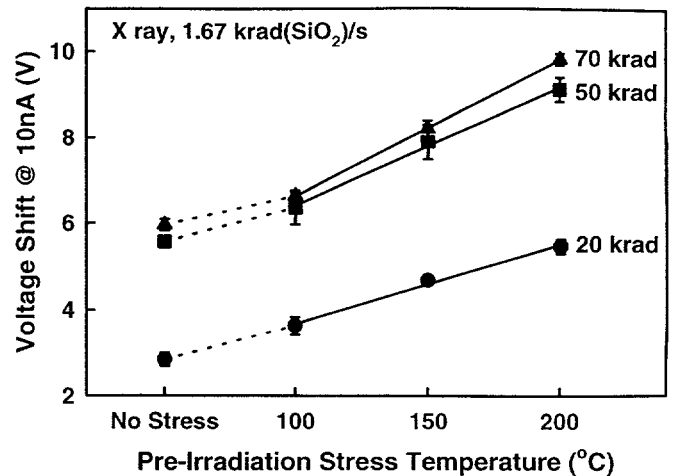


Figure 3: Voltage shift at 10 nA for field-oxide transistors plotted as a function of the pre-irradiation stress temperature. The radiation response of the transistors at total doses of 20, 50, and 70 krad(SiO₂) are shown. The gate-to-source irradiation and stress bias was 5 V.

cannot characterize the radiation-induced threshold-voltage shift due to interface- and oxide-trap charge, as discussed earlier, we can make some general comments about the charge buildup based on the I-V characteristics. The nearly parallel shift in the subthreshold region of the I-V curves suggests that pre-irradiation stress primarily enhances oxide-trap charge buildup in these devices. This is in contrast with the gate-oxide transistor data of Ref. [10], where a pre-irradiation burn-in for the gate-oxide transistors affected primarily the amount of radiation-induced interface-trap charge and had less effect on the amount of radiation-induced oxide-trap charge.

In Figure 3, we plot the change in voltage at 10 nA as a function of pre-irradiation stress temperature and total dose. The radiation response of the transistors is shown for total doses of 20, 50, and 70 krad(SiO₂). The voltage shift at 10 nA increases significantly with pre-irradiation stress temperature for all doses shown. The increase in voltage shift is linear with increasing stress temperature. At 20 krad(SiO₂), the voltage shift for transistors without a pre-irradiation stress is ~2.8 V, while the voltage shift for transistors with a 200°C pre-irradiation stress is ~5.5 V. Thus, the 200°C pre-irradiation stress results in a ~2.7 V or 100% increase in the transistor voltage shift. At total doses of 50 and 70 krad(SiO₂) the change in voltage shift between the 200°C and no stress radiation response is 3.5 V and 3.8 V, respectively. That there is little difference between the voltage shift at 50 and 70 krad(SiO₂) is a result of interface-trap buildup with dose (I-V characteristics not shown here) causing a turnaround in the voltage shift [4]. A similar turnaround in voltage

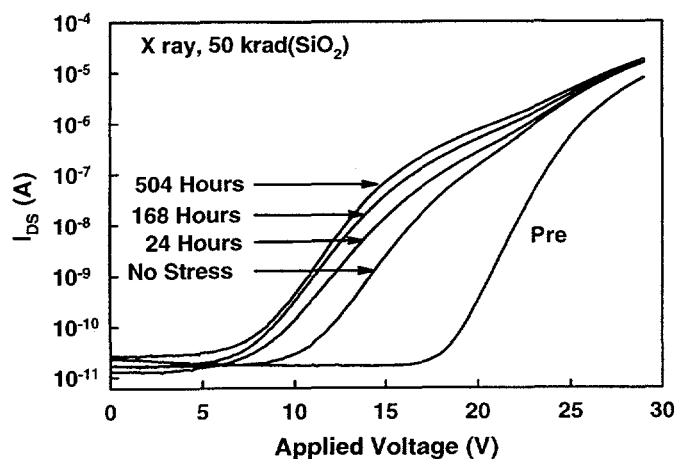


Figure 4: I-V curves for n-channel field-oxide transistors with and without a 150°C pre-irradiation stress. The duration of the stress was 24, 168, and 504 hours. The gate-to-source irradiation and stress bias was 5 V.

shift was observed for the gate- and field-oxide transistors examined in Ref. [10].

B. Time Dependence

Next we examine the effects of pre-irradiation stress time on the radiation response of field-oxide transistors. Figure 4 is a plot of a series of 50 krad(SiO₂) post-irradiation subthreshold current-voltage curves for transistors with or without a pre-irradiation stress. Pre-irradiation stress durations of 24, 168, and 504 hours are examined. The pre-irradiation stress temperature was 150°C with $V_{GS} = 5$ V. As was observed for the temperature dependence data discussed previously, the duration of the pre-irradiation stress has a significant

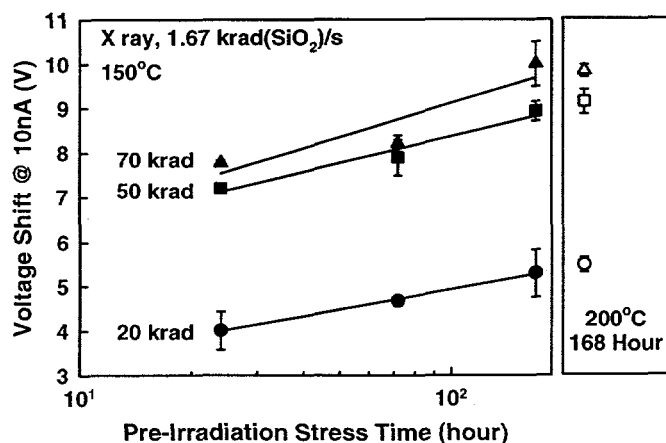


Figure 5: Voltage shift at 10 nA for the field-oxide transistors as a function of the 150°C pre-irradiation stress time. The radiation response of the transistors at total doses of 20, 50, and 70 krad(SiO₂) are shown. Voltage shift data of Figure 3 for the 200°C, 168-hour stress is shown by the open symbols on the right side of the plot. The gate-to-source irradiation and stress bias was 5 V.

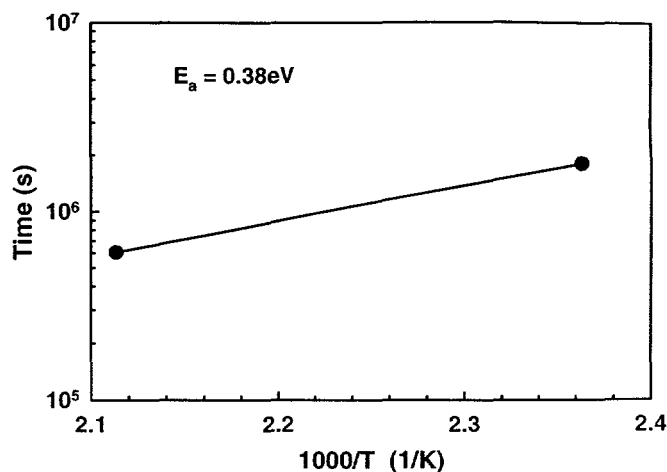


Figure 6: Arrhenius plot of the time to reach equivalent radiation-induced voltage shifts for the 150°C, 504 hour and 200°C, 168 hour pre-irradiation stress. The calculated activation energy is 0.38 eV.

impact on the radiation response of the devices examined in this work. We see an increased negative shift in the post-irradiation I-V curves as the stress time is increased. This shift is primarily a result of enhanced oxide-trap charge buildup. In addition, as the duration of the stress is increased, an increase in the slope of the subthreshold characteristics occurs. Thus, a pre-irradiation stress also appears to slightly suppress interface-trap buildup. The data of Figure 2 and 4 show that the radiation-induced charge buildup in these field-oxide transistors differs from that of gate-oxide transistors. The radiation data for the field-oxide transistor indicates that the differences in charge buildup caused by pre-irradiation stresses cannot be due primarily to a difference in interface traps as observed previously for gate-oxide transistors [10].

The change in voltage shift at 10 nA for the data of Figure 4 is plotted as a function of pre-irradiation stress time in Figure 5. Voltage shifts for transistors irradiated to total doses of 20 and 70 krad(SiO₂) are also shown in the figure. The data points in the box at the right of the figure are the corresponding voltage shifts for transistors with a 168 hour, 200°C pre-irradiation stress irradiated to the same total doses. For each total dose, the radiation-induced threshold voltage increases with increasing pre-irradiation stress time. The difference in the voltage shift between a 24 hour versus 504 hour pre-irradiation stress is approximately 1.4, 1.8, and 2.2 V for the 20, 50, and 70 krad(SiO₂) irradiations, respectively. Note that the radiation-induced voltage shift after a 504 hour (three weeks), 150°C pre-irradiation stress is approximately equal to the radiation-induced voltage shift after a 168 hour (one week), 200°C pre-irradiation stress for all total dose levels examined. This result will

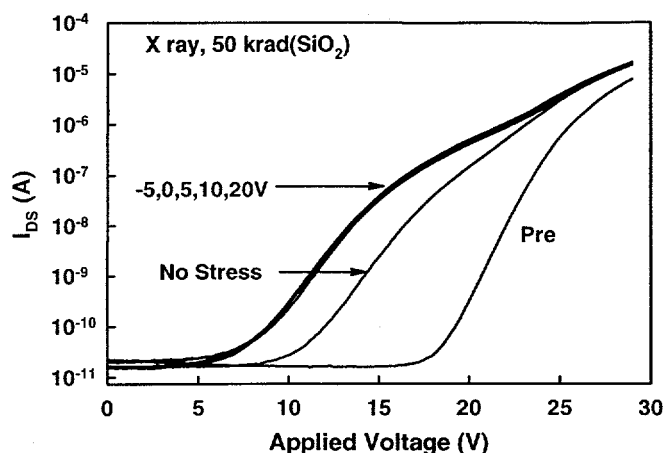


Figure 7: I-V curves for n-channel field-oxide transistors with or without a pre-irradiation 150°C, one-week stress. The bias during the stress was -5, 0, 5, 10, or 20 V. The gate-to-source irradiation bias was 5 V.

enable us to calculate an activation energy for the pre-irradiation stress effect, as discussed next.

The data of Figure 2 through Figure 5 show that the pre-irradiation stress effect is strongly thermally activated. We can estimate an activation energy for this process from the limited data of Figure 5. An Arrhenius plot of the time to an approximately equivalent radiation-induced voltage shift versus inverse temperature is shown in Figure 6. The slope of this curve yields an activation energy of 0.38 eV. This activation energy is very near the activation energy of 0.41 eV for trapped hole compensation [4] and the activation energy of 0.45 eV found for the diffusion of molecular hydrogen in bulk fused silica [15].

C. Bias Dependence

Finally, we examine the bias dependence of the pre-irradiation stress effect in Figure 7. This figure is a plot of a series of I-V curves measured on different transistors with no stress or a 150°C, one-week stress prior to irradiation. The gate-to-source bias during stress was varied from -5 to 20 V in 5 V increments. The gate-to-source bias during irradiation was 5 V for all transistors. The data in this figure clearly show that the I-V curves for the transistors with a pre-irradiation stress shift more negatively than the I-V curve for the transistor without a pre-irradiation stress. However, the magnitude of the shifts appears to be independent of the bias applied during pre-irradiation stress. This is shown in more detail in Figure 8.

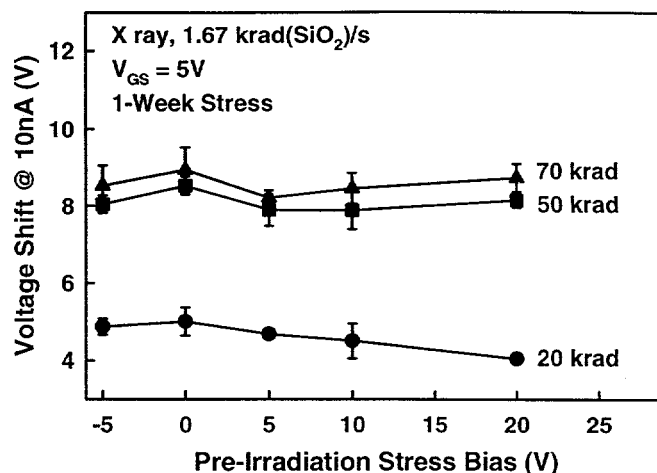


Figure 8: Voltage shift at 10 nA for the field-oxide transistors as a function of the 150°C pre-irradiation stress bias. The radiation response of the transistors at total doses of 20, 50, and 70 krad(SiO₂) are shown.

Plotted in Figure 8 are the voltage shifts at 10 nA as a function of pre-irradiation stress bias for transistors irradiated to total doses of 20, 50, and 70 krad(SiO₂). Within experimental uncertainty, the voltage shift does not appear to depend on the pre-irradiation stress bias for any of the total doses examined.

IV. MECHANISMS

In order to mitigate or reduce the pre-irradiation stress effect, understanding the mechanisms is critical. As mentioned previously, the activation energy of the elevated-temperature pre-irradiation stress effect is close to the activation energy for the diffusion of molecular hydrogen in bulk fused silica and to the activation energy for trapped-hole compensation. If the cause of the pre-irradiation stress effect is related to hydrogen diffusion, the lack of a bias dependence may not be surprising. However, perhaps consistent with its relation to the activation energy for trapped-hole compensation, pre-irradiation stress could also affect the spatial and energy distribution of hole-trap precursors in the oxide (this may also involve the diffusion of hydrogen related species), leading to differences in trapped-hole distributions following irradiation [16]. Clearly, more work is needed to identify the nature of the pre-irradiation stress effect. In any case, the fact that the pre-irradiation stress effect is thermally activated and independent of bias for these devices is important for hardness assurance testing.

V. IMPLICATION FOR HARDNESS ASSURANCE

Elevated-temperature biased stress prior to irradiation has been shown to significantly affect the radiation hardness of MOS devices [10, 11]. The data indicate that, unless a particular technology is shown not to exhibit similar behavior, radiation certification should be performed on devices exposed to all elevated-temperature biased stresses required by reliability qualification and system requirements in order to ensure system survivability in the intended application. For example, as mentioned in the introduction, ICs are commonly given a one-week, 150°C burn-in to reduce the possibility of infant mortalities. This procedure may be performed in either one of two ways. First, a sample of die from a given lot may be burned-in before radiation testing. If the devices pass radiation requirements, the remaining die can be packaged and qualified for delivery. Alternatively, all die may be packaged and burned-in before radiation certification. Then radiation certification can be performed on selected burned-in packages. Unfortunately, both of these procedures will likely increase the cost of certifying products. For example, the first option will delay the delivery of the product by the time it takes to package, stress, and radiation certify selected die. The second option could result in a significant cost penalty if parts did not pass radiation certification and one could not deliver already packaged and burned-in devices.

Based on our evidence that the process is thermally activated, one could potentially shorten the time of the pre-irradiation stress by increasing the stress temperature. Thus, if the first option above is chosen, the delay between die availability and the delivery of parts can be significantly shortened. One question that remains to be answered is whether or not the pre-irradiation stress effect saturates at higher temperatures or longer times. This can be especially important for scenarios where devices can be exposed in actual system applications to elevated temperatures for extended periods of time prior to irradiation. By increasing the temperature of the stress, one can predict device response using considerably shorter stress times. However, caution must be taken to ensure that the temperature is not arbitrarily increased to a point at which the effects of pre-irradiation stress are annealed out or not introduced at all. This is similar to the requirements for "rebound" testing. The temperature during rebound testing is limited to 100°C to ensure that interface-trap effects are accelerated and not annealed

out [4, 17]. Additional testing will be required to determine the maximum temperature that can be used to accelerate the effects of pre-irradiation stress on the radiation response of ICs.

The standard sequence of the U.S. MIL-STD-883D test guideline is currently being rewritten to specify that the test sequence includes all elevated-temperature biased stresses prior to radiation qualification testing. Ideally, one would like to avoid having to perform a pre-irradiation stress. This will require techniques for simulating and predicting the effect of a pre-irradiation stress from accelerated temperature irradiation data. If such a technique could be developed, then it could be incorporated into the MIL-STD-883D test guideline.

It is important to point out that the temperature, time, and bias conditions for the pre-irradiation stress have only been evaluated for field-oxide transistors from the CMOS IIIA technology. It will be important in the future to evaluate other technologies to determine if they have a similar dependence on pre-irradiation stress temperature, time, and bias. However, the IC data for the commercial technology presented in Ref. [10] appear to be consistent with these results. The average maximum post-irradiation standby power supply current for the 125°C burned-in 4-bit counters were only 20 times higher than for devices without a burn-in. For the octal buffer/line drivers (see Figure 1), it was 300 times higher. This reduced difference may be a result of the lower stress temperature used for the 4-bit counter devices (125°C versus 150°C).

Recall that large radiation-induced threshold-voltage shifts for the gate- and field-oxide transistors can cause large increases in the source-to-drain current for the n-channel transistors in the "off" mode (gate-to-source voltage = 0 V). One IC parameter affected by large, negative threshold-voltage shifts is the "standby" power supply leakage current in ICs [18,19]. As threshold voltages tend toward depletion, there is a significant increase in I_{DD} . Source-to-drain current may change exponentially with changes in transistor threshold voltage, and even relatively small changes in threshold voltage can lead to large increases in source-to-drain current. Therefore, a lower starting threshold voltage will lead to more significant effects due to pre-irradiation stress. That is why, for example, we believe larger changes in I_{DD} current were observed for commercial devices in Refs. [10, 11] with starting field-oxide threshold-voltages (~12 V) which are less than the

hardened field-oxide threshold-voltages (~ 23 V) discussed here.

Over the past several years, there has been an increased emphasis on the use of wafer-level radiation qualification testing [19-24] using x-ray radiation sources. This provides rapid feedback on process control, reduced testing costs, and reduced radiation-safety overhead. However, performing elevated-temperature biased stresses before wafer-level x-ray irradiation is usually impractical. Radiation acceptance testing at the wafer level may not be sufficient for technologies showing these kinds of biased-temperature stress effects on radiation response. However, if the pre-irradiation stresses could instead be performed on unbiased devices, and the pre-irradiation effect saturates, then entire wafers or wafer lots could be subjected to elevated-temperature stresses before packaging, and radiation certification could be done at the wafer-level using x-ray irradiation sources. We emphasize that, although we have shown that a pre-irradiation stress at a 0 V bias results in the same effect as for positive and negative biases for this technology, a completely unbiased stress may lead to different results. Note that even if the stress effect does not saturate, this type of procedure could still be used to provide rapid feedback on process control.

VI. SUMMARY

We have shown that radiation-induced charge trapping in field-oxide transistors from a given technology depends strongly on the time and temperature of pre-irradiation elevated-temperature biased stresses. An activation energy of 0.38 eV was measured for these devices. However, the bias of a pre-irradiation stress has no effect on radiation-induced charge trapping in these field-oxide transistors. These data have important implications for cost-effective hardness assurance testing. The effects of all elevated-temperature biased stresses required by the system need to be simulated for a given technology with a single pre-irradiation stress prior to radiation certification testing.

Acknowledgments

The authors acknowledge the technical assistance of L. C. Riewe and technical discussions with Philippe Calvel.

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