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Title: CHARGE TRANSFER EFFICIENCY MODELING/MEASUREMENTS AS FUNCTION OF CCD PIXEL RATE

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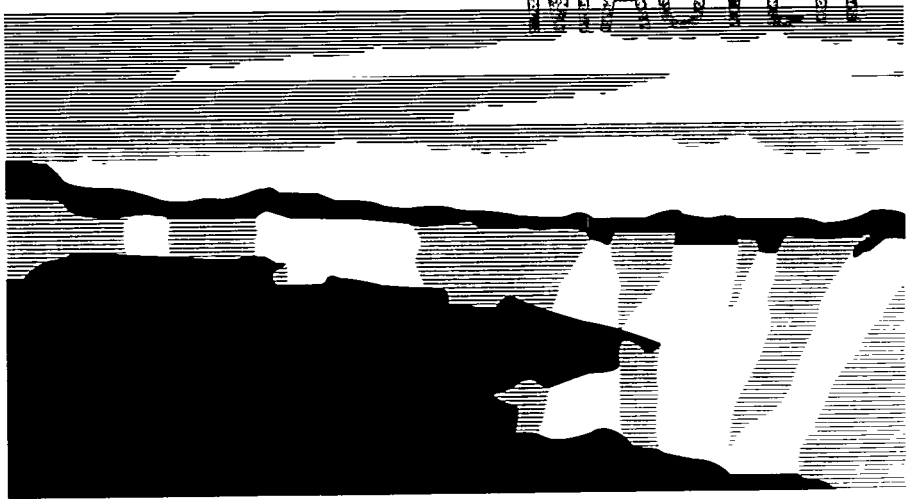

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Charge Transfer Efficiency Modeling/Measurements as Function of CCD Pixel Rate

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Abstract

We have developed a charge transport model for predicting the effects on Charge Transfer Efficiency (CTE) of Charge Coupled Devices (CCDs) as functions of number of transfers, pixel charge flow rate, and magnitude in the CCD's vertical and horizontal charge transport mediums. The model uses carrier lifetime an mobility criteria to establish pixel speed arguments and limitations for various CCD architectures. The model is compared with experimental measurements obtained using strobed single pixel illumination and a variant of the deferred charge tail technique while independently varying the CCD pixel rates for both the vertical and horizontal readout phases. The generic model is discussed and applied to specific real CCDs. Agreement between predicted performance and actual measured performance is presented.

Key words: Charge transport model, Charge Transfer Efficiency, pixel charge flow rate, charge carrier lifetime, transport mediums.

1. INTRODUCTION

The Charge Transfer Efficiency (CTE) characteristics of a CCD is dependent upon how efficiently charge is moved in the CCD pixels and readout registers. For high frame rate applications, the rate at which pixel charge is clocked must also be considered in the context of increased video amplifier bandwidth and settling time requirements. Modern scientific CCDs are designed to provide multiple outputs so that the array can be segmented and individual segments read out simultaneously to provide both higher pixel rates and fewer transfers. This improves both CTE and data rate. To better understand these features for newly-developed mulitport imagers, we have developed a simple charge transport model and have operated CCDs at variable pixel rates to provide experimental data to test the model. Los Alamos National Laboratory's unique high speed solid state imager test station (HSST) (a computer based programmable waveform generator) makes these experiments feasible because of the ease with which CCD clock waveforms can be varied.

2. PREVIOUS RELATED RESEARCH

The fundamental physical properties associated with charge transfer in terms of charge carrier motion due to diffusion and drift have been rigourously studied[1] and quantified for various three phase CCD gate structures/architectures (essentially limited to the serial transfer registers). They attribute degradation in transfer efficiency to loss of charge to trapping centers and to insufficient time for complete transfer of free charge. Contributions from thermal diffusion, fringing-field drift from external clock voltages, and self-induced drift from the CCD's internal electric fields due to signal charge itself are described for the free charge with no analysis of losses or delays from traps.

For self-induced drift, scenarios exist where it is possible for this electric field to aid or hinder (cases are stated for both) foward transfer of charge by the external electric field. For a specific set of conditions, i.e., CCD gate lengths 4 to 10 microns, substrate doping concentrations in 10^{14} to $10^{15}/cm^3$ range, and light-induced charge distribution in the 10^8 to $10^{12}/cm^2$ range, they predict single carrier transit times (the time required to travel the length of the gate) can be improved (reduced) under the influence of external electric fields produced by typical few volt CCD clock wave trains. They suggest pixel clocking rates are possible up to 100 MHz for 4 micron CCD technology. Although the exact properties of the device we tested most comprehensively (EEV CCD-13) are proprietary, we felt they were close to those described in the reference (1). Therefore, our candidate CCD provided a fair test bed to test their predictions (which address primarily charge transport speed due to charge magnitude and CCD substrate doping concentrations), and to evaluate our own predictions which include charge magnitude and CCD pixel clock rate as variables. Their principal conclusion for transfer speed is based upon a final time constant, τ_f, which is related to single carrier transit time, τ_{tr}, by $\tau_f \approx 0.33\ \tau_{tr}$, but indicate that τ_{tr} varies widely with both gate length and dopent concentration, ranging from 288 ps to 4.9 ns for 4 and 10 micron gates and $2 \times 10^{14}/cm^3$ dopent concentrations and 413 ps to 15 ns for $1 \times 10^{15}/cm^3$.

Early theoretical/experimental work[2] was done to device experimental tests to evaluate various CTE loss models, including what were referred to as "fixed", "proportional", and "non-linear" losses. They associated fixed and proportional losses with surface-channel CCD's surface state traps which they claimed were independent of signal magnitude and could be eliminated or minimized with "fat zero" bias techniques. They attributed the proportional losses to traps near the edges of transfer gates and the fixed losses to traps underneath the gates. We view this as essentially deferred charge (not actual loss of charge) where the amount of charge missing from an initial charge packet that is transferred eventually shows up in succeeding transfers, as illustrated in Fig. 1. The non-linear losses are due to the gaps or spaces between gate electrodes and are presumed to be real non-recoverable losses. The mechanism responsible is postulated to be due to creation of charge wells and potential barriers that affect small charge magnitude differently than large charge magnitude, i.e., small charge transfers effectively while large charge does not transfer effectively. An example of non-recoverable losses is shown in Fig. 2 that were obtained from our earlier experiments with saticon and silicon target vidicons[3]. The partial recovery from this type of loss is illustrated in Fig. 2, but complete recovery is unlikely in our view.

The questions of light-induced charge lost to traps or lost to replenishing subthreshold depletion from scanning the CCD while in the dark (between individual pulses of light) are more difficult to access for pulsed light than for CW illumination. For the case of CW illumination, the latter problem does not exist and the former problem is "fixed" for all scans except the initial few following illumination (the traps are quickly "filled" with light-induced charge from the CW light). Our experience[3] with the use of optical or electrical bias techniques ("fat zero" compensation) to compensate for both types of losses (see Fig. 2) is described by others[5] as means for recovery of losses from the subthreshold depletion problem. Our analysis indicates that the depletion losses are probably constant across the CDD array so compensation with a uniform bias is adequate. For the pulsed light case, the amount lost to traps is probably variable across the array which complicates the correction process. However, for small-area illumination patterns, such as single or few pixel excitation, the losses should be site specific and therefore constant and repeatable with little variance in absolute magnitude so their effect on CTE would be to reduce the initial charge (for transfer through and out of the CCD) by a fixed amount. This would require corrections to initial charge for thoses cases where the CTE is measured as a function of input irradiance across the CCD's dynamic range. The references[1,5] either do not address this question specifically[1] (their work used primarily large signals, i.e., $5x10^{11}/cm^2$ carriers but did not repeat the same CTE tests for other distributions and their study neglects effects due to traps), or indicate[5] that CTE is not affected by charge magnitude (although they indicate a loss mechanism which they call Photosite Transfer Loss (PSTL) that is given as a percentage of the total signal, which we feel must alter the initial charge magnitude).

In summary, the charge transfer efficiency is a complicated physical process which is dependent upon operating temperature, light-induced signal charge level, and external electric fields, as well as CCD pixel structure dimensions and free carrier concentrations of its storage and transport mediums.

This paper provides experimental data at various pixel rates and signal levels to study rate-limited performance and to examine agreement with these earlier calculated responses as well as with our calculations/modeling.

3. PREDICTIVE MODELING

Because the CCD-13 has no storage such as normal Frame Transfer CCDs, it is suitable only for pulsed light operation. Smearing will occur vertically for CW light illumination because the CCD-13 is being continuously clocked, transferring consecutive rows of pixels from the image section into the horizontal serial output register. Readout for this type of CCD is essentially in a continuous frame transfer phases, therefore vulnerable to smear.

A diagram of the CCD-13 bi-directional read-out architecture is illustrated in Fig. 3 and key features in Table 1. the speed related characteristics are listed in Table 2. It should be noted that the massively parallel readout architecture provides for fewer thransfers of charge, than for conventional serial single port CCDS, with expected improvements in CTE.

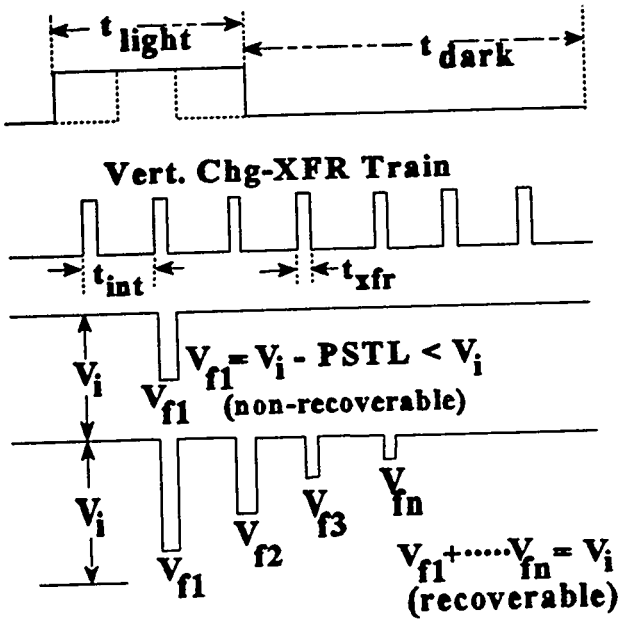

Fig. 1. Illustration (top) of non-recoverable charge and (bottom)of recoverable charge where the amount of charge missing from an initial charge packet that is transferred eventually shows up in succeeding transfers, unaided by biasing.

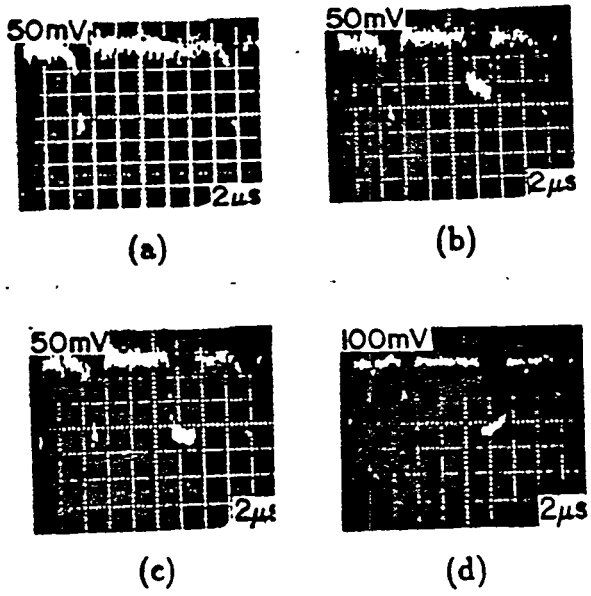

Fig. 2. Optical bias techniques ("fat zero" compensation) to recover losses from traps and and subthreshold depletion from "dark" scanning of silicon target vidicons. The absence of signal in (a) is with no bias light added. The signal is increasingly recovered with increased bias in (b), (c), and (d).

A recent work[4], centered on understanding generic EEV CCDs, identified two additional limitations to high speed clocking of charge in CCDs. These are (a) parallel transfer of charge through the image sections (determined by the electrode time constants, and (b) the bandwidth and slew rate capabilities of the CCD's on-chip amplifiers. The work concludes that the most serious limitation is imposed by the serial (or horizontal) analog shift register which was the mechanism studied in references (1) and (2). These researchers too have estimated that CTE for the top or first decade of charge transfer is primarily a function of self-induced drift owing to the light-induced charge with little added efficiency from external fringe fields. Their estimate for residual or remaining charge after the initial start of charge transfer is determined by τ_f , which they state is a strong function of fringe fields for a particular CCD geometry, dopent concentration, and applied clock voltage amplitude. Their calculation for the remaining charge, N , as a function of time, t , for initial charge, N_ϕ , is $N(t) \approx N_\phi / e^{t/\tau}$ and $\tau \approx L/\mu E$,where μ is the electron mobility, E is the inter-electrode field, and L is the electrode spacing of the three transfer electrodes in their 3-phase clock cells. From this, we can deduce that for $N/N_\phi \approx 10^{-5}$ (99.999% CTE) requires 11 τ_f and for 99.99% CTE, 9 τ_f (i.e., $1/e^{11} = 0.000017$ and $1/e^{9} = 0.000123$). For their (EEV) technology, they estimate that the pixel clock frequency $f(H) \approx (5 \times 10^5\ \mu m^3\ MHz) / L^3$ which, if we use 21 microns for L as being a side dimension of a CCD-13 pixel, gives ≈ 54 MHz.

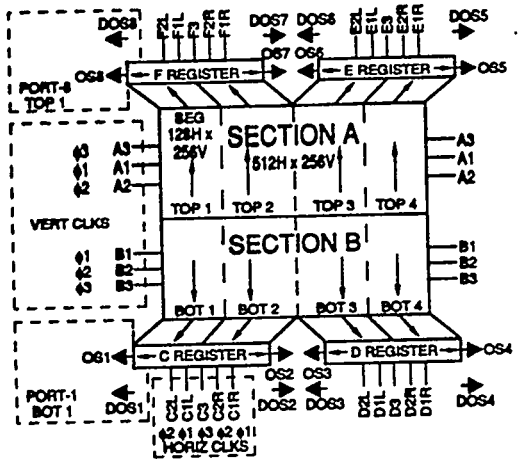

Fig. 3. A diagram of the CCD-13 bi-directional read-out architecture.

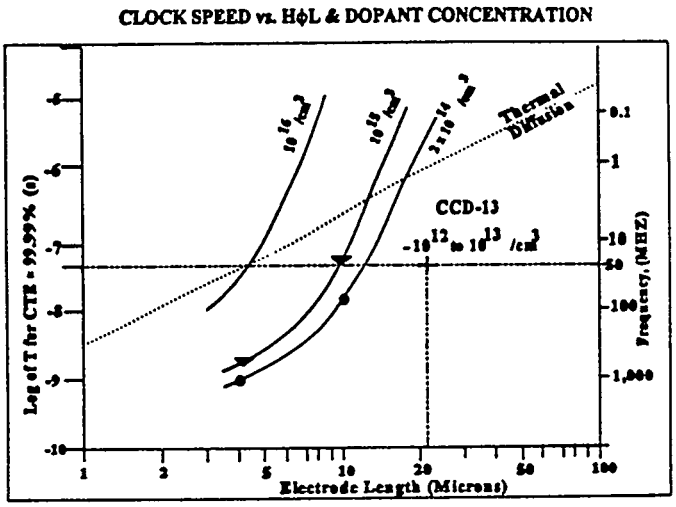

Fig. 4. The expected CTE based upon gate electrode dimensions and various doping concentrations.

Key Feature	*Value*
Clocking	3-phase horizontal and vertical
Pixel Count	512 (H) x 512 (V)
Video Ports	8 real and 8 dummy
Pixels/Segment	256 (V) x 128 (H)
Pixels/Register	256,128 / port
Pixel size	21 (H) x 21(V) microns
Responsivity	2-3 microvolts / electron
Well Capacity	200-400 K electrons

Table 1. EEV CCD-13 architecture featuring mulitple video ports and segmented read-out for improved CTE and increased pixel clocking rates.

Speed Related Characteristic	*Value*
Horizontal Capacitance	9 to 18 pfd
Vertical Capacitance	10 to 20 nfd
Horizontal Clock Drive	1 A / 5 ns
Vertical Clock Drive	2 A / 50 ns
Horizontal Rate Limit	20 MHz
Vertical Rate Limit	1.25 MHz
Pixel Thickness / Resistivity	20 micron / 20 Ω cm
Bandwidth, -3dB	50 MHz

Table 2. Clock and amplifier details for EEV CCD-13. Horizontal drivers are bi-polar high current transistors (2N3960, NPN and 2N4261, PNP) charge pumps; vertical drivers are Micrel CMOS design.

The expected CTE based upon gate electrode dimensions and various doping concentrations is illustrated in Fig. 4 after ref (1) with the EEV CCD-13 located for reference. The predicted CCD-13 maximum clocking frequency before the onset of reduced CTE and resolution is shown in Fig. 5 after ref (4). Both indicate potential clocking rates up to ≈ 50 MHz, although CTE value is unclear but expected to be in the four to five "9's" range.

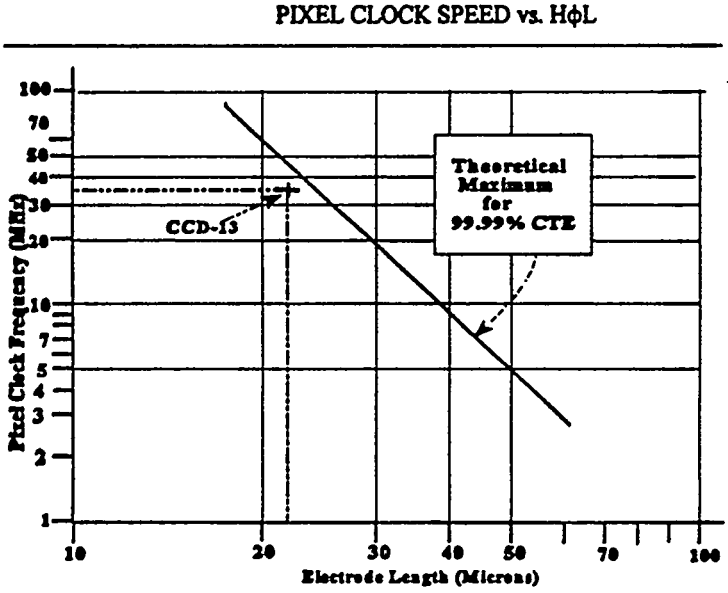

Fig. 5. The predicted CCD-13 maximum clocking frequency before the onset of reduced CTE and resolution.

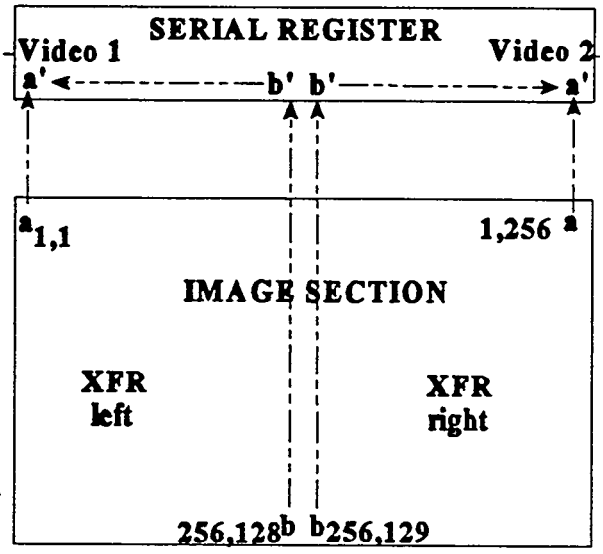

Fig. 6. Simplified charge transfer model of CCD-13, depicting minimum and maximum transfer routes.

The maximum speed at which charge can be transferred through the serial or read-out register is limited by the velocity of electrons in silicon. This is the fundamental limit to pixel clock speed in a CCD device. However, there is also a practical limit associated with the generation and propagation of high speed clock waveforms through and along the CCD clock electrodes. The latter can usually be overcome by use of metalization over the polysilicon clock lines to provide smaller RC time constants, therefore faster charging, and improved speed. Also, the CCD-13 parallel multiport read-out architecture reduces transfers as shown in Fig. 6.

Referring to earlier Fig. 3 and Fig. 6, each CCD-13 segment consists of 128(h) x 256(v) pixels. Each horizontal readout register receives 1/2 row of pixels, ie 256 pixels. For bi-directional read-out in the horizontal serial register, each 1/2 row is effectively reduced to a 1/4 row, and serves 256 1/4 rows. As shown in Fig. 6, the shortest path (a to a^1) involves two transfers, i.e. 1 vertical and 1 horizontal, from excitation site to output amplifier. The longest path (b to b^1 to a^1) involves 256 vertical and 128 horizontal transfers.

VATES

We suggest a simplified first approximation CTE equation that ignores rate effect:

$$CTE \approx (y^{y1})\,(x^{x1}) \qquad (1)$$

where y^1 = quantity of vertical transfers
x^1 = quantity of horizontal transfers
y = fraction of charge transferred/vertical transfer
x= fraction of charge transferred/horizontal transfer

The measurement of CTE in measurable terms requires sampling the output video arising from the two extreme locations of original signal excitation, i.e., pixel a and pixel b of Fig. 6. The initial charge transferred, Δq, eventually arrives (after equation (1)) at the CCD-13's floating diffusion node capacitance, c, where it is transformed to a voltage, Δv, by:

$$\Delta \approx \Delta q/c \qquad (2)$$

combining (1) and (2) allows observation of the CTE in measurable amplitude units:

$$v_f = (v_i)\,(y^{y1})\,(x^{x1}) \qquad (3)$$

where v_f = final value of v
v_i = initial value of v

Assuming four and five "nines" CTE/transfer, i.e. 99.99% and 99.999%, using equation (3) for the (a to a^1) case (fewest transfers) results in maximum values v_f of 0.9998 v_i and 0.99998 v_i respectively. Using similar criteria for minimum the values of v_f from (b to b^1 to a^1) case (most transfers), we obtain 0.9623 v_i and 0.99616 v_i for four and five "nines".

Taking the difference between the two extreme values of v_f for the 99.99% case, (0.9998 - 0.9623 = 0.0375), which is ≈ 10 amplitude units from our 8-bit digitizer. This is a measurable quantity. However, for the 99.999% case, the two values of v_f differ by ≈ 1 amplitude units, which is beyond the resolution of our existing system. For either of these two situations, (the 10 or 1 amplitude units) the value of v_f must use the full 8 bits of the digitizer. For values v_f<25.6 amplitude units our system resolution is even more limited. However, if we restrict our measurements to the four nines range, and assume that v_f>25.6 amplitude units, we should be able to observe the CCD-13 signals from the (b to b^1 to a^1) route. The v_f predictions for the CCD-13, without introduction of rate effects are summarized in Table 3 for the 99.99% case. it is important to stress that our interpretation of these efficiencies is that they pertain to a single transfer (vertical or horizontal) and that each transfer site has the same efficiency. This of course, is over simplification of the real case.

Table 3. CCD-13 CTE effect on video amplitude as function of pixel transfers for it shortest and longest paths.

Path	y^1	h^1	v_f
a to a^1	$(0.9999)^1$	$(0.9999)^1$	0.9998 v_i
b to b^1 to a^1	$(0.9999)^{256}$	$(0.9999)^{128}$	0.9623 v_i

At high pixel clock rates, "apparent" loss in signal amplitude may come from the limited bandwidth of the CCD's on-chip amplifier as indicated earlier. We need to distinguish this from the losses due to CTE. We assume that the charge is conserved, and that the response of the amplifier, as well as the response of the CCD-13's "geometry-caused" capacitance's associated with its serial register, are gaussian. Therefore, these two responses can be taken in guaduation, so the actual or observed bandwidth, B_o, is related to the system bandwidth, B_s, and the pixel clock rate, B_{px}, by the sum of squares:

$$(\frac{1}{B_o})2 = (\frac{1}{B_s})2 + (\frac{1}{B_{px}})2 \qquad (4)$$

Thus as the pixel clock rate approaches the system bandwidth, we expect that the charge read out would decrease in direct proportion to the decrease in the observed bandwidth:

$$\text{CTE} \propto \frac{B_o}{B_{PX}} = \sqrt{\frac{1}{1+(\frac{B_{PX}}{B_s})}}\,2 \qquad (5)$$

Thus even if the pixel rate is only 20% of the system bandwidth, we expect the CTE to decrease to 0.981. Of course when the pixel rate is equal to system bandwidth the CTE would decrease to 0.707.

In earlier work[6], we explored the possibility of increasing photoconductivity to reduce resistivity by "priming" the photoconductor with a pulse of light from an IR laser (1.064 micron, Nd:yag) recording the image from a second visible wavelength light source. In that study we were attempting to increase shuttering speeds of gated image intensifiers by providing reduced RC time constants between gating surfaces (the intensifier photocathode and microchannel plate). A similar technique might provide increased clocking speed in the CCD serial transfer registers, therefore we will summarize the pertinent points of that work next.

The effect of the two light sources on a hypothetical semiconductor is illustrated in Fig. 7. Energy is plotted in the vertical direction with the pertinent energy levels noted: E_{VB} is the energy at the top of the nearly filled valence bands; E_{CB} is the energy at the bottom of the nearly empty conduction bands; $E_g = E_{CB} - E_{VB}$ (the band gap); and E_T is the emission threshold energy, i.e., the energy and electron must have to escape the semiconductor into the vacuum. Electrons with energy E_T in the solid will have zero kinetic energy in the vacuum. For simplicity, we assume light from the image source is monochromatic, with photon energy, $h\nu_1$. With this photon energy, some light will be absorbed resulting in photoelectrons with some kinetic energy (case a), while other electrons photoexcited by light from the image source will not have sufficient energy to escape the semiconductor (case b). Light from the second (primer) source has a lower photon energy, $h\nu_2$, which, when absorbed, can only result in electrons with energy less than E_T (case c). Such electrons cannot escape the semiconductor, but can contribute to increased conductivity. For simplicity, analytically, $h\nu_2$ is constrained to $E_g \le h\nu_2 < E_T - E_{VB}$.

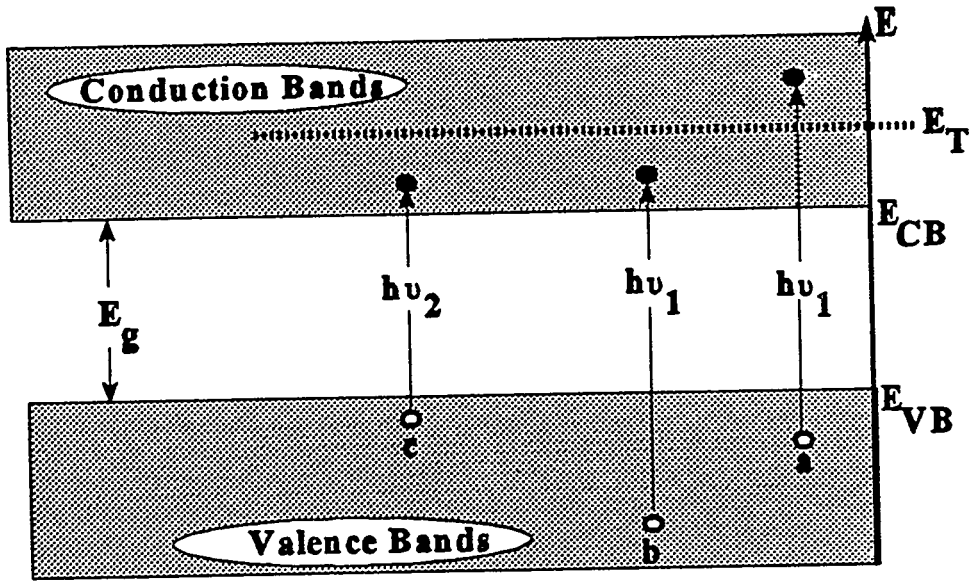

Fig. 7. Simplified energy level diagram for a semiconductor, illustrating excitation of electrons due to absorption of relatively energetic photons, $h\nu_1$, in (a) and (b), and less energetic photons, $h\nu_2$, in (c).

We note, of course, that even if our primer source has photon energy in the appropriate range, some amount of photoemission can still occur. Also, our simplified model does not account for absorption at strategic impurity sites, levels, etc., or multiple photon absorption, etc., which obviously exist in the real case.

The technique was tested using average intensity of approximately 95w/cm^2, from the IR laser. The Nd:yag laser used had photon energy of about 1.17 eV ($h\nu_2$ of Fig. 7), the visible image laser photon energy was about 2 eV ($h\nu_1$ of Fig. 7). The photoconductor bandgap was about 1 eV and the photoelectric threshold was about1.5eV. For our ideal model where all photons are absorbed, I $\approx 5 \times 10^{20}$ photons per square centimeter per second. Some noticeable effects were observed, but the mixing of the prime and image sources made interpretation difficult.

The use of this or similar "priming" techniques to stimulate conductivity in the CCD image section might improve the CTE. If so, it represents elegant solution because such priming can be time-phased with strategic readout phases of the CCD to minimize problems associated with steady state bias techniques. With proper choice of photon energy, the potential for optical interference from the primer source (with the image source) can be minimized. by using a coherent source, localized site-specific priming can be done selectively, if required for some applications.

Generally the conductivity of seimiconductors is directly proportional to the number of excess mobile carriers (i.e., conduction band electrons and valence band holes). Specifically,

$$\sigma = e(n_e\mu_e + n_h\mu_h), \tag{6}$$

where σ is the conductivity, e is the elementary charge, n_e and n_h are the respective conduction electron and valence hole concentrations, and μ_e and μ_h are their respective mobilities. Since mobilities are essentially unaffected by photoabsorption, an increase in n_e and n_h via photoabsorption will result in a corresponding increase in conductivity.

In order to determine a quantitative relationship between the primer source intensity and the conductivity, a simple photoconductivity model is assumed. It is, assumed that every absorbed photon produces a hole in the valence bands and an electron in the conduction bands. Further, these electrons and holes will have identical mobilities, $\mu = \mu_e = \mu_h$, and lifetimes, τ. With an absorbed primer source intensity, I (photons/cm^2 -s), the carrier concentration, n, is governed by

$$\frac{dn}{dt} = \frac{2I}{s} - \frac{n-n_o}{\tau} \tag{7}$$

where n_o is the equilibrium (dark) carrier concentration (both electrons and holes), and s is the semiconductor thickness. If a constant primer source, I, is applied at t=0, the solution for t>0 is

$$n = n_o + \frac{2I\tau}{s}\left(1-e^{-t/\tau}\right) \tag{8}$$

The sheet resistance is given by $R = 1/\sigma s$, so we can write

$$R = R_0 / \left(1 + 2eR_0 I\,\mu\tau(1-1/e^{t/\tau})\right) \tag{9}$$

where $R_o = 1/n_o\, e\mu s$ is the dark sheet resistance. As is clear from (9), R asymptotically approaches the value $R_\infty = R_o/(1 + 2I\mu\tau eR_o)$ for $t > \tau$.

4. EXPERIMENT AND DATA

The CTE experiment setup is shown in Fig. 8 and 9. The Los Alamos National Laboratory's High Speed Solid State Imager Test Station (HSST) was used to drive the EEV CCD-13 at variable clock rates. The HSST described in our earlier work[7] is a computer based programmable waveform generator with supporting 8-channel 8-bit digitizing electronics, a triggerable Q-switched 532 nm laser with $\approx$ 10 ns FWHM light pulse, precision optics with 10 -100 micron pinhole illumination patterns, real-time display, 16-channel high speed digital oscilloscope for clock waveform monitoring, and header preamp/clock drivers. The HSST block diagram is shown in Fig. 10 and the control consol is shown in Fig. 11. The CCD-13 clock waveforms generated by the HSST are shown in Fig. 12 and 13 for 100 ns clock period. The relative features of the waveforms remain constant as the clock frequency is varied, to maintain phasing and duty cycle, etc.

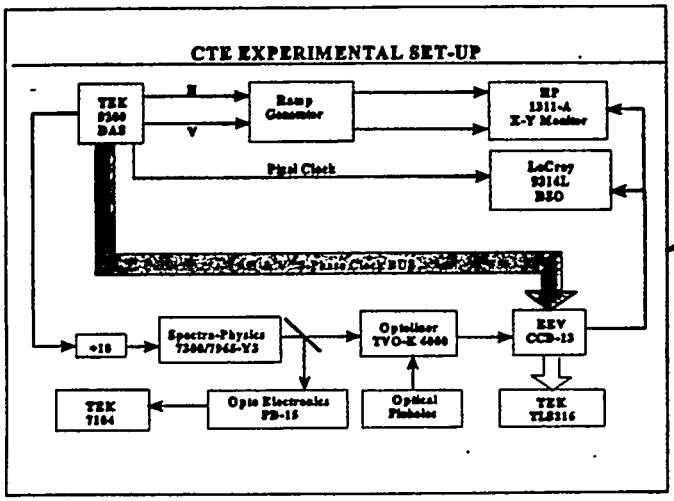

Fig. 8. Block diagram for the CTE experiment setup. A single video output from the 8 - port CCD is shown.

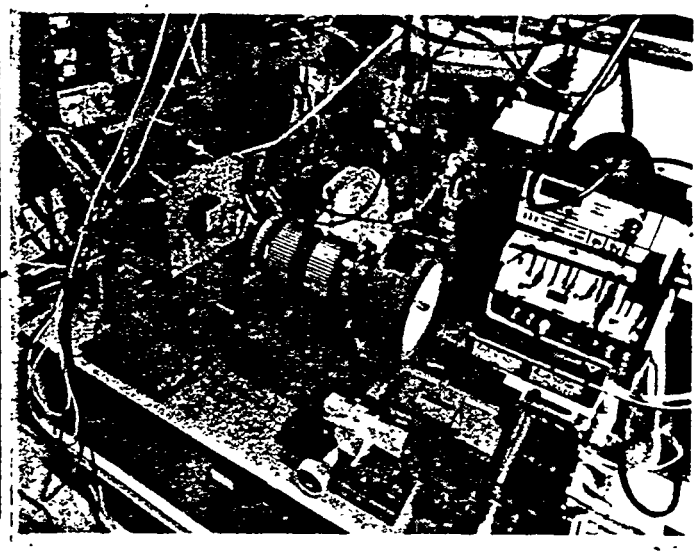

Fig. 9. Optical bench set-up for CTE experiment. The CCD-13 header, optoliner optics, and laser are shown.

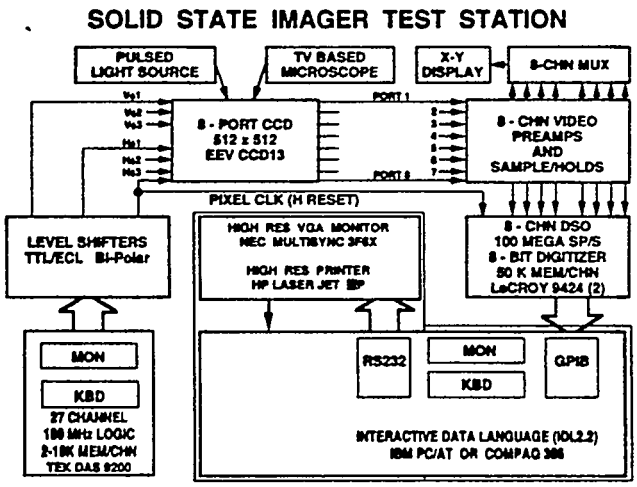

Fig. 10. The HSST block diagram used in the CTE experiment setup.

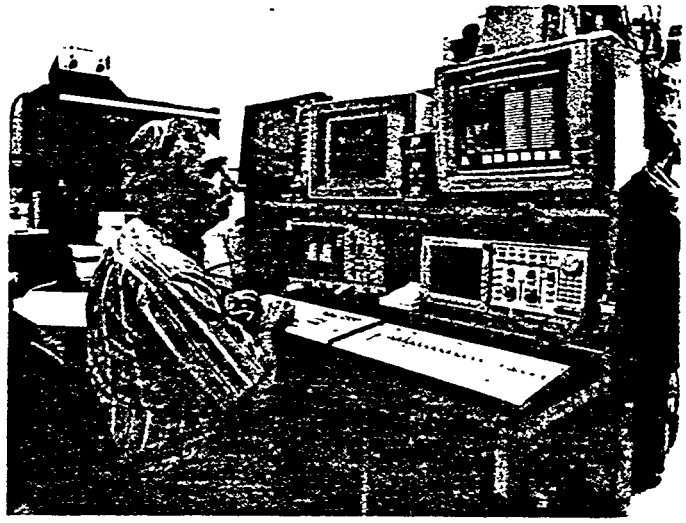

Fig. 11. The control consol for the HSST used in the CTE experiment setup.

The laser light pulse was time-phased to occur just past the vertical sync pulse of the CCD-13. The short duration 10 ns pulses are essentially impulses, representing instantaneous delta functions when compared with the CCD-13 scan line duration. This provided virtually no smear from the continuously clocked mode of the CCD-13. The laser trigger was provided once every ten CCD-13 fields (see the divide by 10 (÷ 10) block in Fig. 8) to allow monitoring of the illuminated pixel up to ten samples following excitation.

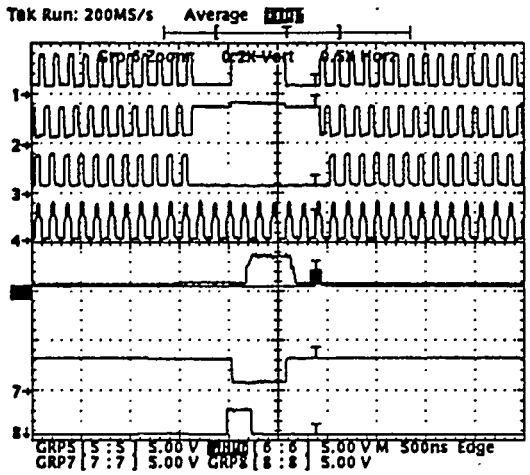

Fig. 12. The timing waveforms obtained from the HSST. The Tektronix TLS216 logic scope was used to measure the Tektronix DAS waveforms from the CCD-13 Code.

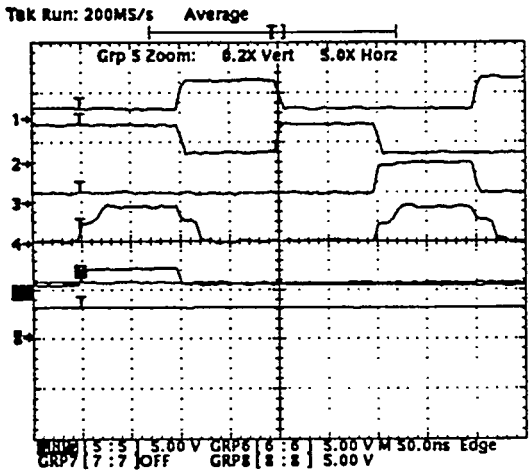

Fig. 13. Expanded view of the reset and horizontal three-phase clocks from Fig. 12 showing overlap.

The CCD-13 spatial frequency response was measured first using standard PR-10 bar patterns. The response was measured at 20 MHz and 40 MHz pixel frequencies. The date are plotted in Fig 14. As indicated earlier, distinguishing between video amplifier response and CCD CTE requires care since both are prone to give reduced amplitude as the pixel clock rate is increased. Two optical patterns were selected, one with a single pinhole to measure low frequency response, and another with four pinholes to measure high frequency response simultaneously in vertical and horizontal axes. Although the low frequency data are not a direct measure of CTE, they are indicators of rate effects on charge transport. These data; shown in Fig. 15, show decreasing signal level for the same input light intensity as the clock rate increases. The clock rate increase is accompanied by reduced pulse width, which may be the real cause of reduced signal. The HSST code for the CCD-13 used a common clock, so when the pixel clock is changed, all horizontal (serial) and vertical (parallel) clocks change proportionally.

The CTE measurements were taken at four pixel clock rates using the 200-micron pinhole pattern. To assure registration between strategic CCD signal spikes in the first and subsequent frames, the laser was fired once every CCD-13 field and the LeCroy DSO time cursors were used to time-locate the same pixels in the first and second fields, as noted in Fig. 16. Then, the laser was fired only once per every ten CCD-13 fields (Fig. 17) and the first and second field signal levels were compared using the time-location cursors as shown in Figs. 18 and 19. The laser pulse was sufficient to operate the CCD-13 near saturation. The data show that the signal is evident only in the first field, and that there is no measurable residual (from charge transfer losses) in the second field. We repeated the test using 20ns, 50ns, 100ns, and 200ns pixel clocks, with essentially the same results. The test also included various input light intensities, again with no measurable signal in the second field.

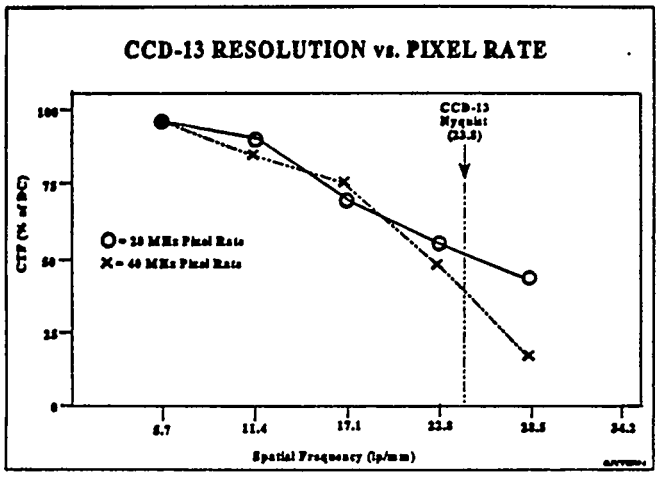

Fig. 14. Spatial resolution of CCD-13, using PR-10 bar sets.

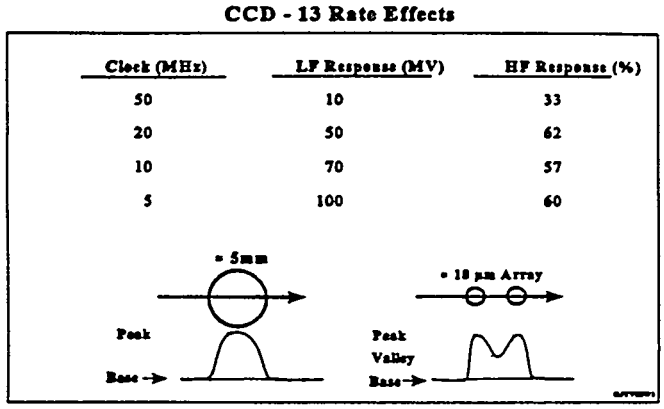

Fig. 15. Rate effects of CCD-13, using single and double apertures.

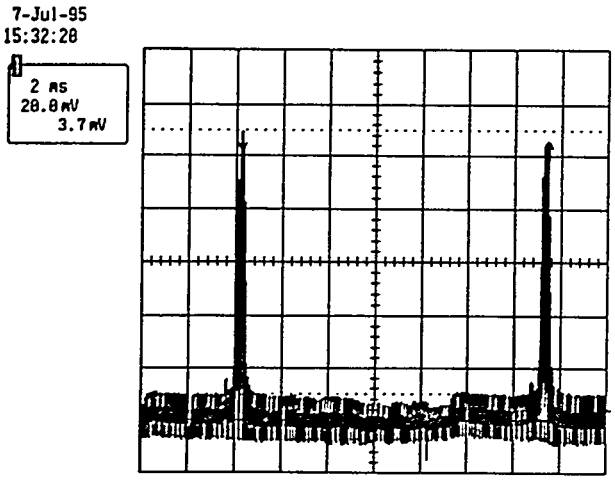

Fig. 16. Laser pulse fired once every CCD-13 field, for pixel co-location in first and second fields.

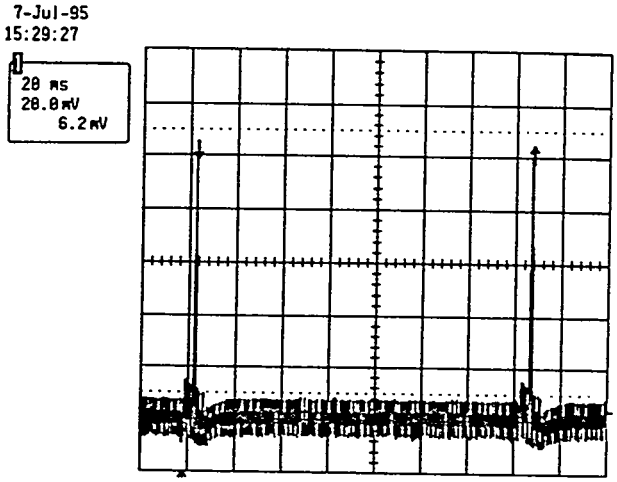

Fig. 17. Laser pulse fired once every tenth CCD-13 field, for CTE measurements in field 1 thru 9..

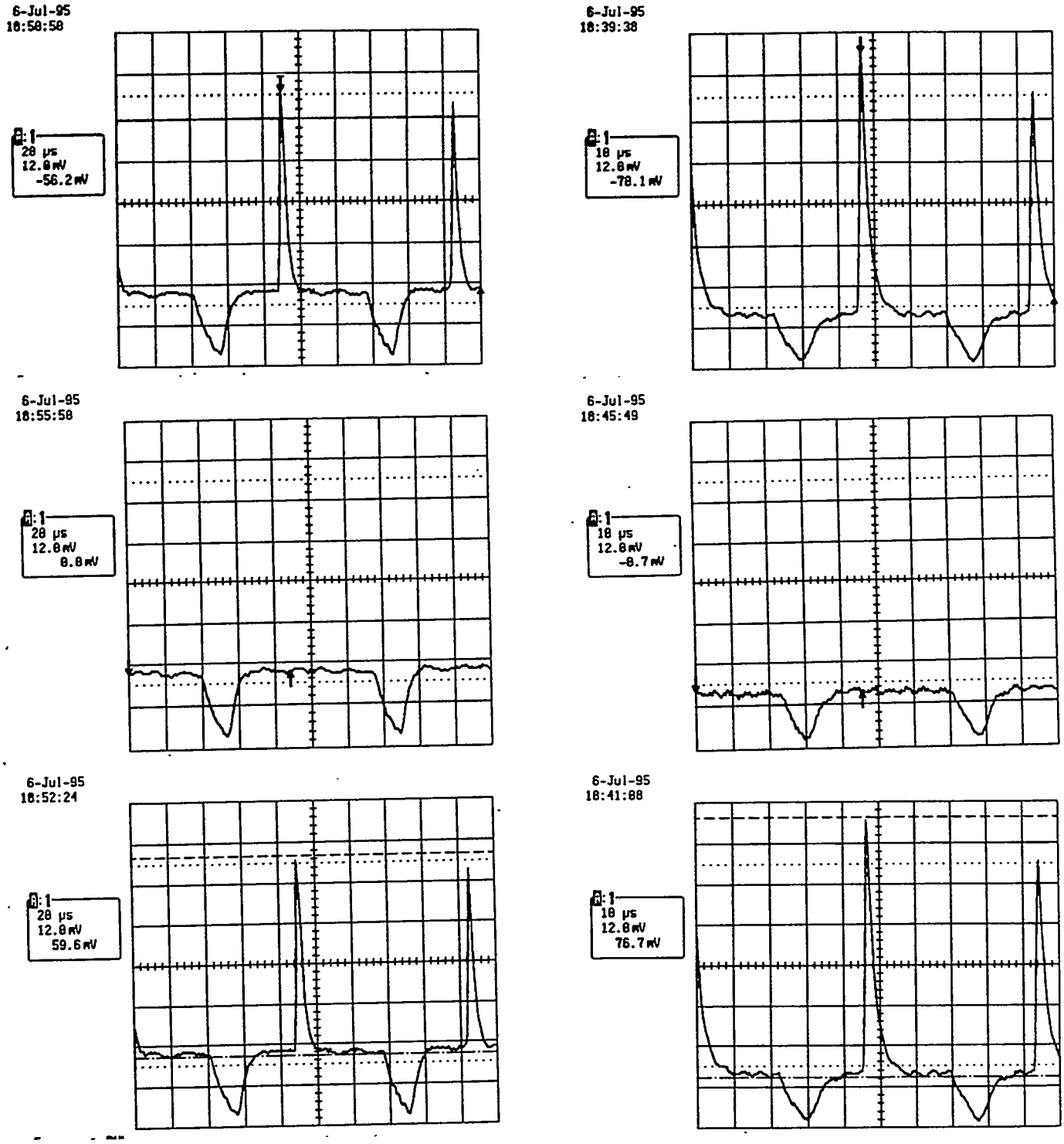

Fig. 18 CCD-13 First and second field data for 200ns (left column) and 100ns (right column) clocks. The top and center traces are time-phased to same pixel location in the first and second fields (see arrows). The bottom trace gives first field signal level and second field signal in read from center trace. The light intensity was constant for both clock rates.

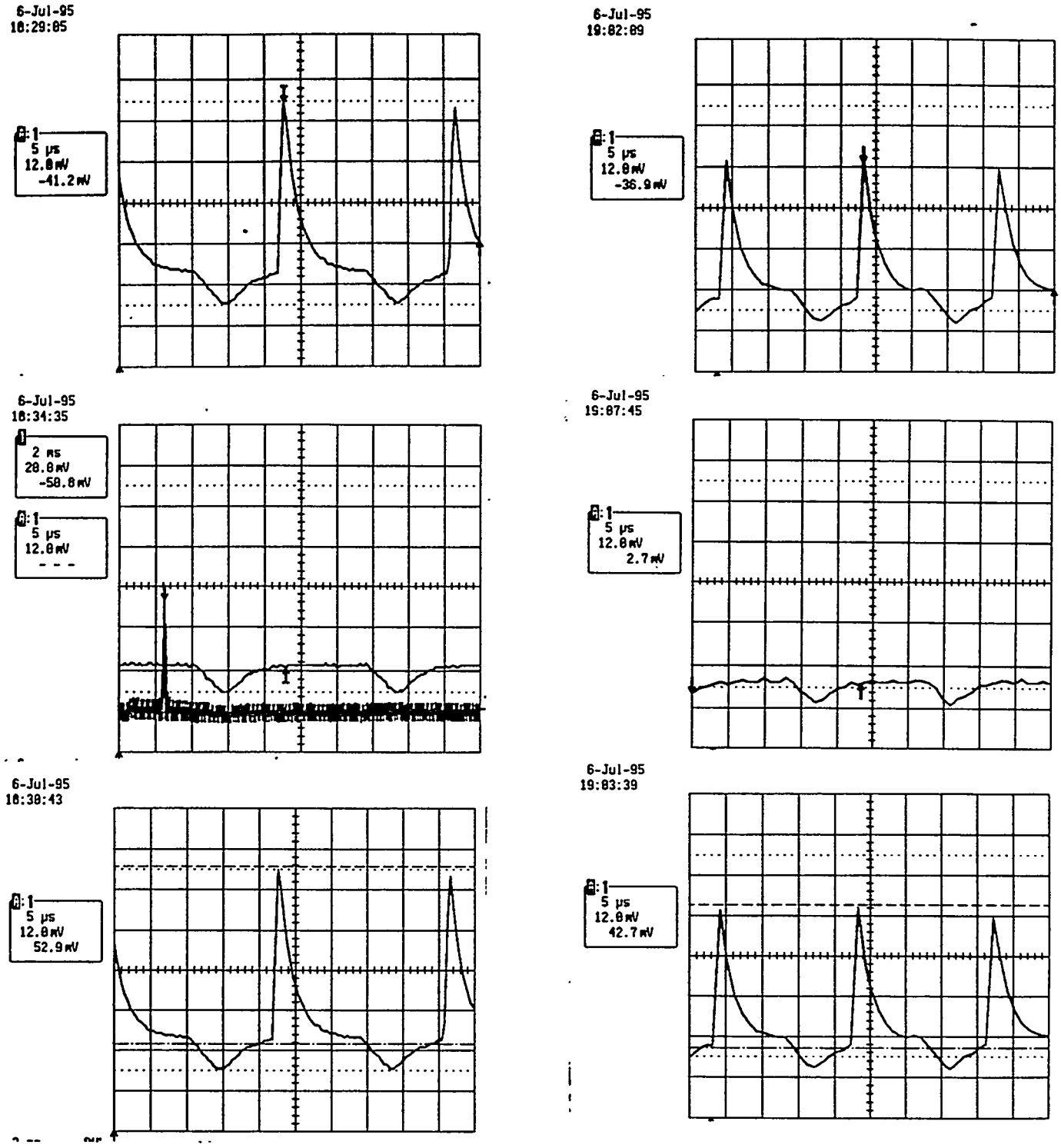

Fig. 19. CCD-13 first and second field data for 50ns (left column) and 20ns (right column) clocks. The top and center trances are time-phased to the same pixel location in the first and second fields (see arrows). The bottom trace gives first field signal level and second field signal is read from center trace. The light intensity was constant for both clock rates.

Our conclusions are that (1) we observed no losses due to CTE at the clock rates used above. Since our resolution was sufficient to detect CTE ≥ 99.99%, the CCD-13 CTE must exceed this level, including losses due to both vertical (parallel) and horizontal (serial) transfers during charge transport from excitation site to output amplifiers; and (2) there is definitely a loss in signal amplitude as the pixel frequency increases, even through we attempted to use resolution patterns of sufficiently low spatial frequency to eliminate losses due to video amplifier bandwidths.

We anticipated difficulty in accurately quantifying CTE to several "nines" because of the uncertainty in our knowledge of initial charge that is to be transferred because of all the mechanisms involved in CCD charge transport and because of the stability and repeatability of incident light energy density.

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